國 立 交 通 大 學

電子工程學系 電子研究所

碩 士 論 文

對基於寫入資料決定之操作輔助技術的靜態隨機存取記憶體進行開路缺陷之測試與分析比較

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中 華 民 國 一 0 一 年 九 月

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國立交通大學 電子工程學系 電子研究所碩士班

摘要

隨著科技的進步，記憶體所佔的面積越來越大，其耗能也變得值得重視。由於低耗能的需求，許多研究已經致力於開發可以在低電壓下操作，且維持良好表現的新靜態隨機存取記憶體。新型記憶體有著新的結構與設計技巧，因此可能會有有別於傳統靜態隨機存取記憶體的錯誤行為，而需要特殊的測試方式來測試這些錯誤模型。在本篇論文中，我們主要著重在測試新型設計中的低電壓對基於寫入資料決定之操作輔助技術的靜態隨機存取記憶體的開路缺陷。這個新型的記憶體協調操作兩條寫入字線與寫入資料決定之動態電壓電路以達成寫入動作，而以一條獨立的讀取道路完成讀取。以此特殊的結構為基準，我們提出了一個稱為自我迴路攻擊的測試方式。這個測試方式能夠測量到對於此種靜態隨機存取記憶體與寫入資料決定之動態電壓電路，過去的測試方法沒辦法偵測到的錯誤。此外，這個方法能更進一步的以較少的時間完成測試。

Comparison and analysis of testing method of open defect for Data-Aware Dynamic-Supply 8T SRAM

Student: Chin-Yuan Huang Advisor: Dr. Chia-Tso Chao

Department of Electronics Engineering
Istitute of Engineering
National Chiao Tung University

Abstract

As technology improves, the occupation area of memory becomes larger, and power consumption of memory is considerable. Due to the lower-power demand, a lot research effort has been devoted to develop new SRAM cell designs that can be operated at low VMIN but with high performance. The new SRAM cell design has its own cell structure and design techniques, which may result in different faulty behaviors than the conventional 6T SRAM and require specialized test methods to detect uncovered fault models. In this thesis, we focus on testing the open defects of a new low-VMIN data-aware dynamic-supply 8T SRAM design. The new SRAM utilizes two write word-lines cooperating a data aware dynamic-supply circuitry for write and an independent path for read. Based on the specific structure, we propose a novel test method called self-loop attacking (SLA). The proposed method detects all the undetected defects of traditional tests no matter in the SRAM cell or in the data-aware dynamic-supply circuitry. Moreover, it can further complete the detection with much less test time.

誌　　謝

首先我要感謝來參加我口試的各位口試委員，能在百忙之中撥空來參加我的口試並給予我良好的建議，知道自己有哪些地方不足，使我獲益良多，謝謝！

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黃欽遠

國立交通大學

2012 年 9 月

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Chapter 1

Introduction

1.1 Background

Low power has been one of the most critical design issues for current electronics products, especially for those portable and battery-limited applications. Among all the low-power design techniques, lowing supply voltage is the most straightforward and effective technique. Previous research works have demonstrated that the most power-saving supply voltage falls around the devices' threshold voltage [1] [2]. However, operating the conventional 6T SRAM at such low supply voltage is much more difficult than logic circuits, which significantly prevents the advance of developing an effective and economic low-power system since most of its area is occupied by the memories.

Trying to operate the conventional 6T SRAM with scaled supply voltage will encounter two major problems: (1) the decreased read static noise margin and (2) the decreased write margin [3][4]. This fact means that the 6T SRAM is vulnerable during read and also difficult to write at the same time, which makes it extremely difficult to find the balance among each transistor's size for the SRAM cell, especially under the

large process variation of the advanced process technologies [5][6]. Therefore, to successfully operate SRAMs with lower supply voltage, it has to rely on new SRAM cell structures along with new SRAM design techniques.

For improving the read static noise margin, [7]–[14] utilized an independent and dedicated read path in addition to the original bitline pair to eliminate the potential read disturb. As to improving the write ability, three design techniques are usually used. The first one is to strengthen the pass gates' driving current during write by using either the boosted word-line voltage [7] or the reverse short channel effect [15]. The second one utilizes extra transistors to break the loop of the cross-coupled inverters when the cell is being written [14] [16]. As to the last, the named data-aware write assist technique [17] [18] [19] separates the written SRAM cell into two halves. By assigning different and data-dependent control signals (WL, VDD, or GND) to each half of the cell, the cell becomes unbalanced and suitable for the new coming data.

Once new SRAM cell designs are used, the conventional SRAM test methods also need to be adjusted accordingly. In [20], the authors categorized the non-conventional SRAM designs into different types and proposed the corresponding test methods. However, the categorization is made based on two simple design criteria, which as well as the test methods cannot cover all the new SRAM cell designs

proposed later on, such as [21]. The SRAM design proposed by C. T. Chang et al. in [21] is a 8T cell design which utilizes a single bitline for both read and write operations. When read, an independent read path transmits the stored data to the bit-line indirectly, which prevents the directly accessing and leads to a disturb-free SRAM cell. For write, two write word-lines select either one of the storing nodes to connect the set-to-zero single bit-line for write-0/1 respectively. According to [18], C. T. Chang et al. further proposed a data-aware dynamic-supply (DADS) circuitry that can cooperate with the two word-lines. The DADS circuitry sets the supply for the two cross-couple inverters unbalanced based on the written data, which can enhance the write ability of the SRAM. As validated through silicon chips, the DADS 8T SRAM design successfully operates at VDD=0.6 volt with memory size 512Kb and operating frequency 209MHz. In the following section, the operation of the SRAM will be introduced in detail.

1.2 Motivation & Goals

In this thesis, we focus on testing the open defects for the DADS 8T SRAM. Open defects are the common defects in the manufacturing process and would reduce the circuit's reliability [22] [23]. To detect the defects, we firstly apply March test. The corresponding test efficacy and the undetectable cases will be shown. Then, for

the undetectable defects in cell, we modify the floating bit-line attacking (FBA) method [20] for the 8T SRAM. The limitation of FBA is also discussed. Finally, we propose a test method which utilizes the design feature of the 8T SRAM cell. The proposed method not only detects all the undetected defects of March/FBA in both the cell and the DADS circuitry but also achieves lower detectable resistance than the two previous methods. Besides, the method can test all the cells in the array at one time which greatly reduces the test time.

1.3 Thesis Organization

In the following section, the chapter 2 presents the architecture of 8T SRAM cell and DADS circuitry, and illustrate the operations of these circuitry. This chapter also states experimental setup we used for simulation. Chapter 3 introduces three methods we used for testing, including: March C-, floating bitline attacking (FBA), and self-loop attacking (SLA). Chapter 4 shows the experiment results of these testing methods, and explain the meaning of results. Chapter 5 is the overall conclusion.

Chapter 2

Preliminary of the low-Vmin

data-aware dynamic-supply 8T SRAM

2.1 Introduction of architecture and operations

Before the discussion of defect and testing, we firstly introduce the low-VMIN data-aware dynamic-supply 8T SRAM and its operations. Figure 1 shows the schematic of the SRAM. The cell is as the lower part in the figure composed by M1–M8, and the data-aware dynamic supply circuitry is as the upper part with M9–M12.

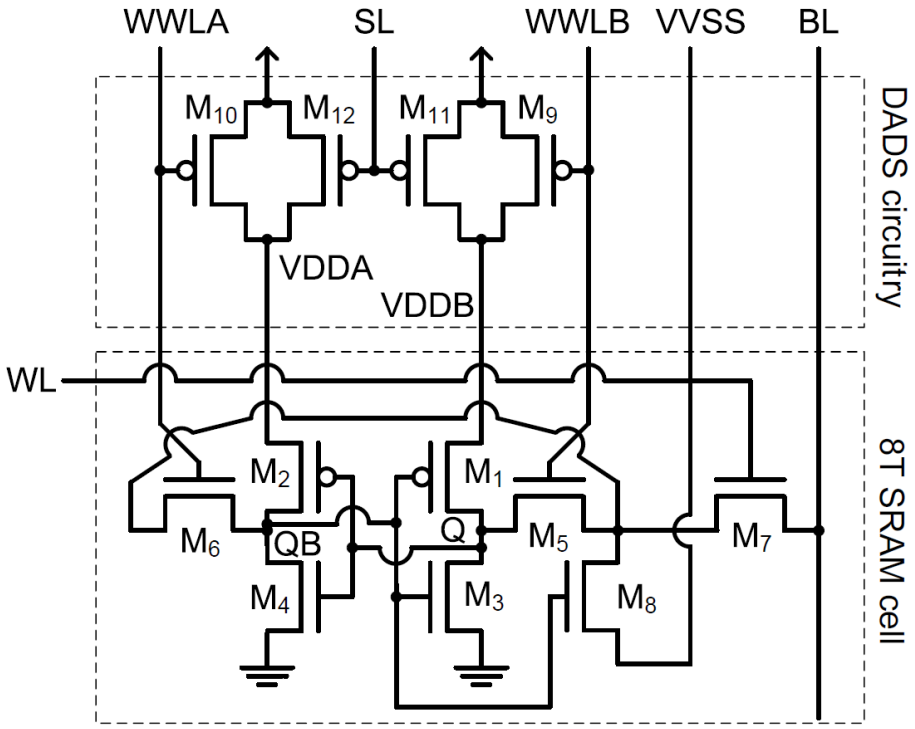


Figure 1
Schematic of the low-VMIN data-aware dynamic-supply 8T SRAM.

The SRAM cell holds data by the cross-coupled inverter M1–M4. Read operation relies on the independent path M7 and M8. To write-0, BL is set to zero and connects the Q through ”M5 and M7”. If write-1, BL is still set to zero but QB on the contrary will be connected to through ”M6 and M7”. Table 1 summarizes the controls for the 8T SRAM including the row-based WL and column-based WWLA/WWLB, BL, and VVSS. The read-write word-line (WL) turns on for both read and write, but WWLA/WWLB turn on only for write. Besides, depending on the written data, only one of WWLA/WWLB is on during the write. BL is floating-1 when read and 0 for write. The VVSS, mainly used for read operation, is suggested to follow WWLA to prevent the write disturb of background cells [21].

Table 1
CONTROL SIGNALS FOR THE 8T SRAM CELL

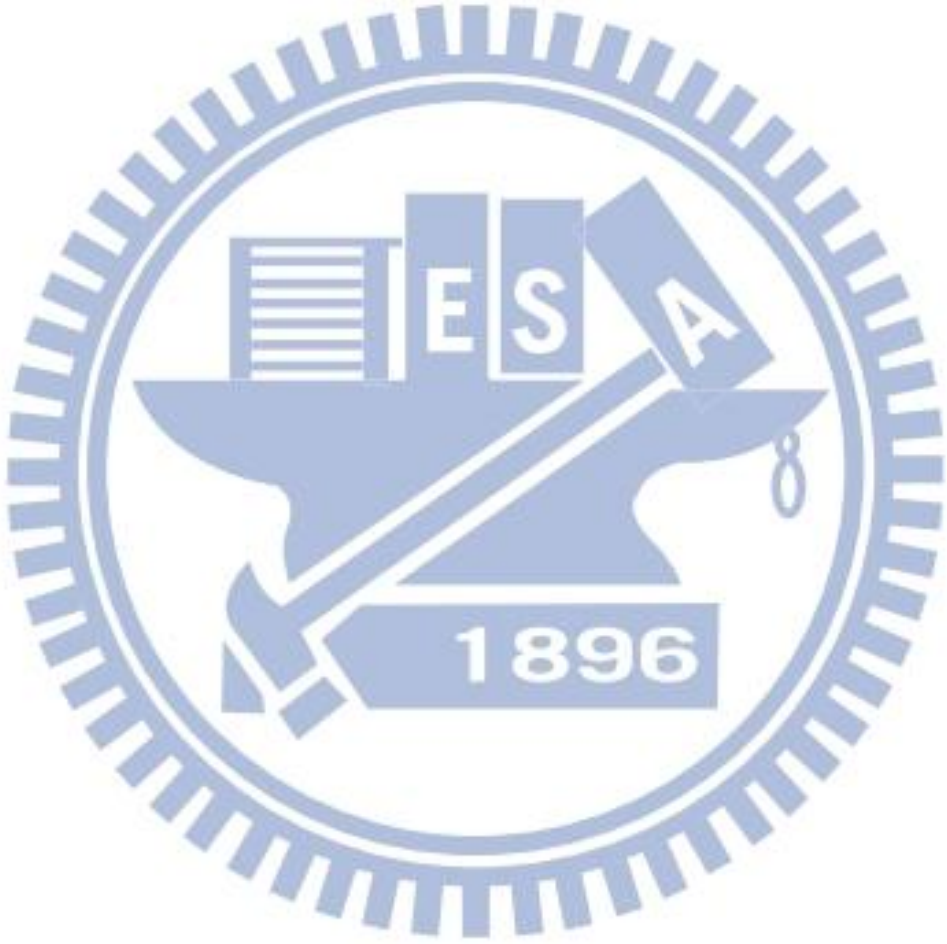
	Read 0	Read 1	Write 0	Write 1	Hold
WL	1	1	1	1	0
BL	Precharge	Precharge	0	0	X
WWLA	0	0	0	1	0
WWLB	0	0	1	0	0
VVSS	0	0	0	1	0

The data-aware dynamic-supply (DADS) circuitry, shown as M9–M12 in Figure 1, controls the supply voltage (VDDA and VDDB) for the cells in column. With WWLA and WWLB as the inputs, either M9 or M10 would be turned off when one of the cells in column is being written. For example, when a cell in the column is at write-1, WWLA is high for BL accessing and pulling down the QB. The M10 is then turned off, and pMOS M2 will get lower supply current from VDDA since only M12 provides that. The DADS then assists the write-1 operation because QB can be pulled down easily. For write- 0, WWLB is high and M9 is turned-off on the contrary. The DADS circuitry assists the write-0 by leaving only M11 supporting VDDB. The supply-level (SL) controlling M11 and M12 is set to provide a minimum supply current for the background cells at write periods. Thus, there is a voltage upper bound for SL. SL still has a voltage lower bound. It's because the SL with voltage too low will turn on M11/M12 too much, which makes VDDA/VDDB always with high supply capability. The data-aware write-assist function would then be canceled.

2.2 Experimental setup

In our experiments, we apply a 256Kb DADS 8T SRAM with eight 32Kb blocks. Each block is composed by 256 rows and 128 columns. Thus a DADS circuitry drives 256 cells in column. The SL is set to 0.5*VDD (VDD=0.6V) which

has been verified that the 8T SRAM can operate correctly from process corner SS to FF. For most of our experiments, we run the simulation under TT corner. Only for our proposed test method, we consider all the process corners to prove the method's validity. This will be shown in the sections later.



Chapter 3

Test methods

3.1 Test Methods & Minimum detectable resistance

To detect open defects, Three methods including March C- algorithm, floating bit-line attacking (FBA), and self-loop attacking (SLA) are used. The defects are simulated by injecting a resister into each MOSFET of the SRAM and DADS circuitry with resistance swept from high (100GΩ) to low. For each single defect, we record the minimum resistance when the SRAM's sense amplifier reports error. If the defect does not fail the SRAM even with 100GΩ, it is considered undetectable. Explanation of FBA and SLA are for the following parts.

3.2 Floating bit-line attacking (FBA)

According to the non-conventional SRAM categorization in [20], the 8T SRAM should be categorized to "Type-A". However, the corresponding test method recommended for the defects at cross-coupled inverters requires dual bit-lines during the test. For the 8T SRAM which has only one bit-line, the method is not applicable. We select the floating bit-line attacking (FBA) method which is for another type of SRAM in [20] but can be modified for single-bit-line based SRAMs. FBA uses the

floating voltage pre-set on bit-line to access and attack the Q (or QB) with inverse logic in the cell. If the data stored in the cell flips, the following read operation can then detect the defect.

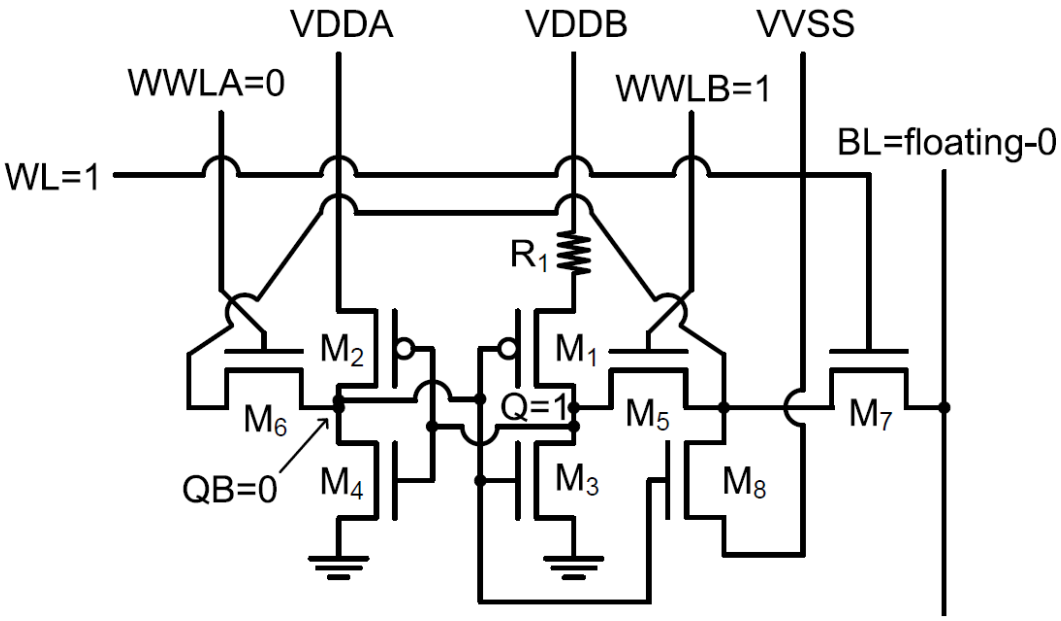


Figure 2
An example of floating bit-line attacking method:
using floating-0 on bit-line for detecting the open defects R1.

Figure 2 shows an example of using floating-0 as the attacking source on BL. The open defect R1 at M1 is the target to test. As shown in the figure, the Q/QB need to be 1/0 initially. The BL with floating-0 is accessing/attacking the Q through the turned-on M5 and M7. If the open defect makesM1 unable to maintain the 1 on Q, the sense amplifier will output 0 in the following read operation. The defect is then

detected. Note that BL with floating-1 can also be applied for detecting R1 if QB is accessed/attacked through M7 and M6 instead. Table 2 lists the complete control signals of FBA for the four open defect locations. WL turns on for every cases. The initial Q/QB value is set depending on the defect locations: 1/0 for M1/M4 and 0/1 for M2/M3. As to WWLA/WWLB, they control the attacking source accessing the node with inverse logic. Besides these control signals, there are still two factors would affect defect detection: the value of VVSS and background cells. Further discussion would be the next section.

Table 2
CONTROL SIGNALS OF THE FBA TEST METHOD

Defect Location	Attacking source on BL	Control signals				
		WL	Q	QB	WWLA	WWLB
M1 & M4	Floating-0	1	1	0	0	1
	Floating-1	1	1	0	1	0
M2 & M3	Floating-0	1	0	1	1	0
	Floating-1	1	0	1	0	1

3.3 Self-loop attacking (SLA)

We introduce a new test method named self-loop attacking (SLA) for the 8T SRAM. The SLA method utilizes the specific dual-write-pass-gate structure of the 8T SRAM cell. By controlling the word-lines, the method creates an internal attacking loop of Q/QB inside the cell without BL's accessing. The Q and QB with

self-attacking each other will go to a final state which depends on the initial Q/QB, background cells, VVSS, process corners, and the most important one: the existence of defects. If the defects result in a different final state from that of defect-free cells, the following read operation can then detect the faults.

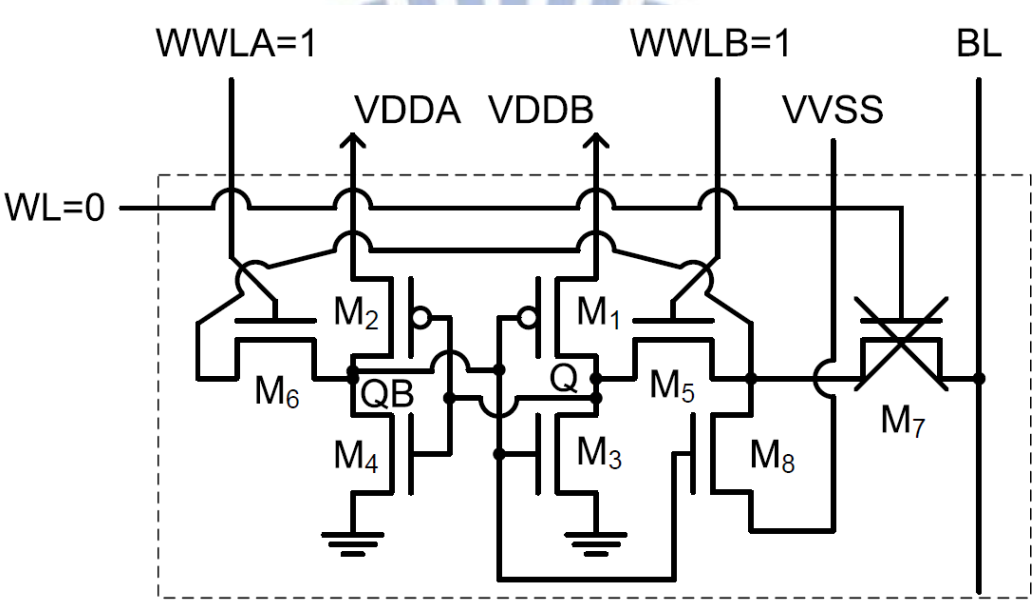
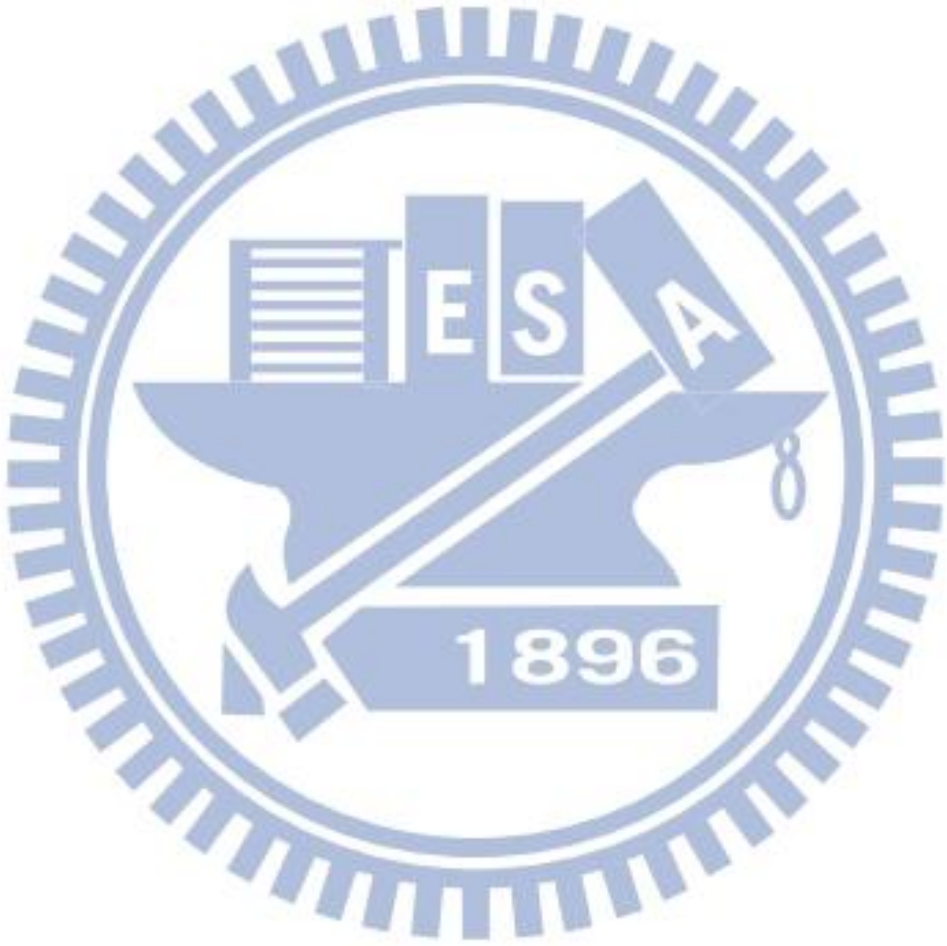


Figure 3
Configuration of the proposed self-loop attacking test method.

Figure 3 shows the configuration of the method. Before the test, Q and QB can store either 1/0 or 0/1. During the test, M7 is off and M5/M6 are on so that Q and QB inside the cell will attack each other. After the test, WWLA/WWLB is off, and the final state of the cell is read. Note that, since the BL is not used during the SLA, the test operation hence has chances to be done for the whole array at one time. Although the test method takes the advantage of 8T SRAM cell structure, it can detects the open

defects not only in the cross-coupled inverters of the cell but also in the DADS circuitry.



Chapter 4

Experiment results

4.1 March C-

Table 3 lists the simulation results of the test. The first two columns are the device type and the device name at which the defect is injected. The third and fourth columns are the detecting operation and the minimum detectable resistance. The word "undetectable" means the fault injection does not fail the SRAM even with 100GΩ.

Table 3
TEST RESULTS OF MARCH C- FOR OPEN DEFECTS

Device type	Device name	Detecting operation	Min-detectable resistance (Ω)
Pull-up pMOS	M1	Write-1	800M
	M2	Write-0	500M
Pull-down nMOS	M3	undetectable	-
	M4	undetectable	-
Write pass-gate	M5	Write-0	8M (Background = 1) 3M (Background = 0)
	M6	Write-1	3M (Background = 1) 800K (Background = 0)
Read-Write Pass-gate	M7	Read-0	300K
Read path	M8	Read-0	50K
Data-aware dynamic-supply circuitry	M9	undetectable	-
	M10	undetectable	-
	M11	undetectable	-
	M12	undetectable	-

As shown in the table, the defects at pull-down nMOSs and in the DADS circuitry are undetectable. For the pull-down nMOSs (M3 and M4), the defects fail neither the write nor the read. In write, Q or QB can always be successfully pulled down by the BL even if the pull-down nMOSs are defective. In read, the independent read path would take charge to transmit the data to the floating-1 on BL in place of the original pull-down nMOSs in 6T SRAM. Thus, normal operations cannot detect the defects. As to the DADS circuitry, when the defect occurs at M9 and M10, the fault is masked. It's because M9 and M10 are originally set to off when write. And even when read/hold, the defect-free M11 and M12 will help support VDDA and VDDB that the stored data never flip due to the defect at M9 and M10. While defects occur at M11 and M12, the background cells do get weak supply from VDDA (or VDDB) when certain cell in the column is written. But the simulation results show the background cells can hold the data correctly during the write period and until M9 or M10 is re-turned on at the end of the write. Thus, the defects at M11 and M12 are also undetectable.

In addition to the pull-down nMOSs and the DADS circuitry, the defects at pull-up pMOSs (M1 and M2) are also belonged to hard-to-detect ones. Although the defects are detected by write operations according to Table 3, the min-detectable resistance is at 500M–800M. This implies the defect could be detected only if the

resistance is large. Hence, we still need other test methods for lowering the detectable resistance.

Open defects at the pass-gates (M5, M6, and M7) and read-path transistor (M8) can be easily detected by write and read operations respectively. The minimum detectable resistance is at MΩ or below. Note that the minimum detectable resistance of the defects at M5 and M6 will vary depending on the data stored in the background cells. As shown in Table 3, when all the background cells store 0, the write operation in the March can detect lower open resistance for both the cases. However, the reasons for the two are different. For the defect at M5, when the defective cell is being tested by the write-0 operation, the Q is being pulled down by the BL, and QB is being pulled up by pMOS M2 with VDDA supply (see Figure 1). While all the background cells store 0, most cells share the VDDA since the corresponding QBs are 1. Hence, the background setting with all 0 causes the most severe write operation for the defective cell. Lower resistance is then detected.

As to the defect at M6, the background cells affect the testing via VVSS unlike the VDDA in the previous case. Figure 4 shows corresponding details with turned off pass-gates ignored.

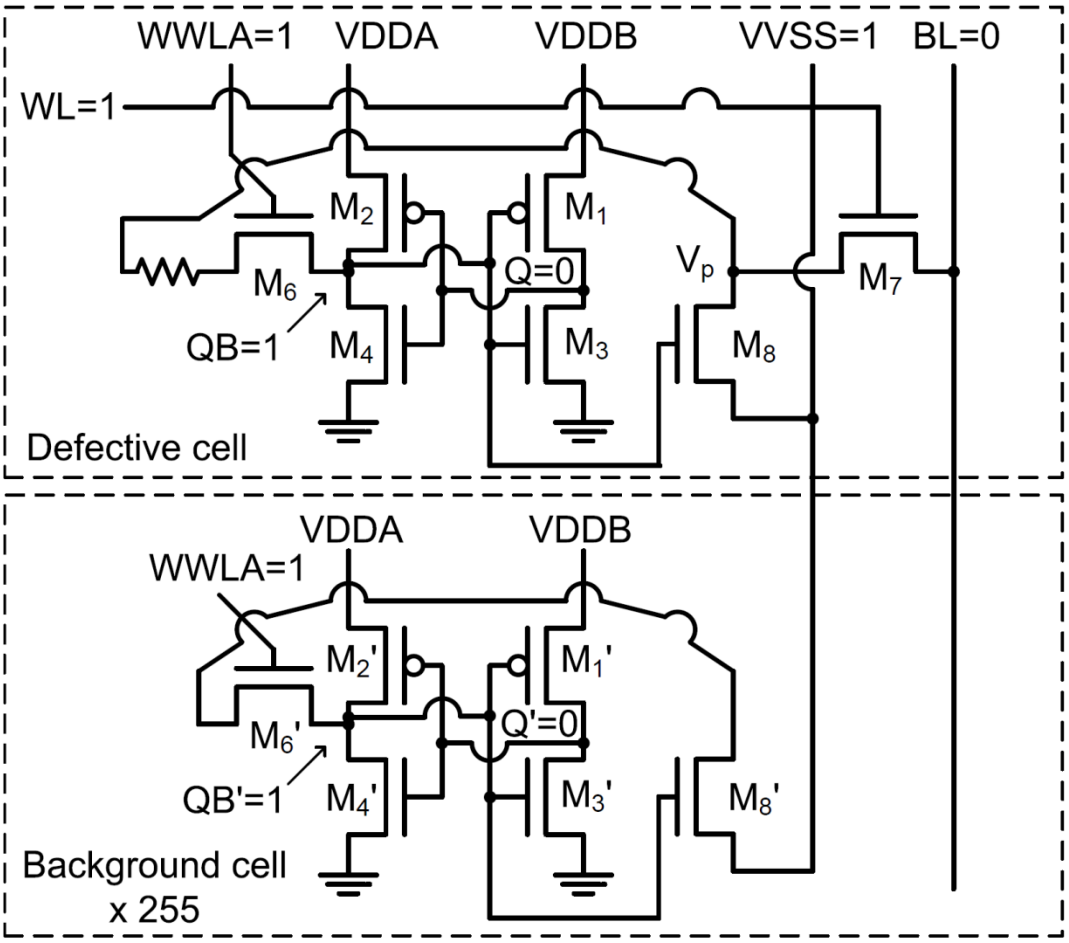


Figure 4

Background effect to VVSS when open defect at M6 is being detected.

In the figure, the above cell is the defective one being tested by a write-1 operation. The initial data in the cell is Q/QB=0/1. The cell below represents the 255 background cells also with Q'/QB'=0/1. In the figure, all the turned-off pass-gates are ignored. Firstly, the BL is accessing and attempting to pull down the QB through M7 and M6. Before the write operation completes, the M8 remains turned on since the QB is originally 1. The turned-on M8 connects VVSS and V_P . The voltage on V_P is then not a perfect zero since it's not only driven by the BL through M7 but also driven

by the VVSS driver through M8. While the background cells all store 0 as shown in the figure, VVSS further connects to VDDA through the M'8, M'6, and M'2 in the background cells. The connection of VVSS–VDDA then raises the voltage on V_P much more. As a result, to succeed the write-1 becomes harder and lower resistance is detected.

To summarize, the March C- detects the defects at M5–M8. For M5–M6, the minimum detectable resistance can be further lowered if all the background cells are set to 0 for write-0 and write-1 respectively. The algorithm {⇳(w0); ⇳ (w1,r1,w0,r0)} as example can achieve the goal. As to the defects at the cross-couple inverters M1–M4 and the DADS circuitry M9–M12, they are either undetectable or hard-to-detect. In the following section, we will introduce the test methods for the detects.

4.2 Floating bitline attacking (FBA)

Table 4 shows the test results of FBA. The first column is the attacking source on bit-line. The second and the third columns are the background cells' data and the VVSS logic during the test. The rest of the table lists the test results of the four open defect locations respective.

Table 4

TEST RESULTS OF THE FBA TEST METHOD

Attacking source on BL	Environments during test		Test results & Minimum detectable resistance			
	BG	VVSS	M1	M2	M3	M4
Floating-0	0	0	X	X	-	-
		1	X	1MΩ	-	-
	1	0	X	X	X	X
		1	X	3MΩ	-	X
Floating-1	0	0	-	-	-	-
		1	-	-	30MΩ	10MΩ
	1	0	-	-	-	30MΩ
		1	-	-	5MΩ	30MΩ

BG: data of the 255 background cells X: overtest -:undetectable

As shown in the table, there are three different results: detected, overtest, and undetectable. For the detected results, the table lists the minimum detectable resistance. For overtests marked "X", the stored data will flip even the SRAM cell is defect-free. Hence, it is also inapplicable as the undetectable cases marked "-".

According to the results, the defect at M1 in never detected since floating-0 in FBA will cause overtest, and floating-1 does not detect any data flipping. However, to M2, floating-0 in FBA with VVSS=1 is applicable for detecting the defect. The minimum detectable resistance is 1MΩ~3MΩ. For nMOSs M3 and M4, floating-1 is more appropriate than floating-0. The minimum detectable resistance of the defect is 5MΩ~30MΩ and 10MΩ~30MΩ for M3 and M4 respectively.

The difference of M1 and M2 is the impact of VVSS. For floating-0, Q/QB is 1/0 for M1. M8 does not turn on while QB is 0; therefore, VVSS does not connect to

the cell. However, Q/QB is 0/1 for M2. In this situation, VVSS connect the cell directly. When VVSS is 0, it strengthen floating-0 attacking and results overtest. On the contrary, if VVSS is 1, it weaken floating-0 attacking and results detectable. For detectable two cases, the minimum resistance of BG sets to 0 is lower than BG sets to 1. It is because if BG sets to 0, VDDA need to supply voltage to cell and background. It means VDDA has larger loading and makes it harder to hold cell's QB. Threfore, the defect can be detected by lower resistance.

For M3, only BG/VVSS sets to 1/0 in floating-0 would result overtest. It is because if BG is 1, VDDA only supply voltage for cell's QB and makes it stronger to turn on M8. When VVSS is 0, it would strengthen floating-0 attacking which results overtest. In floating-1 test, BG/VVSS sets to 0/1 or 1/1 can detect defect. The reason is that initial Q/QB for testing M3 is 0/1 and VVSS strengthen floating-0 attacking. Setting BG/VVSS to 1/1 can detect the lowest detectable resistance because setting BG to 1 makes cell's QB stronger (no BG cells share VDDA), and results floating-1 attacking stronger.

For M4, floating-0 attacking cannot detect defect and the result depends on BG. when BG sets to 0, cell's Q is stronger. Floating-0 attacking does not make the cell fail to hold data. However, if BG sets to 1, cell's Q is too weak that even defect free cell cannot hold data. Because the initial Q/QB set of testing M4 is 1/0, the influence of

VVSS is weaker. Except for BG/VVSS sets to 0/0, other cases in floating-0 can detect defect. While BG sets to 0, Q is stronger and M4 is more sensitive. When QB close to 1 and turns on M8, the value of VVSS would impact the result. If VVSS sets 0, it weaken floating-1 attacking and results in undetectable. If VVSS sets 1, the defect is detectable. While BG sets to 1, Q is weaker and M4 is less sensitive. In this situation, floating-1 can detect defect no matter what value VVSS is.

For test time, FBA requires two operations for each defect on each cell. One is the floating bit-line attacking, and the other is a simple read. Here we ignore the preliminary write operation before each FBA since the 1N operation can usually be omitted by reordering the test elements in March. The total number of operations for the complete FBA is hence 2Nx3 for defects at M2–M4. Note that, although floating-1 in FBA which detects the defects at M3 and M4 are with the same BG and VVSS as shown in Table 4, the actual setups for the two are different. As shown in Table 2, the initial Q/QB set for M3 and M4 should be different. Therefore, detections for M3 and M4 require individual test time 2N for each.

4.3 Self-loop attacking (SLA)

4.3.1 Test for 8T SRAM cell

Table 5 shows the simulations results of the test under process corner TT. The first two columns are the eight possible configurations. The iTG means the ”initial” state of the target cell under the SLA test. iBG is the initial data stored in the background cells. The third column shows the final states of defect-free SRAMs with the corresponding configuration at left. For example, in Config. 1, the target cell and background cells before the test are both set initially to 0. VVSS is also 0. After test, the final states of target cell and background cells both become 1. The background cells have their data changed because their WWLA/WWLB are shared with the target cell. The turned-on WWLA/WWLB also cause the Qs and QBs in background cells attacking each other. Based on the final states in the third column, the open defects causing different ones will be detected by the read operation afterwards. The rest of the table lists the minimum detectable resistance of the defected open defects.

Table 5

FINAL STATES OF DEFECT-FREE CELLS AND TEST RESULTS OF OPEN DEFECTS OF SLA UNDER PROCESS CORNER TT

Config.	Logic setup (iTG, iBG, VVSS)	Final states (TG, BG)	Min-detectable resistance (Ω)			
			M1	M2	M3	M4
1	0/0/0	1/1	10M	-	-	10K
2	0/0/1	1/1	300M	-	-	-
3	0/1/0	0/1	-	-	-	-
4	0/1/1	1/1	300M	-	-	300M
5	1/0/0	0/1	-	5M	1M	-
6	1/0/1	0/1	-	10K	8K	-
7	1/1/0	1/1	800M	-	-	-
8	1/1/1	1/1	800M	-	-	-

(i)TG: (initial) data of target cell -: undetectable

(i)BG: (initial) data of the 255 background cells

For M1, there are 5 Config. can detect defect and the minimum detectable resistance is 10MΩ. All of final states of these Config. are 1. The value of Q of Config. 7, and 8 are 1→1. It is easy for Q to hold data, and the detect resistance is 800MΩ which is larger than other Config. setting. For Config.1, 2, and 4, M1 has to pull up Q. Therefore, the detect resistance is smaller. The difference of Config. 1 and 2 is the value of VVSS. Due to the initial setup of Q/QB is 0/1, QB turn on M8 and makes VVSS impact the cell. While VVSS is 0, it is harder for M1 to pull up Q and makes M1 more sensitive.

For M2, only Config. 5 and 6 can detect defect. The value of Q of Config. 5 and 6 are 0→1. QB has to pull down QB. Similar to test M1, the difference of Config. 5

and 6 is the value of VVSS. When VVSS sets to 1, it can detect the minimum detectable resistance 10KΩ. It is because the cell is construct of nMOS and VVSS has greater influence while it is 0. After SLA, WWLA and WWLB are turned off. If VVSS is 0, the voltage of Q is lower; oppositely, if VVSS is 1, the voltage of Q is higher. The original final state of Q is 0. Thus, VVSS sets to 0 is easier to make Q pull down than sets to 1.

The minimum detectable resistance of M3 is 8KΩ. It is similar to M2 because M3 and M2 are symmetrical. Same as M2, only Config. 5 and 6 can detect defect of M3. The value of Q are 0→1 and M3 has to pull down QB. If VVSS sets to 1, the voltage of Q is higher and makes M3 more sensitive.

For M4, Config. 1 and 4 can detect defect, and the value of Q are 0→1. It is interesting that Config. 2 is also 0→1, but this setting cannot detect M4. The difference between Config. 1 and 2 is the value of VVSS. The initial setup of Q/QB of Config. 1 and 2 are 0/1 and makes VVSS impact the cell. The value of VVSS is 1 in Config. 2. It makes the voltage of Q higher and close to the original final state. The BG and VVSS of Config. 1 and 4 are different, but initial setup of Q/QB are the same. The setting of QB makes VVSS impact the cell. Same as Config. 1 and 2, the value of VVSS is 1 in Config. 2 and 4, which makes the voltage of Q higher and close to the original final state. The influence of M4 is smaller. Therefore, the detectable

resistance is larger. Because BG sets to 1 in Config. 4 makes QB stronger than Config. 2, the influence of M4 is larger than Config. 2 and can be detected.

Although all of configurations for M1–M4 are discussed in detail, only Config.1 is applicable for testing M1 and M4, and only Config.5 is applicable for testing M2 and M3. We would explain the reason in the next section.

For test time, using Config.1 to test M1 and M4 is very fast because the value of TG and BG are the same; therefore, only 2N+C (C is the number of column) is enough (N for initial value set and read, C for self-loop attack). If using Config.5 to test M2 and M3, it costs nearly N^2 because it needs to re-write BG to 0 every time after self-loop attacking. However, if BL driver is strong enough for write whole column at a time, test time would be 4N (including write BG, write cell's data, self-loop attack, and read).

4.3.2 Test for DADS circuitry

For testing for DADS circuitry, the open defects in the DADS circuitry have been shown undetectable by the March C- test. When trying to apply FBA and SLA discussed in previous section for test, the FBA method actually does not detect the defects as well. It's because FBA only triggers one cell in the column by which the requested supply current is limited. The DADS circuitry even with open defects can always provide such supply current that no data is flipped in the cell under FBA. On the contrary, the proposed SLA method triggers all the cells in the column by turning on both the WWLA/WWLB. Much more supply current is requested by the cells in the column. Since the high current loading may not be satisfied, the SLA method therefore has chances to detect the defects in the DADS circuitry. SLA can detect the defect of M9 and M10. However, for M11 and M12, SLA can detect the defect only in certain corner, the reason would be explained in the following part.

We further examine the final states of defect-free cells under various process corners. It's because only if the final states keep equal for various process corners, the feasibility of above configurations can be verified. Table 6 shows the results. In the table, we choose process corners FF and SS as examples since they have most different final states. According to the table, Config. 3, 4, 6, and 7 have different final states when test is under SS or FF. The four configurations are hence not feasible for

test. As a result, for M1, just Config. 1, 2, and 8 remain applicable. For M2/M3 and M4, only Config. 5 and 1 are applicable respectively.

To summarize, we will use the Config.1 for detecting the defects at both M1 and M4. For M1, it's the one detecting minimum resistance. For M4, it's the only applicable configuration. For M2 and M3, even though Config. 6 detects lower resistance under TT corner, we can only choose the Config. 5 which covers various process corners.

Table 6
FINAL STATES OF DEFECT-FREE CELLS UNDER VARIOUS PROCESS CORNERS

Config.	Logic setup (iTG, iBG, VVSS)	Final states (TG/BG) Under process corners		
		TT	SS	FF
1	0/0/0	1/1	-	-
2	0/0/1	1/1	-	-
3	0/1/0	0/1	1/0	-
4	0/1/1	1/1	-	0/0
5	1/0/0	0/1	-	-
6	1/0/1	0/1	1/1	1/1
7	1/1/0	1/1	1/0	0/0
8	1/1/1	1/1	-	-

-: the same as the TT corner

Table 7

TEST RESULTS OF SLA FOR OPEN DEFECTS IN THE DADS CIRCUTRY

Config.	Logic setup (iTG, iBG, VVSS)	Min-detectable resistance (Ω)			
		M9	M10	M11	M12
1	0/0/0	1M	-	-	-
2	0/0/1	1M	-	-	-
5	1/0/0	-	1M	-	-
8	1/1/1	10M	-	-	-

Table 7 shows the test results of SLA in DADS circuitry. For M9, SLA with Config. 1, 2, and 8 can detect the defect. The minimum detectable resistance is 1MΩ. For M10, the defect is detected but with Config. 5 instead. The min-detectable resistance is also 1MΩ. As for M11 and M12, the defects do not cause faults and are still undetected. The reason would be explained in next section.

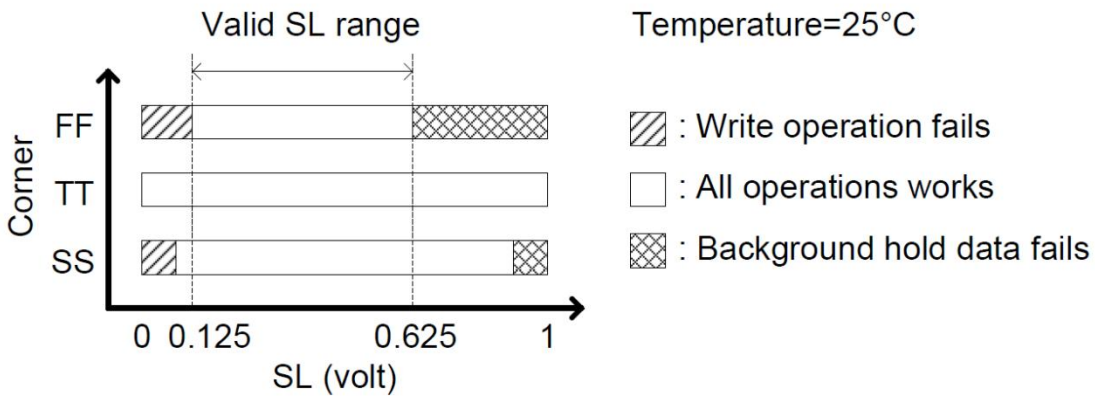
For M9, the final state of Config.1, 2, and 8 are 1/1. Note that Config.1, 2, the value of Q is 0→1, but for Config.8, it is 1→1. While using SLA, WWLA and WWLB are on and M9 is off. M9 impact the pull-up ability of cell after WWLA and WWLB turning off. It is reasonable the final state is 1. The minimum detectable resistance occurs in Config. 1, 2.

Result of M10 is similar to M9 because M10 is symmetrical to M9. Opposite to Config. 1, 2, and 8, the final state of Config 5 is 0/1. That means the value of Q is 1→0. The minimum detectable resistance of M10 is 1MΩ, which is the same as M9.

As for M11 and M12, the defects do not cause faults and are still undetected. In

fact, it's because the function of M11 and M12 for the SRAM operating under process corner TT, as for above experiments, is not crucial. When the SRAM operates under the other process corner that M11 and M12 are critical, the defects would then cause faults and should be detected. Figure 5 as example can help determine the process corner under which the function of M11 and M12 is critical.

Figure 5
Valid SL range under different process corners.



In Figure 5, the x-axis is the voltage of SL which is the control of M11 and M12. The three bars indicate the SRAM's response under each process corner. When SL is very low (as shown in left side of the bars), the write operation may fail depending on the process corner. When SL is too high (right side of the bars), the background cells may fail holding the data. As a result, there is a valid SL range with lower and upper bounds. As shown, the valid SL ranges for various process corners are different. For FF corner, it is most limited, especially with lowest upper bound. This indicates the

SRAM under FF corner is most sensitive to the turning off of M11 and M12 (High SL voltage turns off M11 and M12). Since open defects cause similar effect as turning off a MOSFET, they most likely cause faults for the SRAM under FF corner. Based on the fact, we further simulate the SLA test method for the defects at M11 and M12 under FF corner. The voltage of SL keeps 0.5*VDD as for previous experiments. March C- and FBA are also applied for comparison.

Table 8
SIMULATION RESULTS OF TESTING THE DEFECTS AT M11 AND M12 BUT UNDER FF PROCESS CORNER

Test method (under FF corner)		Min-detectable resistance (Ω)	
		M11	M12
March C-		undetectable	undetectable
FBA		undetectable	undetectable
SLA	Config. 1	undetectable	undetectable
	Config. 2	undetectable	undetectable
	Config. 5	undetectable	10M
	Config. 8	1M	undetectable

As shown in Table 8, March C- and FBA are still unable to detect the defects, but the proposed SLA method with Config. 5, and 8 can. The minimum detectable resistance for M11 and M12 is 1MΩ and 10MΩ respectively. It is because M11 has a greater impact on Q. It is reasonable using final state 1 to detect defect of M11. The initial value of TG/BG of Config. 1, 2 is 0/0, it makes QB stronger. Even without M11, Q can pull-up by QB's attacking. Therefore, it is undetectable. On the contrary, initial

value of TG/BG of Config. 8 is 1/1. If defect inject on M11, Q is weaker and cannot hold the data which makes the difference between defect free M11. For M12, M12 has a greater impact on QB. Only Config. 5 has to pull up QB. Thus, only Config.5 can detect defect on M12.

For test time, Config. 8 can detect defect of M9 and M11, and the test time is N+2C. It is same foe using Config.5 to test M10 and M12. Setting initial TG/BG takes N times, and applying SLA and reading out takes 2C times. In conclusion, test time for using SLA to test DADS circuitry is 2N+4C.

4.4 Test methods comparison

Table 9 summarizes the test methods of test efficacy and corresponding test time. For test efficacy, we list the minimum detectable resistance. Firstly, March C- as the typical test method can only detect the open defects at M1 and M2. The detectable resistance is above 500M. The FBA can detect the defects at M3/M4 and lower the detectable resistance for M2. But the defect at M1 becomes undetectable. The SLA method as the proposed one can detect all the open defects at M1–M4. The detected resistance for M1, M3, and M4 is further lower than that of FBA. For M2, although no lower resistance is detected, the SLA can still achieve 5MΩ near the 1MΩ of FBA.

For test time, March C- is 10N, and FBA is 6N, However, for SLA, there are

two cases: 2N+C and N^2. For testing M2 and M3, the minimum detectable resistance of FBA and SLA are similar, but test time for FBA is much less than SLA (if BL driver cannot write the whole column). Thus, we suggest using SLA for testing M1 and M4, and using FBA for testing M2 and M3.

Table 9
TEST METHODS COMPARISON OF TEST EFFICACY AND TEST TIME

Test method	Min-detectable resistance (Ω)				Test time
	M1	M2	M3	M4	
March C-	800M	500M	-	-	10N
FBA	-	1M	5M	10M	6N
SLA	10M	5M	1M	10K	2N+C (i) N^2 (ii), 4N (iii)

(i): Test time for M1, M4
(ii): Test time for M2, M3
(ii): Test time for M2, M3 (if bit-line driver can write the whole column cells)

Chapter 5

Conclusions

In this thesis, we used three test methods for testing DAWA 8T SRAM and DADS circuitry including March C-, FBA, and SLA. March C- can detect the open defect of nMOS on pass-gate and read-path, but it is not applicable for cross-couple inverters and DADS circuitry. FBA can detect 3 of 4 defects in cross-couple inverters, but it still cannot detect defect of M1. Besides, FBA is not applicable for DADS circuitry. SLA can detect all of defects in cross-couple inverters, and it can detect partial defects in DADS circuitry in TT corner. For FF corner, it can detect all of defects in DADS circuitry.

For test time, March C- is 10N, and FBA is 6N, SLA depends on testing target. For M1 and M4, test time is 2N+C. For M2 and M3, test time is N^2 (if BL driver can write whole column at one time, it is 4N). For DADS circuitry, SLA is the only applicable method, and test time is 2N+4C.

To summarize, we suggest that firstly apply Mach C- for testing M5–M8, then using FBA for testing M2 and M3, and using SLA for testing M1, M4, and DADS circuitry.

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