國立交通大學

電子工程學系 電子研究所

碩士論文

應用於行動照護之

動態取樣全數位心電訊號擷取電路

An All-Digital ADC

with Dynamic Sampling Technique for ECG Acquisition

in Mobile Healthcare Applications

研究生：徐佩妤

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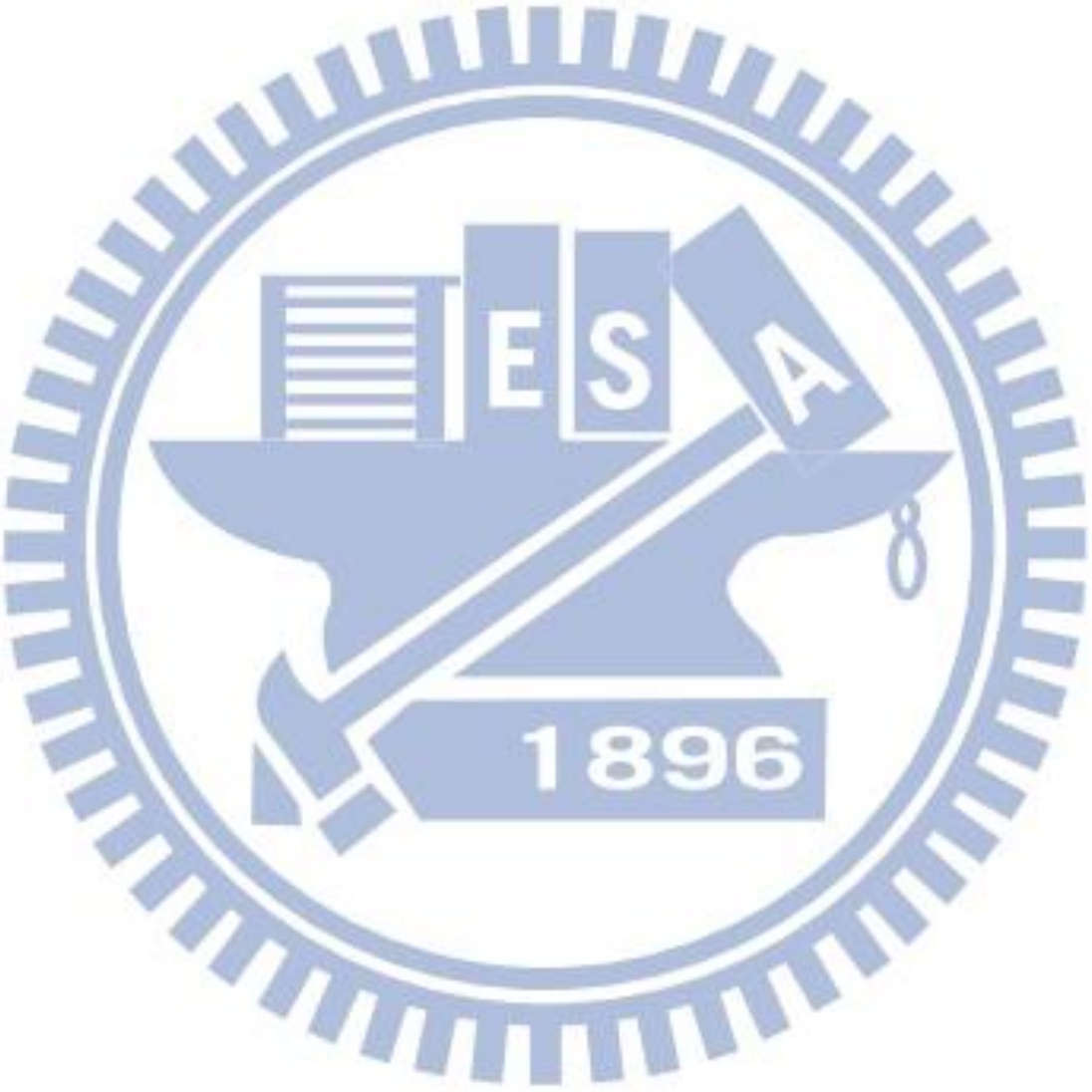
摘要

近年來慢性疾病逐年上升，預防醫學顯得越來越重要。為了可以全天候的監控人體的生理訊號，並減低人們往來醫院的不便，利用可攜式電子進行全天候的行動照護成為一個很好的選擇。此研究設計一個應用於行動照護心電訊號擷取電路之動態取樣全數位類比數位轉換器。以壓控振盪器為主的類比數位轉換器(VCO-based ADC)可達到高的面積使用效率，以及高的數位整合度，這些都是行動醫療照護所需要的。此外，隨著製成的微小化，量化於時域的 VCO-based ADC 擁有較好的解析度。此研究設計一有效位數高於 8 位數的 VCO-based ADC 並以 90 奈米製程實現。此 ADC 可支援單一及多個通道的心電訊號擷取電路。

以單一通道應用而言，取樣頻率為 1k 赫茲，此 ADC 可達到 10.48 位數的有效位數此時的功率消耗為 6.08 瓦特。而在多通道的應用下，此設計可操作在 10k 赫茲底下，以提供 8 個通道的心電訊號擷取。可在維持有效位數為 9.64 位數的情況下，降低單一通道的功率消耗至 0.62 瓦特。

為了更進一步地降低 ADC 的功率消耗，我們根據生理訊號的特性提出動態取樣的機制。利用偵測訊號的變化程度，來調整 ADC 的解析度，使得在變化程

度低的區間 ADC 的功率消耗可大為減少。此機制可在失真率小於 5%的情況下達到 53% 的功率降低量。與現有的其他機制相比，此方法與有最高的功率降低效率。



An All-Digital ADC with Dynamic Sampling Technique for ECG Acquisition in Mobile Healthcare Applications

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Abstract

Heart attack becomes the top cause of death in the U.S. in 2011. The preventive medicine of the heart disease becomes more and more important. To reduce the effort for people going to the hospital, the mobile healthcare device is applied to monitor the electrocardiogram (ECG) signal. Here we design a VCO-based ADC for the ECG acquisition circuit in mobile healthcare applications. The VCO-based ADC has high area efficiency and high integration ability with the digital circuit which are suitable for the mobile device. And also benefits from the technology scaling. Using 90-nm CMOS process technology, the ENOB of more than 8-bit VCO-based ADC is implemented. It can support both single channel and multi-channel ECG acquisition circuit application.

For the single channel, the ENOB of ADC can reach 10.48 bits in sampling frequency of 1k Hz. The power consumption is 6.08 uW. For the multi-channel application, our design can operate in sampling frequency of 10k Hz and be turned off while sampling is finished. In the simulation result, the power of VCO-based ADC is 0.62uW/ channel for 8 channels application and achieves 9.64 bits of effective

number of bit.

To reduce the power consumption of our ADC, we apply the dynamic sampling technique to sense the variation of signal. Then we adjust the resolution of ADC based on the sensing result. This technique can reduce 53% power of ADC while keeping distortion less than 5%. Compare with other technique this work has best power reduction performance under the same distortion factor.

致謝

終於，我的碩士生涯告一段落了。在 SI2 的大家庭裡，我學到了許多事情，不論是課業上、研究上及做人處事上，都讓我成長不少。在這漫長的歲月裡我受到了許多人的幫助，在此要特別感謝那些幫助我給予我鼓勵的人們。

首先，要感謝我的指導教授　李鎮宜教授。李老師常常提醒我們所做的東西要從系統的概念下出發，從整個大方向給予我們指導。並且常常叮嚀我們除了研究之外更要兼顧健康，適時運動放鬆自己，才能有更好的表現。

接著，要感謝 SI2 的學長們。指導我的於爺，常給我許多研究上的幫助及鼓勵，並且常常包容我的一些小錯誤。新加入的何小杰，在口試前辛苦地幫我看了投影片，提醒我一些報告時該注意的地方。在電路設計上常給我許多意見的建螢及昆儒，有點嚴肅講話卻很好笑的宋仔，十分照顧學弟妹擅長當助教的 verilog 達人巴柏，因為有你們的協助，我們碩士研究才可以更加的充實。另外還有其他 430 的學長：阿龍學長、佳龍、長宏、義澤、欣儒、人偉，十分感謝你們給予我的鼓勵及意見。

另外還有一群一起奮鬥的夥伴們：經常互相鼓勵互相安慰的皮皮，常提供我很好的情緒抒發管道，並且一起在互相鞭策下成長。常給我很多各方面意見的美維，讓我可以從更多元的觀點思考問題。隨敲隨應的囧君，有什麼問題都不怕找不到人。陪我說說笑笑的雞皮，讓我的緊繃的生活可以得到放鬆。我的合作夥伴博堯，常常可以互相照應一起實施早起計畫。實驗室的奇葩恕平，常常帶動實驗室活潑的氣氛。以及許多其他給予我鼓勵的朋友們，因為有你們的陪伴，讓我的碩士生涯更加的愉快更有前進的動力。

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Chapter 1: Introduction

1-1 Motivation

Heart attack becomes the top cause of death in the U.S. in 2011. The preventive medicine of the heart disease becomes more and more important. To reduce the effort for people going to the hospital, the mobile healthcare devices are applied to monitor the electrocardiogram (ECG) signal. In the mobile healthcare system, it contains the acquisition circuit and the digital processor. The analog-to-digital converters (ADCs) are interfaced between the analog and digital domain which play the important role on influencing the performance of systems. The conventional ADCs quantize the voltage information in analog domain. However, as the technology scales, the supply voltages become lower. Therefore, the threshold voltage becomes relative high and results in the difficulty of converting signal in analog domain. And also for the reduction of voltage headroom for signal swing, the signal amplitude is reduced. With the same noise floor, the Signal-to-Noise ratio (SNR) becomes worse.

In contrast, the resolution in time domain is enhanced in the advanced CMOS process. It's better to deal with the signal in time domain rather than voltage domain. The Voltage-Controlled-Oscillator (VCO) based ADCs convert the voltage into the time domain take this advantage. The frequency of time-based signal is modulated by the input voltage, and the information is quantized and processed by the digital logic. The ADC resolution can be determined by the resolution in time domain rather than

voltage domain which is attractive for the low voltage advanced CMOS process. Another benefit for this type of ADC is that it is mostly composed by the digital blocks which can be compatible to the digital design flow and can be easily integrated with the digital system.

1-2 ECG acquisition circuit

1-2.1 ECG signal characteristic

Before we introduce the ECG acquisition circuit, we should understand the characteristic of ECG signal. The Electrocardiogram (ECG) signal is composed of three components: the common-mode signal, differential electrode offset and actual ECG signal as shown in Fig. 1-1.

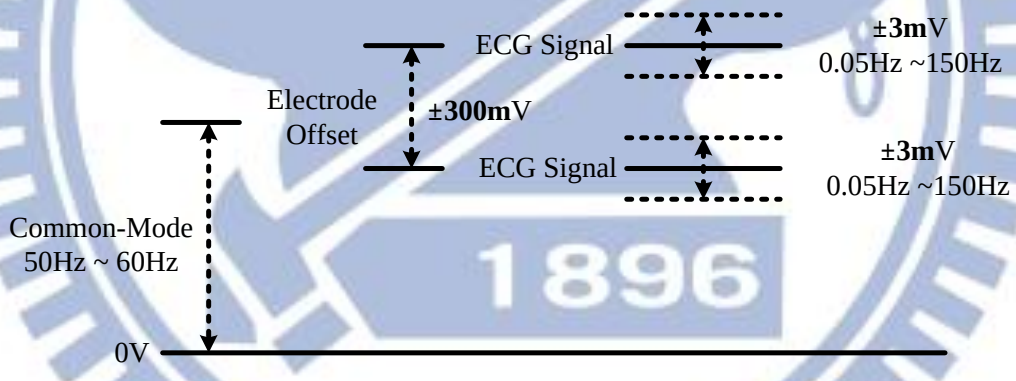


Fig. 1-1 Nature of ECG signal

Common-mode signal are the interferences of 50/60Hz power line coupling, motion artifacts, radio from other electronic equipment, etc. It can be reduced by increasing the isolation of ground of front-end and the ground of earth, or increasing the common mode rejection ratio (CMRR) of the front-end circuit by feeding the signal to cancel the common mode interference by mixed signal feedback loop [1], or driving the body with a common mode feedback (e.g. drive right leg (DRL) circuits for ECG measurement). Differential offset is caused by the different impedance of

electrode-skin interface, which is approximately up to 300mV and the front-end circuits should be made sure that the offset will not cause the saturation of acquisition circuit. It can be reduced by adding AC coupling capacitor, the high pass filter, or the servo feedback. The actual ECG signal appears in each lead is limited to ±6mV in differential amplitude and 0.05Hz to 150Hz in frequency.

1-2.2 ECG acquisition circuit block

Conventionally, an ECG acquisition circuit is consisted of an instrumentation amplifier (IA), a programmable gain amplifier (PGA), an antialiasing filter and an analog to digital convertor (ADC).

The instrumentation amplifier which has high common-mode rejection ratio (CMRR) and high input impedance is used as the input stage with a relative low gain to avoid the saturation due to the DC offset. Based on the resolution of ADC, there are two different approaches to process the signal [2]. The first one uses the high gain amplifier to amplify the signal significantly and uses a low resolution ADC to convert the amplified signal into digital value. In this kind of system, total gain is increased by adding the additional PGA as the main amplifier stage. The noise performance of this stage should be considered carefully to make sure that it will not dominate the total noise of system. Between the input instrumentation amplifier and the PGA, the high pass filter (HPF) should be added to remove the amplified DC offset. After the gain stage, the antialiasing filter is used before signal fed into the convertor. For the Nyquist rate convertor the antialiasing filter should be very sharp to avoid the aliasing noise. [2]

The other way is to use the low gain amplifier and the high resolution ADC to reduce the analog effort of the front-end circuit. In this way the additional amplifier is

removed. Only the low gain instrumentation amplifier is used to amplify the input signal. It makes the amplified noise is less than the traditional architecture, and also DC offset will not be amplified by the high gain amplifier that will not cause the saturation issue. The DC variation can be filtered in the digital domain after converted, so the DC block high pass filter can be eliminated. The active antialiasing filter can also be replaced by the simple RC filter. In this thesis, we design an ADC with low small input range to reduce the amplifier effort.

According to the numbers of input leads, the acquisition circuit can be divided into single-channel and multi-channel two groups. The single-channel contains only one lead at the input as shown in Fig. 1-2. For the ECG signal the sampling frequency of single-channel circuit is set to 1k Hz. The multi-channel contains more than one leads and use the analog MUX to choose the input for the ADC as shown in Fig. 1-3. The ADC for the multi-channel bio-potential acquisition circuit should operate in higher frequency at least N times of the single channel, where N is the channel number. Here, we target our design for both of these two operation ways.

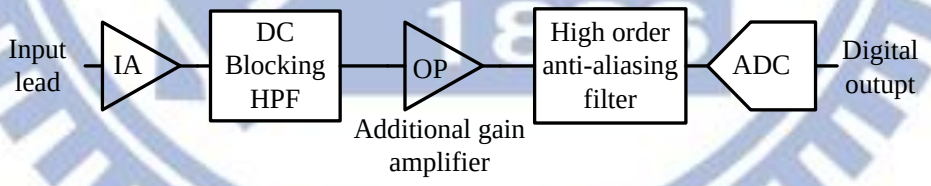


Fig. 1-2 Single channel bio-potential signal acquisition circuit

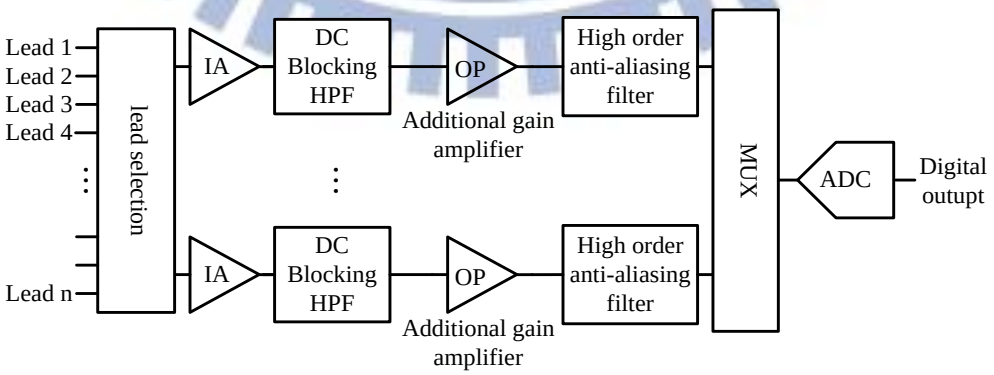


Fig. 1-3 Bio-potential signal acquisition circuit

1-2.3 Design Consideration

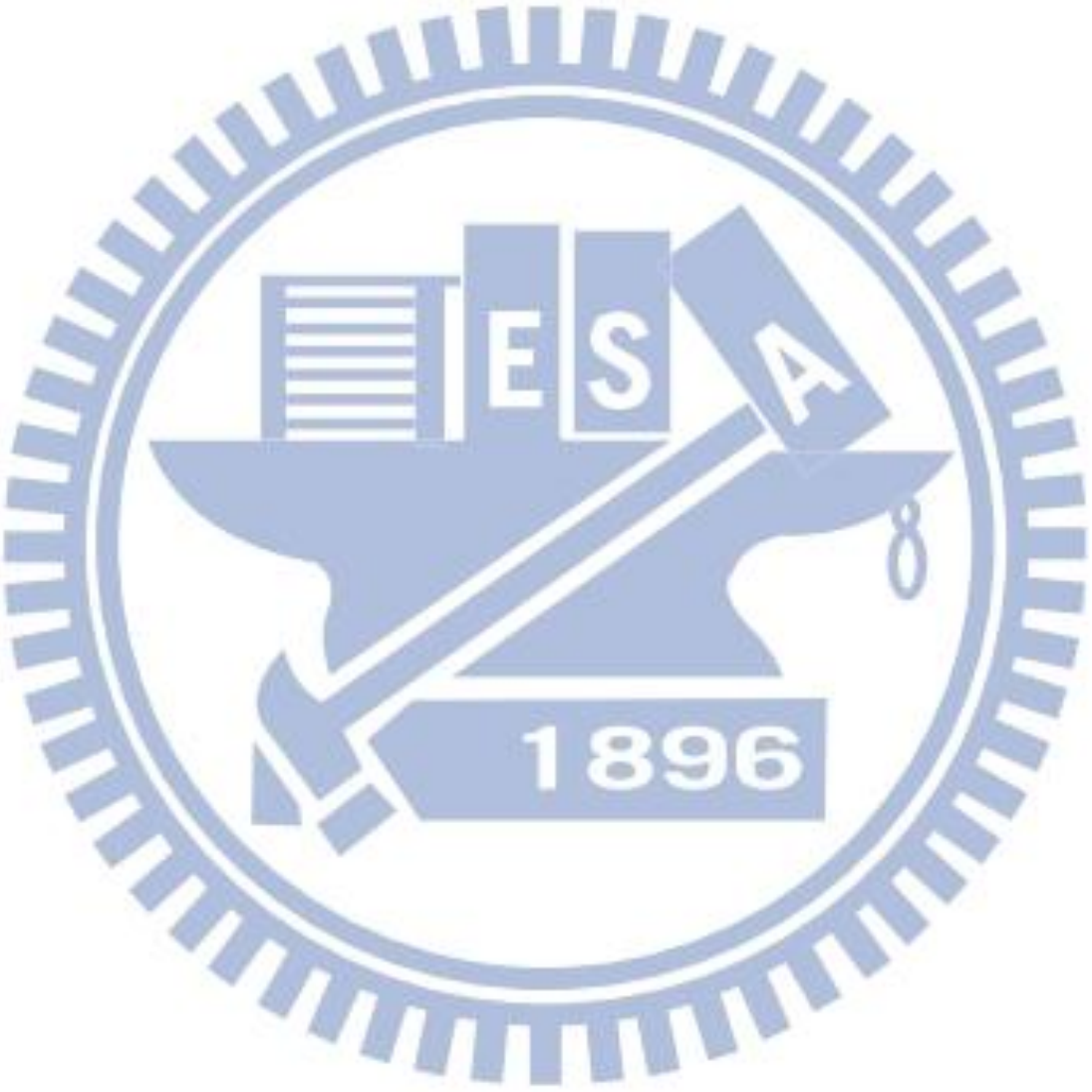
The design considerations for the ECG signal acquisition circuit is given in IEC 60601-2-47 medical electrical instrument standard [3]. First, the input signal is limited to ±6mV in differential amplitude. To get the information of such small amplitude, the resolution of system should more than 50uV/LSB. To achieve this requirement the resolution for ADC should be more than 6.9 bits. Here we design an ADC in 8 bits. The Bandwidth of the acquisition circuit should cover 0.05-150Hz. Second, the design should cover the temperature of 0~45℃. Third, the influence of DC offset and variation should be reduced to ±10%. Forth, the input refer noise of acquisition circuit should less than 50μVrms. Fifth, because of the high impedance of ECG electrodes, the input impedance of acquisition circuit should have high input impedance more than 10 MΩ. The last one is the circuit should have high CMRR which is more than 60dB to reduce the common mode interference. For single-channel application and multi-channel application the sampling frequency is 1k Hz and 10k Hz respectively. The design specification is summarized as follow:

Item	Specification
Input characteristic	Amplitude: ±6mVpp-diff Bandwidth: 0.05-150Hz DC offset: ±300mV (variation <±10%)
Sampling Frequency	1kHz (single-channel)/ 10k Hz (multi-channel)
Resolution	>50uV/LSB (8 bits)
Temperature	0-45℃
Input impedance @ 10MHz	>10 Mohms
CMRR	>60 dB
Input refer noise	<50 uVrms

Table 1-1SPECIFICATION (IEC 60601-2-47 [3])

Some of the requirements of ECG acquisition circuit are taken care by the IA in

the input stage. For the ADC we only consider the bandwidth of input, the input range after amplifying, the sampling frequency and the resolution.



Chapter 2: Theory

2-1 ADC Performance Item

Before we introduce the basic concept of VCO-based ADCs, we will first give some common performance items of ADC. The ADC performance items can generally be separated into two groups: dc accuracy and dynamic performance. For different application, the designer will focus on different type of performance item. For example, for the application which should deal with specific frequency should pay more attention on dynamic performance. For the applications that process dc-like input signal or the measured voltage is relative to some physical measurement, like temperature sensor, should care more about the dc accuracy. For our application, the ADC will sense the ECG signal whose accuracy should be considered and for specific input frequency of ECG signal, the dynamic performance should also be cared about. Here, we list some common items that we focus on.

2-1.1 DC accuracy

DC accuracy can be calculated by sending the sweep voltage as input to get the transfer function of ADCs. Based on the transfer function of ADCs we can define several performance items to estimate the characteristic of ADCs. Here we list two most important items:

Differential Nonlinearity (DNL)

For the ideal ADCs, the voltage difference between each transition should be equal to one Least Significant Bit (LSB). Here, the LSB of ADC means the step size of smallest level that ADC can convert as shown as follow:

$$LSB = \frac{VFS}{2^N} \tag{2.1}$$

where the VFS stands for full scale input and N represent the resolution of ADC. For the N-bit quantizer, it will have 2^N levels.The difference of the voltage transition space between one code to the next is call the differential nonlinearity (DNL) which can be calculated as below:

$$\mathrm{DNL} = \frac{V_{n+1} - V_n}{V_{LSB}} - 1 \tag{2.2}$$

Integral nonlinearity (INL)

The integral nonlinearity (INL) is the deviation of the code from the ideal transfer function. For simplifying the calculation, the ideal transfer function here we defined is the line that directly connects the “zero” and “full scale” of the ADC transfer instead of the best-fit line. The INL is determined by measuring the voltage at code transitions and comparing them to the ideal voltage. Here should be noticed that, the nonlinearity of ADC will cause the distortion. The INL will affect the dynamic performance of ADCs.

2-1.2 Dynamic performance

The other part is about dynamic performance. It is measured by sending a single tone frequency sine wave at input and performing the Fast Fourier Transform (FFT) on the output code of ADC. These types of performance estimate the noise performance in the frequency domain as shown in Fig. 2-1. The fundamental

frequency is the input frequency. Others are regarded as noise and characterized with respect to the desired signal.

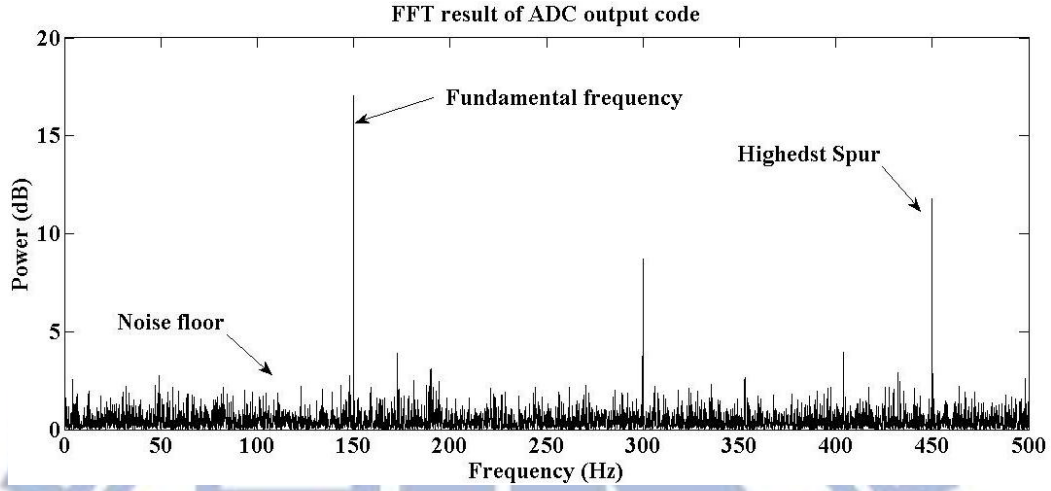


Fig. 2-1 FFT result of ADC output code

Signal-to-Noise Ratio (SNR)

The signal to noise ratio (SNR) is the ratio of power of fundamental signal to the power of noise floor, excluding the DC signal and the spur power as shown in equation(2.3). It is usually expressed in decibels (dB).

$$SNR(dB) = 20\log\left(\frac{V_{signal(rms)}}{V_{noise(rms)}}\right) \tag{2.3}$$

The noise power in SNR calculation doesn't include the harmonic distortion, only the quantization noise is considered. For the ideal ADC with given resolution N bits, the theoretical best SNR is as bellow:

$$SNR(dB) = 6.02N + 1.76 \tag{2.4}$$

Signal-to-Noise and Distortion Ratio (SiNAD also called SNDR)

For the SNR, the noise power doesn't contain the harmonic distortion power. For the SiNAD (SNDR), it gives more complete information about the noise behavior. SNDR calculates the ratio of signal power and noise power including both noise floor

and the harmonic distortion power as shown below:

$$SiNAD\ (SNDR) = 20\log\left(\frac{V_{sig}}{\sqrt{V_2^{\,2}+V_3^{\,2}+V_4^{\,2}+\ldots+V_n^{\,2}+V_{noise}^{\,2}}}\right) \tag{2.5}$$

where V_2 is the amplitude of the second harmonic, V_3 is the amplitude of third harmonic and so on. The other way to calculate the SiNAD (SNDR) is performed in time domain. First, record the output data of ADC and fit the sine wave to the data at the sending frequency. Then the rms noise can be calculated by

$$rms\ noise = \left[\frac{1}{M}\sum_{n=1}^{M}(y_n - y_n')^2\right]^2 \tag{2.6}$$

where

y_n : output data of ADC

y_n' : best-fit sine wave

M : number of record data

The SiNAD (SNDR) can be calculated by equation(2.7)

$$SiNAD\ (SNDR) = \frac{rms\ signal}{rms\ noise} \tag{2.7}$$

Where rms signal is equal to sine wave peak/$\sqrt{2}$.

Spurious-Free Dynamic Range (SFDR)

Spurious-Free Dynamic Range (SFDR) is the magnitude difference between signal and the highest spur peak as shown in Fig. 2-2. Most of highest spur occurs on the second harmonic frequency, but it may not always be.

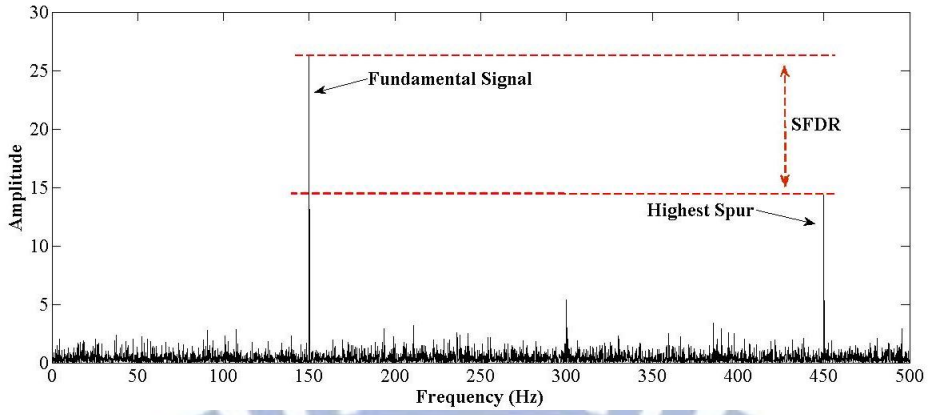


Fig. 2-2 Illustration of SFDR

Effective number of bits (ENOB)

Effective number of bits (ENOB) is the one of the method comparing the rms noise of ADC to the quantization noise of the ideal ADC which has that amount of bits of resolution. For example, if a real 8-bit ADC has ENOB of 7; the rms noise it produces is equal to the one ideal 7-bit ADC produces. There are two common methods to calculate the ENOB. The first one is converted from SNDR by equation(2.8). This formula is similar to the relation between the SNR and ADC resolution in equation(2.4).

$$ENOB = \frac{SNDR - 1.76(dB)}{6.02} \tag{2.8}$$

The second one is to be calculated in the time domain as shown in equation(2.9), where the rms noise is calculated by equation(2.6).

$$\begin{aligned} ENOB &= N - \log_2\left(\frac{rms\ noise}{ideal\ rms\ quantization\ error}\right) \\ &= \log_2\left(\frac{full\ scale\ range}{rms\ noise \times \sqrt{12}}\right) \end{aligned} \tag{2.9}$$

2-2 VCO-based ADC

Here we introduce some basic concept of VCO-based ADC and some non-ideal effects that reduce the performance of ADC.

2-2.1 Architecture

The conventional ADCs are built using analog circuit and quantize the input in voltage domain directly. For the VCO-based ADCs, they convert the analog input into time information that quantized by the digital circuit as shown in Fig. 2-3.

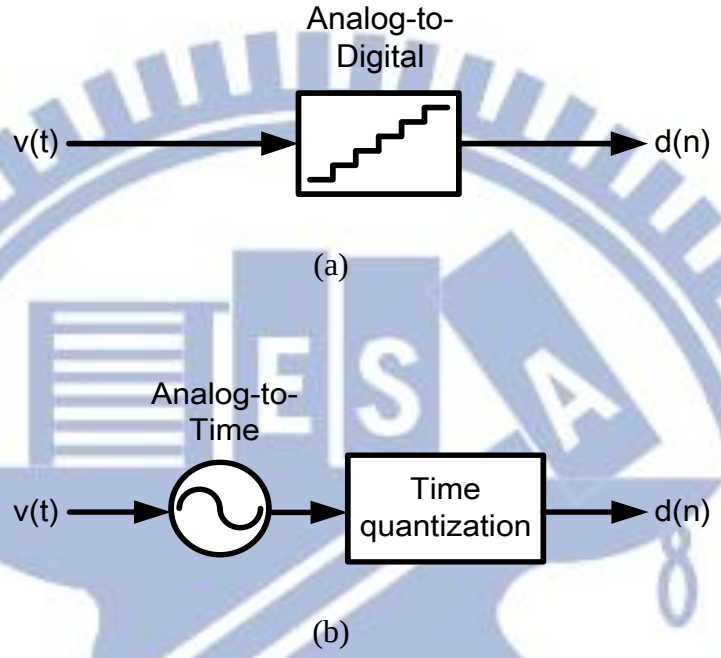


Fig. 2-3 (a) Conventional ADC (b) VCO-based ADC

The VCO converts the analog signal to the phase domain by producing the output whose frequency is proportional to the average of input signal. The counter which is connected followed by the VCO calculates the VCO oscillation number in the given sampling period.

For the single phase VCO-based ADC, the architecture is shown as Fig. 2-4. It applies only single counter to sense the transition of 1-phase VCO. The timing diagram of this architecture is shown as Fig. 2-5.The counter value is read out at the end of very cycle can be seen as the ADC output which has the relation with the analog input as equation(2.10). After value of counter is read, the counter is reset to zero for next sampling counting.

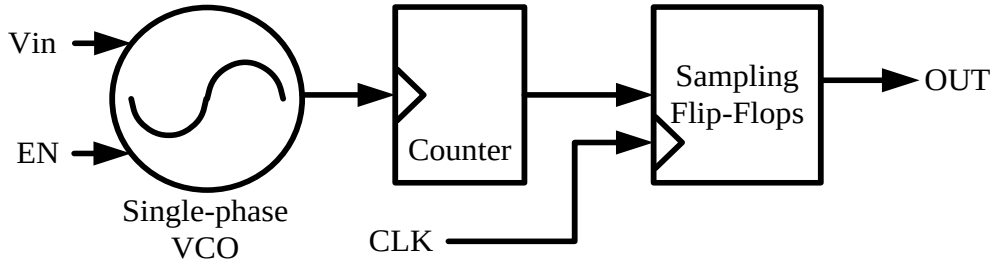


Fig. 2-4 Single phase VCO-based ADC

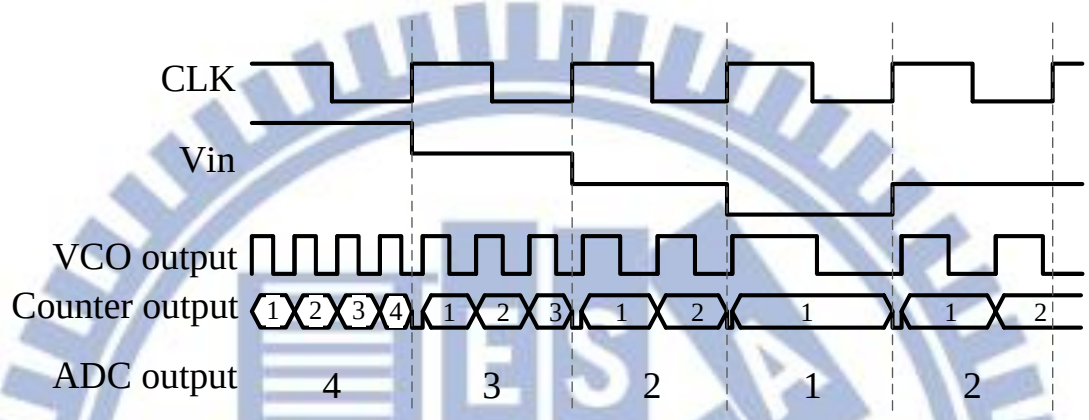


Fig. 2-5 Timing diagram of single-phase VCO-based ADC

$$\begin{aligned} \text{ADC digital output } D(n) &= \frac{\text{Time for VCO oscillation number calculation}}{\text{VCO oscillation period}} \\ &= \frac{P_s}{P_{VCO}(t)}, \text{usually the counter counts whole sampling period} \\ &= \frac{F_{vco}(t)}{F_s} \end{aligned} \tag{2.10}$$

where P_s : Period of sampling CLK

P_{vco} : Period of VCO which is modulated by the analog input

F_s : Frequency of sampling CLK

F_{vco} : Frequency of VCO which is modulated by the analog input

For the single-phase VCO-based ADC the resolution of ADC is depended on the relation between the sampling frequency and the frequency range of VCO as shown below:

$$
\begin{aligned}
\textit{ADC resolution } B &= ceil\left\{\log 2\left(\max(D)-\min(D)\right)\right\} \\
&= ceil\left\{\log 2\left(\frac{\textit{Time for VCO oscillation}}{\min(P_{vco})}-\frac{\textit{Time for VCO oscillation}}{\max(P_{vco})}\right)\right\} \\
&\quad (\textit{usually the osillation cover whole sampling period}) \\
&= ceil\left\{\log 2\left(\frac{\max(F_{vco})}{F_s}-\frac{\min(F_{vco})}{F_s}\right)\right\} \\
&= ceil\left\{\log 2\left(\frac{F_{vco\_range}}{F_s}\right)\right\}
\end{aligned}
\tag{2.11}
$$

The other type of architecture is the multi-phase VCO-based ADC. Counters are applied to more than one phase of VCO as shown in Fig. 2-6, 3-phase VCO-based ADC for example. The ADC output is got by adding the counter value for each phase. In this type of VCO-based ADC, for the N-phase VCO, the resolution can be N times than the single phase one. The timing diagram of the 3-phase VCO-based ADC is shown in Fig. 2-7. However, the power and the complexity of multi-phase VCO-based ADC increase, so for our design, we choose the single-phase VCO-based ADC.

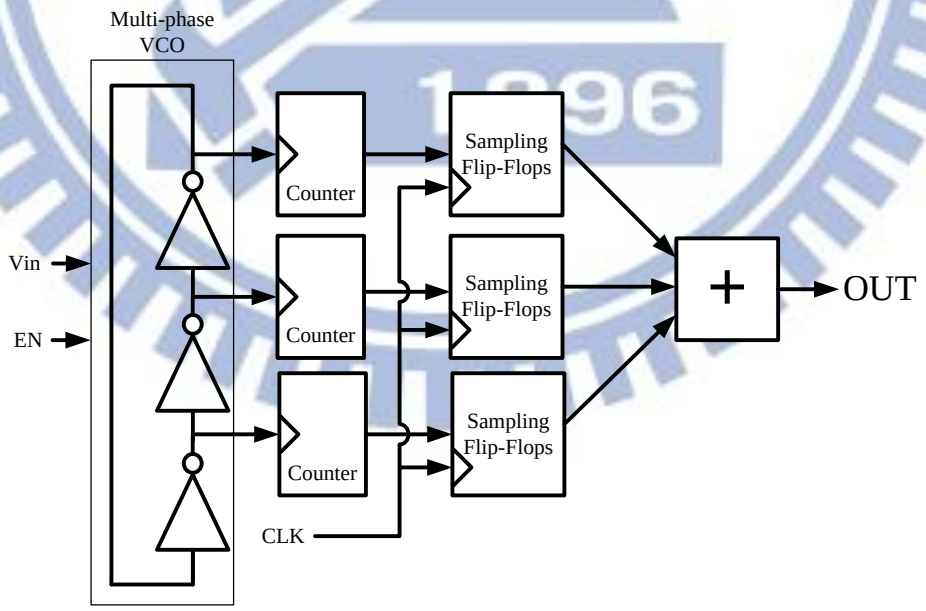


Fig. 2-6 Multi-phase VCO-based ADC

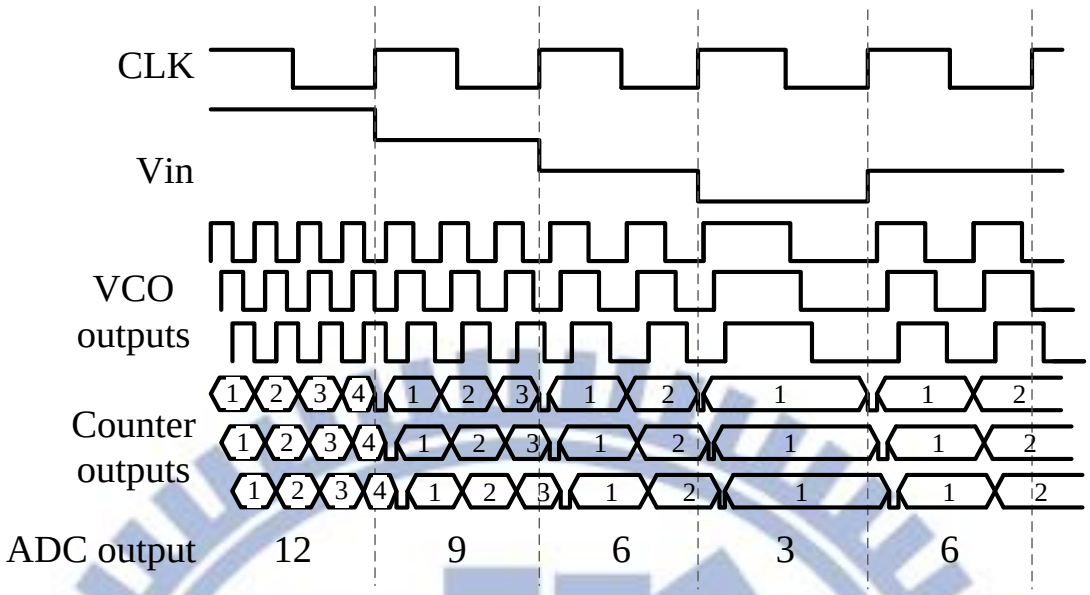


Fig. 2-7 Timing diagram of multi-phase VCO-based ADC

2-2.2 Sample and hold action

Usually, the sample and hold circuit is required when the input voltage is in high frequency relative to the operation of A/D process. In [4], it gives the analysis for the omitting of the sample and hold circuit. We consider the sine wave input as

$$V_{IN}(t) = A\sin(2\pi f_{IN} t) \tag{2.12}$$

Where A is the amplitude and f_{IN} is the input frequency. We set T_C as the maximum conversion time of the voltage control delay cell which is the largest time difference between the input and output digital edge for any input. The input voltage cannot change more than V_{LSB} within T_C. This set the upper bound for input voltage slope

$$slope = \frac{dV_{IN}}{dt} = 2\pi A f_{IN} \le \frac{V_{LSB}}{T_C} \tag{2.13}$$

Where

$$V_{LSB} = \frac{2A}{2^D - 1} \tag{2.14}$$

D is the resolution of ADC. Combine and rearrange the equation(2.13) and equation(2.14)

$$f_{IN} \le \frac{1}{\pi(2^D - 1)T_C} \tag{2.15}$$

If the input frequency and the conversion time satisfy the condition in equation(2.15), the ADC without sample and hold circuit can even achieve the resolution D as the same as the one with sample and hold circuit.

2-2.3 First-order noise shaping

The counter for VCO-based ADC can be seen as the phase quantizer. It quantizes the phase by counting rising or falling edge during sampling period. The step of quantization is 2π for single edge trigger. For both rising and falling edge trigger the quantization step is π . For the multi-phase VCO-based ADC with N phases, the quantization step is $2\pi / N$ for single edge trigger and π / N for double edge trigger.

The phase residue of quantization error will be passed to the next sampling as the initial phase as shown in Fig. 2-8. We set $\phi_q[n]$ as the quantization error in nth sample which will be equal to the initial phase of (n+1)th sample $\phi_i[n+1]$ and $\phi_x[n]$ as the VCO phase change due to the analog input in nth sample. The output of VCO quantizer can be represented as

$$\begin{aligned} y[n] &= \frac{N}{2\pi}(\phi_x[n] + \phi_i[n] - \phi_q[n]) \\ &= \frac{N}{2\pi}(\phi_x[n] + \phi_q[n-1] - \phi_q[n]) \end{aligned} \tag{2.16}$$

The result of taking the z-transform of equation(2.16) is shown as below:

$$Y(z)=\frac{N}{2\pi}\left(\Phi_x(z)+(z^{-1}-1)\Phi_q(z)\right) \tag{2.17}$$

We can see that the quantization error term is first-order shaped, hence, it can be said that the VCO-based ADC has the same performance compared with the first-order delta-sigma ($\Delta\sum$) ADC.

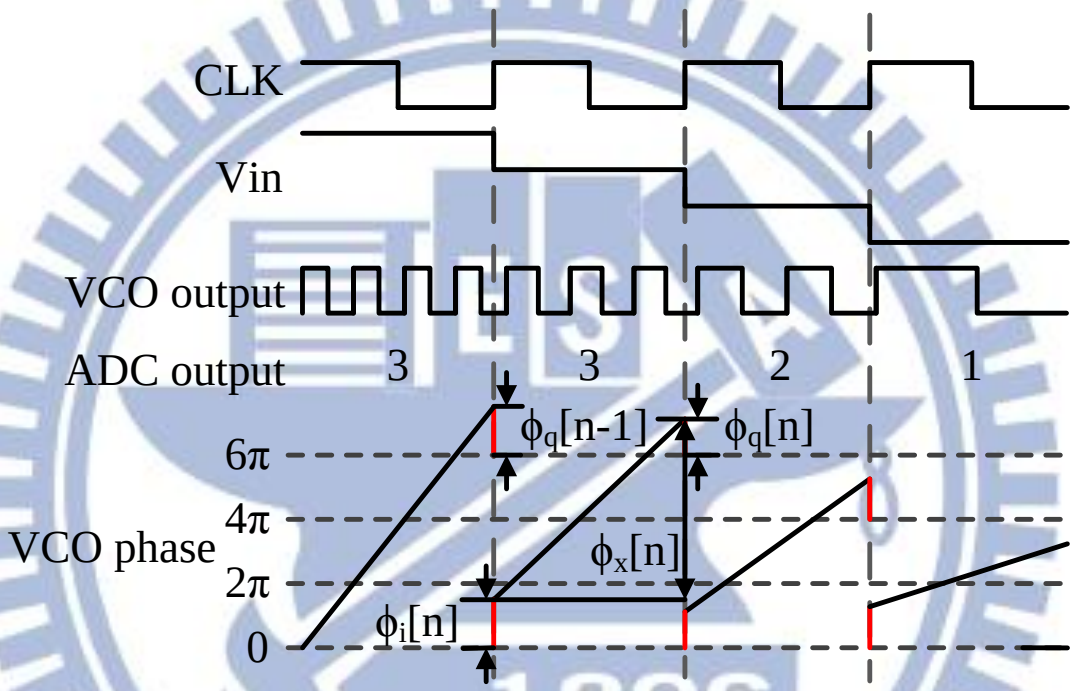


Fig. 2-8 Operation principle of VCO phase quantization

2-2.4 SNR

In [5] it gives the derivation of the Signal-to-Noise Ratio (SNR) of VCO-based ADC. It applies the input $x(t)$ as the sinusoid wave in frequency ω_{in} with amplitude A as equation(2.18).

$$x(t)=A\cos(\omega_{in}t) \tag{2.18}$$

The phase domain input $\phi_x[n]$ can be written as

$$\begin{aligned}\phi_x[n] &= \int_{(n-1)Ts}^{nTs} 2\pi(K_{VCO}x(t)+f_0)dt \\ &= \int_{(n-1)Ts}^{nTs} 2\pi(K_{VCO}A\cos(\omega_{in}t)+f_0)dt \\ &= \frac{2\pi K_{VCO}A}{\omega_{in}} 2\cos\left(\frac{\omega_{in}Ts(2n-1)}{2}\right)\sin\left(\frac{\omega_{in}Ts}{2}\right)+f_0Ts \\ &= \underbrace{2\pi K_{VCO}ATs\,\mathrm{sinc}(f_{in}Ts)}_{A_\phi}\cos\left(\frac{\omega_{in}Ts(2n-1)}{2}\right)+f_0Ts \end{aligned} \quad (2.19)$$

where Ts is the sampling period, f_0 is the free-running frequency of VCO and K_{VCO} is the gain of VCO. The power of signal in phase domain is

$$P_{\phi_x} = \frac{1}{2}A_\phi^2 \quad (2.20)$$

And for the N phase VCO-based ADC the power of quantization noise which is derived in [6] is shown as follows:

$$P_n = \frac{1}{12}\left(\frac{2\pi}{N}\right)^2\frac{\pi^2}{3}\left(\frac{1}{OSR}\right)^3 \quad (2.21)$$

Where $OSR(Over\ Sampling\ Ratio) = \frac{f_s}{2f_{in}}$, f_s represents the sampling frequency and f_{in} represents the input frequency. Finally, the SNR can be calculated by

$$\begin{aligned} SNR &= \frac{P_{\phi_x}}{P_n} \\ &= 6.02M - 3.41 + 30\log OSR + 20\log\left(\mathrm{sinc}(\frac{1}{2OSR})\right) \end{aligned} \quad (2.22)$$

where M is the resolution of ADC as shown in equation(2.23) for N phases VCO-based ADC.

$$M = \log_2(\frac{f_{range}N}{f_s}) \quad (2.23)$$

It should be noted that the influence of the quantization resolution M is different

from the traditional delta-sigma modulator. For the VCO-based ADC, M is inversely proportional to the sampling rate while for the delta-sigma ADC M is proportional to the sampling rate. Another phenomenon should be noted is the low pass filter characteristic of the VCO-based ADC. The average nature of VCO and the absence of the S/H causes the last term of the equation(2.22) which is the sinc -shaped function that filter out the integer multiples of the sampling frequency. This phenomenon causes the reduction of SNR as input frequency increase. When VCO-based ADC is operated in the Nyquist rate, the SNR is reduced by 3 dB and the signal near the integer multiples of the sampling frequency is filtered out.

2-2.5 Non-ideal effects

In the real world there are some non-idealities need to be considered, such as jitter, nonlinearity, mismatch, metastability. These non-ideal effects reduce the performance of the VCO-based ADC. Here, we take these effects into consideration and give the analysis of the influence. These analyses can be referred to [5].

Jitter of sampling CLK

The sampling CLK for VCO-based ADC is not only used for sampling data as other types of ADC but also applying the reference time for integrating the phase of VCO. The effects of jitter of sampling CLK can be separated into two groups: the sampling uncertainty due to the vibration of the rising edge and the integration error caused by the unequal period. The former one is influenced by the absolute jitter $\tau_{aj}[n]$ which is defined as the time difference between the nth edge of the ideal and the practical CLK. The later one is affected by the period jitter $\tau_{pj}[n]$ which is defined as the time difference between nth period of the ideal and the practical CLK as shown in Fig. 2-9. The phase domain input including jitter is written as

equation(2.24).

$$\phi_{x,sj}[n] = \int_{(n)T_s+\tau_{aj}[n]}^{(n+1)T_s+\tau_{aj}[n+1]} 2\pi(K_{VCO}x(t) + f_0)dt \tag{2.24}$$

This equation can be separated into the original phase information ($\phi_x[n]$) phase error term caused by the sampling uncertainty ($\phi_{\varepsilon,su}[n]$) and phase error caused by the integration time ($\phi_{\varepsilon,it}[n]$). It can be reorganized into equation(2.25).

$$\phi_{x,sj}[n] = \phi_x[n] + \phi_{\varepsilon,it}[n] + \phi_{\varepsilon,su}[n] \tag{2.25}$$

where

$$\begin{aligned}\phi_{\varepsilon,it}[n] &= 2\pi\left(K_{VCO}x((n+1)T_s + f_0\right)\tau_{pj}[n] \\ \phi_{\varepsilon,su}[n] &= 2\pi K_{VCO}\left(x((n+1)T_s) - x(nT_s)\right)\tau_{aj}[n]\end{aligned} \tag{2.26}$$

In [5], it concludes the influence of jitter: the effect of absolute jitter of VCO-based ADC is the same as the conventional ADC since the reduction of the SNR cause by sampling uncertainty doesn't depend on the time domain or voltage domain procession; the influence of period jitter is increase as the free running frequency f_0 is decreased, so to minimize the effect of period jitter, free running frequency should be reduced.

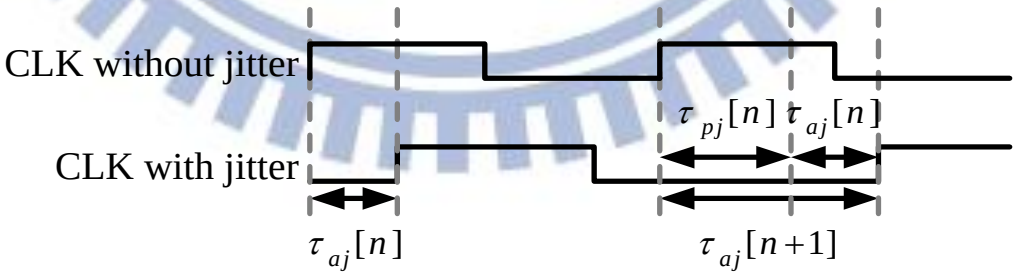


Fig. 2-9 Illustration of jitter definition timing diagram

VCO phase noise

The phase noise of VCO can be seen as an additional voltage noise source is

applied at the input and is converted into the frequency through the gain of VCO. As shown in Fig. 2-10, for a given constant voltage v_{ctrl}, the output frequency of the VCO with conversion gain, K_{VCO} should be the constant value, $K_{VCO}V_{ctrl}$. But if there is a noise source at input, the output frequency will vary in a certain interval. This phenomenon in frequency domain can be characterized in phase noise performance.

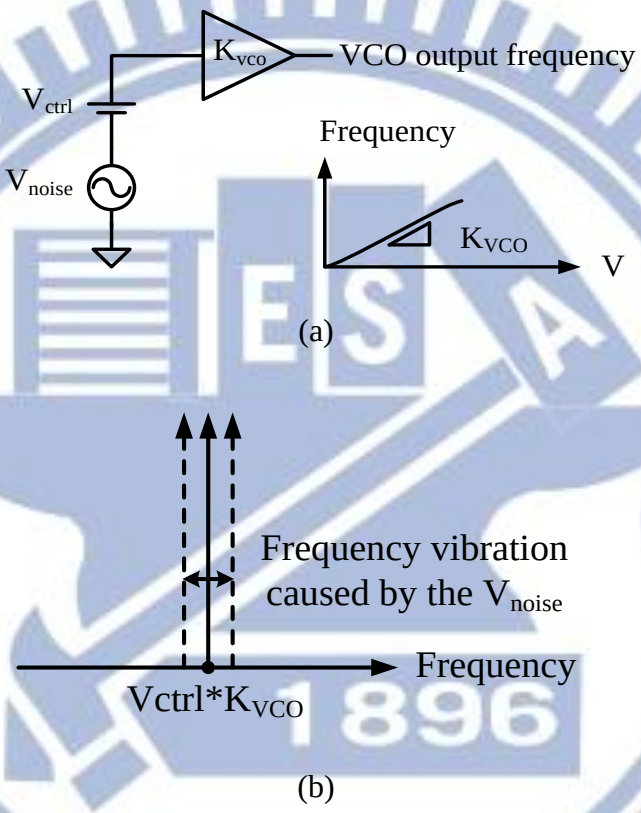


Fig. 2-10 VCO phase noise; (a) phase noise model (b) illustration of phase noise

Based on the description above, the output of VCO-based ADC in phase domain can be represented as follows:

$$\begin{aligned}\phi_{x,pn}[n] &= \int_{nT_s}^{(n+1)T_s} 2\pi(K_{VCO}x(t) + f_0 + K_{VCO}v_n(t))dt \\ &= \phi_x[n] + \int_{nT_s}^{(n+1)T_s} 2\pi K_{VCO}v_n(t)dt \\ &= \phi_x[n] + \phi_{pn}((n+1)T_s) - \phi_{pn}(nT_s) \end{aligned} \quad (2.27)$$

where $v_n(t)$: *input refer noise of the VCO*

ϕ_{pn} : *output phase noise of the VCO*

Taking z-transform of equation (2.27), we can get the result as below:

$$\Phi_{x,pn}(z) = \Phi_x(z) + (z-1)\Phi_{pn}(z) \tag{2.28}$$

It shows that the phase noise of VCO-based ADC is first-order shaped. [5] We further derive the SNR influenced by the VCO phase noise which is shown in equation(2.29). It assumes the VCO has phase noise Ł [dBc/Hz] at the frequency offset, f_{offset} and f_{in} is denoted as the frequency of input signal.

$$SNR_{vpn} = 10\log\left(\frac{(K_{VCO}A)^2}{16Łf_{offset}^2 f_{in}}\right) \tag{2.29}$$

VCO tuning characteristic nonlinearity

The VCO is the key component to convert the analog domain voltage signal into the frequency or phase information. Nonlinearity of VCO tuning characteristic directly influences the linearity of the digital code of the VCO-based ADC. It causes the harmonic spurs occur at the ADC output spectrum and reduces the SNDR of ADC. We expand the VCO gain as the high order polynomial and the phase caused by the nonlinearity of VCO can be represented as follows:

$$\phi_{x,nl}[n] = \int_{(n-1)Ts}^{nTs} 2\pi(f_{fr} + K_{VCO}x(t) + a_2x(t)^2 + a_3x(t)^3 + \cdots)dt$$

where

$$x(t) = A\cos(\omega_{in}t) \tag{2.30}$$

[5] shows the power of second and third harmonic spurs as below:

$$P_{2\omega_{in}} = \frac{(2\pi)^2}{2f_s^2}\left(\frac{1}{2}a_2A^2 + \cdots\right)^2 \operatorname{sinc}^2\left(\frac{2f_{in}}{f_s}\right) \tag{2.31}$$

$$P_{3\omega_{in}} = \frac{(2\pi)^2}{2f_s^{\,2}}\left(\frac{1}{4}a_3A^3+\cdots\right)^2 \operatorname{sinc}^2\left(\frac{3f_{in}}{f_s}\right) \tag{2.32}$$

We can see that the nth harmonic spur is filtered by sinc function which has the nulls at the integrate multiples of f_s. This effect causes the intermodulation products between two signals larger than the input harmonic spurs.

Metastability of flip-flops

For the VCO-based ADC, the counter is usually applied for the phase quantization. The VCO triggers the counter at the signal transition edge and after the counter the sampling flip-flops are applied to capture the value of counter. The sampling flip-flops are triggered by the rising edge of sampling CLK of ADC. If the edge between the VCO transition edge and the sampling CLK are too close, the counter is not ready to be sampled. It causes the timing violation of the sampling flip-flops. The uncertainty result of sampling value reduces the performance of ADC. This phenomenon is called the metastability of flip-flops. In [7], it gives the detail definition of the metastability. The definition of metastability requires some timing item: setup time t_{su} , hold time t_h , propagation delay t_{pcq} and metastable window t_{ms} as shown in Fig. 2-11 and Fig. 2-12.

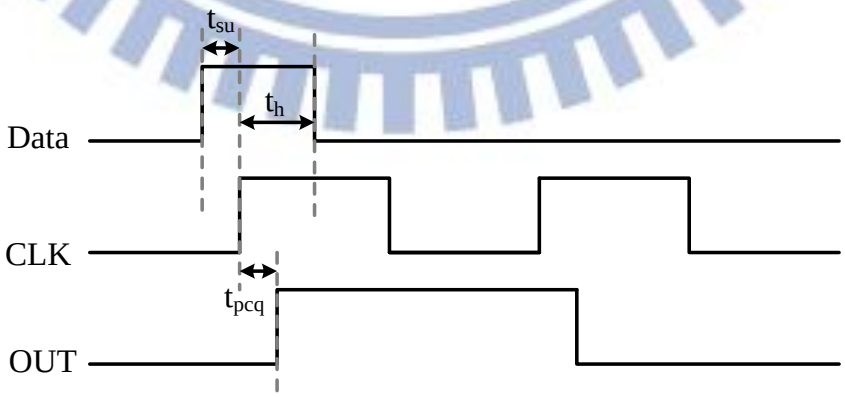


Fig. 2-11 Illustration of timing item definition

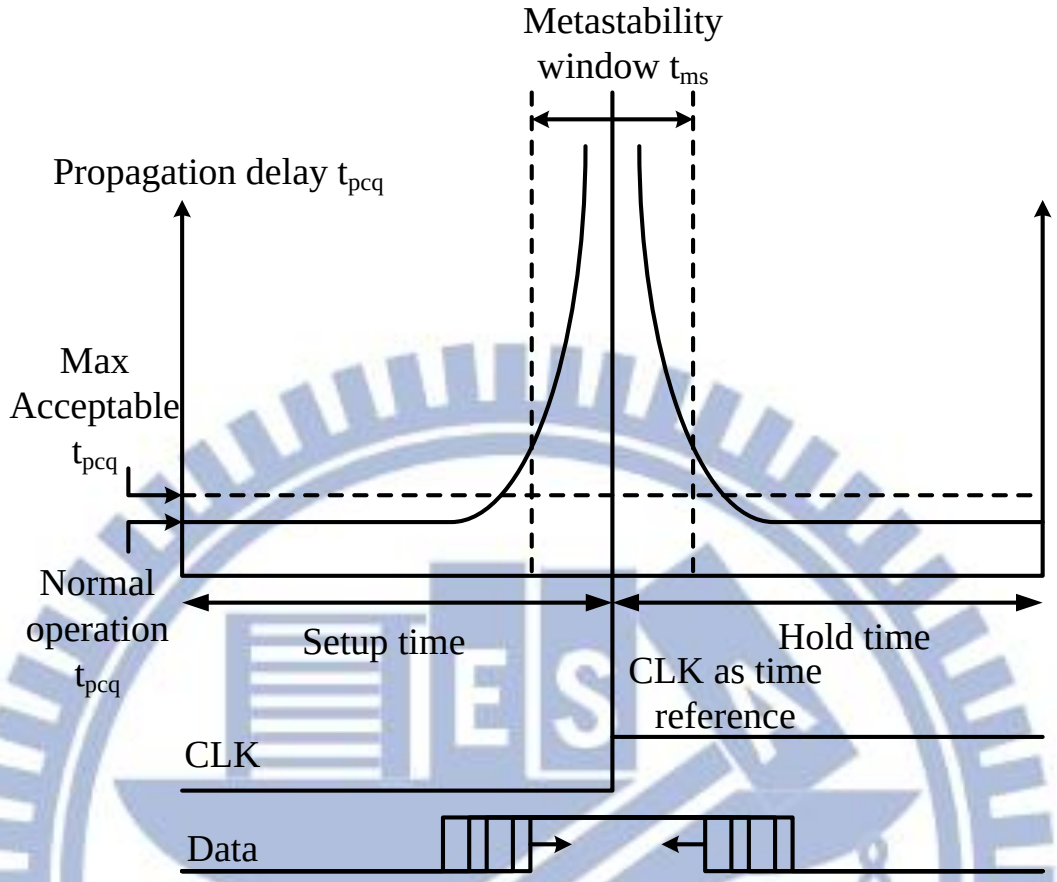


Fig. 2-12 Definition of metastability window

2-3 VCOs

In the barkhausen criteria it states that for negative-feedback circuit to oscillate at ω_0 its loop gain should satisfy the two conditions:

$$|H(j\omega_0)| \geq 1 \tag{2.33}$$

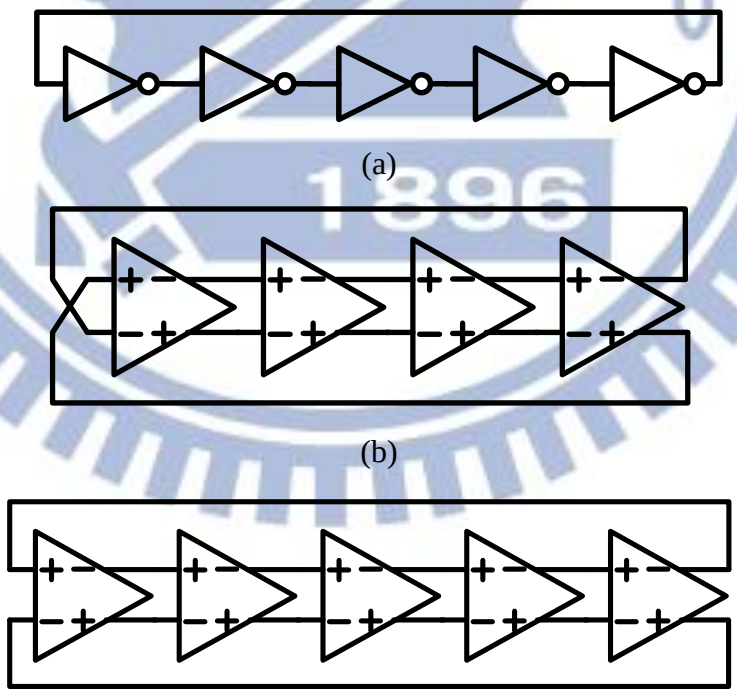
$$\angle H(j\omega_0) = 180° \tag{2.34}$$

These conditions are necessary but not sufficient for oscillation. There are two main topologies of CMOS oscillator in today's technology: the ring VCO and the inductance (L) and capacitance (C) VCO. LC VCO operates at the resonant frequency of the inductor and capacitor while the ring VCO consists of a loop with an inversion stage. Although the LC VCO has good performance in phase noise, it requires large

area for its passive elements and has poor integration and more complicated design. And for the power performance, the ring VCO consumes less power than the LC VCO at low oscillation frequency [8]. For above reasons, we choose the ring VCO for our VCO-based ADC.

2-3.1 Ring oscillator basics

The ring oscillator consists of a delay cell loop which the output of the last cell of the chain fed into the first element with an inversion net. Depending on the signal in the loop, there are two kinds of architecture of ring oscillator: single-end and differential ring oscillator. For both of two types the total inversion number should be odd. As shown in Fig. 2-13, the single-end oscillator should have odd inversion stage and for the differential oscillator the stage number can be odd or even but with a stage connected inversely.



(a)

(b)

(c)

Fig. 2-13 Ring oscillators: (a) single-end oscillator (b) differential oscillator (odd stage) (c) differential oscillator (even stage with inverted net)

For all kinds of ring oscillators, the oscillation frequency is given by equation(2.35).

$$f_{osc} = \frac{1}{N*(t_{PHL} + t_{PLH})}$$

$$\begin{aligned} &where\ N: number\ of\ \ stage \\ &\quad t_{PHL}: propagation\ delay\ of\ \ high\ to\ low\ transition \\ &\quad t_{PLH}: propagation\ delay\ of\ \ low\ to\ high\ transition \end{aligned} \qquad (2.35)$$

If we denote C_L as the loaded capacitance in each node in delay chain which contains the total gate capacitance of input transistors, the total drain capacitance of output transistors, the additional loading capacitance and the routing capacitance. The delay for each stage is determined by the time for charging and discharging the C_L.The time for discharging the C_L from VDD to VSP with the constant I_{D1} is

$$t_1 = C_L \times \frac{VDD - VSP}{I_{D1}} \qquad (2.36)$$

While the time for charging the C_L from 0 to VDD with the constant I_{D2} is

$$t_2 = C_L \times \frac{VSP}{I_{D2}} \qquad (2.37)$$

Then we can find that t_{PHL} and t_{PLH} we talked before is equal to t_1 and t_2 respectively when VSP is set to VDD/2. If we assume $I_{D1} = I_{D2} = I_D$, the sum of t_{PHL} and t_{PLH} is shown as equation(2.38).

$$t_{PHL} + t_{PLH} = C_L \times \frac{VDD}{I_D} \qquad (2.38)$$

The oscillation frequency defined in equation (2.35) can be rewritten as

$$f_{osc} = \frac{I_D}{N \times C_L \times VDD} \tag{2.39}$$

In equation(2.39), it is clear that the oscillation frequency is controlled by stage number N, the current I_D, the loading capacitor C_L and the supply voltage VDD. The stage number N is hard to be modulated by the analog signal. C_L can be controlled by the varactor, but the linearity of this conversion is poor. Control VDD will also affect the I_D and the conversion has great linearity performance. We will take this type of oscillator into consideration for our design. I_D can be controlled by the current-controlled cell which is the most basic type of ring oscillator structure and the threshold voltage both of these two types of VCO will be simulated in the following sections.

2-3.2 Jitter

In [9], it states the jitter prediction equation for single-end and differential ring oscillator. First, it specifies a time window ΔT which is defined as N cycles delay after triggering. Then it calculates the histogram of the crossing of the testing signal during the window. The deviation of this histogram result is denoted as $\sigma_{(\Delta T)}$. Then we can find the relationship between standard deviation $\sigma_{(\Delta T)}$ and any delay ΔT in equation(2.40). Other time domain measurement such as cycle jitter or cycle-to-cycle jitter can be seen as the special case of the two-sample standard deviation. Although we develop the result presenting in periods of signal cycle, the result is also valid when developing in individual gate delays. The figure-of-merit κ is the bridge connecting the jitter at any delay to a description of jitter process in one gate delay.

$$\sigma_{(\Delta T)} = \kappa\sqrt{\Delta T} \tag{2.40}$$

It also gives the jitter performance comparison between the single-end and differential ring VCO. It denotes noise source has a voltage density of e_n $[V/\sqrt{Hz}]$. The VCO has control constant K_0 [rad/V*s] and the center frequency of $\omega_0 = 2\pi f_0$. The κ of both single-end and differential VCO is shown as below:

Single-end ring VCO:

$$\kappa = \sqrt{\left[2.00 + 2.66\left(\frac{V_{DD}}{V_{DD} - V_t}\right)\right]\frac{kT}{I_{PK}V_{DD}} + 0.50\left(\frac{K_0}{\omega_0}\right)^2 e^2_{n(CTL)}} \tag{2.41}$$

Differential ring VCO:

$$\kappa = \sqrt{\left[4.82 + 1.44\left(\frac{V_{SWING}}{V_{DEGEN}}\right)\right]\frac{kT}{I_{TAIL}V_{SWING}} + 0.50\left(\frac{K_0}{\omega_0}\right)^2 e^2_{n(CTL)}} \tag{2.42}$$

It states that for the best fundamental jitter performance, the single-end ring VCO is preferred. Single-end ring VCO has several advantages shown as below:

A. Better jitter performance for given supply voltage since single-end ring has larger swing than fully differential VCO. $V_{SWING} < V_{DD}$
B. Better jitter performance for given current since single-end ring has smaller average current than fully differential VCO. Peak current I_{PK} only occurs during the transition for single stage while bias current I_{TAIL} flows in every stage continuously.
C. Single-end ring VCO doesn't need the bias source, avoiding the additional noise contribution.

Chapter 3: Proposed VCO-based differential input ADC

3-1 Brief Architecture

Our VCO-based ADC architecture with differential input is shown in Fig. 3-1. The input signals VIN+, VIN- modulate the VCO frequency individually. Two counters are applied for both VCOs and quantize the frequency of VCO into digital values. As considering power issue, asynchronous counter is applied for reducing the dynamic power for data transition. To avoid sampling the counter value during counter propagating, we use two group flip-flops to sample the counter for each terminal and apply a determination circuit to choose the proper result. And also for the power consideration, we use the flip-flop with gated input (G-FF) to reduce the spur power. To avoid the metastability of flip-flop sampling, we disable the counter earlier before sampling. The differential information is got by subtracting counter value of each end. We design the circuit in UMC 90nm CMOS technology process. The details for each block will show in the following sections.

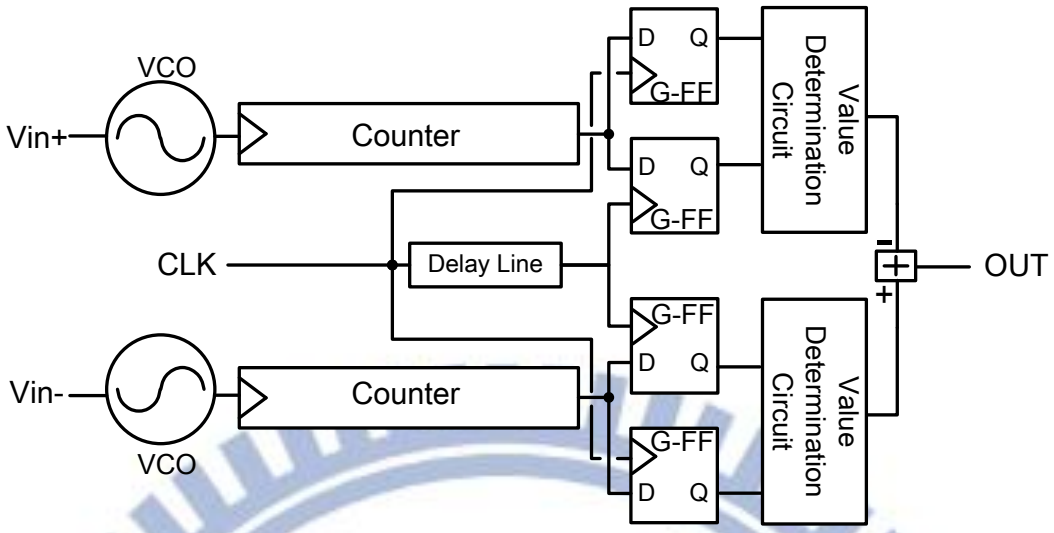


Fig. 3-1 VCO-based ADC architecture

3-2 VCO Design

For the VCO-based ADC, VCO is the key component which has great influence on the performance. Here, we choose the inverter-based ring VCO for simpler design and smaller area. The basic invertor-based ring oscillator is shown as Fig. 3-2. Each stage of ring oscillator is consisted of the invertor-like cell. According to the introduction in section 2-3.1 , the frequency of ring oscillator is calculated as

$$f_{osc} = \frac{1}{N(t_{PLH} + t_{PHL})} \approx \frac{I_D}{N \times VDD \times C_L} \quad (3.1)$$

where C_L is the input and output capacitance. In [10], it gives the digital model for the MOS transistor as shown in Fig. 3-4. In this model, it neglects the depletion capacitance of source and drain implants to substrate. It assumes that both of the gate-drain capacitance and gate-source capacitance is equal to half of C_{ox} as shown in Fig. 3-3. Because the voltage across C_{gd} changes by $2*V_{DD}$ as gate change from 0 to V_{DD}, C_{gd} can be separated into the gate to ground and drain to ground capacitance

of value C_{ox}. The total capacitance at the gate terminal is equal to $\frac{3}{2}C_{ox}$ including the gate-source capacitance $\frac{1}{2}C_{ox}$ and the drain to ground capacitance is equal to C_{ox} .

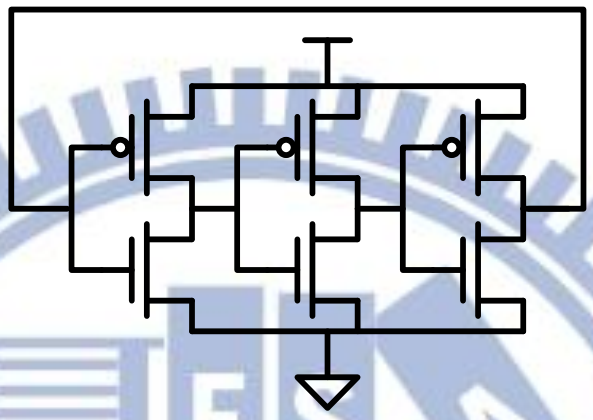


Fig. 3-2 Invertor based ring oscillator

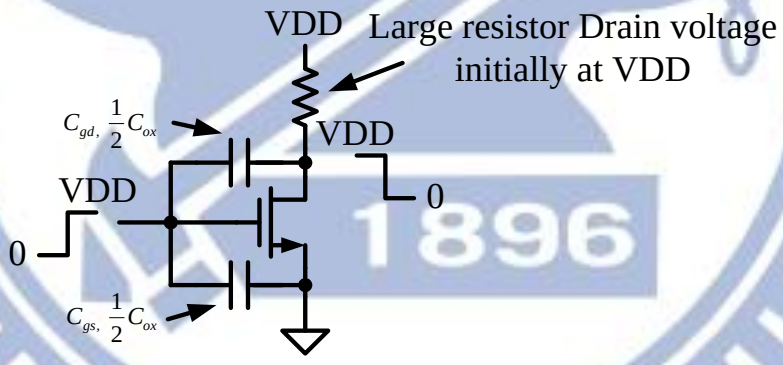


Fig. 3-3 MOSFET switching circuit with capacitance

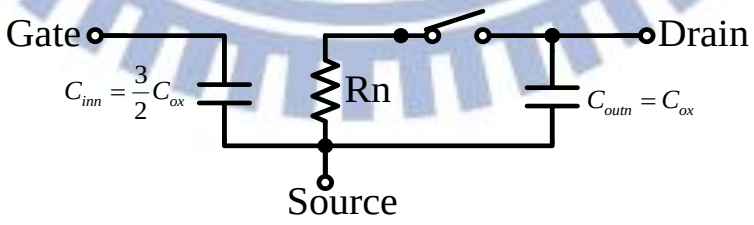


Fig. 3-4 Simple digital MOSFET model

Based on this model, the C_L of the invertor cell is given as

$$
\begin{aligned}
C_L &= C_{in} + C_{out} \\
&= (\frac{3}{2}C_p + \frac{3}{2}C_n) + (C_p + C_n) \\
&= \frac{3}{2}C_{ox}(W_pL_p + W_nL_n) + C_{ox}(W_pL_p + W_nL_n) \\
&= \frac{5}{2}Cox(W_pL_p + W_nL_n) \qquad (3.2)
\end{aligned}
$$

We can see that the frequency of VCO can be influenced greatly by the capacitance at the output of each stage which may change with the loading. To reduce the frequency varying with the output loading, we can add the buffer to the output of VCO. Here, we add an inverter as the buffer, whose loading is given as $\frac{3}{2}C_{ox}(W_pL_p + W_nL_n)$.

For our specification shown in Table 1-1, the ENOB of ADC should be more than 8 bits. For the margin of the quantization error and the non-ideal effect reducing performance, we set the resolution of ADC to be 10 bits. Through the equation(2.11), we can calculate the frequency requirement for our VCO is more than 10.24MHz. As we introduce in section 2-2.5 , the nonlinearity of VCO is one of most important characteristic should be cared about. We applied a simple DNL, INL test during VCO design to characterize the linearity performance. Also, for our application, ECG acquisition for mobile healthcare, the power of ADC should be considered, so power consumption is also an issue for VCO chosen. Here we give some different types of inverter based VCO delay cell for the ring structure VCOs. Their analysis and the simulation results are shown below. And the chosen decision will be given in the end.

3-2.1 Current controlled delay cell

For the current control delay cell, the delay of current control delay cell is controlled by the current. In this cell the input voltage is connected to the gate of the

MOS to modify the current of cell. In our application, the dc voltage of input signal is in the relative low level, so we use the PMOS as the current control cell as shown in Fig. 3-5.

Circuit description and Design Methodology

Fig. 3-5 shows the schematic of our current-starved delay cell. For each cell, it contains two current controlled inverter based delay elements. Let's look into one delay element DE1, transistor Mp1 and Mn1 operate as an inverter and do the oscillating function of the VCO. And the transistor Mc operates as the current source which limiting the current of the Mp1 and Mn1. The current is controlled by the V_{ctrl} at gate terminal of the Mc as equation(3.3) and further influences the delay of cell.

$$I_D = \frac{1}{2}\mu Cox\frac{W}{L}(V_{DD} - V_{ctrl} - V_{th})^2 \quad (3.3)$$

As shown is equation(3.1), the frequency of VCO is proportional to the current of the delay cell. The relationship of frequency of the VCO is related to the square of control voltage V_{ctrl} as shown in follow

$$f_{osc} \propto I_D \propto V_{ctrl}{}^2 \quad (3.4)$$

The delay characteristic is shown in Fig. 3-6. The delay of each cell is from 0.36 to 0.42 ns when control voltage is 0 to 0.1V at 25℃ in TT corner.

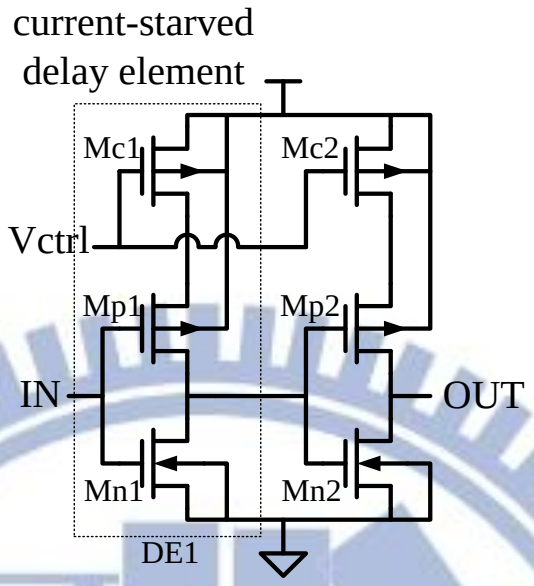


Fig. 3-5 Schematic of current controlled delay cell

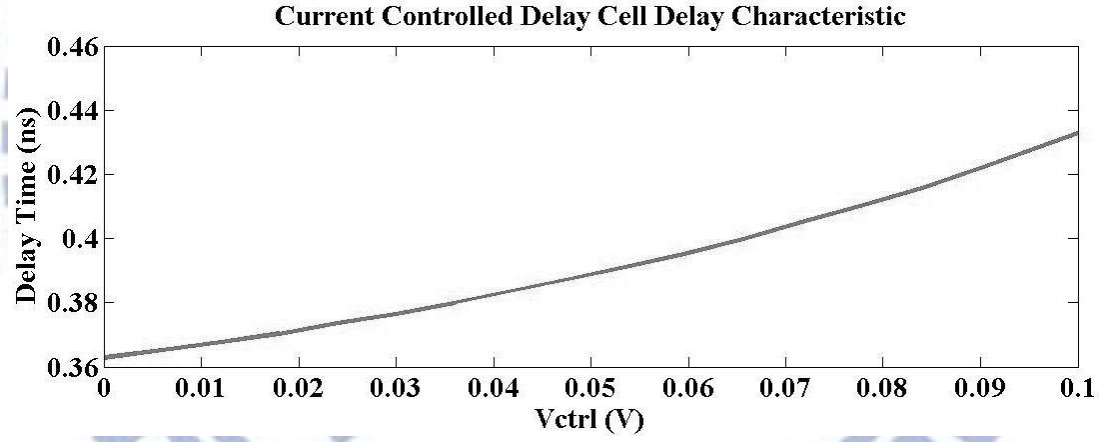


Fig. 3-6 delay characteristic of current controlled delay cell

f_{vco} vs. V_{ctrl}, linearity

To meet the specification of VCO, we use 16 stage delay cells. The first stage of the ring oscillator is implemented by the NAND gate for inversing the signal and the start triggering. The overall VCO schematic is shown as Fig. 3-7. The frequency performance is shown in Fig. 3-8. From equation (3.4) we can see that the control linearity of current-starved delay cell is poor due to the square relation between control voltage and the VCO frequency. To quantify the linearity we applied the

simple DNL and INL calculation for the frequency transfer line. To make the comparison with other types of VCO faired, we set the LSB_{freq} as the frequency range divided by 100 as shown in equation(3.5). Due to the frequency transfer function is got in 100 steps; LSB_{freq} is represented as the frequency resolution for each voltage step. The DNL of the current controlled ring VCO is 1.4625 LSB and INL of this kind of VCO is 8.88 LSB which is really poor.

$$LSB_{freq} = \frac{f_{\max}(VCO) - f_{\min}(VCO)}{100} \tag{3.5}$$

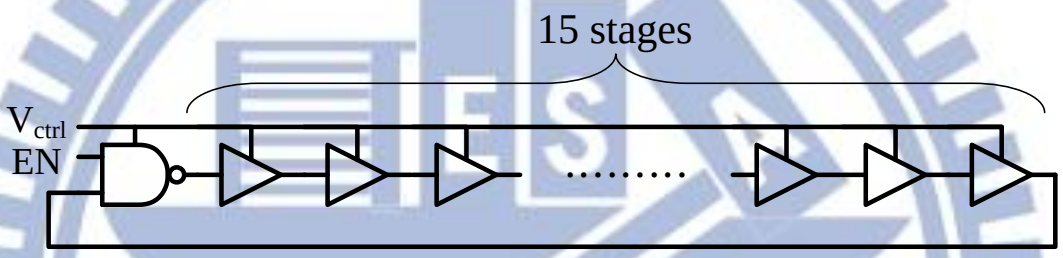


Fig. 3-7 Overall VCO schematic

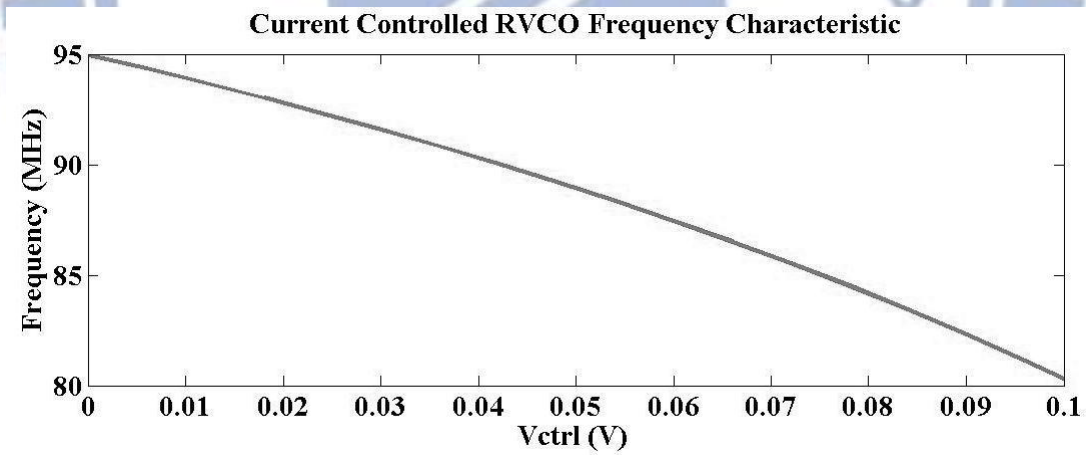


Fig. 3-8 Frequency characteristic of current controlled ring VCO

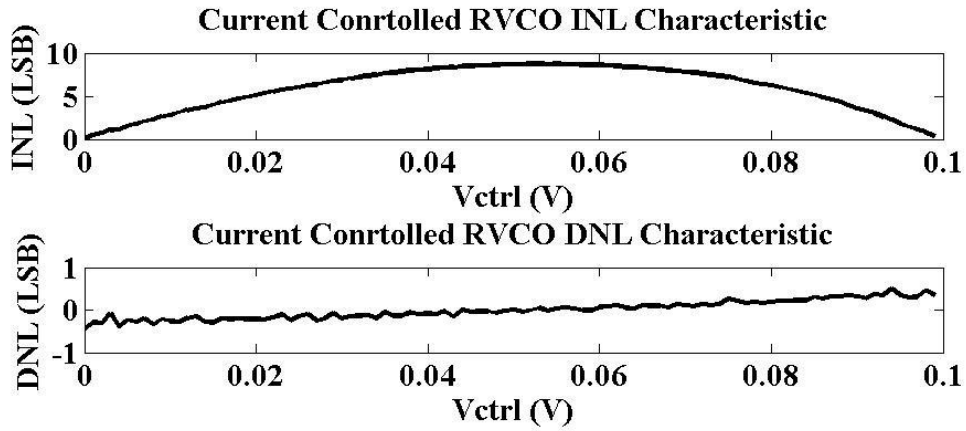


Fig. 3-9 INL and DNL result of current controlled ring VCO

Jitter performance

The jitter performance is simulated by the SPICE with 1000 delay cases. If the V_{ctrl} is fixed to 0, the distribution of VCO period is shown as Fig. 3-10. We use the Gaussian distribution to model the period of the VCO. The probability of fitting model is shown in Fig. 3-11. If the data are normal the plot will be near to the dashed line. The standard deviation for each voltage value is shown in Fig. 3-12. The maximum standard deviation is 14.9117 ps.

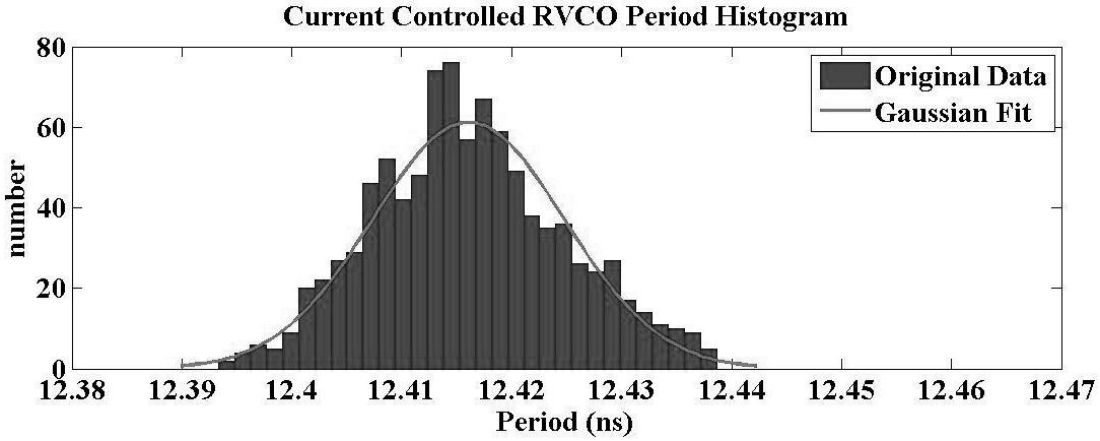


Fig. 3-10 Distribution of period of current controlled ring VCO

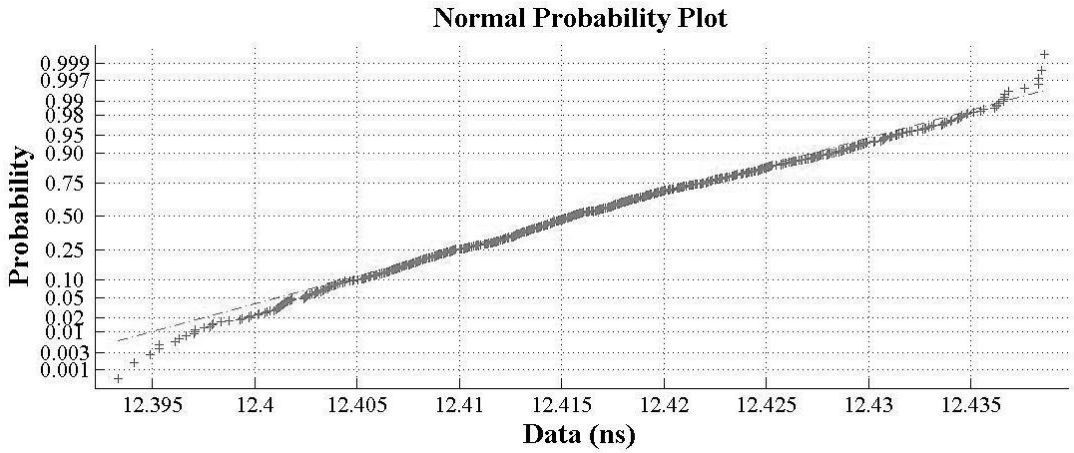


Fig. 3-11 Probability plot of current controlled ring VCO

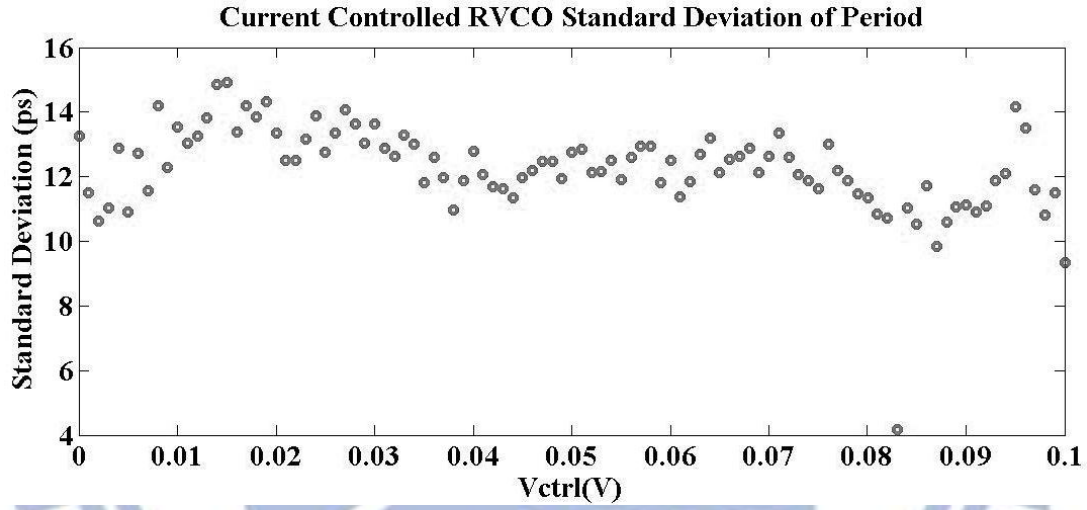


Fig. 3-12 Standard deviation of the period of current controlled ring VCO

Power consumption

The power consumption of each V_{ctrl} is shown in Fig. 3-13. The average power of this VCO is 2.3 uW.

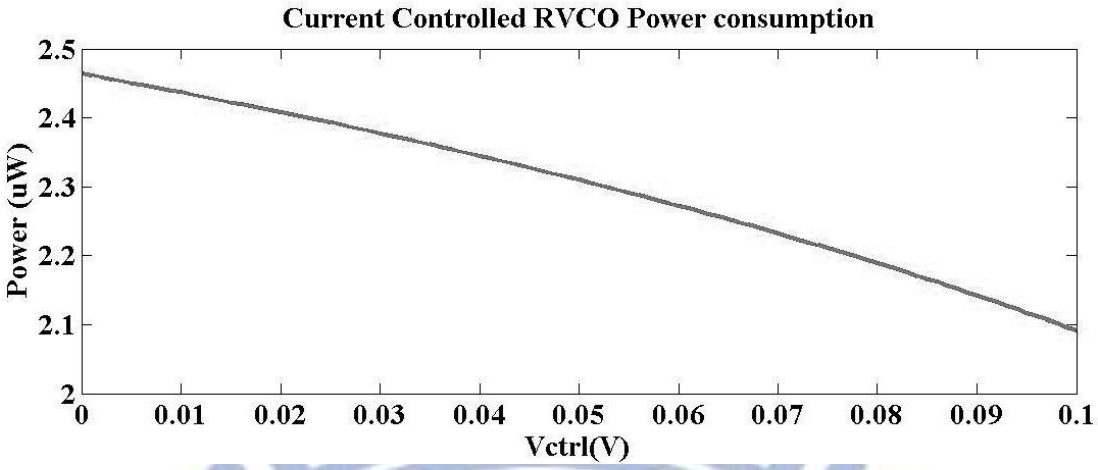


Fig. 3-13 Power consumption of current controlled VCO

3-2.2 Supply controlled delay cell

Supply controlled delay cell control the delay time by applying the control voltage to the supply terminal of the delay cell as shown in Fig. 3-14. The control voltage applied to supply of the invertor-based cell not only modulate the supply voltage directly but also modulate the current of the delay cell. The detail of operation is described below:

Circuit description and Design Methodology

Fig. 3-14 shows the schematic of our supply controlled delay cell. The same as the current-starved delay cell: for each cell, it contains two supply controlled inverter based delay elements. In single delay element DE1, transistor Mp1 and Mn1 operate as an inverter and do the oscillating function of the VCO. The supply is controlled by the V_{ctrl} at source terminal of the Mp1. This operation also influences the current of the delay of cell as equation(3.6).

$$I_D = \frac{1}{2}\mu Cox\frac{W}{L}(V_{DD} - V_{ctrl} - V_{th})^2 \tag{3.6}$$

As shown in equation(3.1), the frequency of VCO is proportional to the current of the delay cell and inverse proportional to the supply voltage. The relationship of

frequency of the VCO is proportional to the control voltage V_{ctrl} as shown in follow

$$f_{osc} \propto \frac{I_D}{V_{DD}} \propto \frac{V_{ctrl}^{\ 2}}{V_{ctrl}} \propto V_{ctrl} \tag{3.7}$$

The delay characteristic is shown in Fig. 3-15. The delay range is from 0.63 to 0.82 picoseconds when control voltage is applied from 0.5 to 0.6V at 25℃ in TT corner.

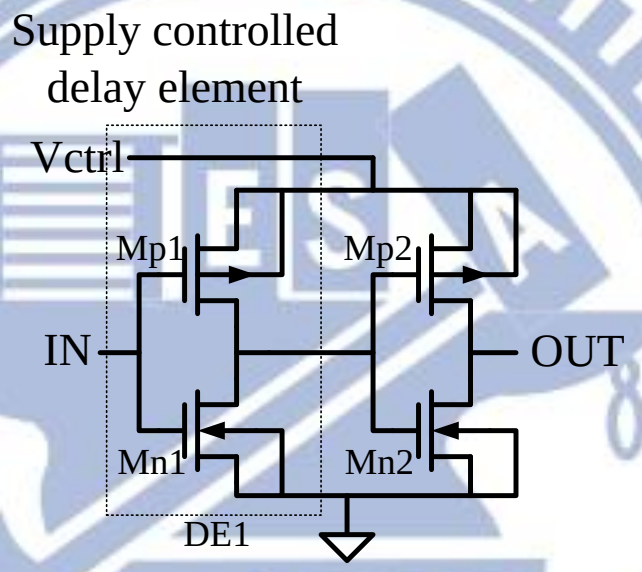


Fig. 3-14 Schematic of supply controlled delay cell

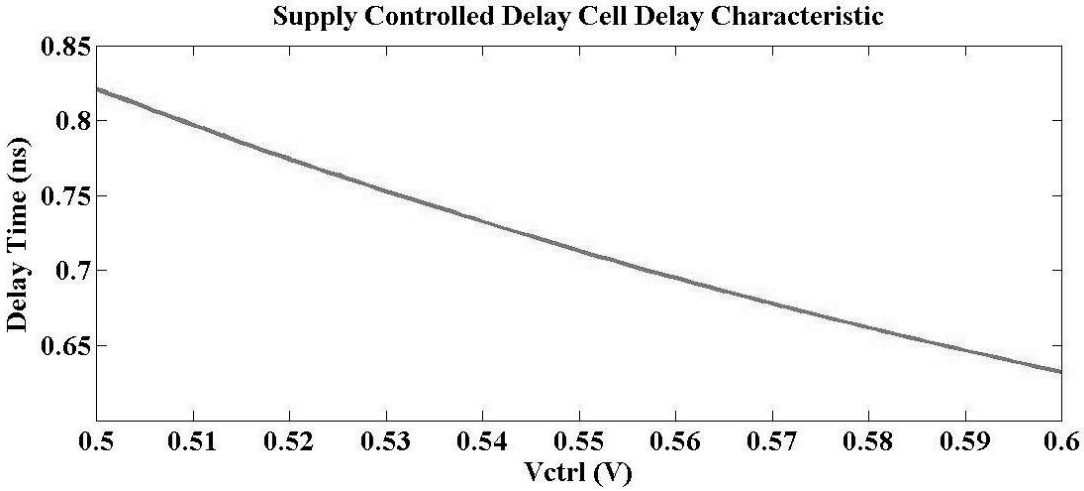


Fig. 3-15 Delay characteristic of supply controlled delay cell

f_{vco} vs. V_{ctrl}, linearity

The overall architecture of VCO is the same as the current controlled ring VCO as shown in Fig. 3-7. The frequency performance is shown in Fig. 3-16. From equation (3.7) we can see that the control linearity of supply controlled delay cell is great due to the influence of both I_D and V_{DD} to the VCO frequency. The maximum INL and DNL is 0.5937 and 0.0288 LSB respectively.

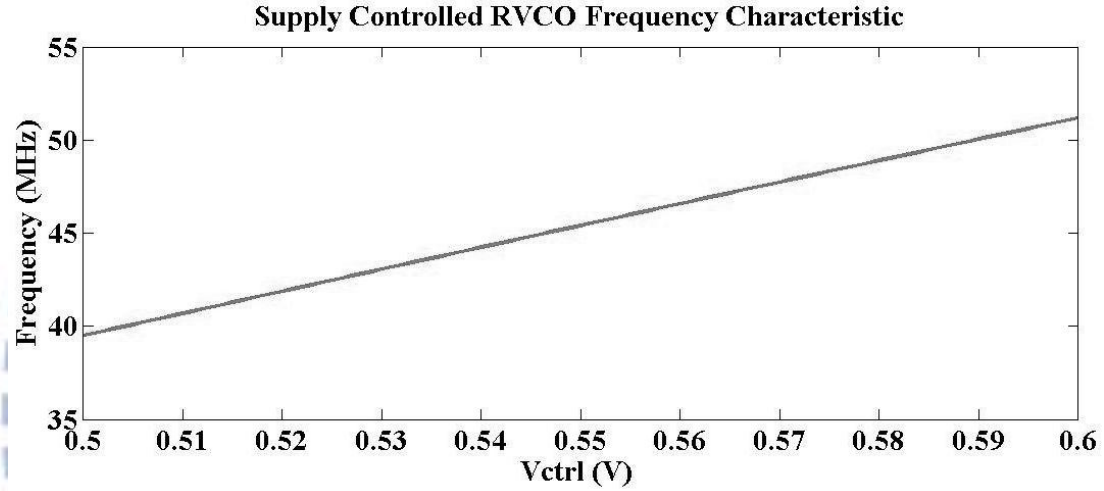


Fig. 3-16 Frequency characteristic of supply controlled ring VCO

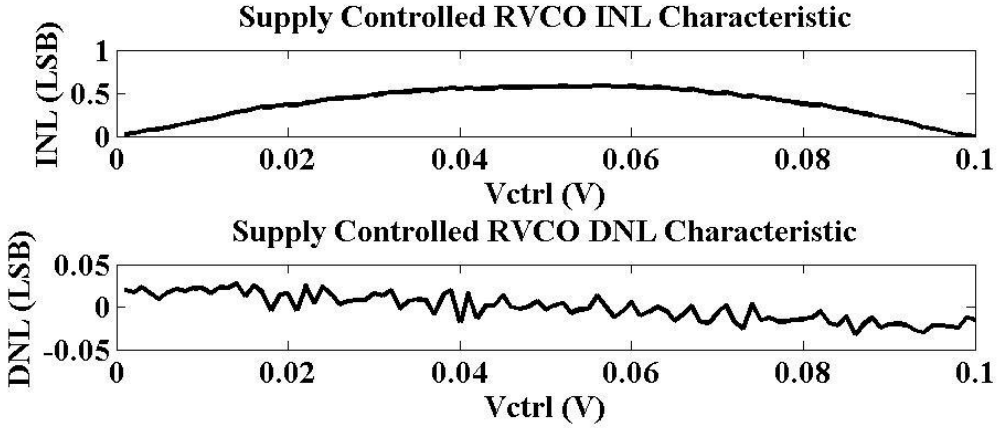


Fig. 3-17 INL and DNL characteristic of supply controlled ring VCO

Jitter performance

The jitter performance is simulated by the SPICE with 1000 delay cases. The distribution is shown as Fig. 3-18. If we use the Gaussian distribution to model it, the fitting graph is shown in Fig. 3-18. The same with the previous architecture, we applied the probability plot for checking the model of Gaussian as shown in Fig. 3-19. To characterize the jitter performance, we calculate the standard deviation of period distribution. The result is shown in Fig. 3-20. The maximum standard deviation is 8.17 ps.

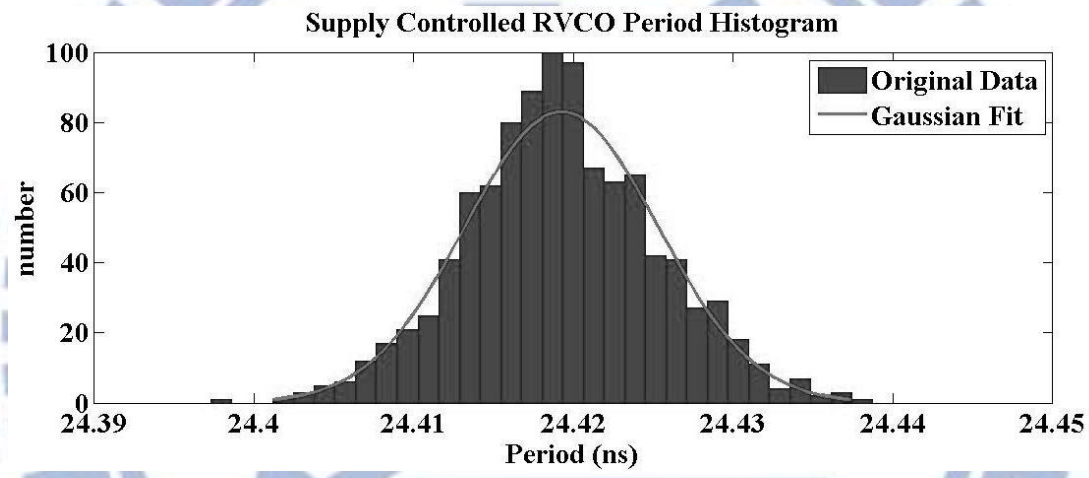


Fig. 3-18 Distribution of Period of supply controlled ring VCO

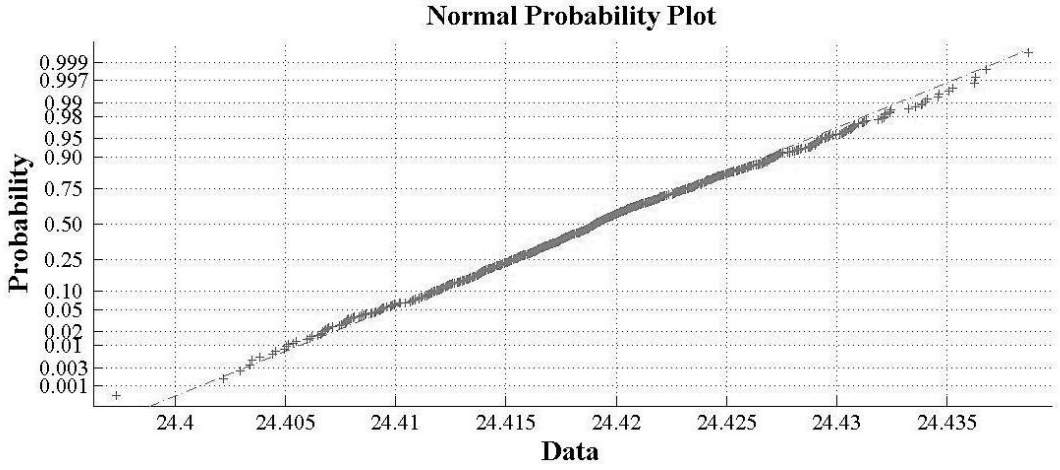


Fig. 3-19 Gaussian probability plot of supply controlled ring VCO

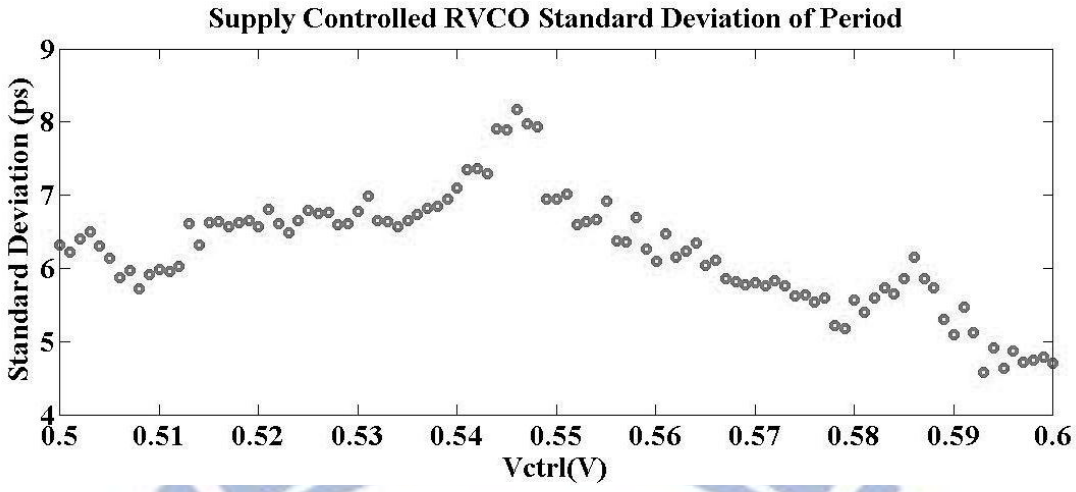


Fig. 3-20 Standard deviation of period of supply controlled ring VCO

Power consumption

The simulation result of power is shown in Fig. 3-21. The average power is 3.13uW.

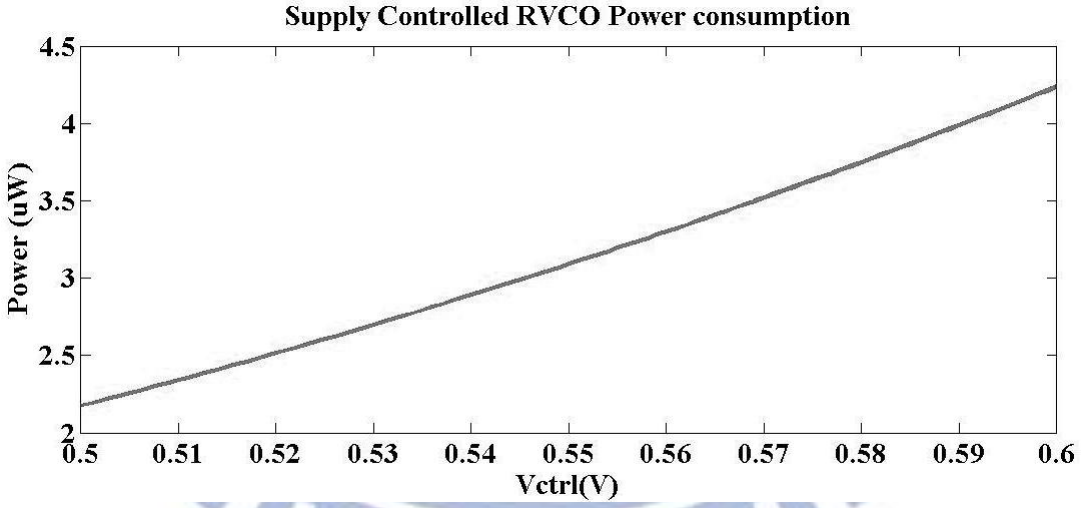


Fig. 3-21 Power consumption of supply controlled ring VCO

3-2.3 Bulk controlled delay cell

This type of delay cell is controlled by the bulk voltage. The control voltage is applied to the NMOS bulk terminal of the delay cell as shown in Fig. 3-22. The bulk voltage can modulate the threshold voltage and further modulate the current of the delay cell. The details of the circuit are shown in the following section.

Circuit description and Design Methodology

Fig. 3-22 shows the schematic of our supply controlled delay cell. The same with the previous delay cell, for each cell, it contains two bulk controlled inverter based delay elements. In single delay element DE1, transistor Mp1 and Mn1 operate as an inverter and do the oscillating function of the VCO. Due to the low voltage level of the input signal, the control signal is applied to the NMOS. In DE1, Mn1 is controlled by the Vctrl. This operation also influences the threshold voltage of Mn1 as

$$V_{th} = V_{t0} + \gamma\left(\sqrt{2\Phi_f - V_{BS}} - \sqrt{2\Phi_f}\right) \tag{3.8}$$

where V_{t0} is the threshold voltage when $V_{BS} = 0$, γ is the process constant and Φ_f is the surface potential of the MOS transistor. If we set $K_\Phi = V_{t0} - \gamma\sqrt{2\Phi_f}$ and $y = \sqrt{2\Phi_f - V_{BS}}$, we can rewrite the current of delay cell as

$$\begin{aligned} I_D &= \frac{1}{2}\mu Cox\frac{W}{L}(V_{DD} - V_{th})^2 \\ &= \frac{1}{2}\mu Cox\frac{W}{L}({V_{DD}}^2 + {V_{th}}^2 - 2V_{DD}V_{th}) \\ &= \frac{1}{2}\mu Cox\frac{W}{L}({V_{DD}}^2 + {K_\Phi}^2 - 2V_{DD}K_\Phi + \gamma^2 y^2 - 2\gamma(V_{DD} - K_\Phi)y) \end{aligned} \tag{3.9}$$

If the supply voltage is low, the current is dominanted by the square of y which is proportional to the V_{BS} .The dependency between control voltage and current is much linear.

As shown is equation(3.1), the frequency of VCO is proportional to the current of the delay cell and inversely proportional to the supply voltage. The relationship of frequency of the VCO is proportional to the control voltage V_{ctrl} as shown below

$$f_{osc} \propto I_D \propto (V_t)^2 \propto (\sqrt{V_{ctrl}})^2 \propto V_{ctrl} \tag{3.10}$$

The delay characteristic is shown in Fig. 3-23. The delay of bulk controlled delay

cell is from 109.88ps to 106.95ps when control voltage sweeps from 0 to 0.1V.

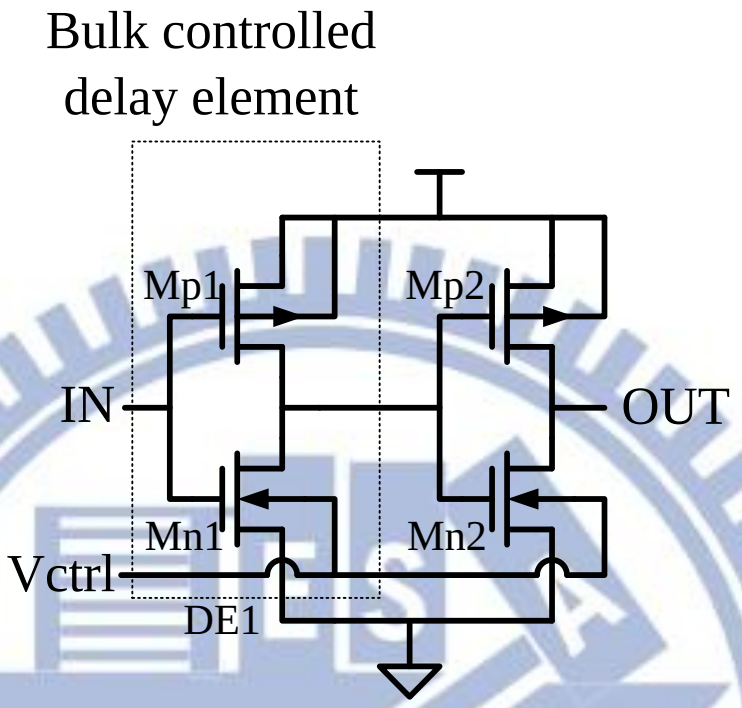


Fig. 3-22 Schematic of bulk controlled delay cell

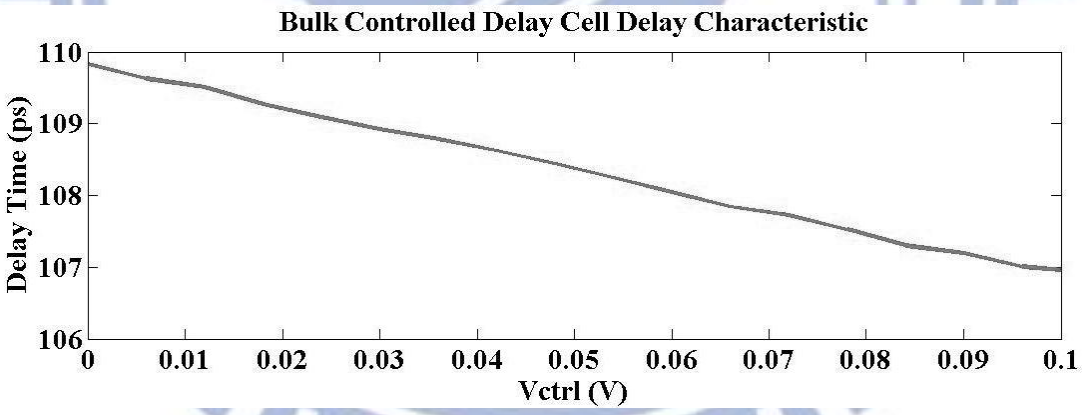


Fig. 3-23 Delay characteristic of bulk controlled delay cell

f_{vco} vs. V_{ctrl}, linearity

The same as the previous architecture, we use 16 stage delay cells with the first NAND stage. The overall VCO schematic is shown as Fig. 3-7. The frequency performance is shown in Fig. 3-24. From equation (3.10) we can see that the control linearity of bulk controlled delay cell is much better than the current controlled delay

ring VCO. There should be mentioned that the frequency offset of this type of architecture is quite large due to the influence on the constant V_{gs}. The offset frequency affects the bit number requirement of counter. The larger frequency the larger number of bit requirement of the counter and the larger power consumption. The INL and DNL simulation result is shown in Fig. 3-25. The maximum INL is 1.3448 LSB and the maximum DNL is 0.8889 LSB, which is quite better than the current controlled ring VCO.

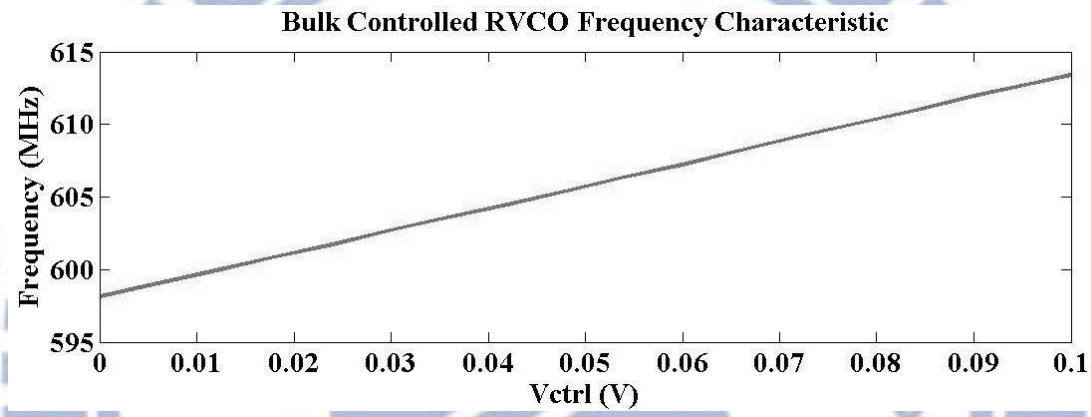


Fig. 3-24 Frequency characteristic of bulk controlled ring VCO

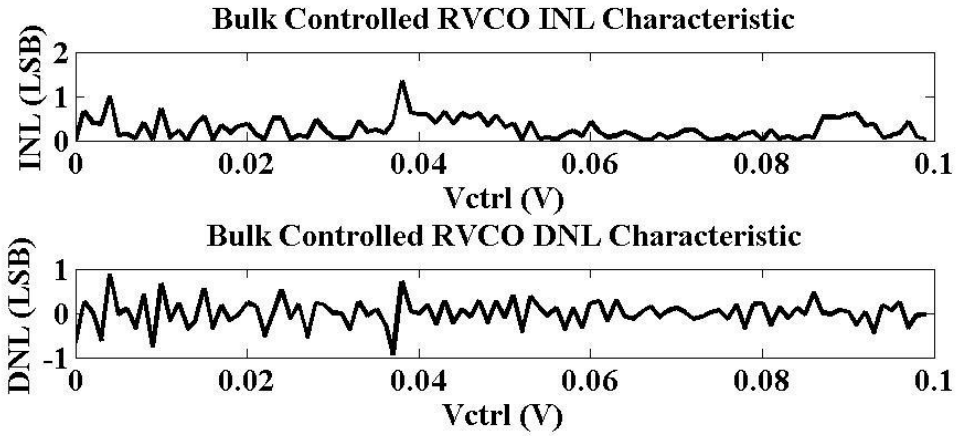


Fig. 3-25 INL and DNL result of bulk controlled ring VCO

Jitter performance

To characterize the jitter performance of the VCO, we collect 1000 cycle periods. If we set the V_{ctrl} to be a constant value, the distribution of period is shown as Fig.

3-26. We fit the Gaussian function to the distribution. The fitting graph is shown in Fig. 3-26. We use the normal probability plot to check the relation between the origin data and the Gaussian function as shown in Fig. 3-27. If the data are normal the plot will be near to the dashed line. To characterize the performance of jitter, we calculate the standard deviation of the Gaussian model of each control voltage. The result is shown in Fig. 3-28. The maximum σ is 1.0972ps.

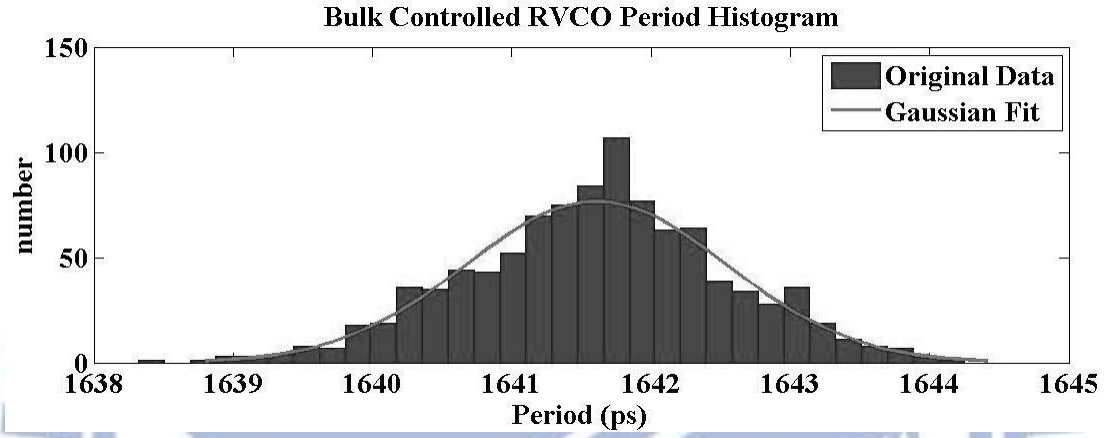


Fig. 3-26 Distribution of period data and the Gaussian fitting line

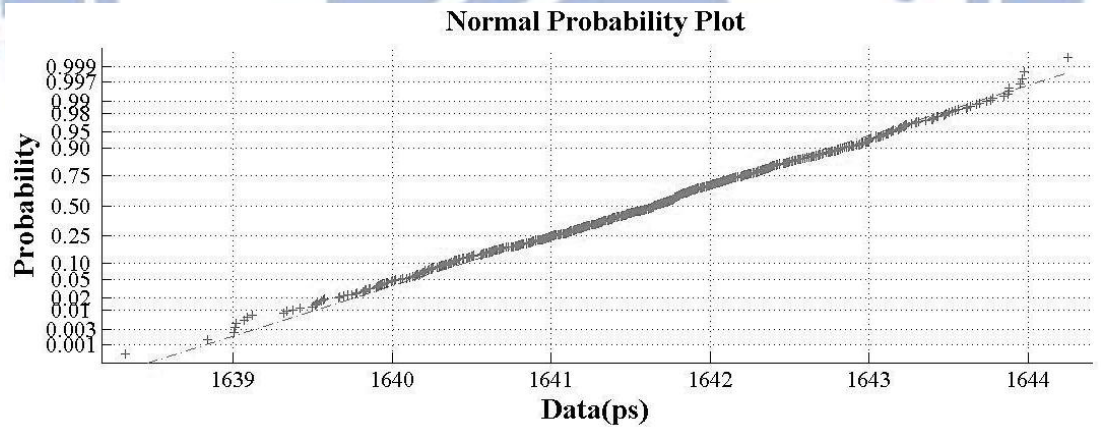


Fig. 3-27 Gaussian distribution probability plot

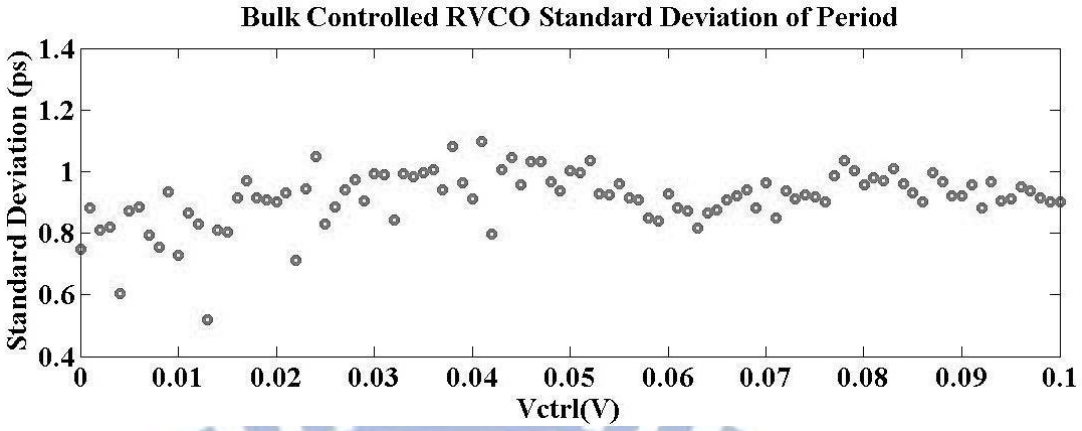


Fig. 3-28 Standard deviation of period of bulk controlled ring VCO

Power consumption

The power consumption of this architecture is shown in Fig. 3-29. Due to the large offset frequency of this architecture, the power consumption is very large compared to other architecture. The average power is 38.19uW.

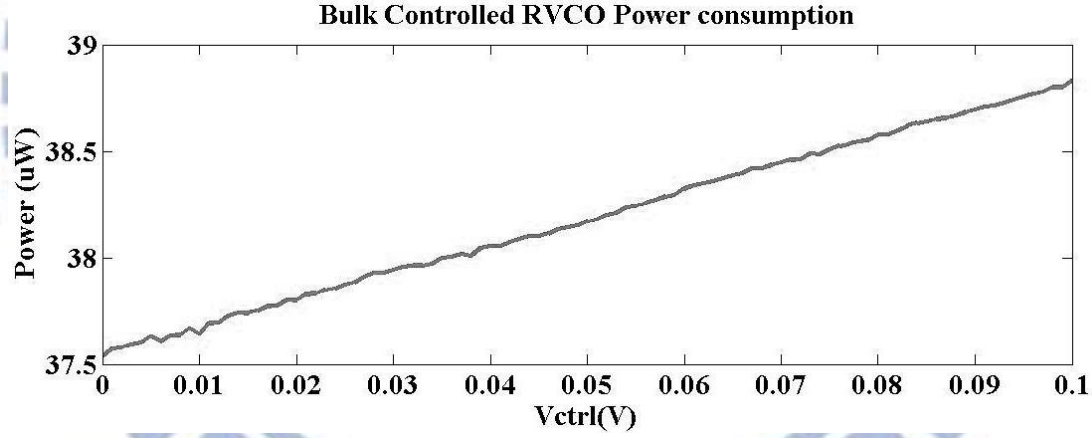


Fig. 3-29 Power consumption of bulk controlled ring VCO

3-2.4 Ground controlled delay cell

This type of delay cell is controlled by the ground voltage. The control voltage is applied to the NMOS source terminal of the delay cell as shown in Fig. 3-30. The influence of the ground terminal is similar to the supply control. It modulates the reference voltage of the delay cell and also influences the current of cell. The details of the circuit are shown in the following section.

Circuit description and Design Methodology

Fig. 3-30 shows the schematic of our ground controlled delay cell. The same with the previous delay cell, for each cell, it contains two ground controlled inverter based delay elements. In the delay element DE1, transistor Mp1 and Mn1 operate as an inverter and do the oscillating function of the VCO. We apply the control signal to the source of the NMOS. The ground controlled delay cell modulates the voltage swing of the delay cell. The initial voltage for the capacitance charging is equal to control voltage rather than 0. So, the propagation delay of low to high signal is modified as

$$t_{PLH} = C_L \times \frac{\frac{1}{2}V_{DD} - V_{ctrl}}{I_D} \tag{3.11}$$

The frequency of VCO in equation (3.1) can be rewritten as

$$f_{osc} \approx \frac{I_D}{N \times (V_{DD} - V_{ctrl}) \times C_L} \tag{3.12}$$

The control voltage also influence the current as $I_D = \frac{1}{2}\mu Cox\frac{W}{L}(V_{DD} - V_{ctrl} - V_t)^2$. The relationship of frequency of the VCO is proportional to the control voltage V_{ctrl} as shown below

$$f_{osc} \propto \frac{I_D}{V_{ctrl}} \propto \frac{(V_{ctrl})^2}{V_{ctrl}} \propto V_{ctrl} \tag{3.13}$$

The delay characteristic is shown in Fig. 3-31. The delay range is from 0.82 to 1.21 nanoseconds as control voltage is 0 to 0.1V at 25 ℃ in TT corner.

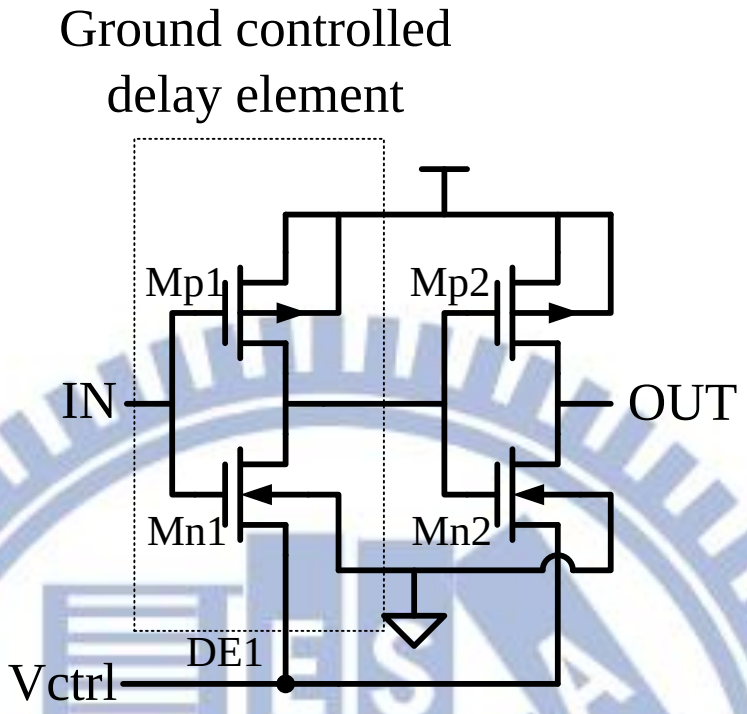


Fig. 3-30 Schematic of ground controlled delay cell

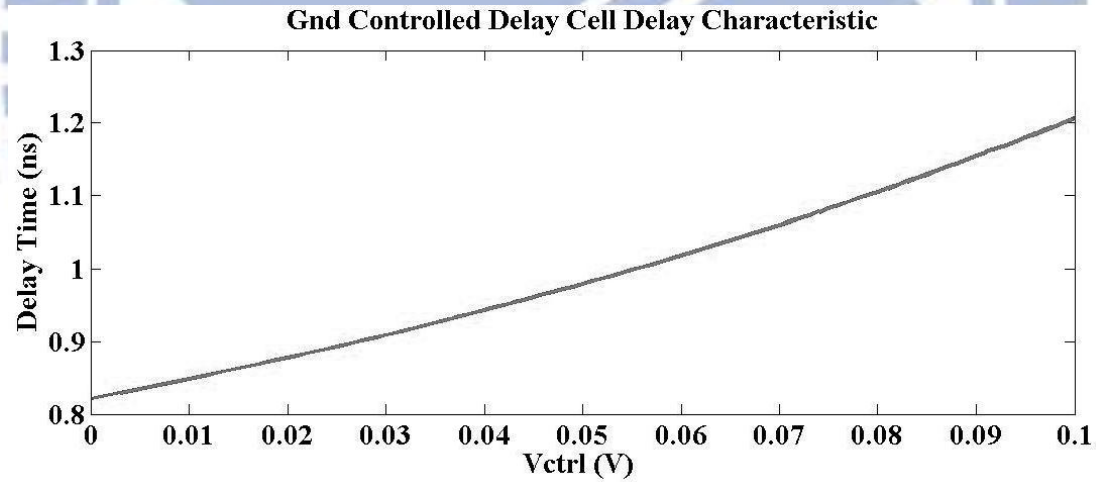


Fig. 3-31 Delay characteristic of ground controlled delay cell

f_{vco} vs. V_{ctrl}, linearity

The overall architecture of VCO is the same as the current-starved ring VCO as shown in Fig. 3-7. The frequency performance is shown in Fig. 3-32. From equation (3.13)we can see that the control linearity of ground controlled delay cell is great due to the influence of both I_D and V_{DD} to the VCO frequency. The INL and DNL

result is shown in Fig. 3-33. The maximum absolute value of INL and DNL is 0.1369 and 0.0157 LSB respectively.

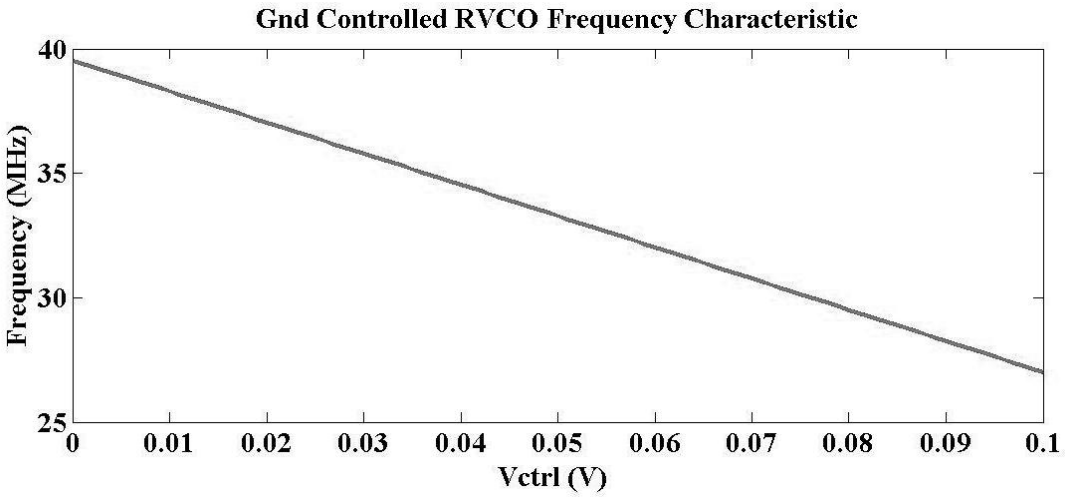


Fig. 3-32 Frequency characteristic of ground controlled ring VCO

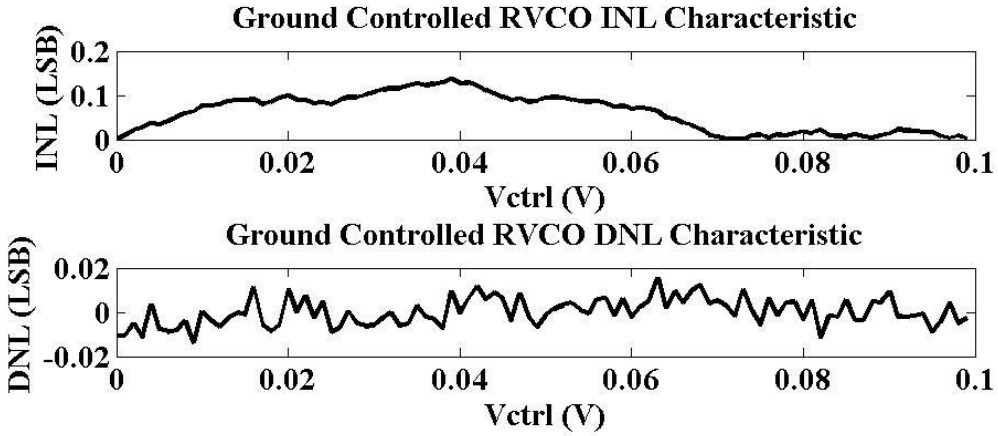


Fig. 3-33 INL and DNL of ground controlled ring VCO

Jitter performance

The jitter performance is simulated by the SPICE with 1000 delay cases. The distribution is shown as Fig. 3-34. The stick plot is the original data of the period while the line is the Gaussian model fitting. Fig. 3-35 shows the probability of Gaussian fitting. The cross note is represented as the original data and the dashed line represent the ideal Gaussian distribution probability of the data value. If the distribution is the Gaussian distribution, the crosses are close to the dashed line. To

characterize the period, we calculate the standard deviation of period for each controlled voltage. The result is shown in Fig. 3-36. The maximum σ is 11.3052ps.

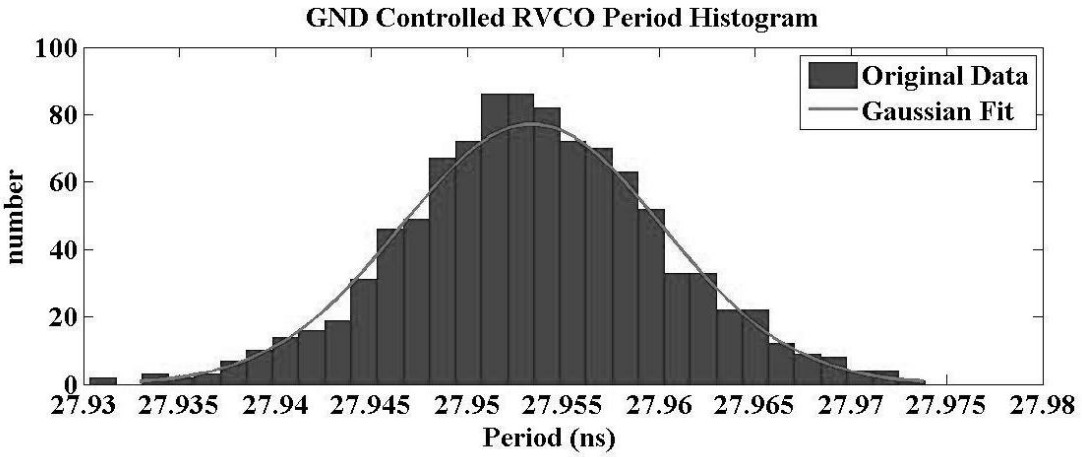


Fig. 3-34 Distribution of period of ground controlled ring VCO

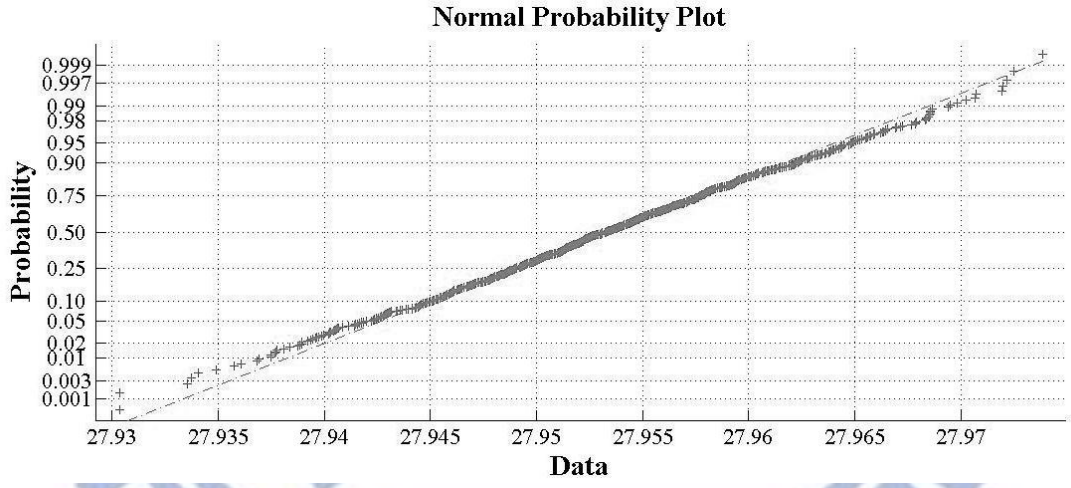


Fig. 3-35 Probability plot of Gaussian fitting model

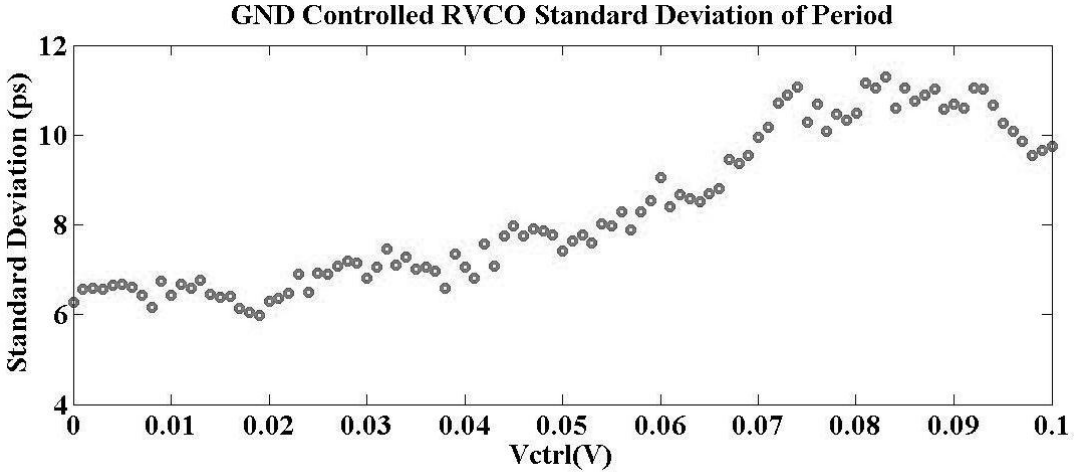


Fig. 3-36 Standard deviation of period of ground controlled ring VCO

Power consumption

The power consumption for each control voltage of the ground controlled ring VCO is shown as Fig. 3-37. The average power is 1.4796 uW.

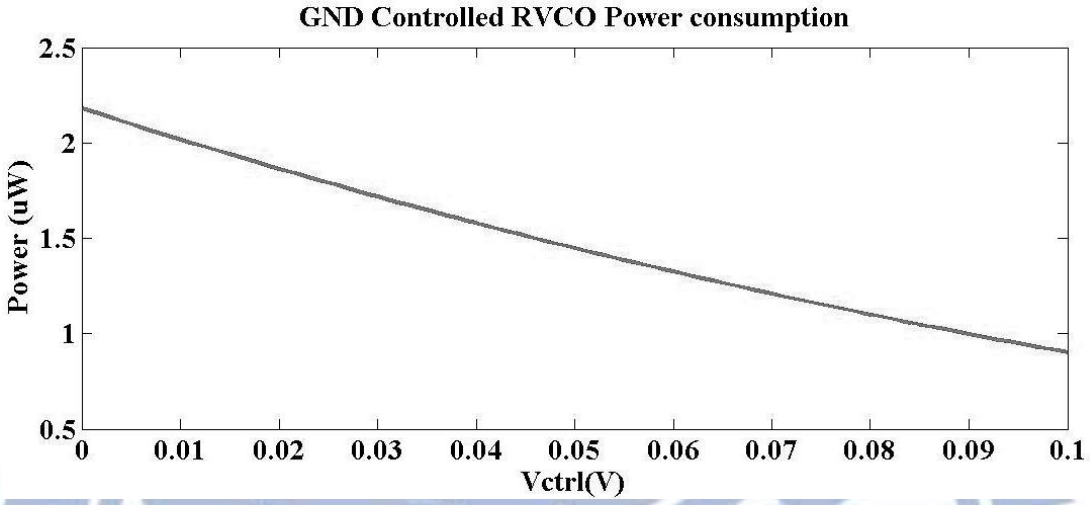


Fig. 3-37 Power consumption of ground controlled ring VCO

3-2.5 Choice of VCO topology

The choice of the VCO architecture is based on the consideration of linearity, jitter performance, power and some implementation issue. We give the summary of the performance of the VCOs in TT-25℃ in Table 3-1. In Table 3-1, it shows the poor linearity of the current-starved VCO due to the second order relationship between V_{ctrl} and frequency. The linearity of the supply controlled VCO is great, but this type of VCO is only suitable for the high voltage level of the control voltage. For our application the input is in the low voltage level so the additional bias circuit is required for this architecture which costs the additional power consumption. For the bulk-control VCO the linearity is good but the offset frequency is large that causes too large power consumption. For the ground controlled ring VCO, it has good linearity and good jitter performance. Its offset frequency is low, so the power consumption is

less than other architectures. And the voltage range is also suitable for our application. So, with these reasons, we choose the ground controlled ring VCO for our design.

Architecture	linearity		Jitter (max)		Frequency (MHz)	Power (uW)	Voltage Range (V)
	INL (LSB)	DNL (LSB)	Standard deviation (RMS Jitter) (s)	Normalize to frequency (%)			
Current	8.88	0.46	14.9117p	0.1392	80.33 ~94.96	2.3	0~0.1
Supply	0.59	0.03	8.17p	0.0367	39.52 ~51.21	3.13	0.5~0.6
Bulk	1.34	0.89	1.0972p	0.0663	598.14 ~613.39	38.19	0~0.1
Ground	0.14	0.02	11.3052p	0.0334	26.99 ~39.52	1.48	0~0.1

Table 3-1 Performance comparison of VCO

3-3 Counter

Counter which is triggered by the transition edge of VCO output is the component that converts the time information into the digital value. The requirement of counter should cover the oscillation number which VCO operates at the maximum frequency in whole sampling period as equation(3.14).

$$Bit\ number\ of\ Counter \geq log_2(\frac{max(F_{vco})}{F_s}) \quad (3.14)$$

According to the spec in Table 1-1, the sampling frequency of ADC is 10k Hz. We can calculate the bit requirement for the counter should be more than 17 bits. For this large bit number requirement, the dynamic power of counter may be one of the issues. In the following section, we compare both of the synchronous and asynchronous counters and choose the suitable one for our ADC.

3-3.1 Synchronous

Synchronous counter is composed of an adder and the flip-flop. The adder calculates next the counter value during each VCO oscillation cycle. And flip flops pass the result of adder to the counter output at once as shown in Fig.3-38. In this architecture, the counter CLK is the output of VCO. The synchronous counter all the flip-flops are triggered by the CLK. The high operating frequency of counter causes the power consumption of counter is quite large. For the 17 bits counter, operating in 65MHz its power is about 4.5uW dominating the overall power consumption of VCO-based ADC. To overcome this problem, we applied the asynchronous counter for our ADC architecture.

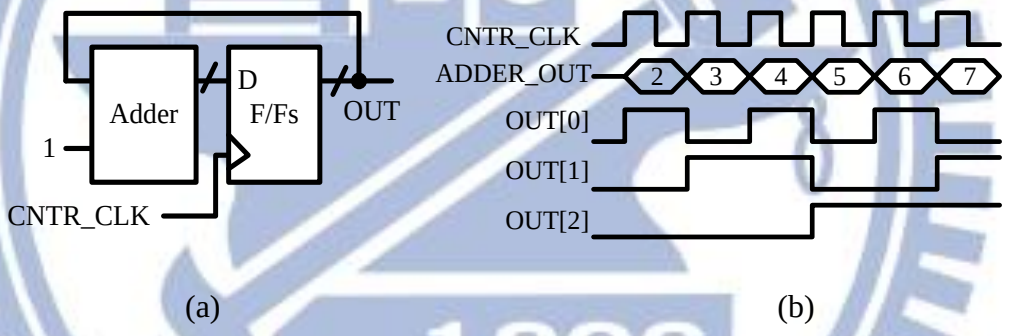


Fig.3-38 synchronous counter: (a) Architecture; (b) Timing diagram

3-3.2 Asynchronous

The architecture of asynchronous counter is shown in Fig.3-39. In this architecture, only the LSB of counter triggered from the VCO output. Other bits of counter sense the negative edge of previous stage to reverse its state. The data transition of the MSB is significantly reduced, causes the power consumption of counter has greatly improvement from the synchronous version. Also, adder is not needed in this type of counter, so the power of combination circuit is zero. But, due to the carry-in information is propagated by each stage flip-flops, the timing criteria of

counter is depended on the propagation delay from D to Q of flip-flops. Here, we choose the high performance flip-flop in standard cell to ensure the counter operation.

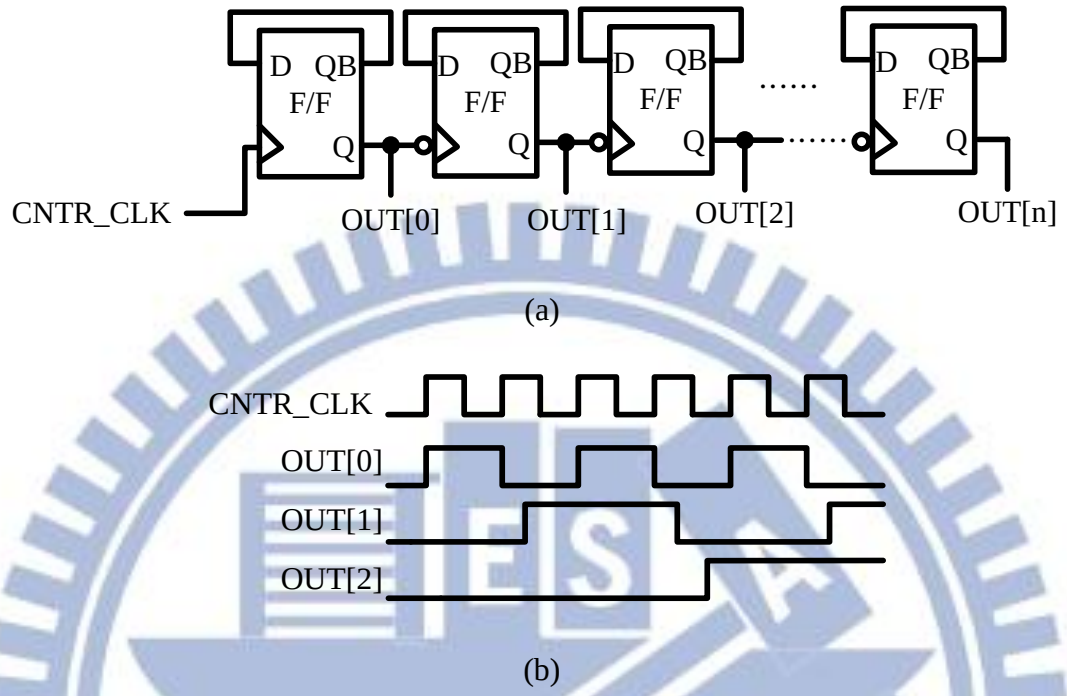


Fig.3-39 Asynchronous counter: (a) Architecture; (b) Timing diagram

But still, in the timing diagram shown in Fig.3-39(b), we can see that the carry-in propagation delay is quite large. There might have large probability of flip-flops sample the intermediate value of counting. For avoiding the sampling flip-flops sampled the wrong value during propagation, we add the other set of flip-flops which triggered by the delayed CLK to double sample the counter value. The delays for CLKs triggered these two sets flip-flops should cover the region of carry in propagation. Due to the working principle of asynchronous counter, the propagating is starting from the LSB, we can determine the correct value from flip-flops. During the propagation, LSBs will first turn to 0 before the MSB turns to 1, the value of counter will first decrease before carrying in. So, if the value triggered from the delayed CLK is smaller than the value of regular CLK, we can judge that the counter is during propagation at the delayed CLK the proper value is chosen as the regular CLK.

In Fig.3-40, we denote FF_SP as flip-flops triggered by the regular sampling CLK, FF_SP_D as flip-flops triggered by the CLK with delay. There are 3 different sampling situations:

A. FF_SP samples the value before propagation and FF_SP_D samples the value after propagation.
B. FF_SP samples the value before propagation and FF_SP_D samples the value during propagation.
C. FF_SP samples the value during propagation and FF_SP_D samples the value after propagation.

Due to the delay for sampling CLK is designed to be larger than the carry-in propagation, the case that both FF_SP and FF_SP_D sample the value during propagation will not happen. The value during propagation is always smaller than the value is settled, no matter before or after propagation for case B and C. For case A, both two values are settled, so the correct value is depended on which sampling CLK we want. Here, we choose the value of original sampling clk. So, we choose FF_SP for case A. and value of case B is modified by FF_SP_D-1.

Algorithm 1: Asynchronous F/Fs determination

Input: FF_SP and FF_SP_D

Output: OUT

ifFF_SP_D< FF_SP**then**

OUT = FF_SP

else

OUT = FF_SP_D-1

End

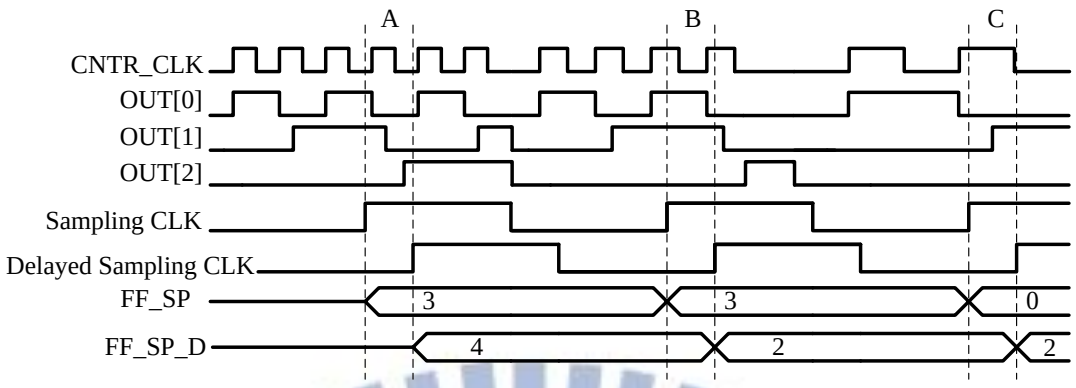


Fig.3-40Timing diagram for asynchronous sampling

3-3.3 Performance comparison

The power trend of synchronous and asynchronous counter is shown in Fig.3-41. The more bits the counter has, the more power is saved by replacing the synchronous counter with asynchronous one. For our design, 17-bit counter, synchronous counter will consume 4.53uW, where the asynchronous one will only consume 0.94uW. The overhead of using asynchronous counter is about 0.5uW at 10 kHz sampling frequency. It has about 68% power reduction overall.

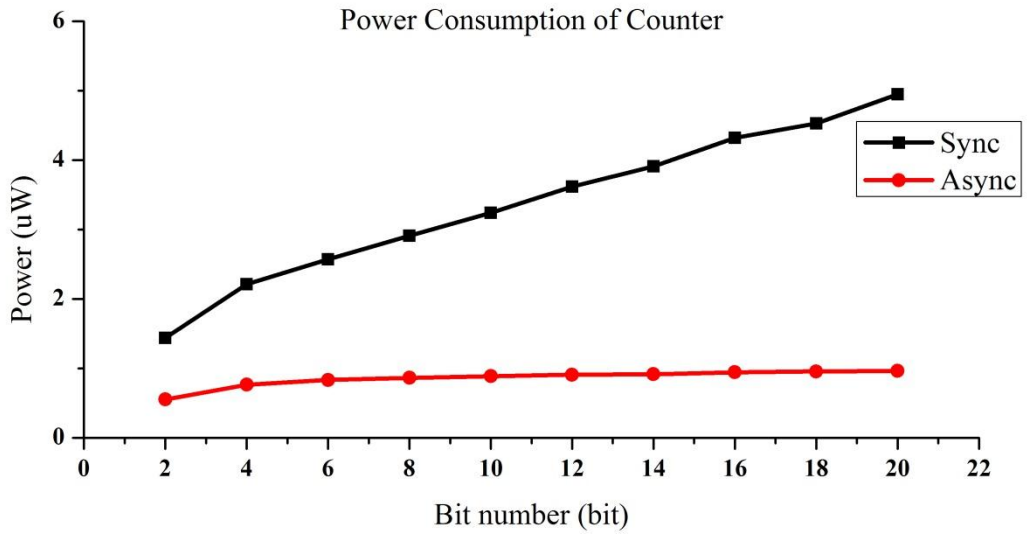


Fig.3-41 Power trend of synchronous and asynchronous counter

3-4 Sampling Flip-Flop

For the sampling flip-flops, not only the power consumption, sampling window of setup time and hold time is also the considered issue. As we introduced in 2-2.5 , the metastability of flip-flops causes the performance degradation of ADC. Here we first consider power issue to choose a suitable type of standard cell for the sampling flip-flops and then do the timing simulation for the chosen type of flip-flops. To improve the power consumption, we modify the sampling flip-flop with input gated. The details are shown below:

3-4.1 Standard cell flip-flop

For the flip-flop analysis, there are three main timing parameters we should care about: $CLK-Q$ delay, setup time and hold time. Here gives the definition in [11], where C, Q, D is referred to CLK, output, input respectively:

D_{CQ} : Propagation delay from the C terminal to the Q terminal, assuming that D signal has been set early enough relative to the leading edge of the C pulse.

U : Setup time, the minimum time between a D change and the triggering edge of C pulse, such that, even under the worst conditions, the output Q will be changed to equal to the new D value, assuming C is wide enough.

H : Hold time, the minimum time that D signal must be held constant after triggering, so that, even under the worst conditions, the Q output will remain stable assuming the time between latest change of D and the triggering C is more than U.

Three operation regions are defined in [12]: stable, metastable and failure regions. The stable region is the region that the region in Data-CLK (time difference between the last transition of data and the CLK trigger) axis that D_{CQ} does not depend on the

Data-CLK time. As the Data-CLK decrease, at the certain point of Data-CLK time, the operation starts entering the metastability region. In this region, the D_{CQ} increases significantly until the output goes fail. Then the operation goes into the failure region. The test circuit is shown in Fig. 3-42.

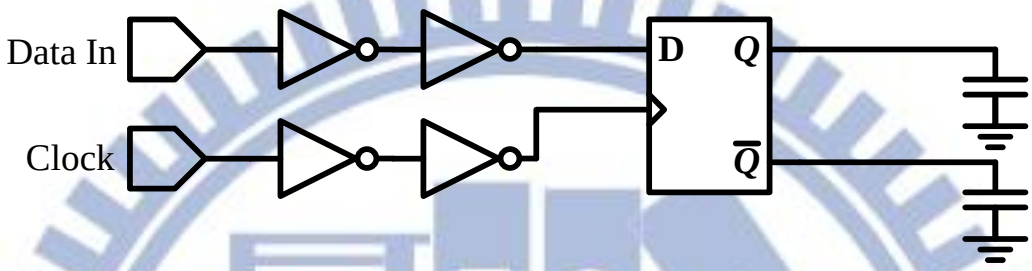


Fig. 3-42 flip flop testing circuit

There are many different types of flip-flops in umc90nm standard cell library. First, we simulate the power for each standard cell. The simulation result is shown in Table 3-2. For the low power requirement, we choose the low power flip-flops in standard cell library. Its setup time, hold time and D-Q delay simulation results are shown in Fig. 3-43. The optimal setup time is the Data-CLK time difference which makes the D-Q point minimal. The minimum D-Q point is 0.62ns at the setup time Data-CLK of 0.191ns which is the setup time of the flip-flop. At this point the CLK-Q propagation delay is 0.427ns. With near propagation delay 0.426ns the hold time is -0.04ns. The metastability window is 0.151 ns.

Flip-flop Type	**Power consumption (W)**
DFQRM0N	6.021e-08
DFQM0N	5.807e-08
LDFQRM0N	7.977e-08
LDFQM0N	4.947e-08
LACM0N	9.393e-08
LAM0N	9.302e-08

Table 3-2 Power comparison of standard cell flip-flops

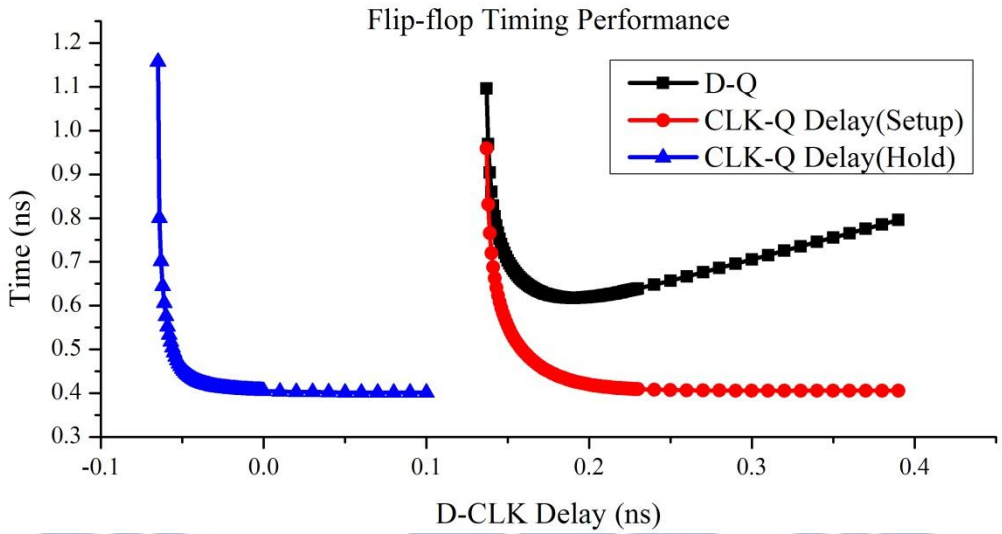


Fig. 3-43 Simulation results of timing items of low power flip flop cells. The metastability due to the minimal data-to-output delay is 0.151 ns.

3-4.2 Gated flip-flop

To further reduce the power of flip-flops, we do the power analysis about the flip-flop. We found that the most part of power consumption is due to the high frequency transition of input transition D. The spur is happening with the input variation as shown in Fig.3-44.

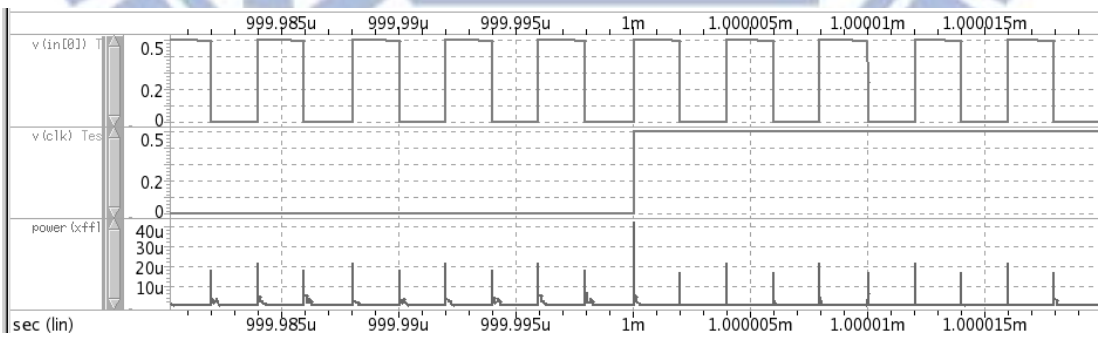


Fig.3-44 Power consumption of flip-flops

So, we applied the gated flip-flop, which is with an AND gate at the input of flip-flop, as Fig.3-45. The AND gate separates the input signal and the input D terminal of the flip-flop. Only the signal in the EN window can be transmitted to the

flip-flop input and influences the power of flip-flops. The EN window for the gated flip-flops is generated by the intersection of the CLK and its inverted delay. To ensure the setup time and hold time requirement, we generate two delayed CLK and use the original one and the last one for the EN window. The sampling CLK for the flip-flop is the middle delayed CLK as shown inFig.3-45 .

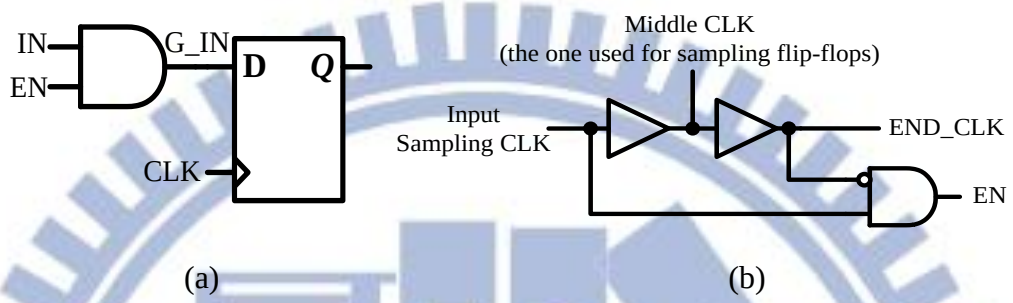


Fig.3-45 Gated flip-flop: (a) Gated flip-flop circuit; (b) En window circuit

After applying the gated flip-flop, the power of flip-flop is shown as Fig.3-46. We can see that the spur causing from the input transition is reduce significantly. The spur occurs only in the window around positive edge of CLK.

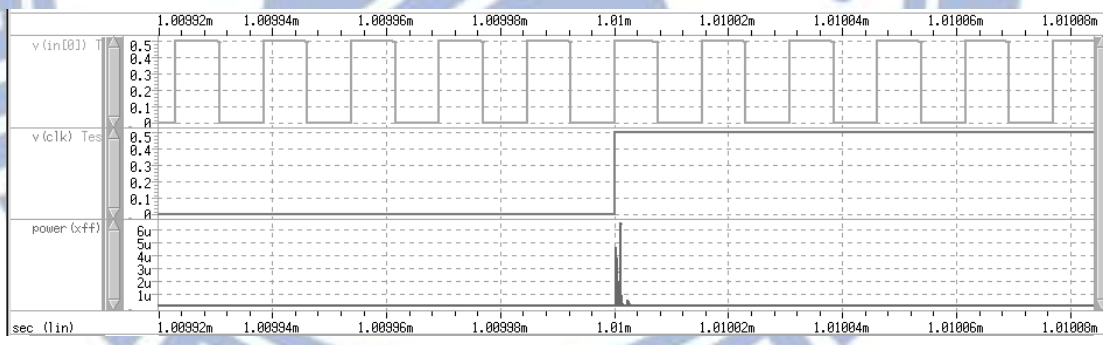


Fig.3-46 Power of gated flip-flop

3-4.3 Power comparison

Although the flip-flop power is reduced by applying the gated-cell in front of the input, this method adds the additional power of AND gated-cell and the EN window circuit. Here, we compare the power of gated-flip-flop with its overhead and the original flip-flop. For the fixed input frequency the power of modified input-gated

flip-flop has more than 83% reduction compared with the standard cell flip-flops and for the lower sampling frequency the reduction is more significant.

3-5 Flip-flops metastability compensation circuit

The metastability of flip-flops is caused by the setup or hold time violation. The way we avoid this situation is to use the DISABLE signal to stop counter counting before sampling CLK triggers. The DISABLE window is got by the intersection of the CLK and its delay and the real sampling is the delayed CLK. The delay of generating the DISABLE window should cover the metastability window of flip flops. The simulation result of delay line on each corner is shown in Table 3-3.

Time (ns)	**TT-25**	**SS-0**	**SS-45**	**FF-0**	**FF-45**
Tdr	2.84	5.10	5.00	1.85	1.95
Tdf	3.03	5.84	5.60	1.92	2.03

Table 3-3 Delay time in each corner

Chapter 4:
Simulation Results

Here shows the simulation results of our VCO-based ADC and gives the comparison with state-of-the-art. We give two different specifications for the VCO-based ADC for different applications. The first one is applied for single channel ECG acquisition circuit. For the normal high resolution ECG sampled sequence, the sampling frequency is set to 1k Hz. The other one is applied for multi-channel ECG acquisition circuit which needs higher sampling frequency CLK. We set the sampling frequency to 10k Hz for 8 channels ECG acquisition circuit.

4-1 INL and DNL

The INL and DNL simulation results are shown in Fig. 4-1 and Fig. 4-2. The maximum absolutely DNL value is 0.0481 LSB and maximum absolutely INL is 0.0688 LSB.

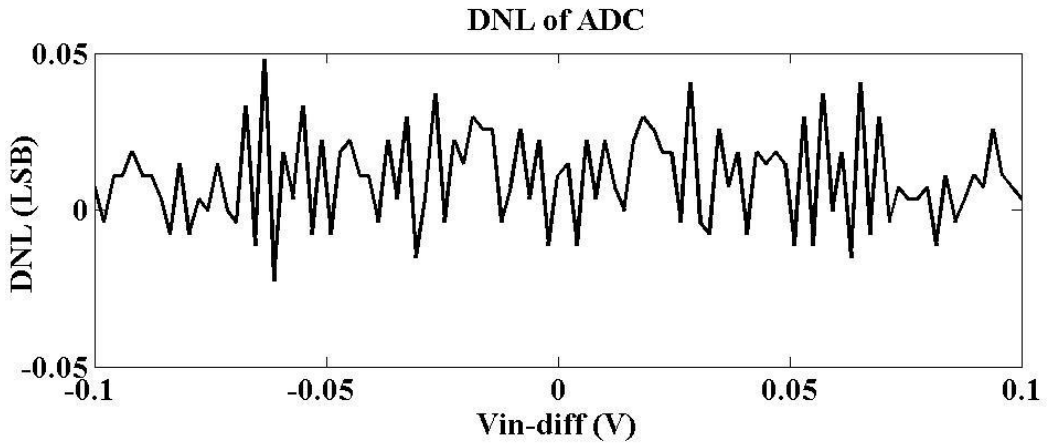


Fig. 4-1 DNL of ADC

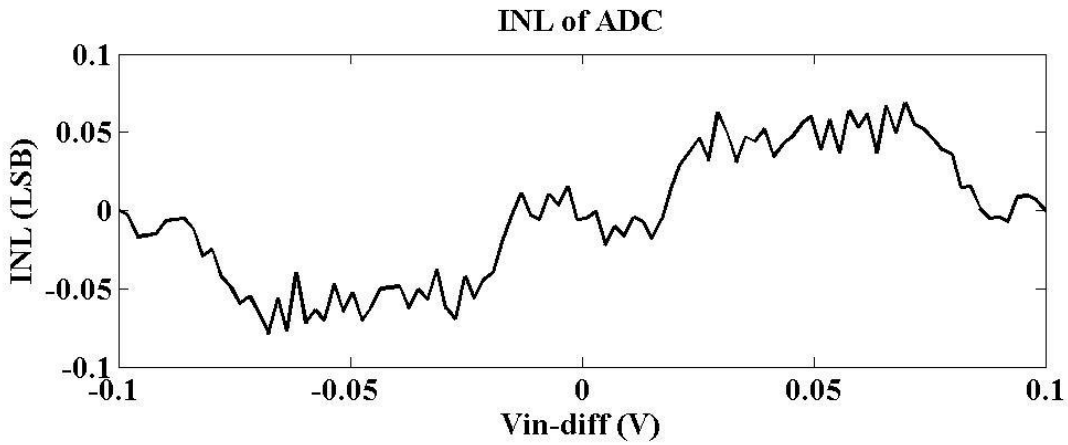


Fig. 4-2 INL of ADC

4-2 Waveform

Here shows the waveform of the ADC output. As we said before, two operating frequency of ADC is applied. In Fig. 4-3, the output result of ADC operating in 1k Hz is shown. And the output result of ADC operating in 10k Hz is shown in Fig. 4-4. Both of these input signals are two out-of-phase sine waves with amplitude 0.1V in frequency 150Hz. Both of the results are looked like the sine wave. The detail performance will be checked through performing the Fast Fourier Transform which will be shown in next section.

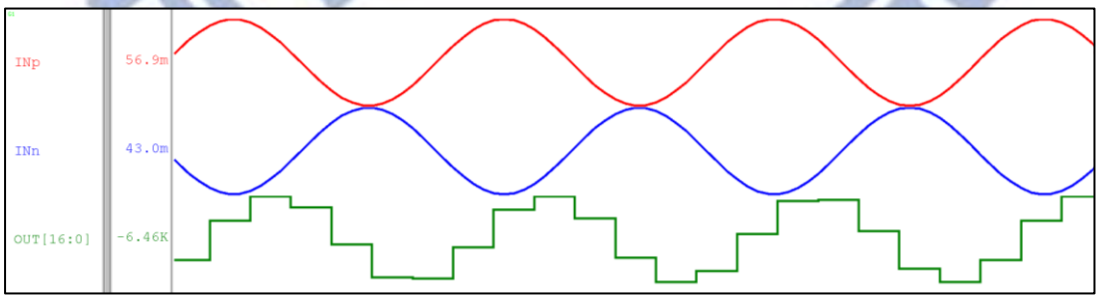


Fig. 4-3 ADC output of 1k Hz sampling rate

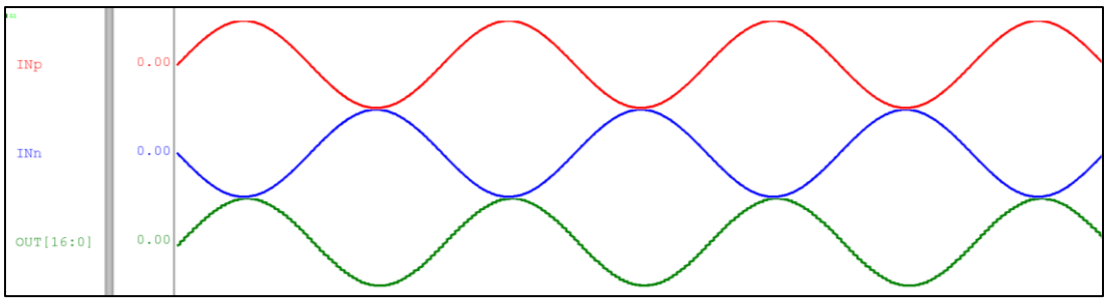


Fig. 4-4 ADC output of 10k Hz sampling rate

4-3 FFT result

We do the FFT to look details of the frequency composition of output of ADC. The power spectral density is got from the square of the FFT coefficient. Here shows the results.

For single channel, the power spectral density (PSD) result is shown in Fig. 4-5. The sampling frequency is 1k Hz and input frequency is 150 Hz. For multi channels, the input frequency is the same as the single channel and the sampling frequency is 10k Hz. This PSD result is shown in Fig. 4-4. We can calculate the SNR and SNDR through the PSD data to estimate the performance of ADC. The performance of ADC will be listed on Table 4-1 in next section.

Fig. 4-5 Power Spectral Density of ADC output in 1k Hz sampling frequency

Fig. 4-6 Power Spectral Density of ADC output in 10k Hz sampling frequency

4-4 Performance Summary

Here we summarize the performance of our ADC. The compared items are introduced in section 2-1. To calculate the efficiency of the ADC, there are two additional items we should consider: FOM and FOM2. FOM takes power, ENOB and

sampling frequency in consider to conclude the performance into a single value, where the calculation is shown in equation(4.1). FOM2 further includes the area to give more fairly comparison as shown in equation(4.2).

$$FOM = \frac{Power}{2^{ENOB} \times Fs} \tag{4.1}$$

$$FOM2 = FOM * area \tag{4.2}$$

As shown in section 1-2.2 , our ADC can be operated in two different applications. The first one is the single-channel ECG acquisition circuit. The sampling CLK is 1k Hz and ENOB can reach 10.4777 bits. In this operation speed, the ADC consumes 6.08uW and FOM is 4262.94 (fJ/conv. Step). FOM2 is 21.3147 which is more competitive to the state-of-the-art. The area we use is according to the layout in section 5-6. The power of this application is too large and need to be improved. We will give the power analysis and the reduce technique in the following sections.

The other application is the multi-channel ECG acquisition circuit. The sampling CLK is 10k Hz for 8 channels application. The mux switches alternately for each channel in frequency of 10k Hz and with two cycles rest. In this way, the equivalent sampling frequency of each channel is 1k Hz. Total power consumption is 6.16uW, so the power per channel can be divided by 10. The final power is 0.62uW. ENOB of the ADC which operating in 10k Hz is 9.6427 bits. The FOM can be calculated as 77.56 (fJ/conv. Step). The FOM2 is 0.3878.

	[13] 2012 JSSC	[14]2011 VLSI	[15]2012 ISCAS	[16]2009 JSSC	This Work (multi)	This Work (single)
Technology	0.13um	0.13um	0.18um	0.35um	90nm	90nm
Sampling Frequency(Hz)	1k	31.25k	16k	1k	10k	1k
Supply Voltage(V)	1/0.4	1.2	1.2	1	0.5	0.5
Power(W)	53n	* 1.1u	450n	230n	*0.62u	6.08u
ENOB(bit)	9.1	9.7243	8	10.2	9.6427	10.4777
SNDR(dB)	56.7	60.3	49.72	63	59.8088	64.8356
SFDR(dB)	67.6	-	-	74	62.2436	80.591
FOM (fJ/conv. step)	94.5	41.5	132	195	77.5621	4262.94
Area(mm^2)	0.191	0.11	0.078	0.28	0.005	0.005
FOM2($fJ\text{-}mm^2$/ conv. step)	18.082	4.565	10.296	54.6	0.3878	21.3147
**FOM2_N (pJ /conv. step)	1.0699	0.2701	0.3178	0.4457	0.0479	2.6314

Table 4-1 Comparison Table

(*: power per channel **: FOM2 with area normalized to technology)

To further improve the power performance, we do the power analysis to calculate the power of each block. The distribution is shown in Fig. 4-7 and the detail value is listed in Table 4-2. Here we separate ADC into 5 blocks for considering the power distribution. VCO block is the total power of 2 VCOs and some buffers of the VCO output. CNTR block includes the 2 asynchronous counters. ASY_OH block is composited of the additional flip-flops for sampling the value of asynchronous counter and the decision circuit of value chosen. FF block include the sampling input gated flip-flops and additional circuit for gated flip-flops. OUT_CAL block is the

block of subtraction circuit between two differential ends. We can figure out that the power consumption of VCO dominates the total power and counter comes after VCO. To reduce the power of ADC we should turn off the VCO. And in this way the power of CNTR can be also reduced due to the VCO output is the trigger signal of CNTR.

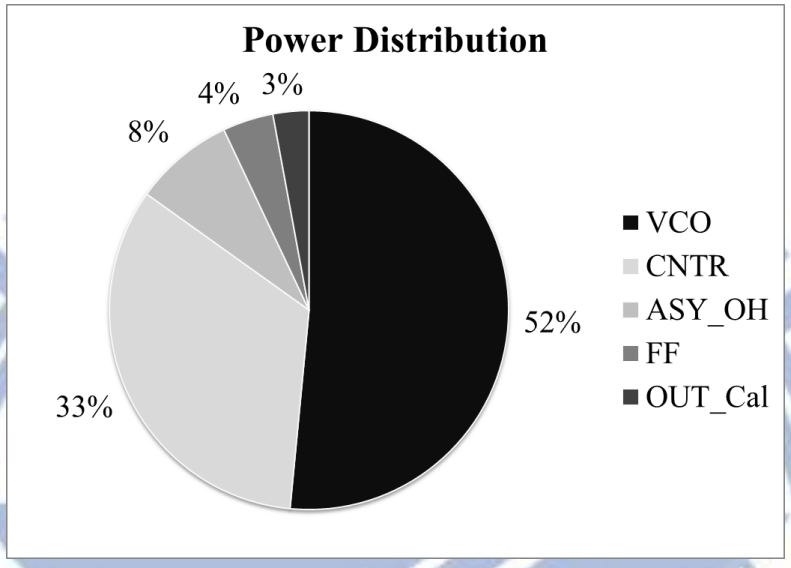


Fig. 4-7 Power distribution

Function Block	Power (uW)
VCO	3.1321
CNTR	2.0265
FF	0.250294
OUT_Cal	0.1772
ASY_OH	0.492614
Total	6.078708

Table 4-2 Details power consumption of each block

Chapter 5:
Dynamic Sampling Technique

For the bio-signal, information is concentrated in a part of duration instead of the whole period. For example, the ECG information is concentrated in the QRS complex and P, T waves as shown in Fig. 5-1. So, in this kind of application, we apply the dynamic sampling technique to reduce the power effort on the low information segment. The briefly architecture of ADC with dynamic sampling is shown in Fig. 5-2. There are two main parts for the dynamic mechanism: signal information estimation and controller for power reduction. The signal is first estimated by sensing the variation of signal. If the variation is large, we treat it as the high information part. If the signal changes smoothly, it will be treated as the low information part. And based on the estimation the control signal is applied to reduce the power. The details will be shown in the following sections.

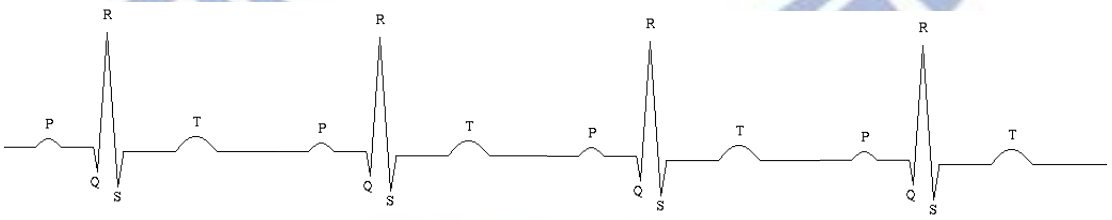


Fig. 5-1 ECG signal

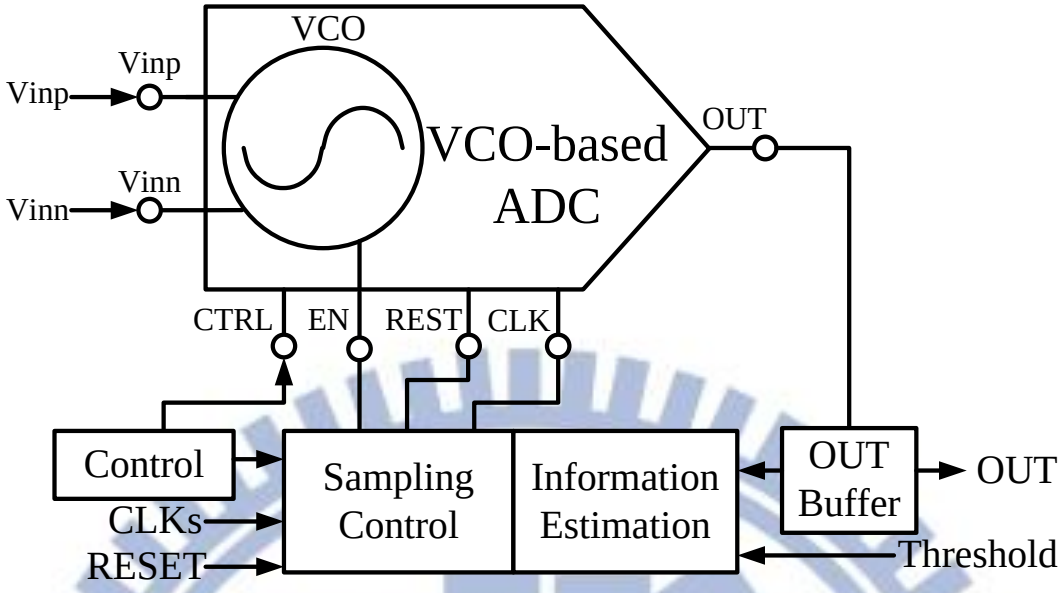


Fig. 5-2 briefly architecture of ADC with dynamic sampling

5-1 Dynamic sampling principle

5-1.1 Information estimation

In our dynamic sampling technique, we sense the variation of signal to estimate the information quantity for the input signal. The variation is determined by the slope of the signal. We subtract the two adjacent values (OUT1, OUT2) sampled in time difference, T_{DEL} .Due to the output code of VCO-based ADC is converted by counting the VCO oscillation number during a given period, for estimating the OUT1, OUT2, we need to apply additional period for each one to sense input. The period for each value sensing the input is the also set to T_{DEL} .After the difference is got, we further compare the value with a given threshold to determinate the information quantity. If the difference is large than the threshold, we regard the signal as high information part. Otherwise, if the difference is smaller than the threshold, we declare the signal having low information.

According to the frequency of information estimation processing, the dynamic sampling technique we proposed can be divided into 3 categories:

Partial ADC-SP cycle estimation

Estimate the input information in every ADC sampling cycle. This type of estimation takes partial of ADC sampling (ADC-SP) cycle (1/N ADC-SP cycle) to determine the information volume. As shown in Fig. 5-3, OUT1, OUT2 are sampled by DEL-SP CLK in time difference T_{DEL} in each ADC-SP period, T_{ADC-SP} .The information estimation calculates the difference between the OUT1 and OUT2 to compute the slope in the estimation region, T_{ADC-SP} / N .

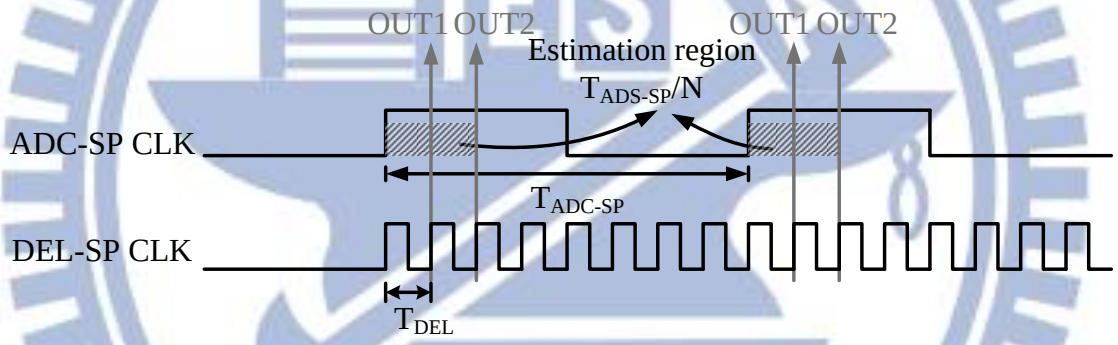


Fig. 5-3 Brief illustration of partial ADC-SP cycle estimation

Fixed DS CLK estimation

Estimate the input information in every given dynamic sampling (DS) cycle. This type of estimation requires another DS CLK to determine the estimation frequency. The input variation is estimated in each DS cycle as shown in Fig. 5-4. Here the DS CLK can be more or less than the ADC sampling frequency. If the DS CLK we use is equal to the ADC sampling frequency, the estimation is equal to the partial ADC-SP cycle estimation. OUT1, OUT2 are sampled by DEL-SP CLK in time difference T_{DEL} in each DS cycle. The information estimation calculates the difference between the OUT1 and OUT2 to compute the slope in the estimation region.

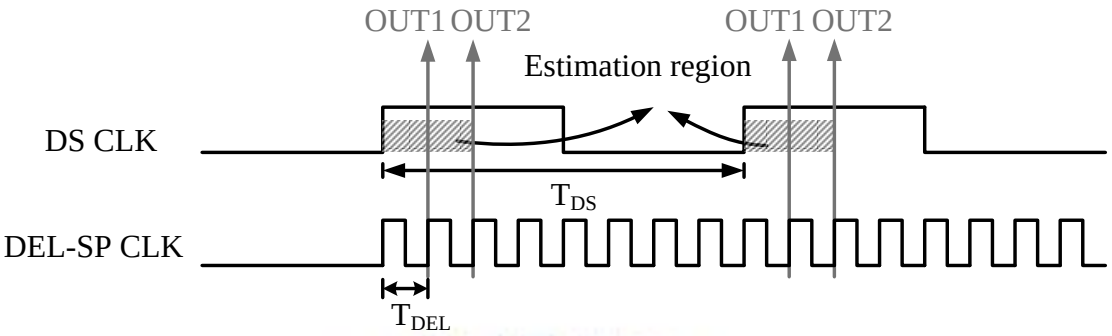


Fig. 5-4 Brief illustration of fixed DS CLK estimation

Various DS frequency estimation

Different from previous two kinds of estimation technique, VDS doesn't have the regular frequency for estimation. This type of estimation calculates the difference only when OUTPUT of ADC is sampling as shown in Fig. 5-5. When each OUTPUT is calculating, OUT1, OUT2 are sampled by DEL-SP CLK in time difference, T_{DEL}. The information estimation calculates the difference between the OUT1 and OUT2 to compute the slope in the estimation region.

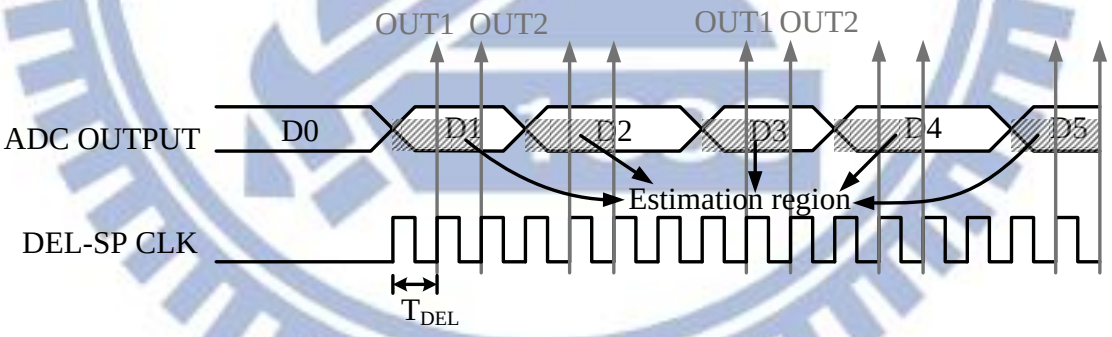


Fig. 5-5 Brief illustration of various DS frequency estimation

As the description above, there are three important parameters need to be mentioned:

f_{DS}: The frequency of DS CLK, this value determines the sensitivity of the signal estimation: how often the estimation processes.

f_{DEL}: The frequency of DEL-SP CLK, this value determines the resolution of

OUT1, OUT2 for slope calculation further influence the absolute value of difference between OUT1, OUT2.

Threshold: The boundary of low and high information determination. This value influences the power reduction percentage and the distortion between the original signal and the one applied dynamic sampling technique.

5-1.2 Sampling Control for power reduction

After information estimation is done, the control is adjusting according to the estimation result. There are two kinds of control methods we propose:

ADC resolution adjustment

For the VCO-based ADC the resolution of ADC is determined as equation(2.11). So, we can modify ADC resolution by adjusting the time for VCO oscillation according to the activity of the input signal. Turn off the oscillation of VCO in part of cycles to reduce the ADC resolution and the power of VCO can also be saved in this period of time.

ADC-SP CLK frequency adjustment

In this type of adjustment, the power of can be saved by applying ADC sampling CLKs in different frequencies. There are two types of CLKs adjustments. The first one is giving two kinds of fixed frequency CLKs, CLK-H and CLK-H represent as CLK in high/ low frequency respectively. The chosen of ADC-SP CLK is determined by the information estimation result. For the high information segment, CLK-H is applied for ADC sampling. Otherwise, the low information part is sampled by CLK-L. The other type of adjustment is skipping sample the value in given ADC-SP CLK frequency. It samples the value only when high information segment is sensing. The ADC OUTPUT in low information segment will be skipped without sampling. In

these ways, the power consumption of the unimportant part can be reduced.

5-2 Performance Item

Before stating the technique we proposed, there are some performance item should be mentioned.

5-2.1 Percentage Reduction Distortion (PRD)

Percentage reduction distortion (PRD) represents the distortion amount between the original signal and the reconstructed signal. There are two kinds of definition for PRD. The first one is shown in equation(5.1). This kind of calculation doesn't consider the influence of the absolutely value of signal.

$$PRD(\%) = \sqrt{\frac{\sum_1^N \{x(n) - x'(n)\}^2}{\sum_1^N \{x(n)\}^2}} \times 100\%$$

$$where\ x(n): Original\ signal$$
$$x'(n): Reconstructed\ signal \tag{5.1}$$

For the larger $x(n)$ the performance of this type of PRD will be better. So, here comes the second definition which we use in follow section:

$$PRD(\%) = \sqrt{\frac{\sum_1^N \{x(n) - x'(n)\}^2}{\sum_1^N \{x(n) - \bar{x}(n)\}^2}} \times 100\%$$

$$where\ x(n): Original\ signal$$
$$\bar{x}(n): Mean\ of\ original\ signal$$
$$x'(n): Reconstructed\ signal \tag{5.2}$$

It subtracts the mean value of the testing signal, so the influence of absolute value is reduced. The comparison is more fair between each test pattern. In this thesis we use the second type of PRD definition.

5-2.2 Compression Ratio (CR)

Compression ratio (CR) is the ratio of compressed signal to the original signal as shown in equation(5.3). It represents the compressive performance for the mechanism. For the smaller value, the higher compression is performed. From the point of view of data transmission, the smaller CR can safe more transmission power.

$$CR = Orginal\ Size / Compressed\ Size \tag{5.3}$$

5-2.3 Percentage Power Reduction (PPR)

Percentage power reduction (PPR) is the item we most curious about. The formula is shown in equation(5.4). It represents the reduction percentage after our dynamic sampling technique is applied.

$$PPR(\%) = \frac{(Original\ Power - Reduced\ Power)}{Original\ Power} \times 100\% \tag{5.4}$$

Our design goal is to maintain the acceptable PRD while increasing the PPR. CR is not curious in every dynamic sampling technique we proposed. But, with the lower CR, the power consumption during data transmission can be even further reduced.

5-3 Architecture

There are 3 main kinds of dynamic sampling technique we proposed: partial dynamic sampling (PDS) technique, fixed dynamic sampling (FDS) technique and various dynamic sampling (VDS) technique. The main difference between these 3 kinds of DS techniques is the information estimation as we mentioned in section 5-1.1 .The PDS technique estimates signal information in partial ADC-SP cycle estimation method while the FDS technique is applied by fixed DS CLK estimation and the VDS technique is compute through various DS frequency estimation. Further

in the PDS technique, according to different control method, 2 modes are applied: low distortion mode and data compression mode. The details will be shown in the following section.

5-3.1 Partial dynamic sampling (PDS) technique: low distortion mode

Dynamic sampling mechanism

The information estimation of this technique is the partial ADC-SP cycle estimation. It takes 1/N ADC sampling period to do the slope calculation, where N is the even number for simpler hardware design. After slope calculation, in this mode we control the ADC by adjusting the resolution. We turn off the VCO in the rest of the cycle for the low information segment to reduce the power of VCO as shown in Fig. 5-6, N is taken as 4 for example.

The ADC-SP CLK is for the sampling for ADC OUTPUT and the DEL-SP CLK applies time difference of T_{DEL} for OUT1, OUT2 sampling for the slope calculation. The diagonal stripe region is presented as the estimation region for slope calculation and the diamond pattern region is presented as the region VCO oscillates. It takes 1/4 ADC-SP cycle for calculation, in order to get 2 values, OUT1, OUT2 for subtraction the frequency of DEL-SP CLK should be 16 times of the ADC-SP CLK. The decision for the power reduction will make after estimation. Estimation region A (ER-A) determines the enable for oscillation of VCO in power reduction region A (PR-A). If the high information segment is sensed in ER-A, the VCO continues oscillating in the PR-A. There is no reduction for this kind of situation. On the other hand, if the low information segment is sensed as the ER-C in Fig. 5-6, VCO is turned off in the rest cycle. The power in PR-C is saved. Only the power for estimation is consumed in this

situation.

Finally, in the low distortion mode the output of ADC is multiplied by N for the low information segment. By this method, MSB of OUTPUT is determined by the input information and LSB are all 0s. In the high information segment, the output of ADC is the one sampled by ADC-SP CLK and both MSB and LSB are determined by the input. In this mode the input information is kept within the OUTPUT more or less the distortion for power reduction technique is low.

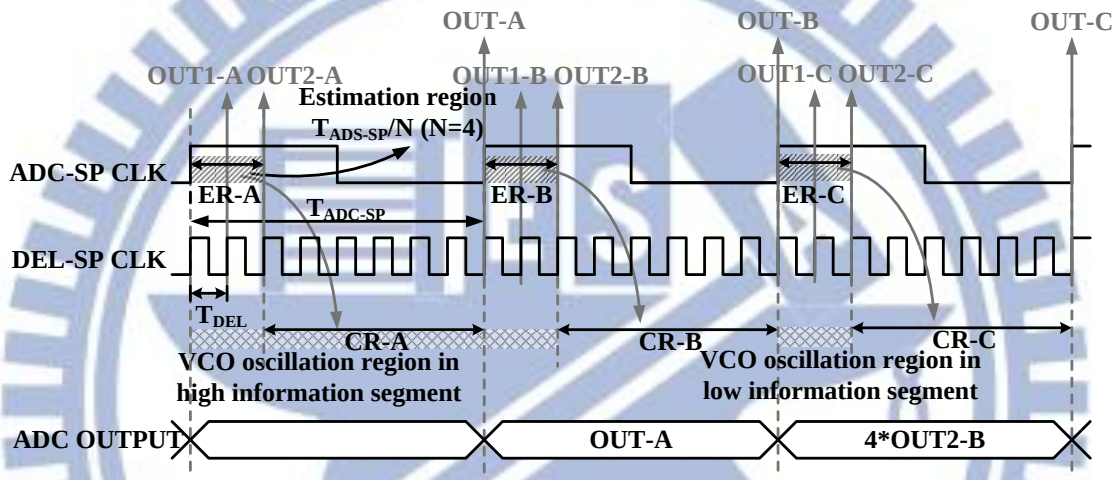


Fig. 5-6 illustration of PDS-low distortion mode technique

Simulation result in MATLAB

We do the brief simulation in the MATLAB. Applying the ECG signal into the circuit, Fig. 5-7 shows the relation between the relation between PRD and the power consumption of this kind of method. For different data points are relative to different thresholds which influence the VCO turn-off percentage and further affect the power consumption. And for this technique, the power and PRD will saturate when all signals are treated as the low information part and VCO turns off in almost every cycle. The power reduction will reach 1/N of the original power. For different N value, it can cover different PRD range. The detail performance values will be listed in section 5-3.5 .

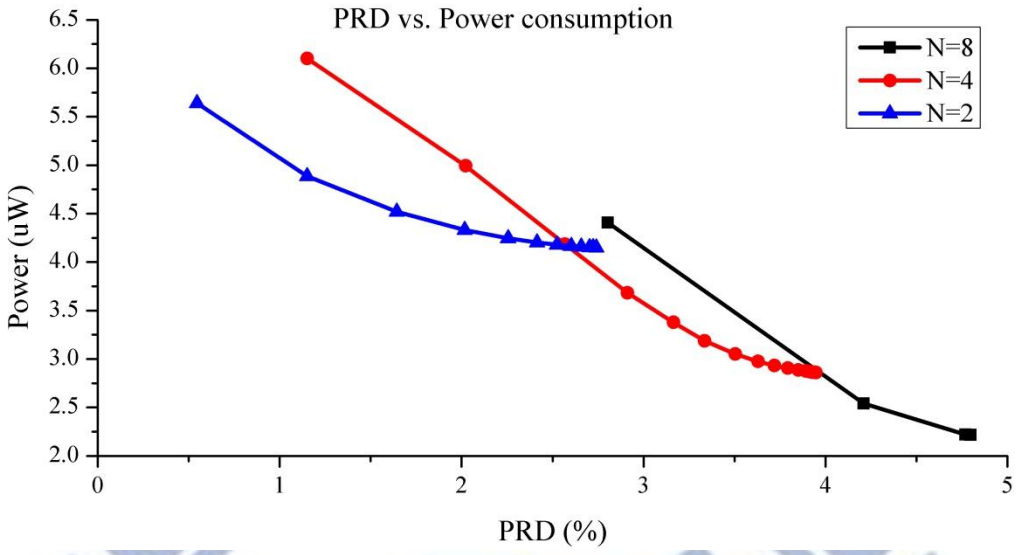


Fig. 5-7 PRD vs. Power consumption of PDS high resolution mode

5-3.2 Partial dynamic sampling (PDS) technique: data compression mode

Dynamic sampling mechanism

The information estimation of this mode is also the partial ADC-SP cycle estimation. The difference between this mode and the pervious one is the control mechanism. In the high compression mode, the estimation result influences the sampling of the ADC. The OUTPUT for low information segment is skipped as shown in Fig. 5-8. This method can support the data compression in low information segment to reduce the data transmission power. But due to the information of low information segment is thrown away in the OUTPUTs, the distortion is higher than the low distortion mode. Especially, when the signal contains low information in the long period, the input information will lose in this case in a long period.

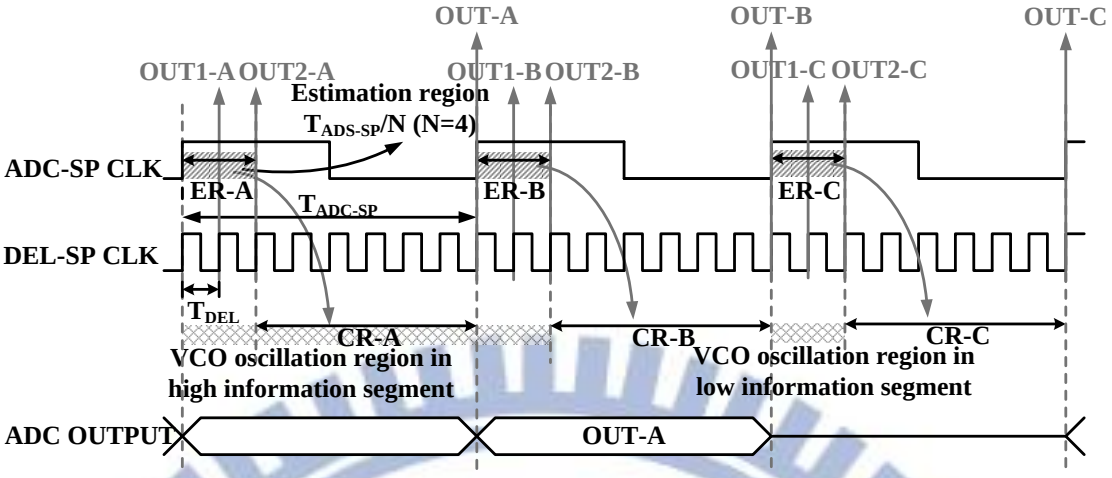


Fig. 5-8 illustration of PDS-data compression mode technique

Simulation result in MATLAB

The same with previous method, we do the simulation in the MATLAB. The distortion of this method is quite large relative to the high resolution mode. We plot the PRD vs. power consumption figure in the region of PRD less than 20%. Fig. 5-9 shows the result. The detail performance values will be listed in section 5-3.5 .

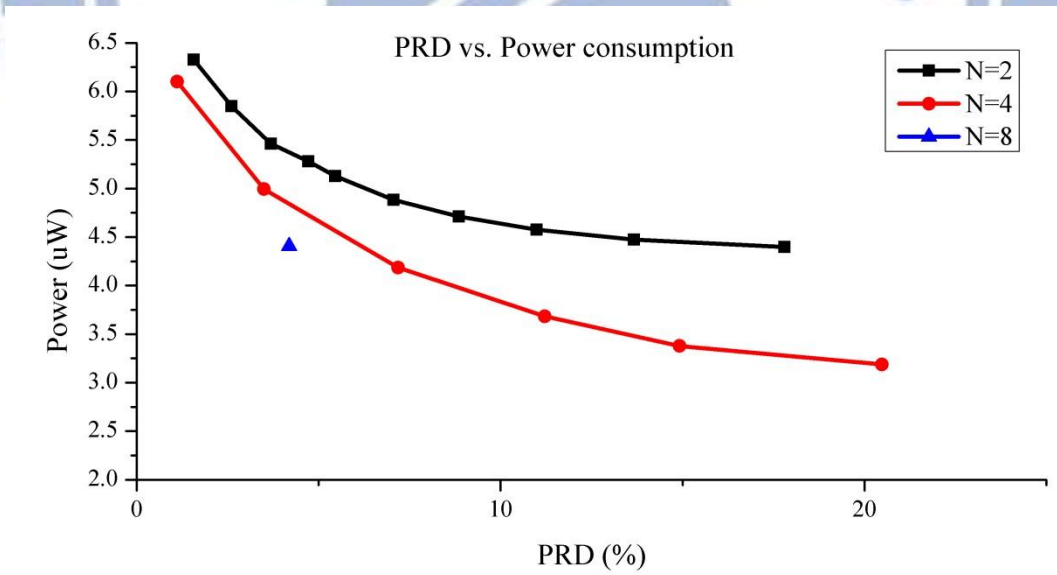


Fig. 5-9 PRD vs. Power consumption of PDS data compression mode

5-3.3 Fixed dynamic sampling (FDS) technique

Dynamic sampling mechanism

The fixed dynamic sampling (FDS) technique as its name applied the fixed DS frequency for information estimation. For the ADC control, two different fixed ADC sampling CLKs, ADC-SP CLK-H and ADC-SP CLK-L represented as the high frequency and low frequency respectively, are applied and be chosen according to the estimation result.

As shown in Fig. 5-10, ADC-SP CLK-H and ADC-SP CLK-L are the two kinds of CLK for ADC sampling. ADC-SP CLK-H is also served as DEL-SP CLK which applies time difference of T_{DEL} for OUT1, OUT2 sampling for the slope calculation. The DS CLK will determine the estimation frequency and for each estimation it takes 2*TDEL for calculation. The decision for the power reduction will make after estimation. Estimation region A (ER-A) determines the ADC sampling CLK in power reduction region A (PR-A). If the high information segment is sensed in ER-A, the ADC-SP CLK-H is chosen as the ADC-SP CLK and VCO continues oscillating in the whole sampling cycle in PR-A. There is no reduction for this kind of situation. On the other hand, if the low information segment is sensed as the ER-B in Fig. 5-10, ADC-SP CLK-L is chosen as the ADC-SP CLK and VCO is turned off until the edge trigger of ADC-SP CLK-L and also in order to keep the same resolution for both CLK-H and CLK-L, the VCO oscillates only 1 CLK-H cycle as shown in the PR-B others will be turned off to save the power.

Finally, ADC output is sampled by the varying ADC-SP CLK for each sampling the oscillation time for VCO is set to equal to the period of CLK-H (TDEL). The drawbacks of this technique are that complexity of the control is increase for the

sampling mechanism and the additional power for information estimation is consumed.

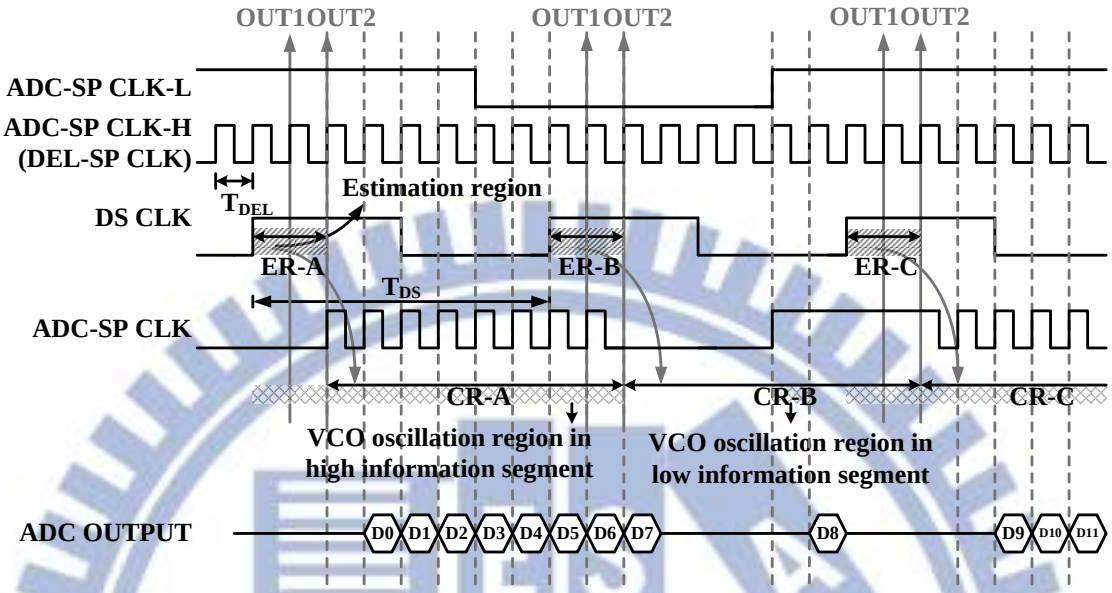


Fig. 5-10 illustration of FDS technique

Simulation result in MATLAB

The result of the relation between PRD and the power consumption is shown in Fig. 5-11. The power is reduced as PRD is increased. The detail performance values will be listed in section 5-3.5 .

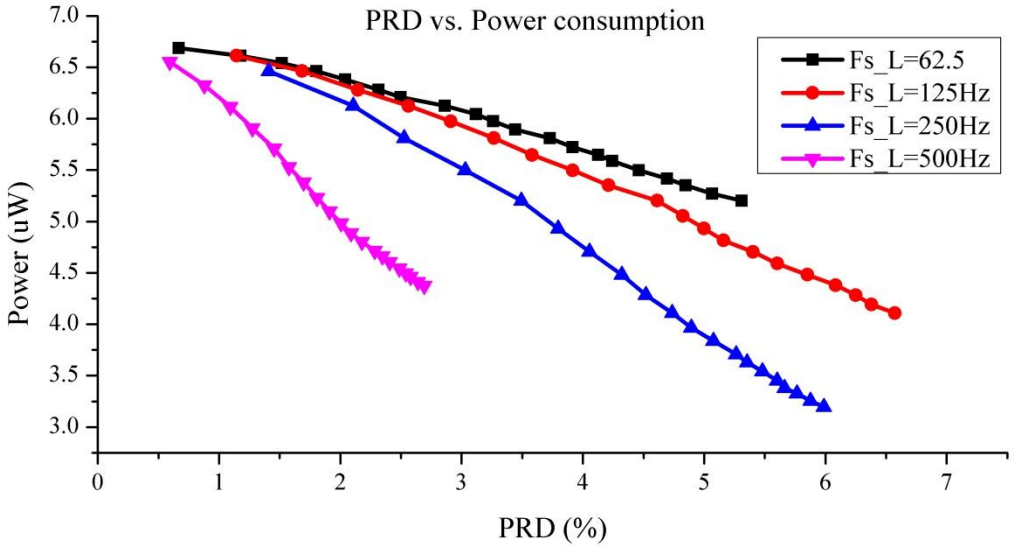


Fig. 5-11 PRD vs. Power consumption of FDS

5-3.4 Various dynamic sampling (VDS) technique

Dynamic sampling mechanism

The various dynamic sampling (VDS) technique applies the various DS frequency in information estimation stage. The performing of estimation depends on the OUTPUT transition. The same with FDC, two different fixed ADC sampling CLKs are applied for control method.

As shown in Fig. 5-12, ADC-SP CLK-H and ADC-SP CLK-L are the two kinds of CLK for ADC sampling. Additional DEL-SP CLK applies time difference of T_{DEL} for OUT1, OUT2 sampling for the slope calculation. In order to get 2 values, OUT1, OUT2 in the ADC-SP CLK_H cycle for subtraction the frequency of DEL-SP CLK should be 2 times of the ADC-SP CLK-H. After estimation, the power reduction mechanism is the same with the FDS technique.

When the ADC OUTPUT, D_0 is calculated, the information estimation is given in ER-B and further determine the sampling CLK in PR-B. As the next OUPUT, D_1 is sampled, the next estimation will be make in ER-C.

For each ADC output sampling, the oscillation time for VCO is set to equal to the period of ADC-SP CLK-H. And the time for slope calculation is equal to 2*TDEL. The complexity of the control is increase for the sampling and estimation mechanism.

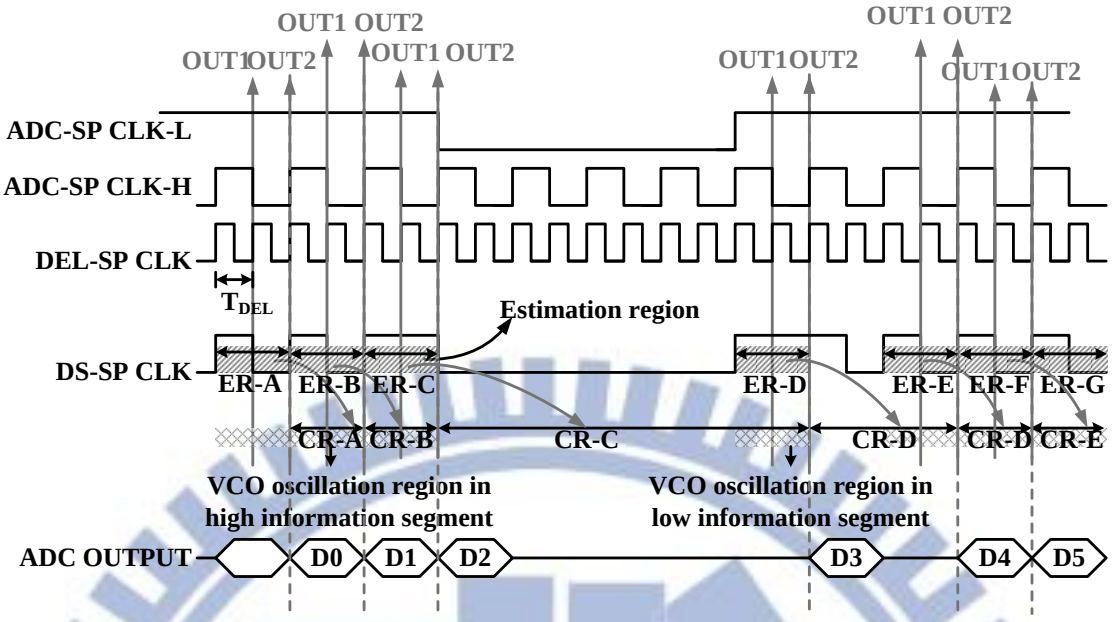


Fig. 5-12 illustration of VDS technique

Simulation result in MATLAB

Fig. 5-13 shows the relation between the relation between PRD and the power consumption of this kind of method. We can see that the distortion of this method is very large. The power reduction is less to maintain 5% PRD performance. The detail performance values will be listed in section 5-3.5 .

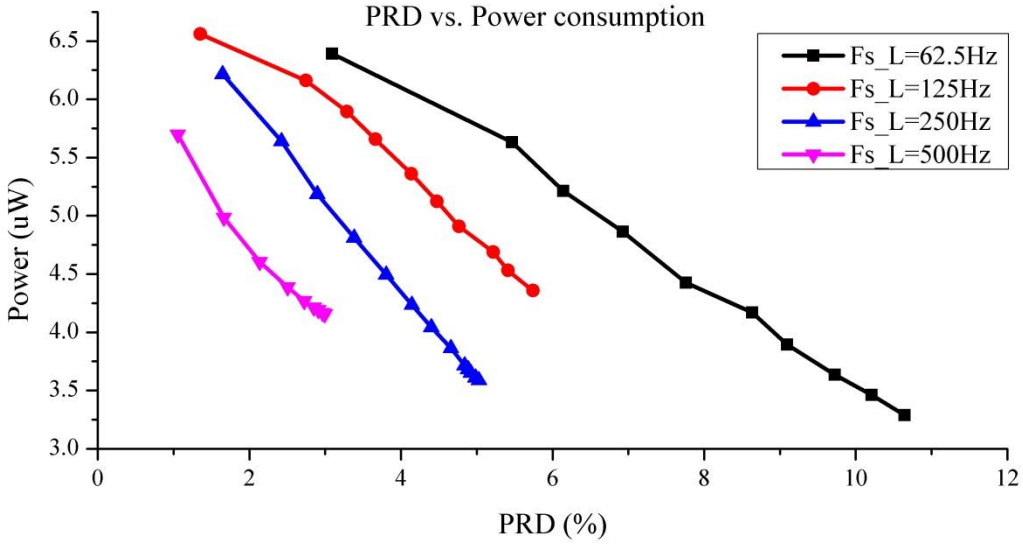


Fig. 5-13 PRD vs. Power consumption of VDS

5-3.5 Performance summary and comparison

We compare the proposed technique in previous section in the same sampling frequency as shown in Table 5-1. We use the sampling frequency as 1k Hz which is the specification for single channel ECG acquisition circuit. We set the PRD requirement to be less than 5 %. The power reduction of PDS-mode1 (low distortion mode) is much than others. So we apply this technique to our design.

Method	**Fs/ Fs_H (Hz)**	**Fs_L (Hz)**	F_{DS}	F_{DEL}	CR	**PRD (%)**	**Power (uW)**	**PPR (%)**
PDS-mode1 low distortion mode	1k	-	-	16k	-	4.80	2.22	63.53
	1k	-	-	8k	-	3.95	2.86	52.93
	1k	-	-	4k	-	2.74	4.15	31.71
PDS-mode2 data compression mode	1k	-		8k	1.8	3.50	5.57	8.33
	1k	-		4k	2.29	4.72	5.28	13.16
FDS	1k	62.5	250		1.36	4.85	5.35	11.95
	1k	125	250		1.53	5.00	4.93	18.88
	1k	250	250		2.27	4.97	3.91	35.61
VDS	1k	62.5	-	2k	1.07	3.09	6.39	-5.17
	1k	125	-	2k	1.54	4.77	4.91	19.23
	1k	250	-	2k	2.53	4.98	3.61	40.62
CS [17]	1k	-	-	-	1.5	4.76	3.47	42.86

Table 5-1 Comparison table of dynamic sampling

5-4 Circuit simulation

We further implement the proposed dynamic sampling technique into the circuit level. To have more flexible on the PRD range, we choose N=4 for the

implementation. The simulation results are shown in the following sections.

5-4.1 ECG Waveform

We apply the ECG signal to our design. Here shows the waveform of simulation result. We can see that the output of ADC and the original signal are the same in naked eye.

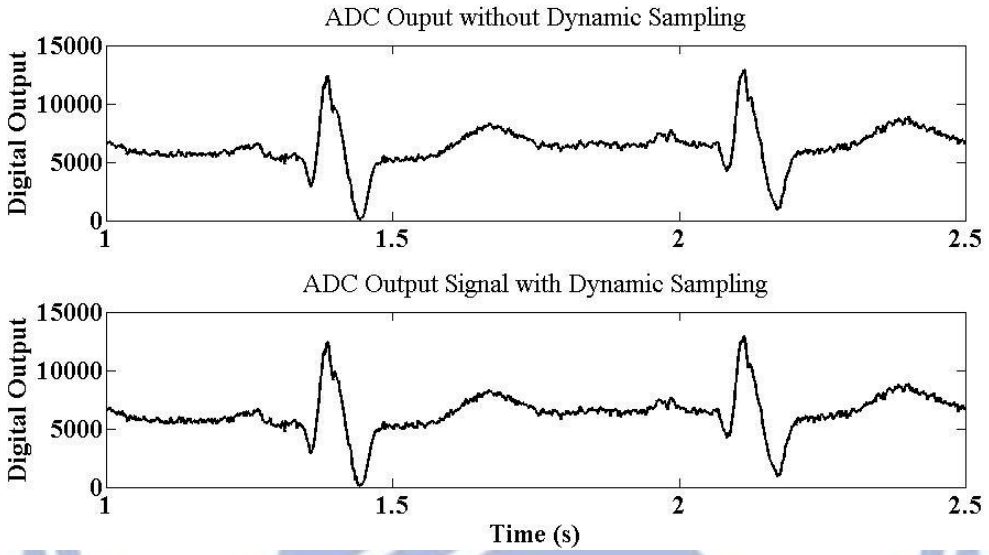


Fig. 5-14 ECG signal simulation result

5-4.2 Noise Influence

We apply the noise to the original ECG signal and send the combined signal to our design to see if the noise will influence the output of ADC. The results are shown below.

Power Line Interference (PLI)

The 60Hz sine wave is added to the ECG signal to generate the one which influenced by the PLI noise as shown in Fig. 5-15. The signal in 60 Hz passes directly to the output of ADC. We can see that the one with dynamic sampling output still contains the PLI noise. The PLI noise should be filtered out by the digital filter.

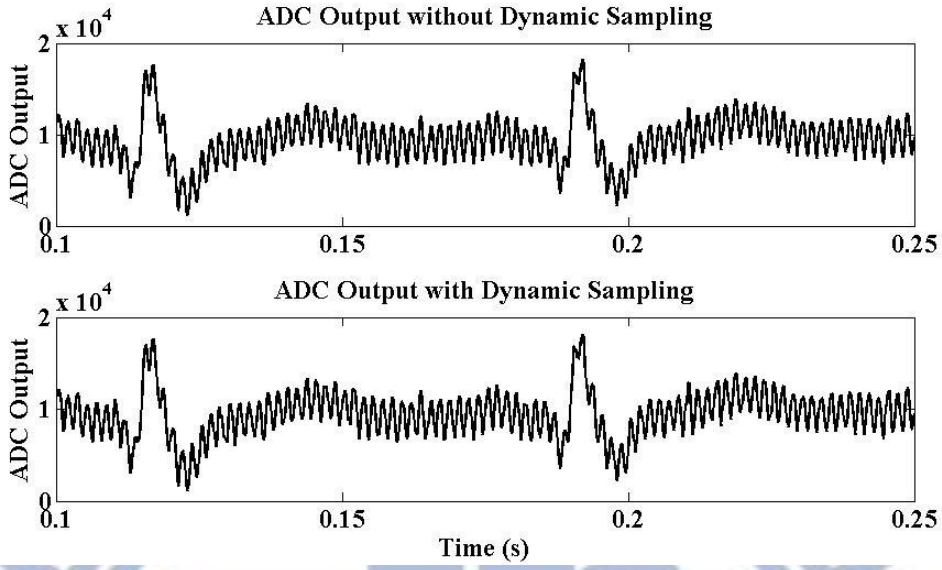


Fig. 5-15 PLI noise influence

AWGN noise

We add the AWGN noise to the input. The simulation result is shown in Fig. 5-16. The same as the PLI noise, the noise parts must be filtered out in digital domain after ADC.

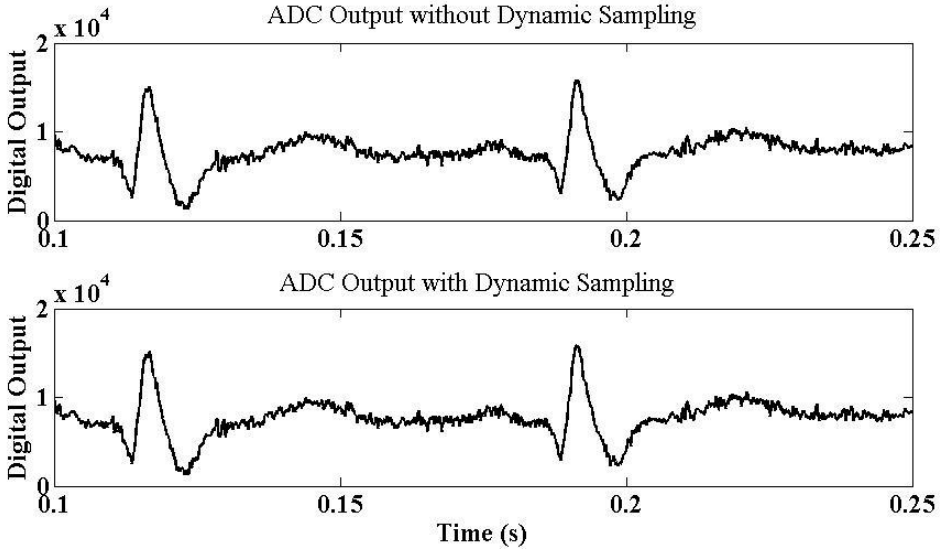


Fig. 5-16 AWGN noise influence

5-5 PRD &Power reduction result

Here shows the distortion versus power consumption result. For the 5% limit of

the PRD, the total power of ADC with dynamic sampling technique is 2.86uW. Compared with the 6.08uW power consumption without dynamic sampling technique, the reduction of power can achieve 53%.

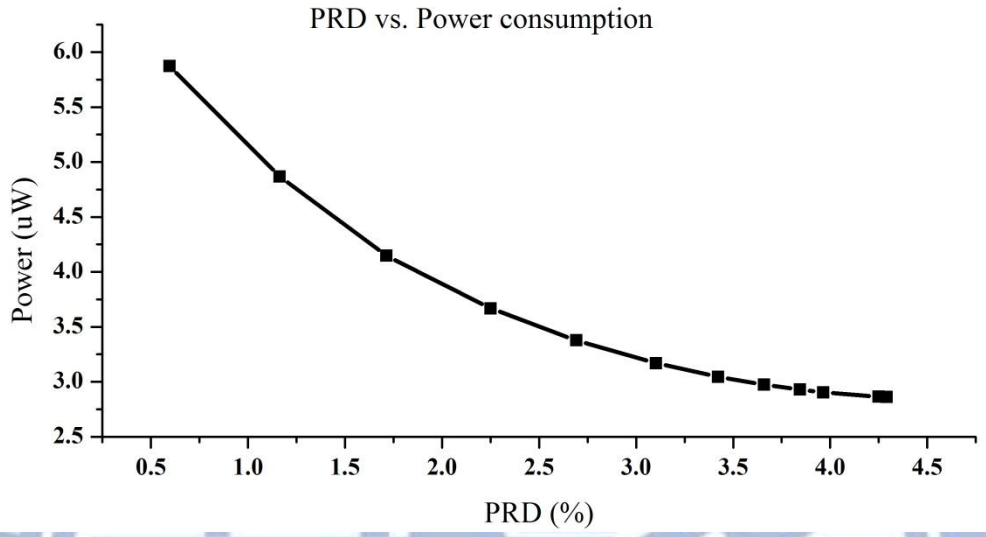


Fig. 5-17 PRD vs. Power consumption

5-6 Chip Implementation

The ADC with dynamic sampling is implemented in UMC 90nm CMOS process technology. Total area is 97.24 um*181.8 um as shown in Fig. 5-18. The core area is 106.4um*55.44um for ADC and 33.6um * 55.44 um for dynamic sampling. To avoid the interference between analog and digital signal, we add the routing blockage above the VCO to restrict the signal routing across the VCO circuit. To reduce the noise coupling from the power line and substrate, we also separate the power between VCO and the rest of the design and add the guard ring around the VCO.

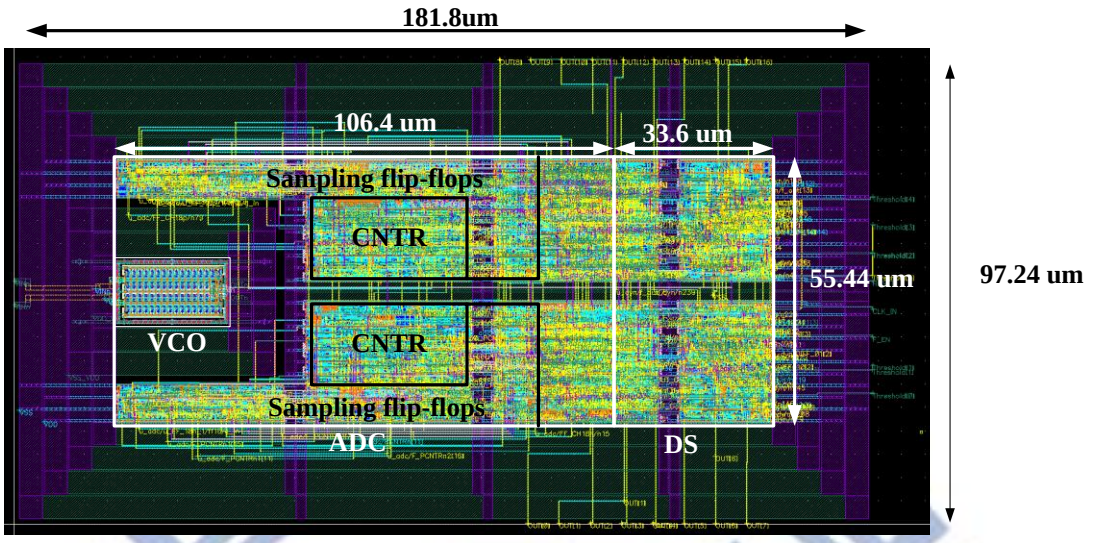


Fig. 5-18 ADC with dynamic sampling chip implementation

Chapter 6:
Conclusion and Future work

6-1 Conclusion

In this thesis we design a VCO-based ADC with dynamic sampling for ECG acquisition in mobile healthcare applications. We use the ground controlled VCO which has good linearity performance and the low power consumption as our VCO stage. For the low power requirement, we use the asynchronous counter for the quantization whose power is 68% lower than the synchronous one. To avoid the sampling error of the asynchronous counter, the additional sampling flip-flops are applied with the determination circuit. To further reduce the ADC power, we apply the gated-input flip-flops. The transition of counter will not influence the flip-flops out of the EN window. 83% power reduction can achieve with this technique. To prevent the metastability of flip-flops, we turn off the VCO nearing the sampling CLK. By this way the data transition around sampling is eliminated and the metastability can be prevented.

Our design can be used in both single channel and multi-channel application. For the single channel application, the sampling frequency is 1k Hz. The ADC can achieve ENOB as 10.48 bits and the SNDR is 64.8356 dB. SFDR is 80.591 dB. The power of this application is 6.08uW which causes the large FOM as 4 pJ/conv.step.

The normalized FOM2 is 2.6314 fJ/conv.step which is still larger but quite close to the state-of-the-art.

For the multi-channel application, the sampling frequency can reach 10k Hz for 8 channels leads. The ENOB of 10k Hz sampling frequency is 9.6427 bits and SNDR can is 59.8088dB. SFDR is 62.2436 dB. The power consumption per channel is 0.62uW. The FOM of multi-channel application is 77.56 fJ/conv.step. The VCO-based ADC can gain from the small area. The normalized FOM2 is only 0.0479 fJ/conv.step.

To further reduce the power consumption of our ADC, we apply the dynamic sampling technique. For the ECG signal the information is concentrated in a part of signal segment, so we can control the ADC based on the signal variation. We propose 4 kinds of dynamic sampling techniques in the thesis and compare with the state-of-the-art. The PDS high resolution mode is the final technique we choose for our design. This method takes 1/4 cycles of sampling period to sense the variation of the signal through the slope calculation. For the low information part, the VCO turns off in rest of cycle and reduces ADC resolution. The power of VCO can be saved in this kind of situation. For the information contained part, the VCO oscillates in whole sampling period and the resolution of ADC maintains the same. The dynamic sampling technique can achieve 53% reduction on the power while keeping the distortion less than 5%.

6-2 Future work

In our design, the threshold for dynamic sampling is given by user. In the future, it may be determined by the auto adjusting method. Due to the dynamic technique for

our design can apply both with dynamic sampling value and without dynamic sampling value. We can do the calibration regularly and calculate the PRD to adjust the threshold. The calibration technique may cost additional power, but for the same patient in the similar statue, the characteristic of ECG signal may not have large variation. The calibration does not need be too often. The other is the PVT calibration for our ADC. In our thesis, we do not implement the PVT calibration. It can be done in future work. The PVT calibration can be implemented as the lookup table for digital output mapping. We can build the table based on the simulation result. For the calibration state, we apply two determined voltage inputs to the ADC and the slope of the output can be got. Based on the slope we can know which PVT is the chip face and the relation between with variation output and without variation output can be modeled as the polynomial equation. In the measurement mode, we can base on this equation to map the digital output to the proper value.

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