應用於無線個人區域網路之多組態 TB-LDPC-CC 解碼器晶片設計與實作

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摘　要

在無線通訊系統中，通道編碼模組往往扮演著重要的角色，不僅要達到高吞吐量的傳輸需求，也必須降低伴隨而來的功率消耗，以提供具有技術競爭力的解決方案。由於優越的錯誤更正能力與適合什行運算之架構，低密度奇偶校驗區塊碼(LDPC block codes，簡稱 LDPC-BCs)因而受到矚目，但是此解碼器在實作時會面臨高繞線複雜度之困難。此外，在設計技援多碼率之 LDPC-BCs 時也會面臨許多挑戰。低密度奇偶校驗迴旋碼(LDPC convolutional codes，簡稱 LDPC-CCs)於 1999 年提出，此碼可對任意長度的資料區塊做編解碼，且易於經由穿孔(puncturing)機制提供彈性的碼率。相較於傳統 LDPC-BCs，LDPC-CCs 具有較低的線複雜度並且依然具有相當優秀的錯誤更正能力。

然而，LDPC-CCs 需採用尾碼消除(tail-biting)或是終止數列(termination sequence)的技術方能應用在實際的系統應用中。為避免碼率的降低，我們採用尾碼消除的方式在我們的 LDPC-CCs 設計中。此外，我們也採用以記憶體為主的架構設計以降低功率消耗。解碼排程的最佳化同時提升錯誤更正能力及晶片之吞吐量。經由 UMC 90nm 的製程下線，我們所提出的 TB-LDPC-CC 解碼器晶片在 305 MHz 的操作頻率及 0.8V 之供給電壓下，其資料吞吐量可達到 1.83 Gb/s 在 4 次的重複解碼過程下，而功率的消耗為 275 mW。 總使用之核心面積為 2.27 mm^2 並且擁有 90.2%之晶片使用率。

Design and Implementation of Multi-Mode TB-LDPC-CC Decoder Chip for WPAN Applications

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ABSTRACT

In wireless communication system, channel coding modules play an important role. For providing a highly competitive solution, both high throughput transmission and low power consumption are required. Due to the capacity-approaching performance and inherent parallel architecture, LDPC block codes have attracted great interests in recent years. However, the problem of high routing complexity is a serious design challenge in VLSI implementations. Moreover, the complexity of designing multiple code-rates LDPC block codes is increased since dedicated parity-check matrices are needed to be jointly considered. Developed in 1999, LDPC convolutional codes are capable of handling arbitrary data frame length and possess flexible code-rates through puncturing. While performing the capacity-approaching performance, the routing complexity of the convolutional version is much lower than that of the LDPC block code's.

For real applications, however, tail-biting scheme or termination sequence should be employed. To avoid the code-rate loss, a LDPC convolutional code which can have the tail-bitten version is constructed in our work. Besides, a memory-based architecture is adopted to save the power consumption. Scheduling optimization which enhances both the performance and throughput is also provided in our design. Fabricated in UMC 90nm 1P9M CMOS process, the proposed TB-LDPC-CC decoder chip could achieve 1.83 Gb/s throughput under 305 MHz operating frequency with 0.8V supply voltage at 4 decoding iterations. The total core area is 2.27 mm^2 with 90.2% chip utilization.