國立交通大學

電子工程學系電子研究所碩士班

碩士論文

延續正反器之測試策略

Testing Strategies for Retention Flip-flops

學生：徐浩文

指導教授：趙家佐 博士

中華民國一０一年八月

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延續正反器之測試策略

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摘　要

本篇論文提及關於測試延續正反器的幾項爭議，並且提供相對應的解決方法。嶄新的延續正反器測試程序被提出用來檢測延續正反器因製成所致的缺陷。此外，本篇論文提出特殊的測試向量自動產生器用於產生出基於盡量引發連線上的訊號轉換的測試向量。最後，整體實驗是運行在 ISCAS 的標桿電路上，並且證實此測試向量自動產生器的優點以及能有效地測試延續正反器。

TESTING STRATEGIES FOR RETENTION FLIP-FLOPS

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Abstract

This thesis presents several issues about testing for retention flip-flops and proposes the corresponding solutions to those issues. A novel test procedure is proposed for detect many defects of retention flip-flops. Furthermore, a specialized ATPG framework is proposed to generate the test vectors for creating as many effective transitions on interconnects in the circuit as possible. The experimental results based on large ISCAS benchmark circuits demonstrate the efficiency of testing retention flip-flops and the advantages of using our proposed ATPG framework.

誌　　謝

首先我要謝謝所有來參加我口試的委員，非常感謝各位口試委員在百忙之中還可以撥空參加我的口試，並且願意聆聽我分享碩士兩年的研究成果以及給予我研究方面意見。

並且我要感謝我的指導老師 趙家佐教授，在我每次研究遇到困難時，總有一位老師可以並且願意和我討論在研究上遇到的瓶頸並教導我有關電子方面的專業知識。不僅對於我們的學業給予指導，更對於我們的英文能力十分注意，要求我每學期都要修習英文課。在日常生活方面，老師也會教我許多待人處事的態度，並要我們對於每一件事全力以赴。所以我要感謝老師在碩士這兩年對我用心地栽培，讓我在碩士階段的學習如此充實且豐富。

接下來我要謝謝每一位在實驗室陪伴我的學長、同學和學弟們。振安學長的知識經驗總能拓展我對於專業知識的視野。啟銘學長和耀德學長總是很親切地和我分享在工作上面的經驗。政偉學長在我遇到困難時，總是能給予我相當大的幫助。智為學長與偉勝學長讓我在編寫程式時更為輕鬆且有效率。穆思邦學長在演算法的部分常給予我意見，讓我對研究更可以得心應手。此外，我要感謝皓宇學長在課業上面給予我極大的幫助以及學業知識互相的討論。在研究上，除了老師之外，我也會詢問皓宇學長意見，學長也會給予我許多解決問題的方法，讓我可以順利解決問題。弘昕學長在我剛進入實驗室時，幫我採買及準備了許多實驗室所需要的軟硬體設備。淳仁學長讓我熟悉整個晶片的設計流程。擴安學長在我遇到各種的困難都願意伸出援手，解決我所面對的問題。陳世豪主管、玟翔和易民在我到創意工讀的時候給予我相當多的幫助，無論是在研究或是在工作環境上。欽遠則是會與我分享在旅遊的一些經驗。另外，召穎和昱安在平時空閒時間時，也會和我打打球。

再來我要感謝與我一起念研究所的朋友，宗霖、祐誠、昌澄、哲維、哲鎮、俊豪等同學讓我在平時可以煩悶的時候可以一起聊聊、吃吃飯等。另外，我也要特別感謝鵬先從大學以來，對於我寫程式能力的指導。在研究所時也幫我解決了許多問題。

最後我要感謝我的家人，雖然在碩士學習的過程中遇到了許多困難及挫折，但是因為有你們的支持與鼓勵，並且在我需要幫忙時都能給予協助。除此之外，也不曾給我任何壓力，讓我能順利完成碩士學位，最大的功勞就是你們。我願與你們共享這份喜悅!

徐浩文

國立交通大學

2012 年 8 月

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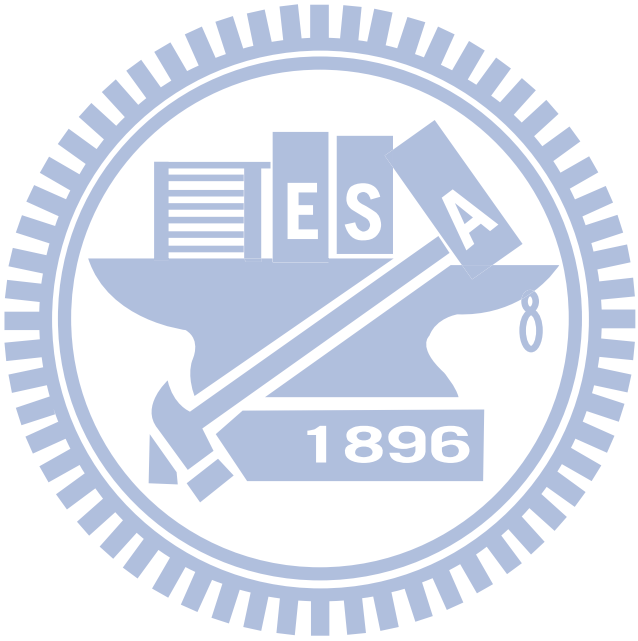

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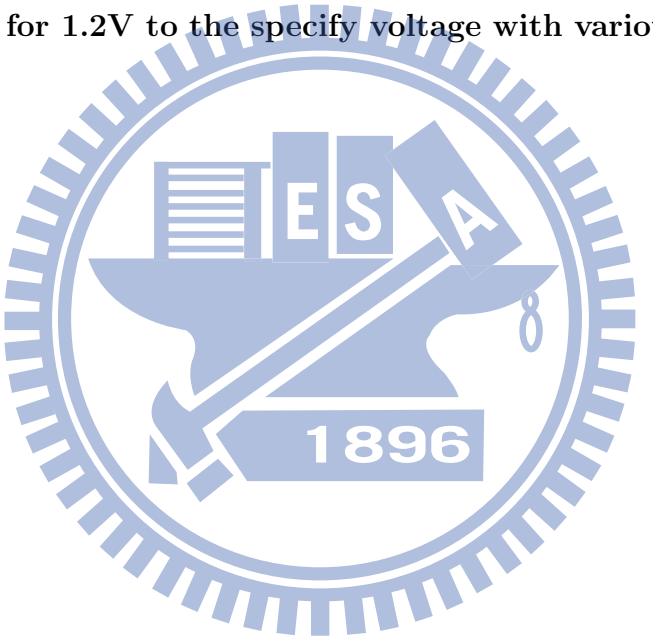

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Chapter 1

Introduction

In nowadays, the power consumption has been the major issue for producing IC design. Therefore, increasing the clock frequency is no longer the first priority for the criteria of IC [1]. Since the leakage power has increased and is not able to be ignored for the in the past few years due to scaling of process technologies [2][3], several devices have been developed for reducing the leakage power such as power switch, retention flip-flop, level shifter and isolation cell. Those devices are used for the technique called power-gating which is able to reduce much leakage current when that power domain does not activate. This technique is extremely useful in the portable design since limited power is provided for all these designs and some functional blocks in these designs are in the idle states most of the time.

During the past decade, few testing methodologies for testing power gating devices have been proposed. [4][5][6] introduced many ways for detecting the failures of power switches. [4] tried to generate a longest possible robust test as create as many effective transitions in the switch-centered region as possible. Moreover, [4] observed the delay of the longest path and determined whether the power switches were fail or not. [5] proposed the improved DFT structure for testing power switches and generated the test vector to test a given segmented power switches. [6] mentioned that the discharge time would be very long from the result of spice simulation. [6] stood for adding the DFT of power switches for balancing the charge

time and discharge time of power switches. [7] simulated many kinds of faults on level shifter such as resistive open, bridging and resistive short faults which caused to functional failure as well as the performance degradation in timing. Furthermore, [7] believed that faults on level shifter could be tested with conventional digital DFT since consideration of purely digital fault effects is sufficient.

However, there are only few researches focused on the retention flip-flop testing. In [8], the device related to low power devices testing were mentioned and some basic strategies for testing retention flip-flop suggested. [9] proposed some fault models of retention flip-flop; nevertheless, [9] did not mention about the fault models corresponded with fault defects in physical layer. Moreover, since the characteristic of the retention flip-flop, few issues would be discussed in this work but not in [9].

In this thesis, we would like to share the experience from testing the retention flip-flop and analyze the retention flip-flop structure. We provide a new test procedure for detecting the faults which traditional testing method is not able to cover. In addition, since we have noticed that it costs lots of time for the virtual-V_{DD} mesh discharges and it is necessary to decrease the voltage of virtual-V_{DD} mesh in testing retention flip-flop [8] [9], we also provide the a technique to reduce the time for the voltage of virtual-V_{DD} mesh to a lower voltage. Without our technique, the time for the voltage of virtual-V_{DD} mesh to the lower voltage may take hundreds of microseconds or even milliseconds depending on the gate count of the circuit.

The remaining of this thesis is organized as follow. Chapter 2 briefly introduces the structure of retention flip-flop. Chapter 3 lists two issues about testing the retention flip-flop which should be considered in testing the retention flip-flop and the corresponding new test procedure for solving problems. Due to few research

efforts focus on the second issue, more discussions will present in the following chapter. Chapter 4 shows the problem formulation for the issue. Chapter 5 presents the overall flow of proposed test pattern generation. Chapter 6 presents the details and algorithm of proposed test pattern generation. Chapter 7 shows the experimental result and the efficiency of proposed algorithm. The conclusion is given in Chapter 8.

Chapter 2

Retention Flip-flop

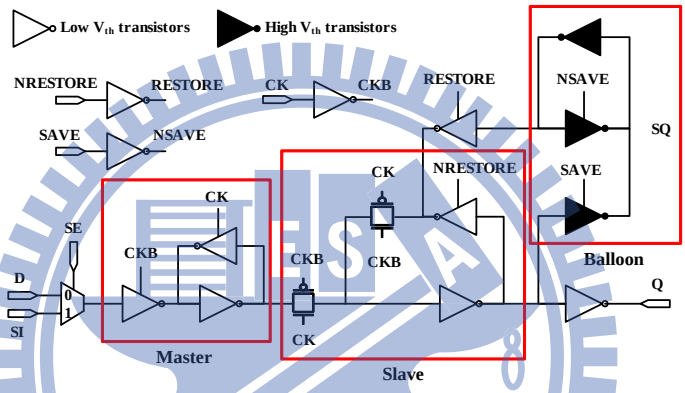


Figure 2.1: **The structure of retention flip-flop.**

Retention flip-flop is one of the most important devices in the low power design nowadays. Retention flip-flop works as the regular flip-flop when the power supply turns on (*awake-mode*). However, as the power supply turns off (*sleep-mode*), few critical states or data remain in the retention flip-flops for diminishing the latency of accessing memories. Moreover, with the increasing leakage power in the deep submicron designs, the reduction of the leakage power is desired even if the power supply turns off for reducing the dynamic power. The leakage current of transistor with high threshold voltage (*high* V_{th}) is smaller than transistor with low threshold voltage (*low* V_{th}). Due to the retention flip-flop is the low power

design that saves the leakage power when the power supply turns off, both high threshold voltage transistors and low threshold voltage transistors are used in the retention flip-flop design. Figure 2.1 shows the structure of the retention flip-flop, the white block consists the cells of low threshold voltage transistors and the black block consists the cells of high threshold voltage transistors. The balloon is used for retaining the data which is also called balloon and SQ is the saved value. As the power domain turns into the sleep mode, the power supply of the low threshold voltage cells turn off while the power supply of high threshold voltage cells still turn on for retaining the data in the balloon with low leakage current.

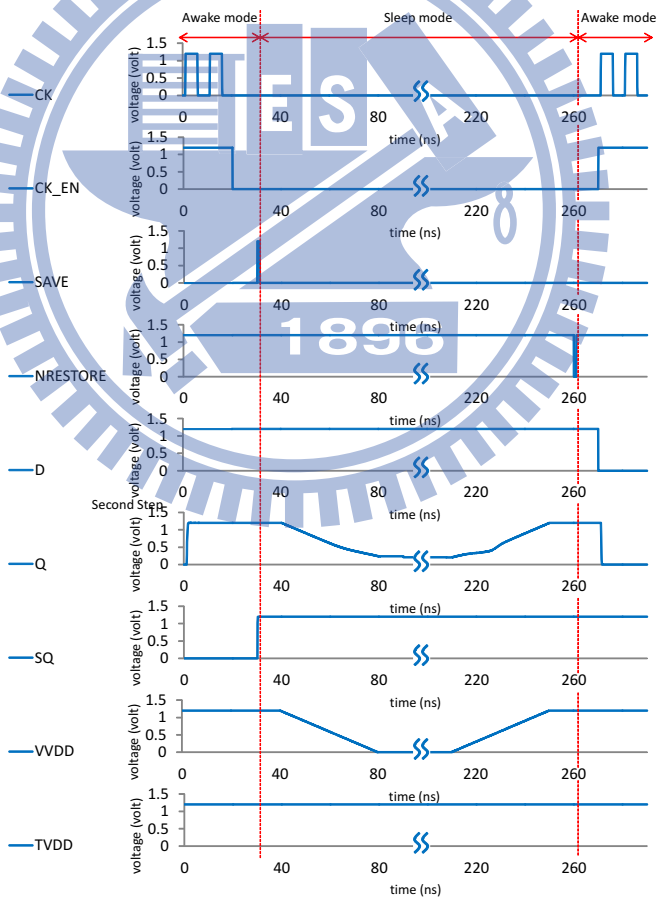
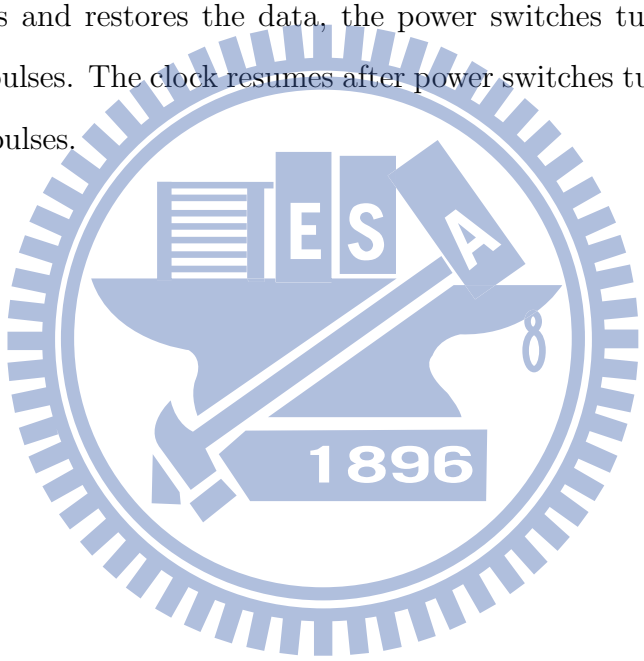


Figure 2.2: **The waveform of retention flip-flop in functional operation.**

Figure 2.2 shows the waveform of the retention flip-flop in functional operation. When the retention flip-flop is in the awake-mode, the function of the retention flip-flop is same as the regular flip-flop. For the retention flip-flop saves the data and sleeps, the clock is gated and the signal *SAVE* pulses for saving the data into balloon. The retention flip-flop turns into sleep mode when the power switches turn off. Since the power supply of the balloon(*true-*V_{DD}) remains on, the data retain even though the virtual-V_{DD} no longer charges by the true-V_{DD}. For the retention flip-flop awakes and restores the data, the power switches turn on and the signal *NRESTORE* pulses. The clock resumes after power switches turns on and the signal *NRESTORE* pulses.

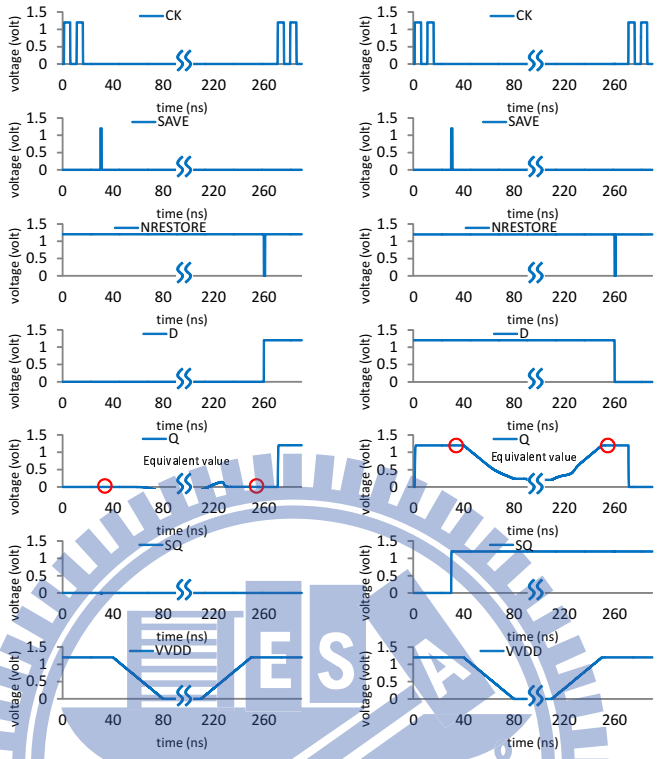


Chapter 3

Testing for Retention Flip-flop

3.1 Background of testing retention flip-flop

There are two states that the retention flip-flop should be tested. First, the retention flip-flop is tested as the regular retention flip-flop. A toggle sequence 001100110011 is used to cover most single stuck-at faults of retention flip-flop as well as verify the correctness of the shift operation. Second, since data will retain in the retention flip-flops and the retention flip-flops are able to be powered down and powered up in system application, it is necessary to make sure the data that restore after powering up match with the data that save before powering down. Therefore, the test procedure of retention flip-flop is likely to be the waveform of Figure 2.2. Test vectors shift in the retention flip-flop and the data are retained in the balloon while the signal *SAVE* pulses. After the power supply powers down, the data should retain in the balloon and the data restore after the power supply powers up. The data in balloon of the retention flip-flop is inspected and is expected to match the retained state before the retention flip-flop powers down. However, there are two major issues which make all these test procedures unrealistic.



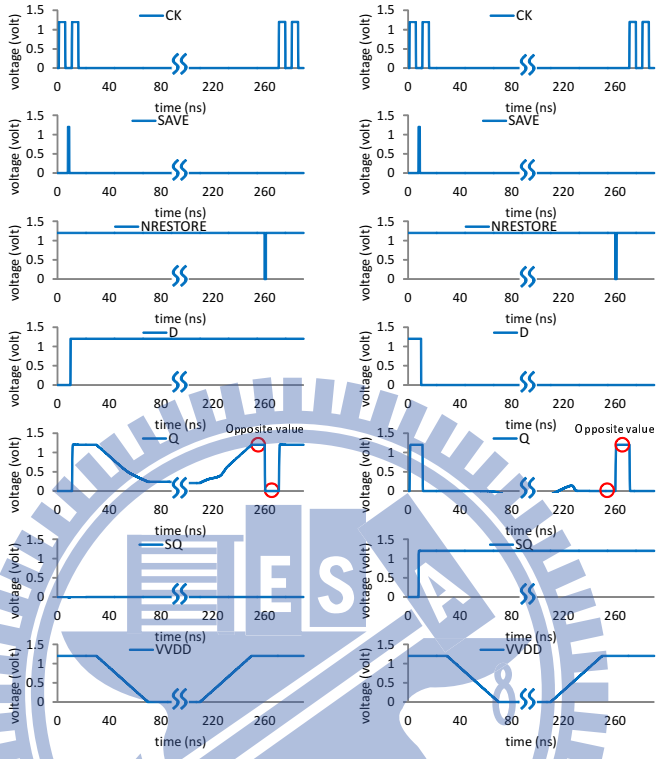
(a) $SQ = 0$, $Q = 0$ (b) $SQ = 1$, $Q = 1$

Figure 3.1: **The waveform of testing retention flip-flop.**

3.2 The characteristic for memorizing Q's value

As Figure 3.1 shows that after the retention flip-flop awakes, the retention flip-flop gets the previous Q's value (*before retention flip-flop sleeps*) easily. In Figure 3.1(a), the Q's value equals to 0 before the retention flip-flop sleeps, and the Q's value becomes 0 before the signal *NRESTORE* pulses. Furthermore, same result happens if Q's value equals to 1 as Figure 3.1(b) shows. The reason is that although the power switches have been turned off, few charges still remain in the retention flip-flop if the sleep time is not long enough. Thus, if the retention flip-flop restores the data after the retention flip-flop wakes up, it's hard to identify whether the pin *SAVE* and pin *NRSTORE* work correctly. Therefore, we propose a test

procedure for solving this problem.



(a) $SQ = 0$, $Q = 1$ (b) $SQ = 1$, $Q = 0$

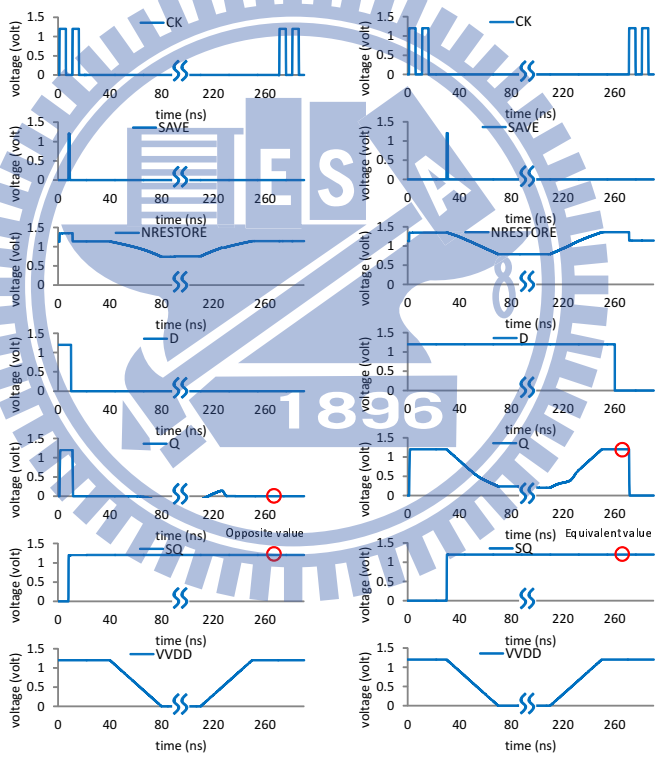
Figure 3.2: **The waveform of a novel procedure for testing retention flip-flop.**

- Balloon saves the value which is opposite to the value of pin Q before clock is gated.
  - Shift in 10101...101 to retention flip-flops and save the value to balloon.
  - Shift the value on the scan cells making the retention flip-flops' value become 01010...010.
  - Gate the clock and power down.
  - Power up and restore.

– Clock resume.

– Shift out retention flip-flops' value.

As Figure 3.2 shows that if the value which is saved in the balloon opposites to the Q's value before the retention flip-flop sleeps, the Q'value before restoring from balloon will be opposite to the value in balloon. In Figure 3.2(a), the value saved in the balloon is 0, and the Q's value before the signal *NRESTORE* pulses is 1. The situation in Figure 3.2(b) is opposite to Figure 3.2(a).



(a) Noval test procedure: $SQ = 1$, $Q = 0$

(b) Traditional test procedure: $SQ = 1$, $Q = 1$

Figure 3.3: **The waveform of fault inject to *NRESTORE* with 10G resistance.**

We inject faults to pin *NRESTORE* with 10G resistance. Figure 3.3 shows the fault injects to pin *NRESTORE*. Q's value and SQ's value are different at the

time when retention flip-flop does the restore operation in Figure 3.3(a). However, the retention flip-flop restores the value same as the SQ's value in Figure 3.3(b) which means the fault is not able to detect by the traditional test procedure.

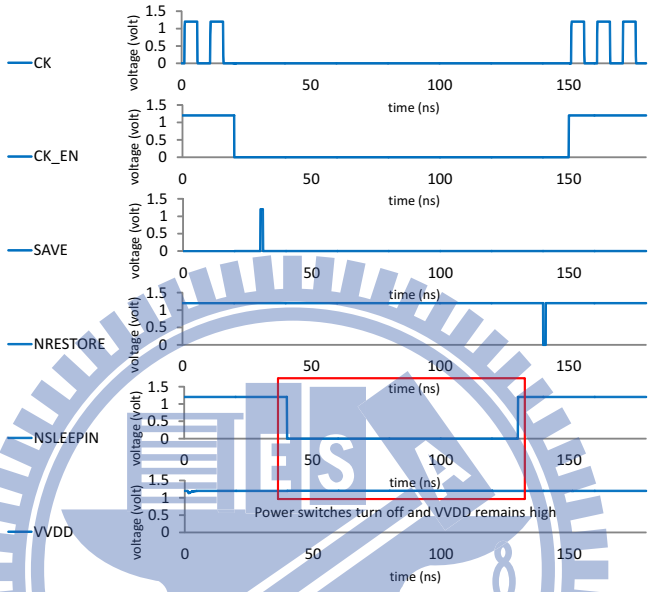
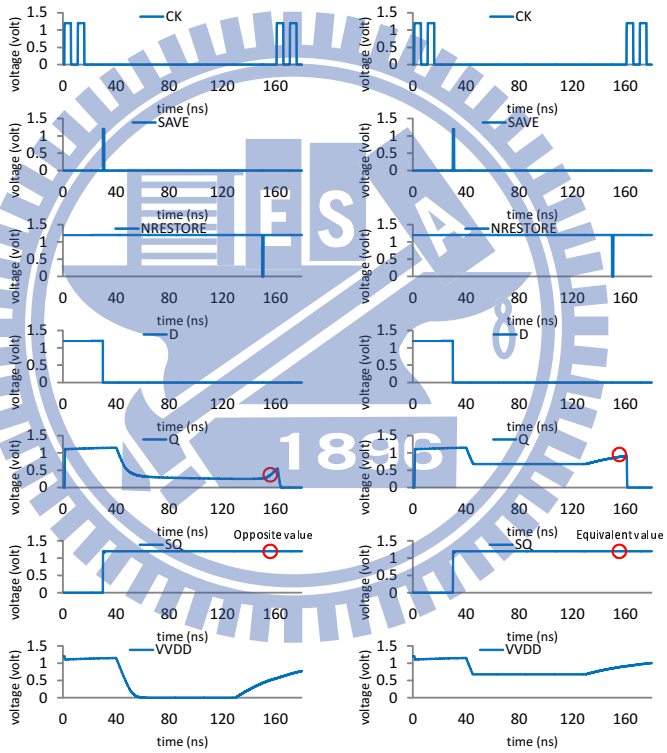


Figure 3.4: **The waveform of non-ideal retention flip-flop.**

3.3 Virtual-V_{DD} mesh discharges weakly

Even though the power switches have been turned off, the charges on the virtual-V_{DD} mesh will remain on the metal. We set an experiment for using one power switch and the loading of power switch is 1.5 pF. The power switch turns off when the pin *NSLEEPIN* becomes 0. In spite of the power switch turns off, the voltage of virtual-V_{DD} mesh is still high for a period time. Thus, the waveform of virtual-V_{DD} mesh will not be the same as Figure 3.1 shows but Figure 3.4. Most researches [8][9] have pointed out that the stage of power down the power supply is needed in the testing the retention flip-flop. Figure 3.5 shows that if there are defects (*e.g. power switches fail*) which causes the voltage of virtual-V_{DD} raise too slow,

the value restores from the balloon maybe incorrect. In Figure 3.5(a), the voltage of virtual-V_{DD} mesh equals to zero which means the virtual-V_{DD} mesh fully discharged while many charges remain on the virtual-V_{DD} mesh in Figure 3.5(b). From Figure 3.5(a), we are able to observe that Q's value and SQ's value are different if the defect occurs. However, Figure 3.5(b) shows that Q's value equals SQ's value which causes the fault is not able to detect. Thus, it is necessary to lower the voltage of virtual-V_{DD} mesh for testing retention flip-flop.



(a) VVDD = 0V as sleep mode (b) VVDD = 0.7V as sleep mode

Figure 3.5: **The waveform of defect causing virtual-V_{DD} mesh fails.**

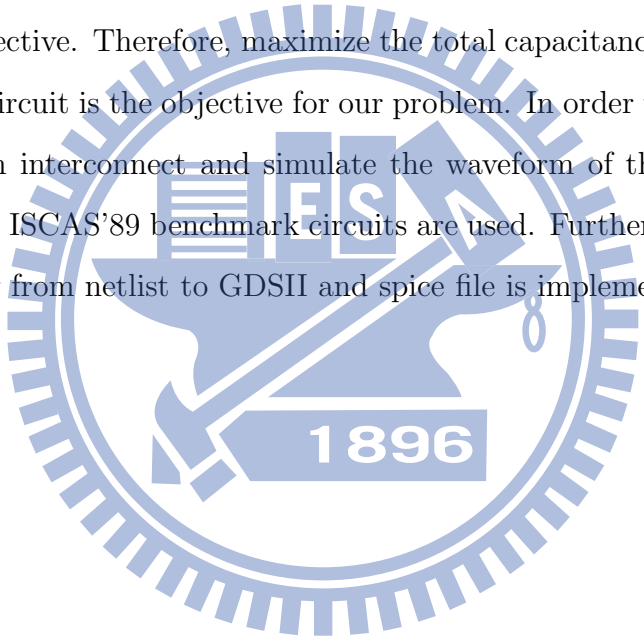
Since the charges remain on the virtual-V_{DD} mesh for a period of time even though the power switches turn off, we propose an approach for forcing the charges on the virtual-V_{DD} mesh to the ground without any additional device.

For making the charges discharge from virtual-V_{DD} mesh to ground quickly, the concept of charge sharing has been used. In CMOS technology, as the inputs of the standard cell transfer making the pMOS transistors turn on, the charges on the virtual-V_{DD} mesh share the charges to the output loading. Ideally, the amount of the charges distribute from virtual-V_{DD} mesh to output loading are equal. Thus, the voltage of virtual-V_{DD} mesh becomes $\frac{C_{mesh}}{C_{mesh}+C_{loading}} \times V_{previous}$. When the inputs transit and make the nMOS transistors turn on, the charges on the output loading discharge to the ground. Combine with the test procedure of the retention flip-flop, since the clock is gated as testing the retention flip-flops, only the inputs of the circuit are able to transit. Supposing the nets in the circuit toggle as the inputs of the circuit transit, the voltage of virtual-V_{DD} mesh will decrease to the transistor's threshold voltage.

Chapter 4

Problem formulation

According to the concept of charge sharing, if the lower voltage of the virtual-V_{DD} mesh is desired, maximize the capacitance of the standard cell's output port will be the objective. Therefore, maximize the total capacitance of the nets toggling for the whole circuit is the objective for our problem. In order to acquire the output loading of each interconnect and simulate the waveform of the voltage of virtual-V_{DD} mesh, the ISCAS'89 benchmark circuits are used. Furthermore, the flow of the circuit starting from netlist to GDSII and spice file is implemented.



Chapter 5

Overview of Test Pattern Generation and Waveform Simulation

Figure 5.1 shows the overall flow of the test pattern generation and waveform simulation, which requires the following inputs files:

- .v file: the Verilog file of the target MTCMOS design. This file is an input of the synthesis tool.
- .sdc file: the timing constraint file generates from Design Compiler[11]. This file is an input file of the APR tool.
- .bench file: the netlist file of the target MTCMOS design. This netlist format is only used by our own ATPG and can be directly transferred from the .v file.
- .cap file: the file of capacitance of each interconnect including pin capacitance and wire capacitance. This file generates from Encounter[12] and is an input file for our own ATPG for the objective above mentioned.
- .cnf file: the file of SAT solver constraint file. Since the pins Q of the flip-flops are not allowed transitions, constraints should be added to the SAT based ATPG.
- .pttn file: the pattern file generates from the SAT based ATPG. This file is an input file of spice for generating the waveform.

- .spf file: the file generates from RC extraction[13][14] of the circuit.
- .tr0: the waveform file shows the voltage of virtual-V_{DD} mesh for the patterns generated from our own ATPG.

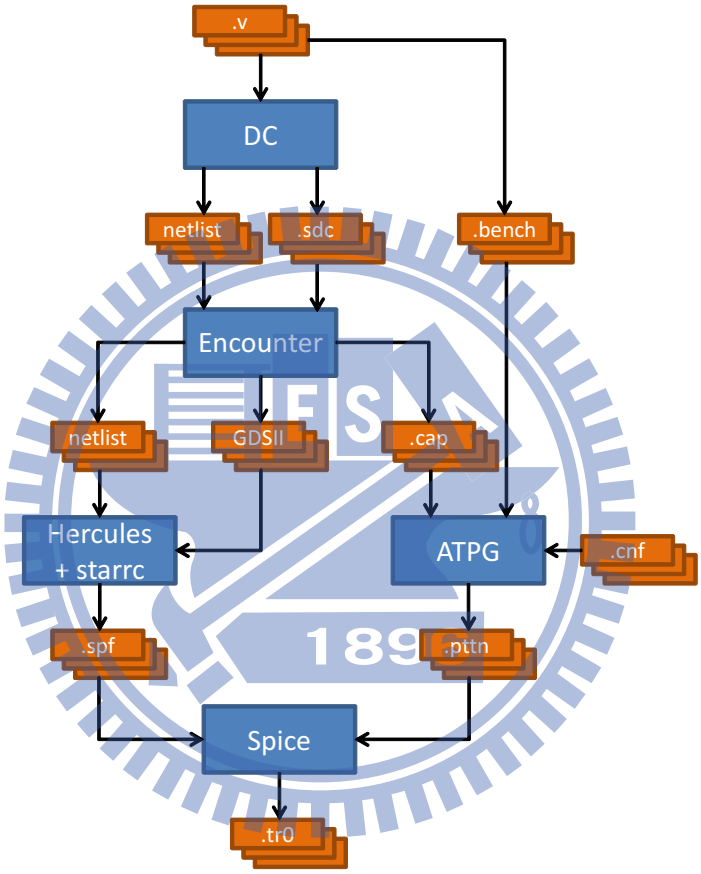


Figure 5.1: **Overall flow of the test pattern generation and waveform simulation.**

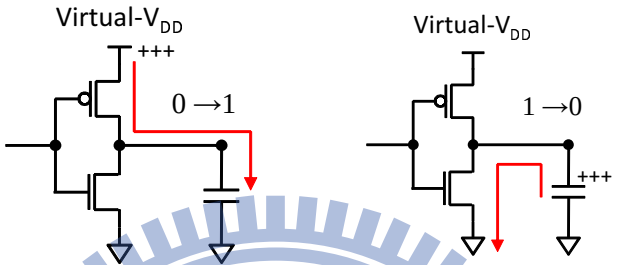
Chapter 6

Detail of Lower The Voltage of Virtual-V_{DD} Mesh With Test Patterns

6.1 Basic concept for proposed algorithm

Because the voltage of virtual-V_{DD} mesh does not decrease as expected, patterns generated from our own ATPG will be inserted after the clock gated and power switches turns off. The patterns are the two time-frames test vectors. The values of the patterns for primary inputs are able to be different in two time-frames while the values of the patterns for pseudo primary inputs have to be equal in two time-frames since the clock is gated when testing the retention flip-flops. The test vectors of first time-frame cause some values of interconnects to become 0 and some values of interconnects to become 1. The test vectors of second time-frame make the values on the interconnects to rise if the test vectors of the first time-frame makes the values to 0 and the test vectors of the second time-frame make the value to 1. The charges on virtual-V_{DD} mesh are forced to those interconnects with rising value as Figure 6.1(a) shows. Similarly, the test vectors of second time-frame make the values on the interconnects to fall if the test vectors of the first time-frame make the values to 1 and the test vectors of the second time-frame make the values to 0. The charges on those interconnects with falling value are forced to ground as Figure

6.1(b) shows. Repeat these two time-frames test vectors for a period of time; the values on interconnects will transit with the repeated test vectors. Therefore, the voltage of virtual-V_{DD} mesh drops each time as the two time-frames test vectors repeated.



(a) VVDD to loading (b) Loading to ground

Figure 6.1: **Examples of discharge path for virtual-V_{DD} mesh to ground.**

From our observation that if the voltage of virtual-V_{DD} mesh drops to about the threshold voltage, the transitions that are close to the primary inputs influence the virtual-V_{DD} mesh's voltage drop much effectively. The reason is that the values in the circuit become weaker accompany with the voltage drop of virtual-V_{DD} mesh. However, the voltage of the primary inputs are still integrated which makes the transitions of the primary inputs become the major sources for forcing the voltage drop of virtual-V_{DD} mesh. Therefore, there are two steps for our approach. Before the voltage of virtual-V_{DD} mesh drops to about the threshold voltage will be the first step, and after the voltage of virtual-V_{DD} mesh drops to about the threshold voltage will be the second step. Generate a pair of test vector for the first step with our own SAT based ATPG in our approach. Moreover, regenerate a pair of test vector which all the primary inputs are transited for the second step with our own SAT based ATPG. Base on the problem formulation, the test vectors generated from these two steps are objective to maximize the total capacitance of the nets toggled.

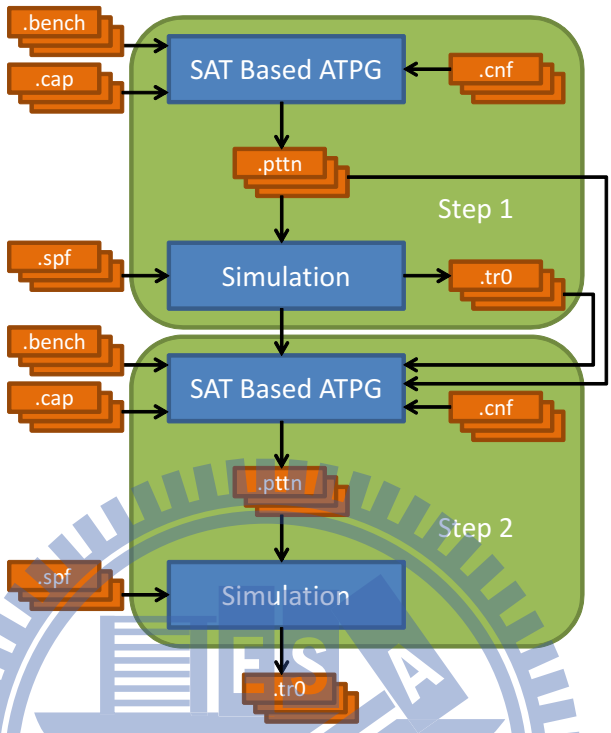


Figure 6.2: **Overview of SAT Based ATPG.**

6.2 Overview of SAT Based ATPG

Since the SAT Based ATPG separate to two steps, the SAT based ATPG will require two constraint files (.cnf). In the first step, the constraint file only needs to describe all the pseudo primary inputs are not able to transit. However, in the second step not only all the pseudo primary inputs must be same as the first time-frame vector's value, but all the primary inputs are set to transit. Therefore, the patterns generated in the first step as well as the constraint file are needed in the second step. Furthermore, in order to acquire the time for the voltage of virtual-V_{DD} mesh reaches about threshold voltage, the waveform file generated from the first step is also needed in the second step. Figure 6.2 shows the overview of SAT Based ATPG, which indicates the overall flow of generating pattern needed.

- From power supply voltage to about threshold voltage:
  - Step 1. Set the constraints for the SAT based solver (.cnf in step 1) to ensure that all the values of pseudo primary inputs will be solved to 0 or 1 in two time frames.
  - Step 2. Using our algorithm with SAT based solver to solve a pair of patterns which maximize the total loading capacitance with transitions.
  - Step 3. Fix all the values of pseudo primary inputs for the second iteration optimization.
- From about threshold voltage to very low voltage:
  - Step 4. Add the constraints all the values of primary inputs needs to transit in two time frames (.cnf in step 2).
  - Step 5. With the previous constraints, using our algorithm with SAT based solver again to acquire the optimized pattern.

6.3 Algorithm for maximizing the loading capacitance with transitions

Since we need to maximize the loading capacitance with transitions, we develop the greedy approach for our algorithm. For all interconnects in the circuit, sort all interconnects except the input ports in descending order. Pick the interconnect with the largest capacitance and try whether the value of this interconnect is able to be set to rising or falling with SAT solver or not. If yes, add the constraint of this interconnect to the SAT solver. If not, give up this interconnect and choose interconnect with the second large capacitance. Repeat the step mentions above until all interconnects except the input ports in the circuit are selected. Eventually,

with the solvable SAT constraints determined by the previous selection, many bits will be specified for the two time-frames test vector. For those bits of primary inputs are not specified in the first step will be set to 0 and in the second step will be set to transit (rising or falling). For those bits of pseudo primary inputs are not specified in both step will be set to 0. Figure 6.3 is the pseudo code for our algorithm.

```
01 begin
02   Add all Vs(Gates) to the Queue except primary inputs
03   Sort Vs' capacitance in the Queue in descending order
04   for(i=0; n <= Queue.size(); i++)
05     Add V with rising value in SAT constraint
06     Solve the SAT constraints with SAT solver
07     if(not SATed)
08       Pop V with rising value out of SAT constraints
09       Add V with falling value in SAT constraint
10       Solve the SAT constraints with SAT solver
11       if(not SATed)
12         Pop V with falling value out of SAT constraints
13 end
```

Figure 6.3: **The algorithm of maximizing the total loading capacitance with transitions.**

Table 6.1: **Result for proposed algorithm and exhaustive approach.**

Circuit	# of Selected Gate / # of Gate	Proposed Approach (pF)	Exhaustive Approach (pF)	Execution Time (s)
s1196	10(50%)/358	0.282588	0.306928	18
s5378	93(75%)/1043	0.201127	0.210979	7267
s9234	115(75%)/1379	0.233793	0.233793	50379
s13207	57(75%)/2142	0	0	27
s15850	27(75%)/2711	0.473389	0.473389	3592
s35932	16(50%)/8243	1.42019	1.5117	7640
s38417	126(75%)/8256	0.236587	0.236587	977
s38584	18(50%)/9542	2.09441	2.09441	10520

Table 6.1 shows that the different between our algorithm and the exhaustive

approach for the capacitance of interconnects which larger than 0.75×(maximum capacitance+capacitance) or 0.5×(maximum capacitance+capacitance).

The capacitance of interconnects solved by our algorithm is closer to the exhaustive approach. Moreover, the column of execution time shows the exhaustive approach is very inefficiently.

Chapter 7

Experimental Results on Benchmark Circuits

7.1 Experiment setup

The benchmark circuits used in our experiments are the ISCAS benchmark circuits. The 65nm MTCMOS library is used in our experiment and the voltage of true-V_{DD} is 1.2V. We set 0.5V for the voltage dividing two steps of generating patterns. Since we would like to observe the influence of the voltage of virtual-V_{DD} mesh with our test vectors, the waveform for the benchmark circuits-s13207 is provided in Figure 7.1. Furthermore, we also provide other two methods of generating test vectors. For the first method(*2 random values*), we assign rising or falling to the primary inputs randomly. However, since the clock is gated when testing the retention flip-flops, the pseudo primary inputs are only able to be set to value 0 or value 1 randomly. For the second method(*4 random values*), we assign value 0, value 1, rising or falling to the primary inputs and value 0 or value 1 to the pseudo primary inputs randomly. We random one thousand times based on these two approaches and select the best solution for the test vectors.

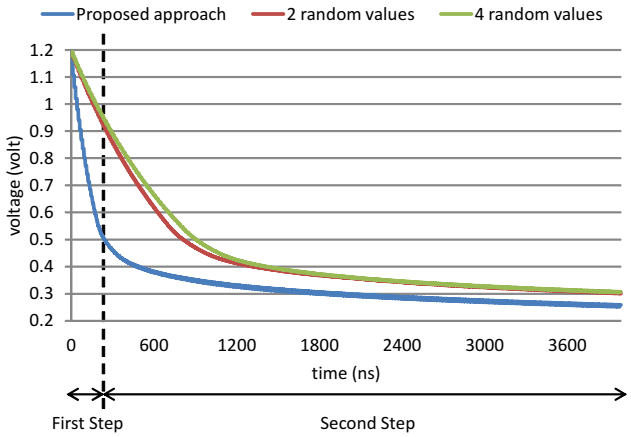


Figure 7.1: **Waveform of 1.2V to the specify voltage with various approaches.**

7.2 The efficiency of our approach compares to the randomly assignment approaches

Table 7.1 shows the result for the total capacitance of interconnects with transitions that our SAT Based ATPG is able to solve. Some benchmark circuits show that the total capacitance interconnects with transitions of the second step will be less than the one of first step. This is due to the values of pseudo primary inputs of the second step must same as the first step while all values of primary inputs need to transit in the second step. From the last column shows that more primary inputs transit will not relate to higher total capacitance of interconnects with transitions.

Table 7.2 shows the comparison between our approach and two kinds of random value assignment approach above mentioned. The symbol (2) in the Table 7.2 represents the approach of assign value 0 or value 1 to the primary inputs and pseudo primary inputs randomly. Besides, the symbol (4) in the Table 7.2 represents the approach of assign value 0, value 1, rising or falling to the primary inputs and value 0 or value 1 to the pseudo primary inputs randomly. The solutions solved

from our approach are much better than any randomly assignment method in most ISCAS benchmark.

7.3 Improvement for speeding up the voltage drop of virtual-V_{DD} mesh

Since as the voltage of virtual-V_{DD} mesh drops to threshold voltage, the pMOS no longer makes the charges on the virtual-V_{DD} mesh to interconnect, we present the result for the voltage of virtual-V_{DD} mesh drops to 0.3V. Figure 7.1 shows the waveform simulation for benchmark circuits of s5378, s9234, s13207 and s15850. Note that using HSPICE[10] to simulate a test vector on the complete circuit of s15850 takes around 72 hours. To run similar SPICE simulation on a larger ISCAS circuit (such as s35932, s38417, or s38584) may take weeks or even months. Thus, we have already generated the test vector and computed the effect on capacitance of interconnects with transitions for s35932, s38417, and s38584 but we do not have the SPICE result for these three circuits. As Figure 7.1 shows that the test vector generated by SAT based ATPG performs better than the test vector which primary inputs and pseudo primary inputs assign randomly. Note that since the simulation time for without any test vector's waveform is too long to reach the low voltage, this waveform is not shown in Figure 7.1. However, Table 7.3 shows the exact time for the voltage of the virtual-V_{DD} mesh from 1.2V to the specify voltage including all primary inputs fix to value 0 or value 1 (without test vector). From Table 7.3, it is obvious that maximizing the loading capacitance with transition indeed reduces the time that the voltage of virtual-V_{DD} mesh to the lower voltage. The proposed algorithm performs much better than the patterns generated with inputs and pseudo inputs randomly assign. From Figure 7.1 and Table 7.2, we are able to observe that more capacitance of interconnects with transitions, the voltage

of virtual-V_{DD} mesh drops to lower voltage much rapidly. Moreover, if all primary inputs fix to value 0 or value 1 (without test vector), the voltage of virtual-V_{DD} mesh drops extremely slow which leads the assumption of once the power switches turn off, the voltage of virtual-V_{DD} mesh becomes 0 wrong.

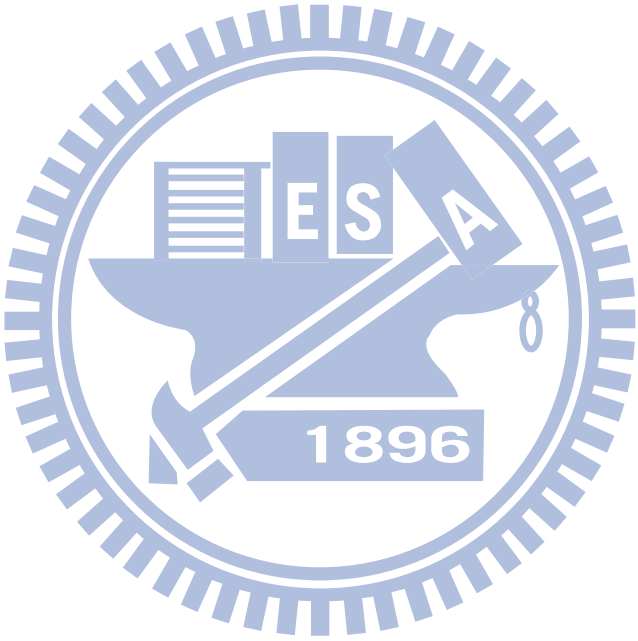


Table 7.1: **Experiment Result on ISCAS benchmark circuit with proposed algorithm.**

Circuit	# of Switches	# of FFs	# of Gates	Total Capacitance of Interconnects with Transition (pF) (1st step)	Total Capacitance of Interconnects with Transition (pF) (2nd step)	Execution Time (s) (1st step)	Execution Time (s) (2nd step)	Transition Bits / Total Bits (Primary Inputs)
s1196	2	18	385	0.842	0.816	1.24	1.38	0.571429
s5378	3	179	1043	0.783	0.567	9.6	12.1	0.828571
s9234	3	211	1379	1.067	0.777	18.77	22.04	0.777778
s13207	9	669	2142	0.466	0.466	23.86	82.54	0.903226
s15850	9	597	2711	2.175	2.175	72.83	123.32	0.714286
s35932	24	1728	8243	11.605	11.605	803.17	1271.61	0.457143
s38417	13	1636	8256	1.579	1.579	283.65	854.69	0.321429
s38584	24	1451	9542	15.245	15.245	904.19	1390.14	0.916667

Table 7.2: **Comparison with primary inputs assign randomly method.**

Circuit	Random Test Vector(2) (Total Capacitance) (pF)	Random Test Vector(4) (Total Capacitance) (pF)	Average capacitance(2) (pF)	Average capacitance(4) (pF)	Proposed method/ Random Test Vector(2)	Proposed method/ Random Test Vector(4)
s1196	0.745	0.634	0.573	0.431	1.13	1.328
s5378	0.387	0.392	0.26	0.21	2.023	1.997
s9234	0.496	0.409	0.349	0.231	2.151	2.609
s13207	0.14	0.103	0.1	0.05	3.329	4.524
s15850	1.13	1.154	0.92	0.468	1.925	1.885
s35932	11.446	11.402	10.736	5.582	1.014	1.018
s38417	1.109	1.009	0.713	0.355	1.424	1.565
s38584	13.76	13.675	13.433	6.83	1.108	1.115
Avg.	-	-	-	-	1.763	2.005

Table 7.3: **Time for 1.2V to the specify voltage with various approaches.**

s5378							
Voltage of Virtual-V_{DD} mesh (V)	Proposed Algorithm Test Vector (ns)	Random Test Vector(2) (ns)	Random Test Vector(4) (ns)	Without Test Vector (ns)	Random Test Vector(2)/ Proposed Algorithm	Random Test Vector(4)/ Proposed Algorithm	Without Test Vector/ Proposed Algorithm
0.7	42	62	71	31100	1.476	1.69	740.476
0.6	54	98	97	42000	1.815	1.796	777.778
0.5	77	125	125	53900	1.623	1.623	700
0.4	132	202	242	68300	1.53	1.833	517.424
0.3	355	538	803	86700	1.515	2.262	244.225
Avg.	-	-	-	-	1.592	1.841	595.981
s9234							
Voltage of Virtual-V_{DD} mesh (V)	Proposed Algorithm Test Vector (ns)	Random Test Vector(2) (ns)	Random Test Vector(4) (ns)	Without Test Vector (ns)	Random Test Vector(2)/ Proposed Algorithm	Random Test Vector(4)/ Proposed Algorithm	Without Test Vector/ Proposed Algorithm
0.7	40	71	82	34400	1.775	2.05	860
0.6	48	82	110	45600	1.708	2.292	950
0.5	64	92	150	59600	1.438	2.344	931.25
0.4	119	200	310	76200	1.681	2.605	640.336
0.3	550	780	1250	96100	1.418	2.273	174.727
Avg.	-	-	-	-	1.604	2.313	711.263
s13207							
Voltage of Virtual-V_{DD} mesh (V)	Proposed Algorithm Test Vector (ns)	Random Test Vector(2) (ns)	Random Test Vector(4) (ns)	Without Test Vector (ns)	Random Test Vector(2)/ Proposed Algorithm	Random Test Vector(4)/ Proposed Algorithm	Without Test Vector/ Proposed Algorithm
0.7	140	494	660	38400	3.529	4.714	274.286
0.6	182	639	850	51100	3.511	4.67	280.769
0.5	251	820	1100	66000	3.267	4.382	262.948
0.4	481	1320	1740	84100	2.744	3.617	174.844
0.3	1780	4000	4220	106000	2.247	2.371	59.551
Avg.	-	-	-	-	3.06	3.951	210.48
s15850							
Voltage of Virtual-V_{DD} mesh (V)	Proposed Algorithm Test Vector (ns)	Random Test Vector(2) (ns)	Random Test Vector(4) (ns)	Without Test Vector (ns)	Random Test Vector(2)/ Proposed Algorithm	Random Test Vector(4)/ Proposed Algorithm	Without Test Vector/ Proposed Algorithm
0.7	41	71	64	35600	1.732	1.561	868.293
0.6	51	94	88	47500	1.843	1.725	931.373
0.5	74	129	120	61600	1.743	1.622	832.432
0.4	293	433	379	78500	1.478	1.294	267.918
0.3	1690	2600	2330	987000	1.538	1.379	58.402
Avg.	-	-	-	-	1.667	1.516	591.684

Chapter 8

Conclusion

In this thesis, we point out two issues in testing retention flip-flop. First, since the characteristic of retention flip-flop, the value saved in the balloon must opposites to the value of pin Q before the retention flip-flop sleeps in order to cover the faults of the retention flip-flop. Second, we have proposed a SAT based ATPG for forcing the voltage of virtual-V_{DD} mesh to reach the low voltage without redundant device. The experimental results based on a current MTCMOS technology demonstrated testing for retention flip-flops are able to be more robust and efficient with proposed ATPG framework.

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