


國立交通大學

電子工程學系 電子研究所

碩士論文

考慮可繞線度之數位微流體生物晶片叢集演算法



ACER: An Agglomerative Clustering Based Electrode
Addressing and Routing Algorithm for
Pin-Constrained EWOD Chips

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A Thesis

Submitted to Department of Electronics Engineering and
Institute of Electronics

College of Electrical and Computer Engineering
National Chiao Tung University

In partial Fulfillment of the Requirements

for the Degree of

Master of Science

In

Electronics Engineering

October 2012

Hsinchu, Taiwan, Republic of China

中華民國一〇一年十月

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摘 要

在此篇論文中，我們主要針對微流體生物晶片做一個探討。在晶片設計越來越複雜的狀況下，如何有效的在微流體生物晶片上減少針腳的使用量，以減少製作的成本已經變成一個重要的議題。在此篇論文中，我們提出了一個考慮可繞線度的叢集演算法，在叢集的過程中，我們會針對每個針腳做有效的估計，決定出一組最適合的繞線順序。並且我們在繞線過程中，會考慮到每一條路徑的擁擠程度。試著將比較擁擠的地方給予一些空間，使的後面的繞線路徑更為順暢。最後我們提出了一個線性規畫的逃脫繞線演算法，我們的演算法同時可以實現在有障礙物的晶片上。在我們的演算法中平均可以減少 11% 針腳的使用量，同時繞線長度也有 151% 的降幅。

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ABSTRACT

With the increasing design complexities, the design of pin-constrained electrowetting-on-dielectric (EWOD) biochips is of practical importance for the emerging marketplace. However, as the system complexity increases, the number of control pads also rapidly increases that may necessitate multiple PCB layers, which potentially raise the price of fabrication cost. To tackle this problem, we present **ACER**, an agglomerative clustering-based electrode addressing and routing algorithm for pin-constrained EWOD chip that solves both pin merging and routing effectively. An agglomerative clustering technique is applied to determine merging priority of electrical pins. Furthermore, in consideration of routability, we propose an effective estimation method to incorporate routability to our objective during clustering. At routing stage, we formulate the consequent multi-source multi-sink escape routing problem using a set of integer linear constraints. Our algorithm can handle designs with and without obstacles. Compared to work [8] without considering presence of obstacles, *ACER* can further reduce activation sequences by 11% with 151% reduction in routed wirelength within comparable execution time. In comparison with obstacle aware algorithm proposed in [3], our algorithm can achieve equivalent reduction using 25% less routed wirelength.

誌 謝

兩年的碩士班生活即將結束，在這兩年裡學習到很多東西。無論是課業方面，或是人際關係，或是專業知識。而如今能夠順利畢業，衷心的感謝很多人的協助跟幫忙。

首先感謝陳宏明教授，在我還在無助的尋找研究方向時候，給予我一條明確的目標，在與教授討論的時候，教授也不時給予鼓勵跟支持。

再來我要感謝實驗室VDA的大家。謝謝博班的學長姐，時穎、Benbean、Jerry、篤雄、俊凱和敬雨。感謝學長姐的熱心指導，從我們剛進來對於這個領域不是很了解的時候，學長姐仔細的教導跟訓練，讓我們慢慢熟悉EDA這塊領域，也提供給我們很多資訊。其中我要非常感謝帶我做研究的時穎，你的細心指導不但在研究上在生活上也給予我大的幫助。再來是感謝同屆的好朋友們，冠廷、仁國、建志，謝謝你們陪我一起研究討論，打球，聊天，讓我們一起有繼續做研究的動力。最後是學弟妹們，川嘉、新鈞、天龍、以恩和孟伶，謝謝你們每天在實驗室的歡笑讓我可以每天開心的做研究。

我要感謝我的爸爸，媽媽一直不斷的鼓勵跟支持，沒有你們的支持也沒有今天的我。謝謝怡文陪伴著我度過了我這一段重要的人生。

謝謝一路上幫助過我的人，謝謝大家。

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Chapter 1

Introduction

Electrowetting-on-dielectric (EWOD) becomes a popular actuator for droplet-based digital microfluidic (DMF) applications. EWOD chips offer flexibility and efficiency to manipulate discrete droplets to realize several practical bio-system applications [6][7][9][11]. The structure of EWOD chips is a two dimensional electrode array illustrated in Fig. 1.1(a). To realize a given function, droplets are driven across electrodes to combine with other droplets. The movement of fluidic droplets are actuated by the electrical pins underneath the electrodes. For a specific function, each electrode pin is fed with a specific activation sequence that determines voltage of electrical pin in each time frame. The activation sequences are fed to a control pad located at chip's boundary.

Implementing an EWOD chip consists of two parts: electrode addressing and routing of electrical pins. Electrode addressing assigns an electrode to a designated control pad. Routing of electrical pins is achieved by connecting the electrodes through the underlying substrate to the boundary control pads. In this context, routing refers wire routing of EWOD chip instead of droplet routing in [11].

In terms of electrode addressing, the work done in [5] proposed the direct-addressing method which assigns one electrode to only one control pad. However, modern designs generally has input activation sequences up to thousands and direct-

addressing method is limited to handle large designs. The limited number of signal ports in the micro-controller is infeasible to activate large number of control pads. In addition, as complexity of design increases, additional routing layers are required to ensure a routable design.

In this regard, to reduce complexity and fabrication cost of a given design. The work done in [12] proposed the broadcast-addressing method to reduce number of activation sequences. Several electrical pins with compatible or non-conflicting activation sequences are assigned to one control pad. Fig. 1.1 compares routing result between direct-addressing method and broadcast-addressing method. In Fig. 1.1, a 16 electrical pin design requires 16 control pads using direct-addressing method, but it only requires 4 control pads using broadcast-addressing method.

Despite the potential benefits gained from broadcast addressing method, the benefit is hindered by the routability of the electrical pins. Different broadcast-addressing results lead to different wiring topology. If routing fails to achieve the desired outcome, either additional routing layer is required or electrodes need to be reassigned. The more pragmatic approach is to adjust the electrode addressing since additional routing layer significantly increases the fabrication cost [2]. Viewed in this light, routability emerges as even more complicated issue in broadcast-addressing.

1.1 Previous Works

Here we address our attention on electrode addressing and wire routing of EWOD chips. In [12], a clique partitioned method is proposed to merge electrical pins using minimal number of clusters. However, a minimum clique partition is an NP-hard problem and greedily merging electrical pins only postpone the challenge to subsequent routing stage.

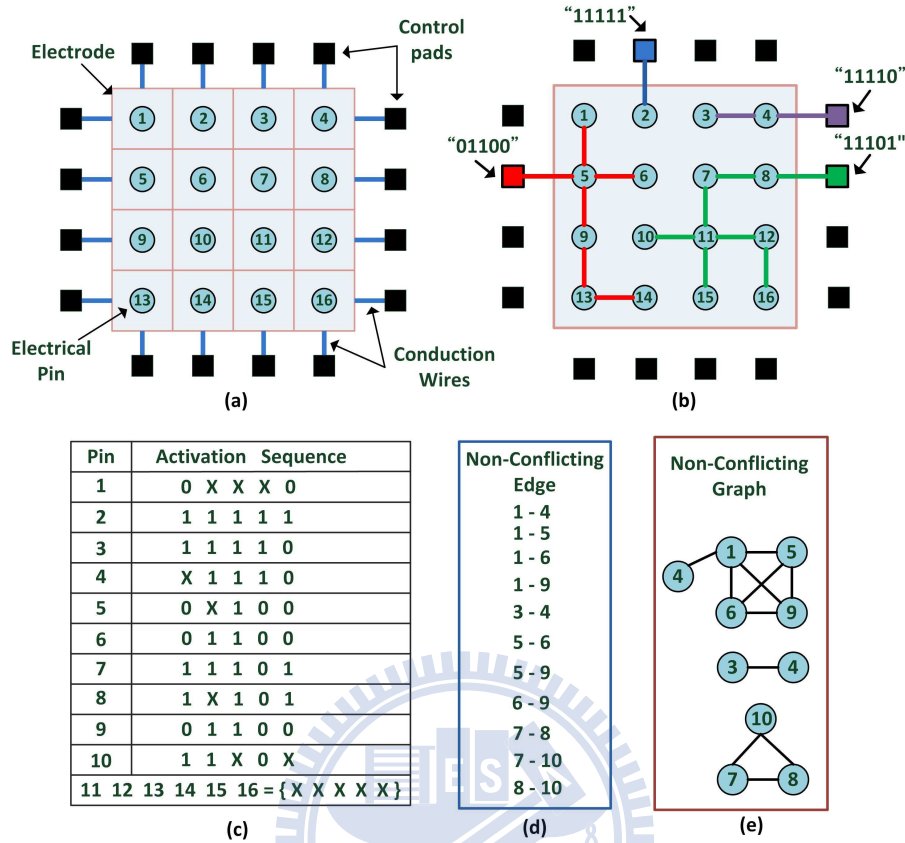


Figure 1.1: Schematic view and problem construction for EWOD chips. (a) Schematic view for EWOD Chips. (b) Broadcast-Addressing method for EWOD Chips. (c) Input activation sequences. (d) Construct non-conflicting edges. (e) Construct non-conflicting graph.

Huang et. al. [8] proposed a network flow algorithm to search for an optimal initial solution. The initial solution is obtained by determining minimal number of global tracks that covers all electrical pins. The merging of electrical pins is achieved by iteratively selecting hard-to-merge electrical pins. The work done in [3] further considers presence of obstacles during electrode addressing.

However, in [8], the minimal track solution is not unique as any min-cut solution will suffice the original problem formulation. Electrical pins on the same track may not even be compatible, finding minimal tracks in this regard is rather futile. In addition, to avoid routing failure, subsequent electrical pin merging drastically change the wire topology by locally adjusting wires. The benefit gained by finding

minimal track solution is unclear as it requires large portions of heuristic refinement in local wire adjustment.

1.2 Our Contributions

To reduce total number of required activation sequences while considering routability, techniques used in agglomerative clustering technique are applied to merge electrical pins. To avoid merging electrical pins that is potentially hard to route, routability is modeled into objective cost during clustering. To increase routing success rate, a congestion estimation technique is applied to update grid cost. Our algorithm is capable of handling designs with and without obstacles and requires no further local wire adjustment during routing stage. All in all, our contributions can be summarized as follows:

- We propose a routability driven clustering algorithm that can effectively incorporate routability into objective during clustering.
- Empirical results show that our algorithm has optimal tradeoff between routed wirelength and reduction in number of activation sequences.
- Given a set of connected electrical pins, the multi-source multi-sink escape routing problem can be optimally solved using ILP formulation. Experimental result shows that such approach can reduce required activation sequences by additional 15% compared to [8]. To accelerate run time, we integrate a maze router which can reduce required activation sequences by 11% with 38x speed up.

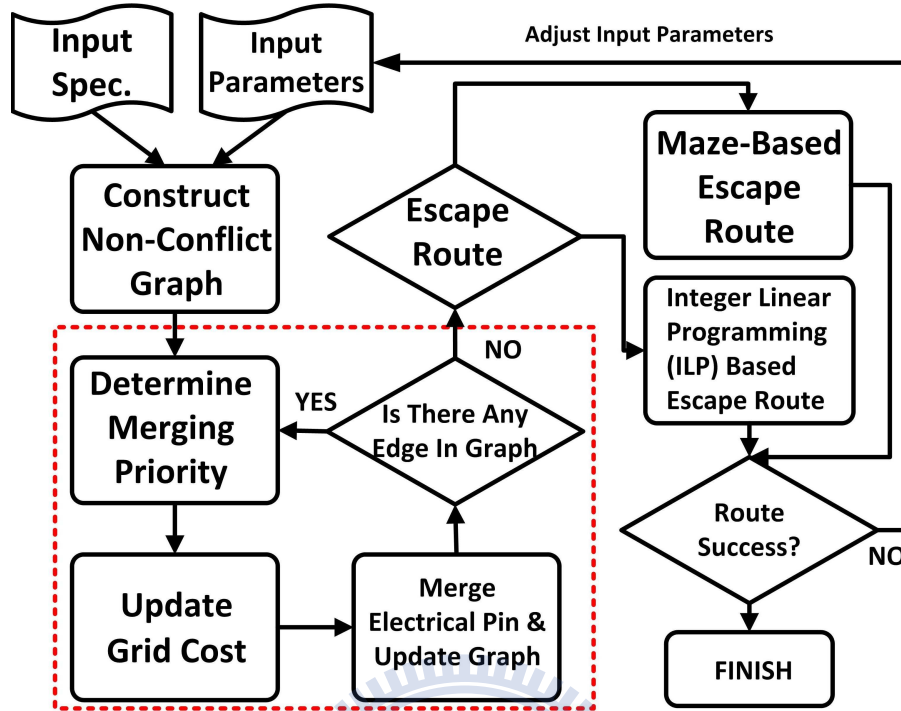


Figure 1.2: Flow chart of our algorithm.

1.3 Overview of our Algorithm

Fig. 1.2 shows a flow chart of our proposed methodology. First the given input activation sequences are converted into non-conflict edges as illustrated in Fig. 1.1(c)(d). Then a non-conflicting graph can be constructed which is shown in Fig. 1.1(e). The merging priority of electrical pins is determined through clustering of electrical pins. The non-conflicting graph is constantly updated to reflect the change. Second, routing of electrical pins is achieved by formulating the routing problem as a multi-source multi-sink escape routing problem using a set of ILP constraints.

The remaining parts of this thesis are organized as follows. Section II introduces some of the preliminary knowledge and formulate the problem. Section III describes how to determine merging priority using agglomerative clustering. Section IV describes how to formulate the escape routing problem using a set of ILP constraints. Section V presents the experimental result and Section VI concludes the thesis.

Chapter 2

Preliminaries and Problem Formulation

In this section, we give a general overview for the pin-constrained electrode addressing for EWOD chip problem, then we formally formulate the problem along with its objective and constraints.

2.1 Preliminaries

In a digital microfluidic biochip (DMFB) design, the function is defined by the activation sequence for each electrical pin. The activation sequence controls the voltage value of an electrical pin at each time step. Each activation sequence is fed to an electrical pad. The sequence is a combination of three values: Value “1” represents logic high value, symbol “0” represents logic low value, and symbol “X” represents don’t care in which an arbitrary value can be assigned without impact to original function. Two sequences are said to be *compatible* if both sequences can be merged into one sequence without affecting the original function. In Fig. 1.1(c), activation sequences to electrical pin 7,8, and 10 are compatible and can be triggered by a single activation sequence: “11101”. Each electrical pin is controlled by a corresponding activation sequence. Electrical pins can be triggered by a single activation sequence if their corresponding activation sequences are compatible. In

this thesis, activation sequence for each electrical pin is given.

2.2 Problem Formulation

Our objective is to minimize total number of activation sequences by merging compatible activation sequences while minimizing total routed wirelength. The direction of routed wire is limited to orthogonal in order to comply with industrial standard in IC or PCB design flow. The problem of electrical pin merging and routing for EWOD chips is defined as follows.

Problem 1: The Pin-Constrained Broadcast-Addressing Merging and Routing Problem for EWOD Chips

Given n activation sequences for n electrical pins, the objective is to minimize total number of activation sequences by triggering multiple compatible electrical pins with one activation sequence using minimal routing wirelength.

Chapter 3

Routability Driven Clustering for Electrical Pins

In this section, a graph representation of electrical pins is presented to model the merging problem. The merging problem is solved by applying agglomerative clustering. In consideration of routability, we propose an estimation method that can reflect routability in the objective during clustering.

3.1 Graph Representation of the Electrical Pin Merging Problem

Before the detail of the algorithm is introduced, we define several terms as follows.

Definition 1: A node (cluster) is defined as a set of electrical pins that is triggered by a single activation sequence.

Definition 2: Two nodes are said to be compatible if all of the electrical pins in two nodes can be triggered by a single activation sequence.

Definition 3: A bounding box of an edge is defined as the minimum spanning rectangle that covers all electrical pins in two nodes.

Definition 4: An overlapping bounding box between two edges i and j , OBB_{ij} is defined as the cross section area between two bounding boxes.

Initially, a single node represents only one electrical pin. The data structure of a node consists of two child nodes and a parent node. When two nodes are merged, a new parent node is created to replace the two merged nodes on the graph and store the merged nodes as child nodes. When entire merging process completes, the merging hierarchy of the electrical pins can be represented by a set of binary trees. The total number of binary trees is the total number of required activation sequences.

An edge exists between two nodes if and only if two nodes can be triggered by compatible activation sequences. An n -degree clique means that the corresponding n nodes are compatible and can be triggered by a single activation sequence. Fig. 3.1 is a representation of non-conflict graph to physical EWOD chips.

A naive approach to solve the merging problem is to iteratively find the maximal clique in non-conflict graph. However, as mentioned previously, such approach has NP-hard complexity and ignores the physical information of electrical pins. To consider the physical information of each electrical pin and maximizing routability during electrical pin merge, the concept of agglomerative clustering is applied. In each step of clustering, edge with the minimum cost is selected and merges the two nodes. Graph is constantly updated by creating and removing edges and nodes.

Agglomerative clustering can be used to minimize a given objective cost. The benefit is two-fold. First, it greedily minimizes the objective cost by selecting edge

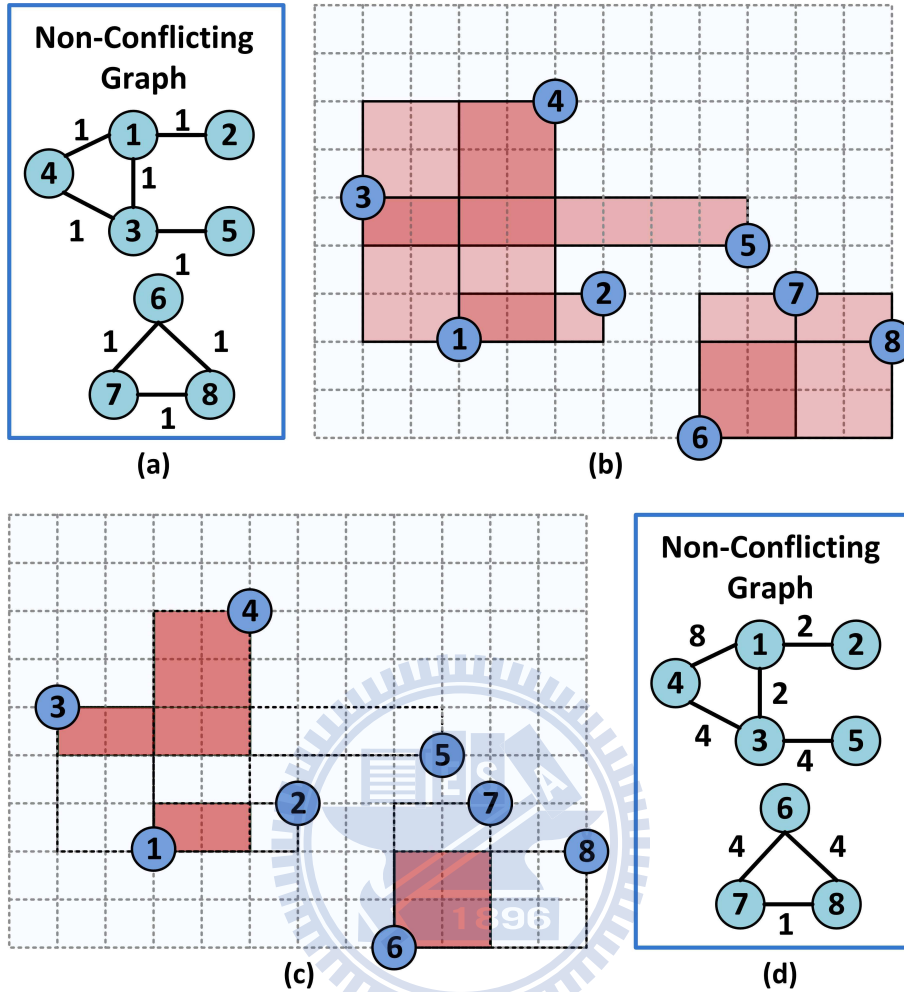


Figure 3.1: Graph representation of the EWOD chip. (a) Non-conflicting graph. (b) Bounding box for all edges. (c) Overlapping bounding boxes. (d) Using area of overlapping bounding boxes as edge cost.

with the minimum cost, the challenge is to model routability into objective cost. Second, each cluster is a collection of merged clusters, solution can always roll back by de-clustering which offers flexibility.

3.2 Agglomerative Clustering of Electrical Pins

The bounding box of an edge indicates potential routing paths to merge two nodes. Overlapping bounding box between two bounding boxes indicates potential congested region and should be used discretely. The overlapping bounding boxes can

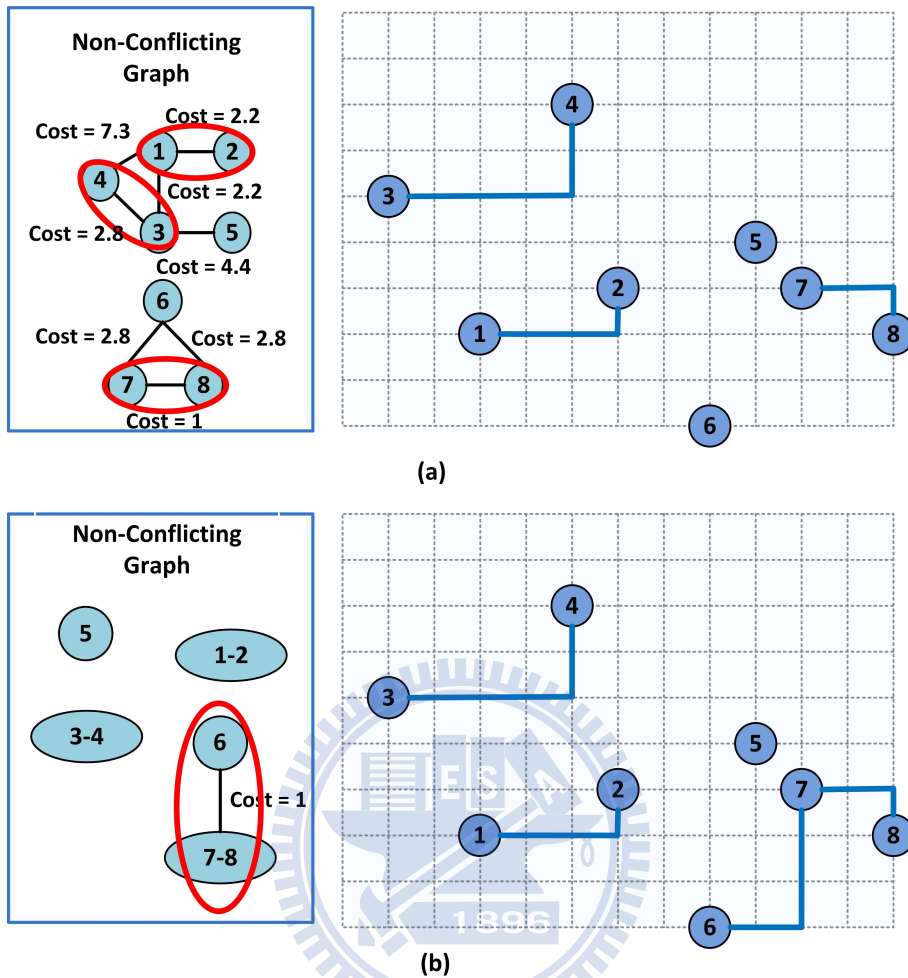


Figure 3.2: Agglomerative clustering of electrical pins.

be identified using line sweep method[4]. The general concept of line sweep method is to sort the x_{min} and x_{max} coordinates of bounding boxes in non-decreasing order. A virtual line sweeps from the minimum x-coordinate to check whether if there are overlaps in y-coordinate. When sweeping line reaches to the end of sorted x-coordinate list, all of the overlapping bounding boxes can be identified.

Fig. 3.2 is an illustration of agglomerative clustering. Edge with least cost in non-conflicting graph is selected and the two connected nodes are merged. Algorithm 1 describes the procedure when two nodes are merged/clustered. Algorithm 1 consists of three operations to update the graph: (1). A new parent node is created to replace the two merged nodes. (2). New edges are created connecting to new parent node.

Algorithm 1 Node Clustering

- 1: Create a new node n_k in Graph G
- 2: $\text{Parent}(n_i) = n_k$
- 3: $\text{Parent}(n_j) = n_k$
- 4: $\text{Left-Child}(n_k) = n_i$
- 5: $\text{Right-Child}(n_k) = n_j$
- 6: **for** all node n_m connected to n_i **do**
- 7: **for** all node n_n connected to node n_j **do**
- 8: **if** $n_m == n_n$ **then**
- 9: Create a new edge $e_{k,m}$ between n_k and n_m
- 10: **end if**
- 11: **end for**
- 12: **end for**
- 13: Set all edges connected to n_i invalid
- 14: Set all edges connected to n_j invalid
- 15: Set node n_i invalid
- 16: Set node n_j invalid

Algorithm 2 Node De-Clustering

- 1: Set n_k invalid
- 2: Set all edges connected to n_k invalid
- 3: $n_j = \text{Left-Child}(n_k)$
- 4: $n_i = \text{Right-Child}(n_k)$
- 5: Set node n_i valid
- 6: Set node n_j valid
- 7: Set all edges connected to n_i valid
- 8: Set all edges connected to n_j valid

(3). Merged nodes and all of the edges connected edges are invalidated from the graph. A new edge $e_{k,m}$ to nodes n_k and n_m is created if and only if both child nodes of n_k have an edge connecting to n_m . When new nodes and new edges are created, merged nodes and all of the edges they connect to are set to invalid in the non-conflicting graph.

Algorithm 2 describes the procedure to de-cluster a given node to two separate child nodes. Parent node n_k and all of its connected edges are invalidated from the graph and its connected child nodes are restored to the graph.

3.2.1 Determining Edge Cost

In this subsection, we explore several methods to determine edge cost and its effectiveness on routability. In [3], electrical pins within shortest Manhattan distance have higher merging priority. However, shorter distance does not accurately reflect routability. In Fig. 3.3, pins in Net B has shortest Manhattan distance but merging Net B first will make Net A unroutable.

To estimate potential routing resources that may be used by other nets, the concept proposed in [10] which estimates congestion based overlapping bounding box of each net is applied. Each edge of two mergeable clusters forms a bounding box on the chip which represents potential consumed routing resource.

The merging priority of two clusters is based on overlapped bounding box to other nets. Fig. 3.3 illustrates how congestion analysis can be applied to avoid routing failure. In Fig. 3.3, the sorted order of nets based on Manhattan distance is $B \rightarrow C \rightarrow A$. However, Net A is unroutable using such order as merging priority. Regarding to Net B , it consumes 4 $unit^2$ of Net A 's routing area and 1 $unit^2$ of Net C 's routing area which is equivalent to Net A . Thus, using area of OBB as a guide, Net A and Net B are equivalent in terms of merging priority.

However, using area of OBB still creates ambiguity in determining merging order. Bounding box having drastic aspect ratio forms a larger routing blockage in one direction. In Fig. 3.4, both Net B and Net A have overlapping area equal to 24 (16+8) $unit^2$, but Net B has an aspect ratio 4:1 while Net A has an aspect ratio 1:1. Net B creates a larger routing obstacle in horizontal direction. Using area of OBB does not reflect the direction of congestion. Merging Net B first instead of Net A creates 2 additional detour wirelength.

To resolve this ambiguity and to reflect aspect ratio of bounding box, diagonal of overlapping bounding box is used to determine edge cost. In Fig. 3.4, the bounding

box of Net A covers a 4×4 OBB to Net C and a 2×4 OBB to Net B . Using total area of OBB to determine edge cost, Net A has an edge cost equal to 24. Using diagonal value of OBB to determine edge cost, Net A has an edge cost equal to $\sqrt[3]{32} + \sqrt[3]{20} = 10.1$. Using diagonal value of OBB resolves the ambiguity between Net A and Net B .

Fig. 3.5 compares the tradeoff between reduction in number of activations sequences to total routed wirelength. Default comparison uses the summation of diagonal length of OBB as edge cost. Fig. 3.5(a) uses the summation of area of OBB as edge cost, Fig. 3.5(b) uses half perimeter of OBB as edge cost and Fig. 3.5(c) uses minimum distance between two electrical pin as edge cost. From Fig. 3.5, merging electrical pin within shortest distance only estimates “least routing resources”. Using OBB as reference to edge cost estimates “least potential routing resources” is more accurate and empirical result demonstrates that it can achieve more reduction.

3.3 Updating Grid Cost

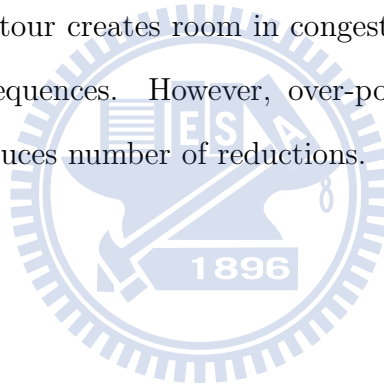
When clustering stage is completed, each node (cluster) contains a hierarchical set of electrical pins. However, clustering only determines routing order of electrical pins, the actual routing path that connects all of the electrical pins is still undetermined. To increase routing success rate, each grid is updated with an offset cost such that router is discouraged to use valuable routing resources during routing stage.

$$g(x, y) = \sum_{\forall j, \text{covers}(x, y)} \frac{\beta}{\sqrt[2]{\text{width}(OBB_j)^2 + \text{height}(OBB_j)^2}} \quad (3.1)$$

Given a set of unconnected electrical pins, it is first decomposed to a set of two-pin nets. For each bounding box spanned by a two-pin net, every grid covered by the bounding box is updated with a cost inversely proportional to the diagonal of

the bounding box. The offset grid cost is defined in Eq. 3.1. β is an empirical value to adjust the quality between detour wirelength and routability.

Fig. 3.6 illustrates an example using testcase amino-acid-1 that how adding offset grid cost can prevent failure. In Fig. 3.6(a), routing failure occurred since electrical pins are routed disregarding of the congestion. By adding offset grid cost, routing path will detour away from congested region and create room for inner electrical pins to escape, as illustrated in Fig. 3.6(b). Fig. 3.7 plot the tradeoff curve between reduction in number of activation sequences and total routed wirelength in response to different adjustment of β . Total routed wirelength increases steadily with increase in β . The response in reduction in activation sequences is a more delicate issue. Slight increase in detour creates room in congested region and enables more reductions in activation sequences. However, over-powering β creates undesired routing blockage which reduces number of reductions.



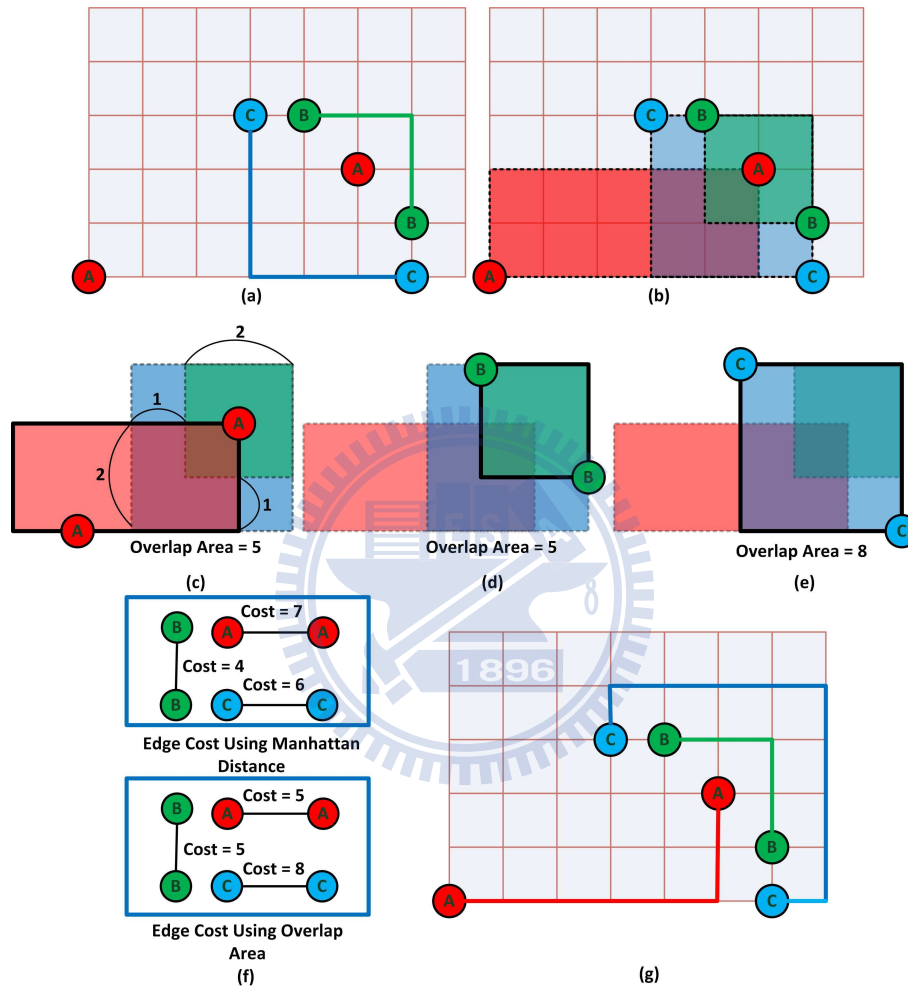


Figure 3.3: Bounding box estimation. (a) Using minimum distance to determine merging priority. (b) Bounding boxes for each edge. (c) Area of overlapping bounding boxes for net A. (d) Area of overlapping bounding boxes for net B. (e) Area of overlapping bounding boxes for net C. (f) Using area of overlapping bounding boxes as edge cost. (g) Using area of overlapping bounding boxes to determine merging priority.

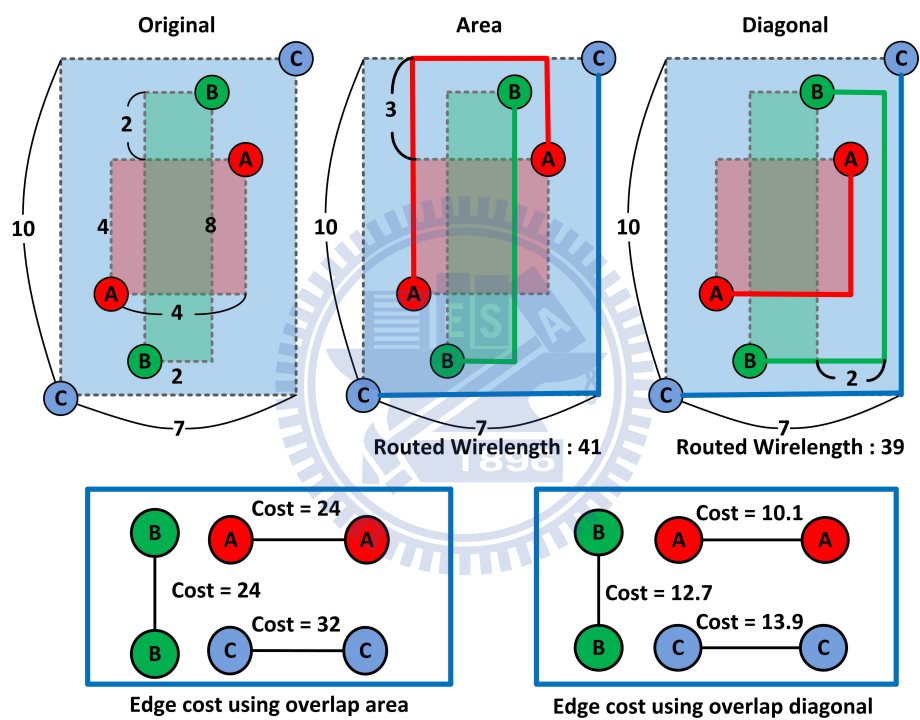
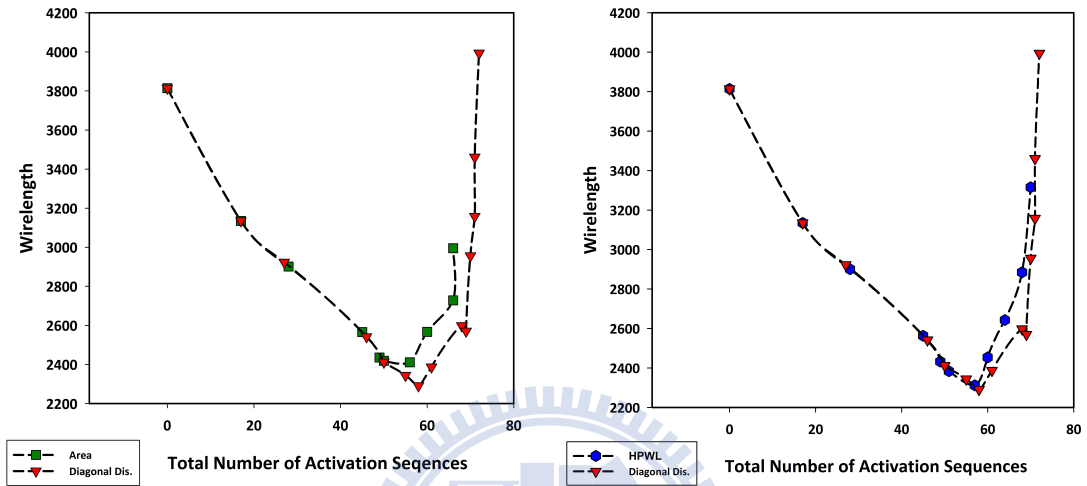
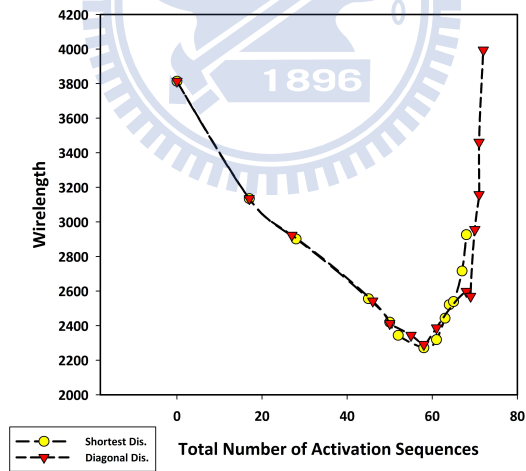


Figure 3.4: Comparison in routed wirelength using area and diagonal of overlapping bounding boxes as edge cost.

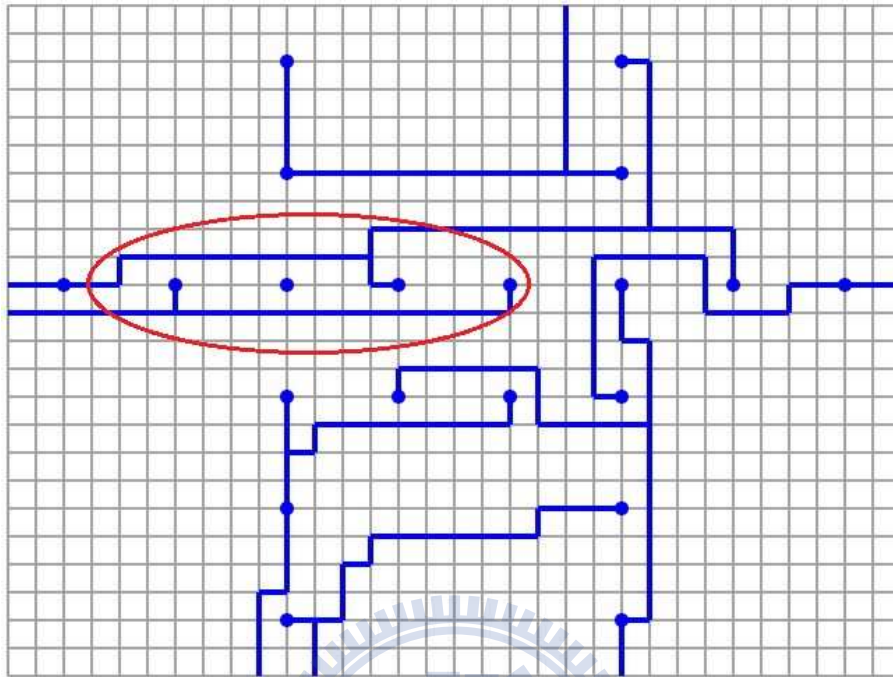


(a) Area of OBB vs. diagonal length of OBB (b) HPWL of OBB vs. diagonal length of OBB

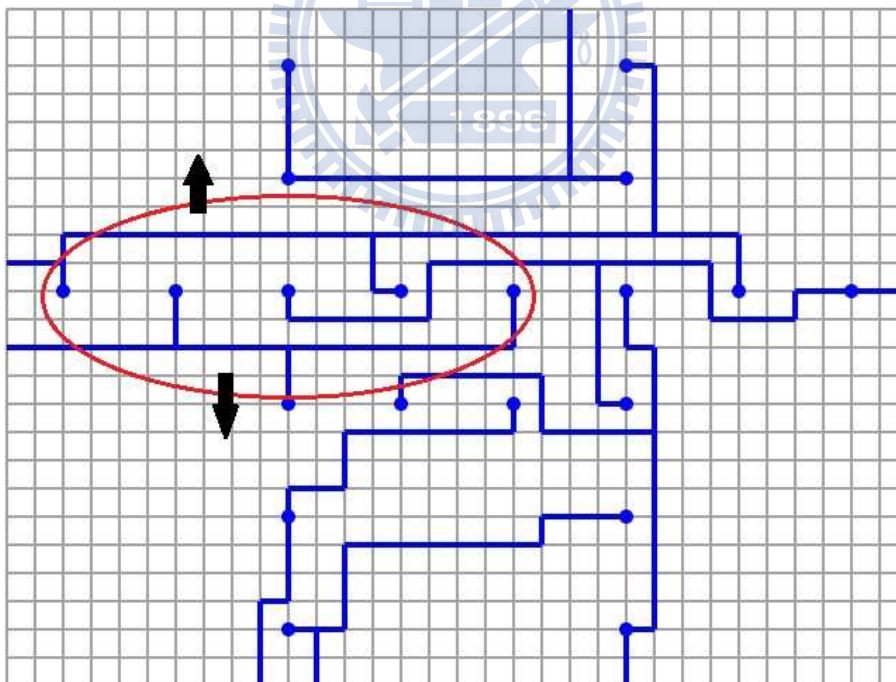


(c) Distance between two electrical pins vs. diagonal length of OBB

Figure 3.5: Comparison in tradeoff between reduction in number of activation sequences versus total routed wirelength.



(a) Routing result without offset grid cost.



(b) Routing result with offset grid cost.

Figure 3.6: Impact on routability with offset grid cost using testcase amino-acid-1. Wires are detoured away from potentially congested region. (a) is a unroutable design and (b) is a routable design.

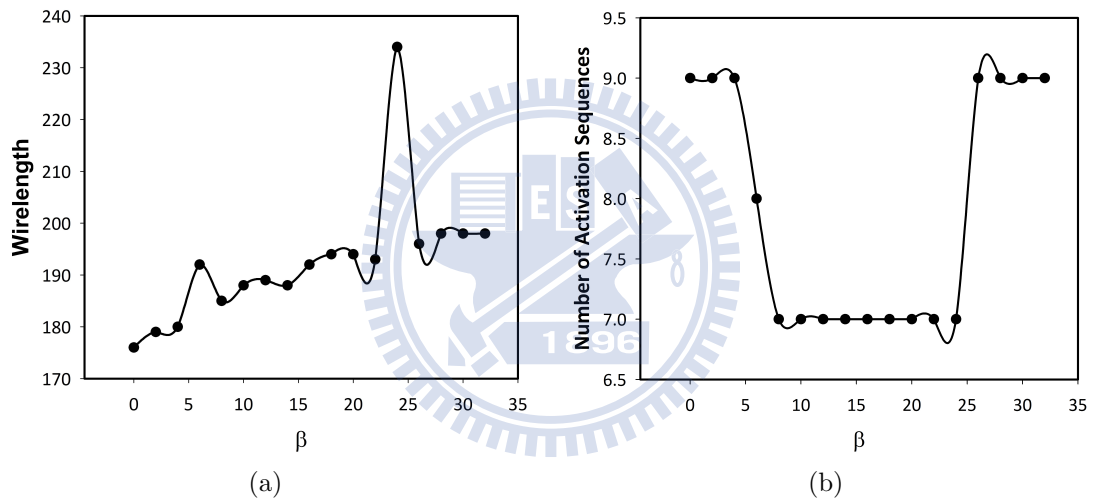


Figure 3.7: Impact on detour wirelength and reduction in number of activation sequences with different adjustment of β in testcase amino-acid-1.

Chapter 4

Multi-Source Multi-Sink ILP Escape Routing

When all electrical pins are connected, the upcoming task is to route connected electrical pins to any peripheral electrical pad. The challenge is to route every merged electrical pins to an electrical pad using minimal routed wirelength. The multi-source multi-sink escape routing problem can be optimally solved by formulating it as an ILP problem. The notations used in the ILP formulation are defined as follows:

- p_k denotes a pin k
- n_j denotes a net j
- $f(u, v)$ denotes flow from p_u , a positive value means an outward flow and negative value means an inward flow.

The ILP formulation for multi-source multi-sink escape routing problem for pin-constrained EWOD chip is formulated as follows. Given a set of nets $N = \{n_1, n_2, \dots, n_j\}$, a set of edges $E = \{e_1, e_2, \dots, e_i\}$, a set of electrical pins $P = \{p_1, p_2, \dots, p_k\}$ and a set of control pads $B = \{b_1, b_2, \dots, b_m\}$, minimize total flow for all pins in P .

The objective function is described in Eq. 4.1. Minimizing total flow value is equivalent to minimizing total escape route wirelength.

$$\min \sum_{v \in P} f(u, v), \forall u \in P \quad (4.1)$$

subject to

$$\sum_{v \in P} f(u, v) = 0, \forall u \in P \quad (4.2)$$

$$\sum_{s \in n_i} \sum_{v \in P} f(s, v) = 1, \forall i \in N \quad (4.3)$$

$$\sum_{v \in P} f(s, v) = |N|, \forall s \in B \quad (4.4)$$

$$\sum_{v \in P} |f(u, v)| \leq 2, \forall u \in P \quad (4.5)$$

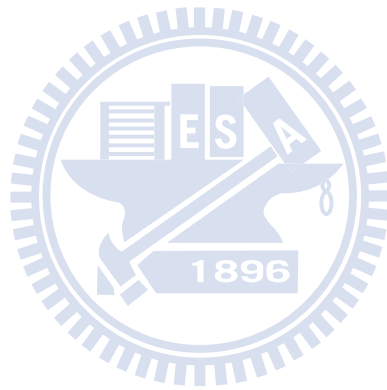
$$|f(u, v)| \leq 1, \forall u \in P, \forall v \in P \quad (4.6)$$

Eq. 4.2 defines the conservation of flow. For a given electrical pin that is neither a source or sink, inward flow must equal to its outward flow. Eq. 4.3 defines the net flow for a given net n_j must equal to 1. In graph representation, every electrical pin for a given net is connected to a super source and each net has an initial flow value equal to 1. Control pads can be regarded as sink nodes and all are connected to a super sink node. Eq. 4.3 defines the initial value such that every net can only have exactly one path escape to boundary electrical pad.

Eq. 4.4 defines terminating condition. When the summation value of flow for every electrical pad equals to the total number of nets, it represents that every net is successfully escaped to an electrical pad. Eq. 4.5 restricts that no routing paths

can be crossed by defining that the absolute value of flow for any given electrical pin is less than or equal to 2. Eq. 4.6 defines the capacity constraint such that the absolute value of flow between any two electrical pins is less than or equal to 1.

Solving the ILP constraints traverses through all possible routing solutions. To accelerate runtime, a maze router is implemented to accelerate run time in exchange for less reduction in activation sequences.



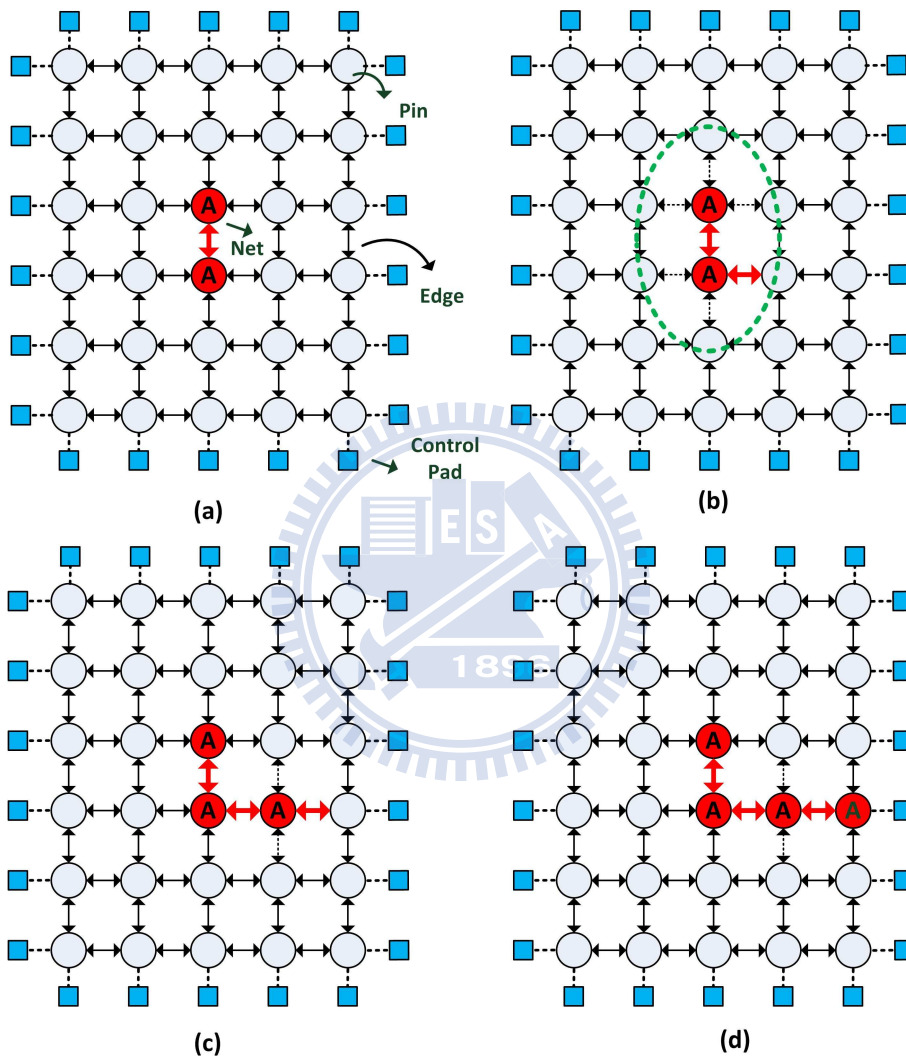


Figure 4.1: Network and routing procedure for ILP formulation. (a) Network-flow for net A. (b) Set net A's around flow equal to 1. (c) In-flow equal to out-flow to pass through flow to boundary. (d) Stop until boundary in-flow equal to total net number.

Chapter 5

Experimental Result

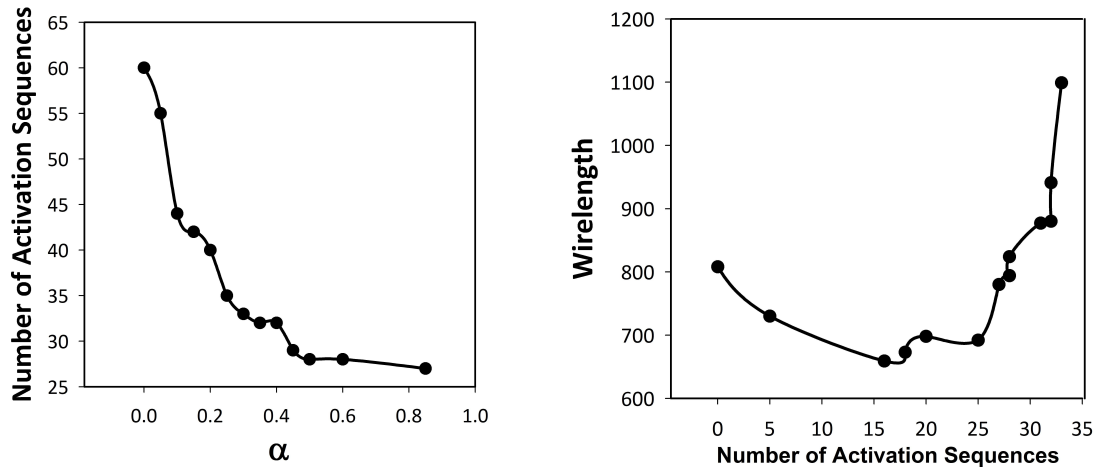
Table 5.1: Comparison with Prior Works [8] on Wire-Length and Pin Counts Without Obstacles

benchmarks	Chip Size	#E	[8]			Our (Maze-Based)			Our (ILP-Based)			Direct Addressing [5]		
			#Pin	#WL	CPU Time(s)	#Pin	#WL	CPU Time(s)	#Pin	#WL	CPU Time(s)	#Pin	#WL	CPU Time(s)
amino-acid-1	6X8	20	9	190	0.08	7	185	0	7	185	0.24	20	136	0.24
amino-acid-2	8X8	24	11	207	0.11	9	180	0	9	180	0.25	24	144	0.32
protein-1	13X13	34	24	462	0.26	10	349	0.01	10	353	0.88	34	348	0.90
protein-2	13X13	51	25	662	0.28	31	566	0.02	31	566	0.92	51	607	0.91
dilution	15X15	54	15	1178	0.17	23	844	0.11	23	820	1.53	54	582	1.40
multiplex	15X15	59	36	1444	0.36	10	527	0.01	10	534	1.76	59	851	1.24
random-1	10X10	20	8	278	0.04	9	183	0.00	9	185	0.54	20	161	0.46
random-2	15X15	30	11	614	0.10	16	421	0.02	16	421	1.63	30	476	1.32
random-3	20X20	60	19	2720	0.31	27	1099	0.25	27	1090	3.53	60	808	3
random-4	30X30	90	26	5975	0.40	46	2127	0.74	45	4076	29.10	90	1826	10
random-5	50X50	100	37	7965	1.53	28	3994	2.22	28	3830	65.82	100	3814	42.70
random-6	60X60	100	41	8901	2.23	39	3247	1.65	35	2695	118.65	100	3223	54.10
random-7	70X70	150	80	16612	6.65	52	5063	6.9	45	7133	232.40	150	6188	59.86
Norm.	-	-	1.11	2.51	1.05	1.00	1.00	1.00	0.96	1.17	38.3	2.58	1.02	31

Table 5.2: Comparison with Prior Work [3] on Obstacle Aware Pin-Constrained Designs

benchmarks	Size	#E	P_{max}	[3]			Our Work(ILP-Based)		
				#Pin	#WL	CPU Time(s)	#Pin	#WL	CPU Time(s)
DNA-1	16X24	211	128	128	3003	3.7	128	2335	7.3
DNA-2	13X21	77	32	32	1113	0.7	32	894	2
random-1	6X8	24	16	16	271	0.0	16	206	0.28
random-2	15X15	59	32	32	991	0.4	32	893	1.47
random-3	15X15	62	32	32	1153	0.5	32	872	1.45
random-4	15X15	91	64	64	1417	0.4	64	1244	1.6
random-5	20X30	256	128	128	4742	11.4	128	3969	16.9
random-6	30X40	400	256	256	9099	26.1	256	6959	72.2
Norm.	-	-	-	1.00	1.25	-	1.00	1.00	-

In this section, experimental result of the proposed algorithm is presented. The entire algorithm is implemented with standard C++ language and experimented on

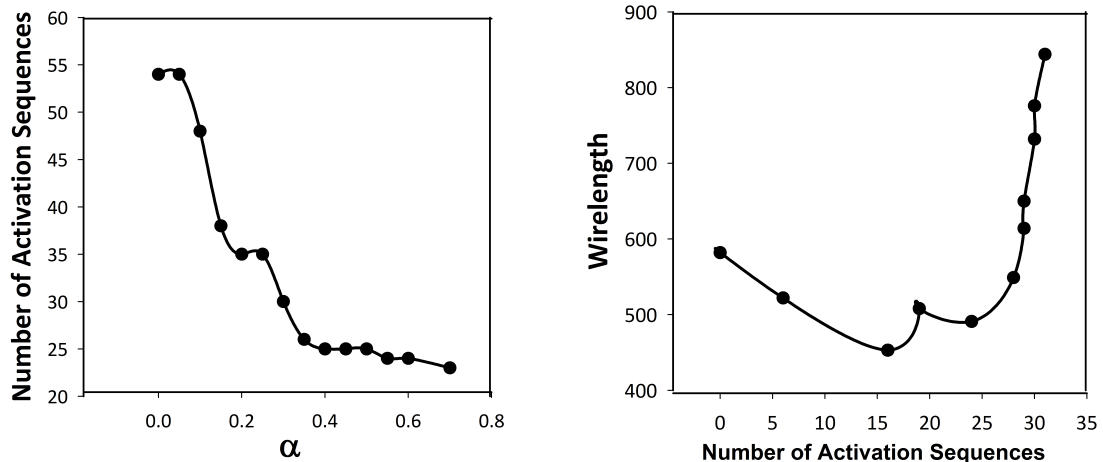


(a) Merging Effort vs Reduction in activation sequences (b) Reduction in activation sequences vs Routed wirelength

Figure 5.1: Tradeoff between reduction number in activation sequences, routed wirelength and merging effort for obstacle free testcase [random-3].

AMD Athlon Dual Core machine operating at 2.6GHz. IBM CPLEX v12.2 [1] is used to solve the ILP constraints in escape routing. Input designs are obtained from [8] and input designs with obstacles are obtained from [3]. Execution time for [8] and [3] is presented based on their reported statistics.

To demonstrate effectiveness of routability driven clustering, we compare our algorithm with [8]. Fig. 5.3 illustrates the routing result using our algorithm and [8]. Unlike [8], our algorithm does not require to find minimal spanning tracks as an initial solution. Our proposed clustering algorithm simply finds a proper merging order to maximize routability. In Table 5.1, #E denotes total number of electrical pins. #Pin denotes total number of required activation sequences and #WL denotes total routed wirelength. In comparison with [8], our proposed algorithm at default mode achieves 11% additional reduction in required activation sequences and routes the designs with an average of 151% less total wirelength using equivalent execution time. The reduction in routed wirelength have direct impact to reduction in activation sequences. In Fig. 5.1 and Fig. 5.2, it can be observed that reduction of activation sequences decreases linearly with routed wirelength. At certain



(a) Merging Effort vs Reduction in activation sequences (b) Reduction in activation sequences vs Routed wirelength

Figure 5.2: Tradeoff between reduction number in activation sequences, routed wirelength and merging effort for obstacle free testcase [dilution].

point, when routed wirelength begins to detour to search for a feasible solution, improvement in reduction of activation sequences terminates almost instantly.

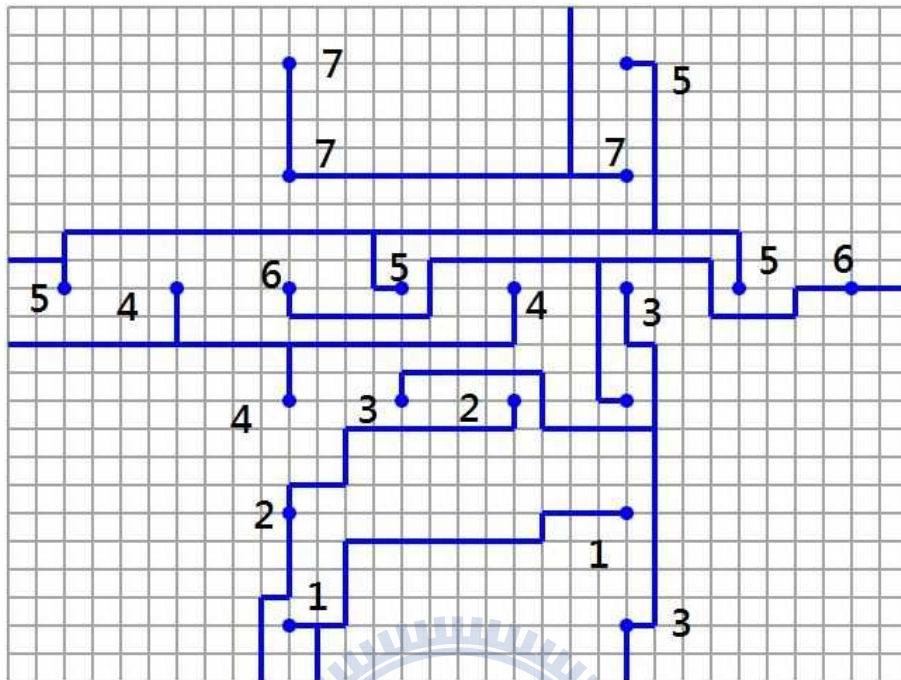
When execution time and routed wirelength are not the primary concerns, using ILP based escape routing algorithm to route all of the paths, we can achieve 15.6% reduction in activation sequences and 113.8% less total wirelength using 38x more execution time compared to default mode. In comparison with direct-addressing method, our proposed framework can reduce activation sequences by 158% with 2% less wirelength. To maximize routing success rate, ILP based escape routing is used to route all of the paths in direct-addressing method.

Our algorithm is also capable of dealing with designs with presence of obstacles. Table 5.2 lists the designs with presence of obstacles and compares our result with work done in [3]. Our framework can still achieve equivalent number of reduction in activation sequences with 25% improvement in total routed wirelength.

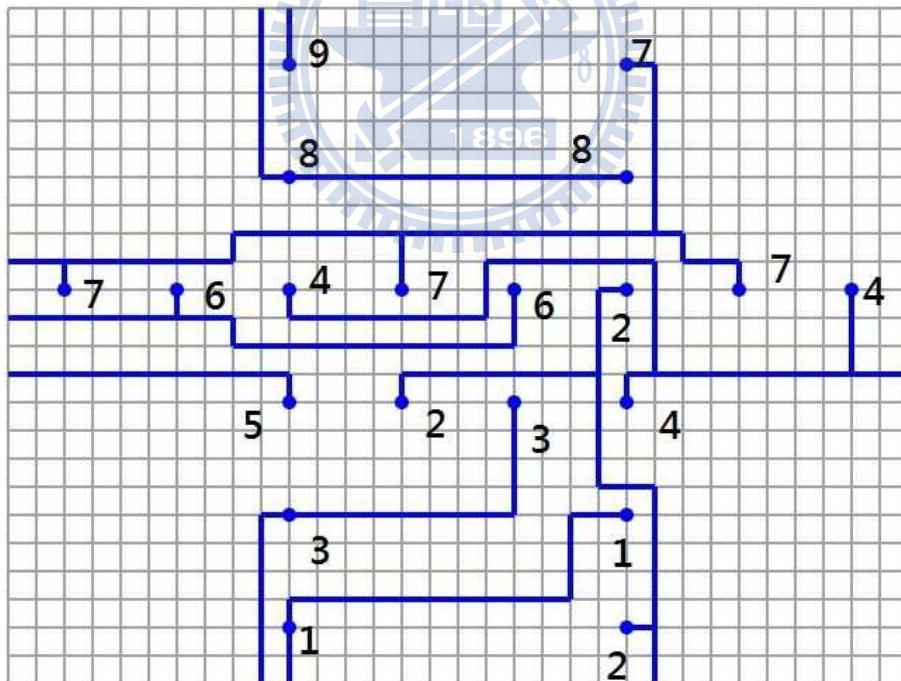
The entire framework has two input parameters, α , to control greediness of clustering and β , to control degree of detour when congested region is encountered.

When α is set to 0, merging effort is set to zero and our framework behaves exactly like direct addressing method. When α is set to 1, merging effort is to the maximum and our framework will greedily reduce total number of activation sequences.





(a)



(b)

Figure 5.3: Merging and routing result for testcase [Amino-Acid-1] Compared with work [8] for test case [amino-acid-1]. (a) Our work requires 7 activation sequences using 185 unit of routed wirelength. (b) [8] requires 9 activation sequences using 190 unit of routed wirelength.

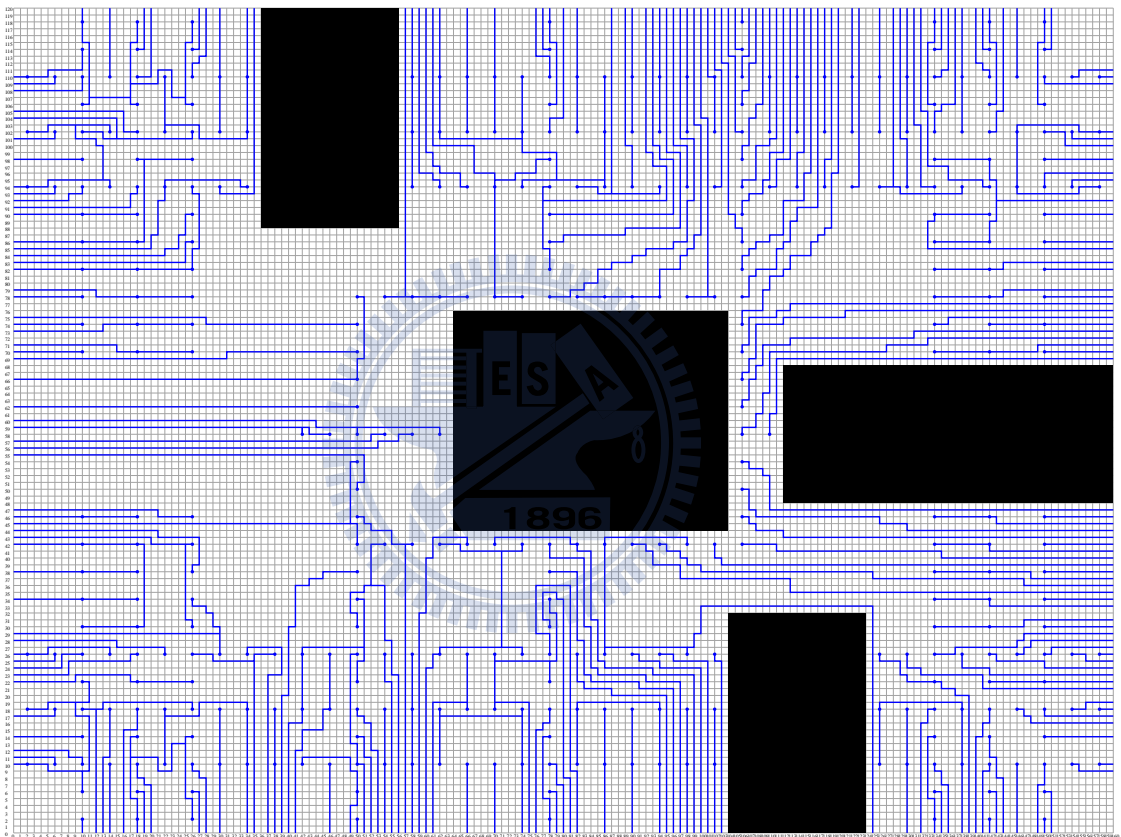


Figure 5.4: Routing result for testcase [random-6] with presence of obstacles.

Chapter 6

Conclusion

In this work, we solved both merging and routing problem for pin constrained Broadcast Addressing EWOD chips. Our main contribution lies in our proposed routability driven clustering to determine merging priority of electrical pins. Using diagonal of overlapping bounding boxes can accurately estimate routability and achieves better reduction in activation sequences. The nature of clustering framework offers flexibility to de-cluster when routing failed and obtains a precise tradeoff between reduction in activation sequences and routed wirelength. The multi-source multi-sink routing problem can be formulated as a set of ILP constraints and optimally solved. As a result, our proposed algorithm outperforms recent works on pin-constrained EWOD designs with and without presence of obstacles with at most 15% reduction in activation sequences.

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