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電子工程學系　電子研究所碩士班

碩　士　論　文

應用於射頻積體電路之靜電放電防護設計

ESD Protection Design for Radio-Frequency Integrated Circuits

研 究 生：蔡翔宇　　(Shiang-Yu Tsai)

指導教授：柯明道教授 (Prof. Ming-Dou Ker)

中華民國一〇一年八月

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摘要

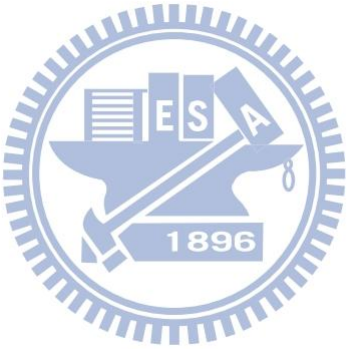
在現今的 IC 設計中，晶片的整合度與成本是相當重要的考量，因此，射頻積體電路 (radio-frequency integrated circuits, RF ICs) 也逐漸傾向於實現在 CMOS 製程中。在 CMOS 製程中，靜電放電 (electrostatic discharge, ESD) 是一項相當重要的可靠度問題，因此針對使用 CMOS 製程的射頻積體電路之靜電放電防護設計自然也是需求孔急。由於射頻積體電路對於任何額外的寄生效應都相當敏感，因此能應用在射頻積體電路之靜電放電防護設計除了要有好的靜電放電耐受度之外，還必須要能將其寄生效應的影響降至最低。

本篇論文提出了兩項可應用在射頻積體電路之靜電放電防護設計。其中之一可應用於 60 GHz 的射頻積體電路，透過適當設計的電感 (inductor) 與電容 (capacitor)，能夠在高頻下將寄生效應的影響降低，同時又能兼顧一定的靜電放電防護能力。

另外一項則為適用於射頻功率放大器 (power amplifier, PA) 之靜電放電防護設計。

透過一個使用齊納二極體 (Zener diode) 來觸發的的矽控整流器 (silicon-controlled rectifier, SCR) 來做為靜電防護元件，並搭配電源端到地端間靜電放電箝制電路 (power-rail ESD clamp circuit) 來完成全晶片防護，同時搭配 2.4 GHz 之射頻功率放大器電路以作驗證。

根據量測結果，這些設計可以有效的提供射頻積體電路適當的靜電放電防護能力，同時又不會影響其正常操作。



ESD Protection Design for Radio-Frequency Integrated Circuits

Student: Shiang-Yu Tsai **Advisor: Prof. Ming-Dou Ker**

Department of Electronics Engineering &Institute of Electronics
National Chiao-Tung University

Abstract

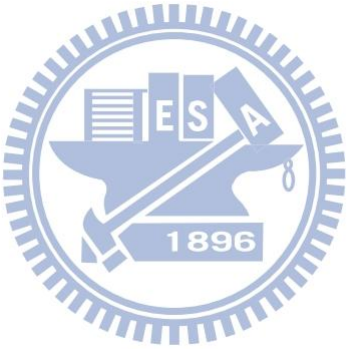
For the consideration of high integration and low cost, radio-frequency integrated circuits (RF ICs) have been fabricated in CMOS processes. Electrostatic discharge (ESD) is one of the most serious reliability issues of CMOS processes, and it also bothers RF IC designers now. A successful RF ESD protection design needs well ESD protection ability and small parasitic effect, since RF ICs are very sensitive to any extra parasitic effect.

In this thesis, two RF ESD protection designs are proposed and verified. One is for RF circuits operating in 60 GHz. With the help of inductor and capacitor, the parasitic capacitance of ESD protection device can be effectively decreased and acceptable ESD level can be required.

The other one is for RF power amplifier (PA). A Zener-diode-triggered silicon-controlled rectifier (ZTSCR) is used as an ESD protection device. In addition, two 2.4 GHz CMOS PAs

with the proposed ZTSCR and power-rail ESD clamp circuit are designed as ESD-protected PAs to verify their ESD level.

According to the experimental results, the ESD protection designs have high ESD robustness without degrading the RF performances.



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101年8月於交大

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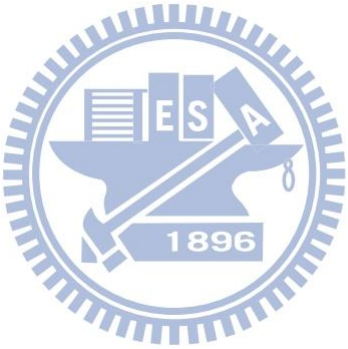

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Chapter 1
Introduction

1.1 Motivation

In recent decades, the development of wireless technologies is explosive and rapid. The requirements of wireless products such as smart phones are overwhelming. For the consideration of low cost and high integration, the whole radio-frequency integrated circuits (RF ICs) have been widely fabricated in CMOS processes [1].

The major reliability issue of CMOS ICs is electrostatic discharge (ESD). As IC technology continuously scales down, ESD issues become more serious and must be carefully considered. Well-designed ESD protection circuits for all I/O pads in ICs are necessary. Conventional ESD protection design, which consists of a pair of diodes inserted beside I/O pads and a power-rail ESD clamp circuit can provide whole-chip ESD protection [2]. Unfortunately, such design would degrade the RF performance of core circuits due to the undesired parasitic effects introduced by those ESD protection devices [3].

ESD protection devices are mainly applied to the I/O interfaces of ICs. For an RF IC, the input interface is typically a low-noise amplifier (LNA), and the output interface is typically a power amplifier (PA). Thus, ESD protection design for CMOS LNA and PA are needed.

While being applied in RF ICs, conventional ESD protection devices with large dimensions have good ESD robustness, but their large parasitic capacitances cause power loss from pads to ground. In addition, the parasitic capacitances also change input and output matching conditions. For these reasons, designing effective ESD protection circuits without

degrading the RF performance of core circuits has become a great challenge.

Since the parasitic capacitances of ESD protection devices are the main obstacle to RF ESD protection design, some methods have been developed to mitigate the negative impact caused by the parasitic capacitances. The parasitic capacitances of ESD protection devices can be cancelled out by using inductors and capacitors [4]-[6]. Some ESD protection designs have been developed to fundamentally reduce the parasitic capacitances of the ESD protection devices [3]. ESD protection devices can also be co-designed with RF circuits or combined with matching networks of RF circuits [7].

However, the rapidly increasing operating frequency of RF ICs makes the parasitic capacitances of ESD protection devices be more strictly limited. It is harder and harder to meet the desired ESD robustness with such limitation. As a result, ESD protection designs for extremely high frequency are necessary. Two new ESD protection circuits with less RF performance degradation and compact layout area are proposed in this work. Both ESD protection circuits are designed for 60 GHz RF circuits. Such ESD protection circuits have been designed and fabricated in a 65-nm CMOS process. The measurement results prove that both ESD protection designs are suitable for 60 GHz RF circuits with required ESD robustness and tolerable degradation of RF performance.

Another ESD protection design for CMOS PA is also proposed in this work. For RF ESD protection designs, silicon-controlled rectifier (SCR) is a useful device. An SCR with proper triggering mechanism has great ESD robustness and low parasitic capacitances within a small layout area. Therefore, carefully designed SCR is expected to be suitable for RF ESD protection [8]. A Zener-diode-triggered SCR (ZTSCR) for PA ESD protection is proposed. Two 2.4 GHz CMOS PAs which utilize ZTSCR and a power-rail ESD clamp circuit as their ESD protection design are presented. The ZTSCR and PAs have been designed and fabricated in a 65-nm CMOS process. The measurement results show that ZTSCR indeed provides desired ESD robustness without degrading RF performance of the 2.4 GHz CMOS PAs.

Besides, for comprehensive investigation of PA ESD protection methods, an ESD-protected PA with ESD protection strategy consists of an RF choke inductor and a power-rail ESD clamp circuit has also been designed and verified in a 65-nm CMOS process. Such ESD protection strategy is used for PA with on-chip RF choke inductor at the output stage. According to the measurement results, the proposed ESD protection strategy also provides desired ESD robustness without degrading PA RF performance.

1.2 Thesis Organization

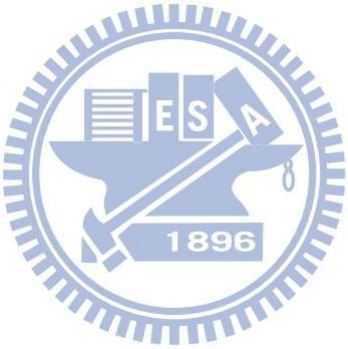
Chapter 2 introduces the basic principles and the crucial considerations of RF ESD protection design as well as basics of RF LNA and RF PA. The issues of RF ESD protection design are investigated. Some practical RF ESD protection designs are exhibited.

Chapter 3 exhibits ESD protection designs for 60 GHz RF circuits. Two ESD protection designs with inductors, capacitors, and diodes are proposed. The architecture, corresponding design equations, and simulation results are presented. The measurement results of the RF performances and the ESD levels of both ESD protection designs, which are fabricated in a 65-nm CMOS process, are summarized. According to the experimental results, the two proposed ESD protection designs exhibit required ESD levels without serious RF performance degradation, and therefore is suitable for 60 GHz RF circuits.

Chapter 4 exhibits an ESD protection design for 2.4-GHz RF PA. A Zener-diode-triggered SCR, which is appropriate for PA ESD protection, is proposed. The architecture of the ESD protection design is presented in detail. In addition, a 2.4 GHz CMOS PA used to verify the ESD level of the proposed ZTSCR is also designed. Both unprotected PA and ESD-protected PA are fabricated in a 65-nm CMOS process. The experimental results of RF performances and ESD levels of the unprotected PA and the ESD-protected PA are

summarized and compared. According to the results, the proposed ZTSCR indeed has enough ESD protection ability without degrading the RF performances of the 2.4 GHz CMOS PA. Besides, a useful ESD protection design for PA with on-chip RF choke inductor at the output stage is also presented and verified in a 65-nm CMOS process.

Chapter 5 is the conclusions of this thesis and the future works on this topic.



Chapter 2

Basics of RF and ESD Protection

2.1 General Considerations of LNA Design

2.1.1 S-Parameters and Noise Figures

To deal with a high-frequency network, conventional method of measuring voltage and current is no longer suitable. Direct measurement under high-frequency conditions usually involves the magnitude and phase of a traveling wave, so the concepts of equivalent voltage, equivalent current, and the related impedance and admittance become abstract. Scattering parameters (S-parameters) with the concepts of incident, reflected, and transmitted waves are more suitable and widely used to describe the characteristics and behaviors of high-frequency networks [9].

Fig. 2.1 shows a two-port network characterized by S-parameters. The S-parameters are defined in

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{2.1}$$

which can also be represented as

$$\begin{cases} b_1 = S_{11}a_1 + S_{12}a_2 \\ b_2 = S_{21}a_1 + S_{22}a_2 \end{cases} \tag{2.2}$$

where a_1 and a_2 represent the incident waves of each port; b_1 and b_2 represent the reflected waves of each port, respectively. Each term in the S-parameters matrix is defined in (2.3).

$$S_{11} = \left. \frac{b_1}{a_1} \right|_{a_2=0}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \tag{2.3}$$

S_{11} is the reflection coefficient seen at port 1 when port 2 is terminated with a load of 50 Ω; S_{22} is the reflection coefficient seen at port 2 when port 1 is terminated with a load of 50 Ω. S_{21} is the forward gain from port 1 to port 2; S_{12} is the reverse gain from port 2 to port 1.

In high-frequency measurement, S_{11} describes input matching condition, and S_{22} describes output matching condition. S_{21} describes the forward gain from port 1 to port 2, and S_{12} describes the reverse isolation condition.

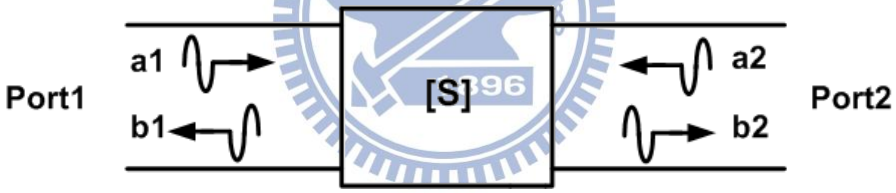


Fig. 2.1. A two-port network described with S-parameters.

For receivers, noise is another important concern. Noise factor is a figure of merit to describe a noisy system [10]. Noise factor is defined as

$$F = \frac{SNR_i}{SNR_o} \tag{2.4}$$

where SNR_i represents the signal-to-noise ratio measured at input, and SNR_o represents the signal-to-noise ratio measured at output. It is a measure of SNR degradation when signal passes through the described system. A commonly used figure of merit named noise figure (NF) is

$$NF = 10\log F(dB) \tag{2.5}$$

The physical meaning can be realized as

$$NF = \frac{Total\ output\ noise\ power}{Output\ noise\ power\ due\ to\ source\ only} \tag{2.6}$$

Form (2.6), if the described system adds no noise of its own, NF would be zero.

Considering a cascade multi-stage system shown in Fig. 2.2, each stage has gain (G) and noise factor (F). The noise factor can be characterized by Friis formula

$$F_{sys} = 1 + (F_1 - 1) + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots \tag{2.7}$$

It is clear that noise of a multi-stage system is mainly contributed by the first stage. For this reason, LNA, which is the first stage of an RF receiver, needs much consideration on noise.

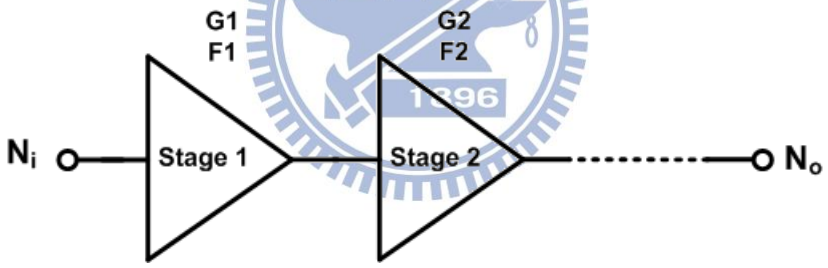


Fig. 2.2. A cascade multi-stage RF system described with gain and noise factor.

2.1.2 Stability

Stability, which can be extracted from S-parameters, is a crucial consideration in RFIC design. To an RF amplifier, it is important to operate stably without going into oscillation under any condition. For unconditionally stable, both input impedance and output impedance cannot be negative resistive. The sufficient and necessary conditions are

$$|\Gamma_S| < 1 \tag{2.8}$$

$$|\Gamma_L| < 1 \tag{2.9}$$

$$\left|\Gamma_{IN}\right| = \left|S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}\right| < 1 \tag{2.10}$$

$$\left|\Gamma_{OUT}\right| = \left|S_{22} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{11}\Gamma_L}\right| < 1 \tag{2.11}$$

where Γ_S is source reflection coefficient; Γ_L is load reflection coefficient; Γ_{IN} is input reflection coefficient; Γ_{OUT} is output reflection coefficient.

These equations can be further derived to

$$K = \frac{1 - \left|S_{11}\right|^2 - \left|S_{22}\right|^2 + \left|\Delta\right|^2}{2\left|S_{12}S_{21}\right|} > 1 \tag{2.12}$$

$$\left|\Delta\right| = \left|S_{11}S_{22} - S_{12}S_{21}\right| < 1 \tag{2.13}$$

(2.12) and (2.13) can be further derived to

$$b = 1 + \left|S_{11}\right|^2 - \left|S_{22}\right|^2 - \left|S_{11}S_{22} - S_{12}S_{21}\right|^2 > 0 \tag{2.14}$$

(2.12) and (2.14) represents the necessary and sufficient conditions for unconditional stability.

2.2 General Considerations of PA Design

2.2.1 Efficiency and Large Signal Characteristics

Since PA consumes large amounts of DC power and simultaneously amplifies and delivers RF power to a load, the problem of whether PA delivers and amplifies RF power efficiently or not is needed to be concerned. Some figures of merit can help evaluating the efficiency. There are three kinds of indicators which are used to evaluate efficiency:

Drain Efficiency:

$$\eta_d = \frac{P_o}{P_{DC}} \tag{2.15}$$

Total Efficiency:

$$\eta_{total} = \frac{P_o - P_{in}}{P_{DC}} \tag{2.16}$$

Power Added Efficiency (PAE):

$$\eta_{PAE} = \frac{P_o}{P_{DC} + P_{in}} \tag{2.17}$$

Where P_{in} represents RF input power, P_o represents RF output power, and P_{DC} represents DC input power. Commonly, PAE is a reasonable and usually used indication of PA performance about efficiency.

To design an RF power amplifier, large signal characteristics are undoubtedly important concern. Ideally, an RF amplifier is considered as a linear amplifier. The power gain remains constant and the relationship between output power and input power is linear. However, the large signal transfer characteristics are different. As input power increases larger and larger, the output power starts to gradually saturate. This makes the linear transfer relationship between input power and output power no longer hold. Under large signal operating conditions, the MOS devices used in PA cannot be considered as linear devices anymore, and the output power will be gradually compressed. Since the power transfer characteristic is no longer linear after the output power starts to be compressed, one indicator, 1-dB gain compression point, is commonly used to estimate the upper limitation of the linear operating region of PA.

At 1-dB gain compression point (P_{1dB}), the power gain is 1 dB smaller than the constant power gain, as shown in Fig. 2.3. IP_{1dB} is the input power at P_{1dB}. The power transfer characteristic is shown in Fig. 2.4. In Fig. 2.4, OP_{1dB} represents the output power at P_{1dB}, and P_{sat} represents saturated output power. OP_{1dB} is often treated as the maximum linear output power of PA, so it is an important indicator of linearity of PA.

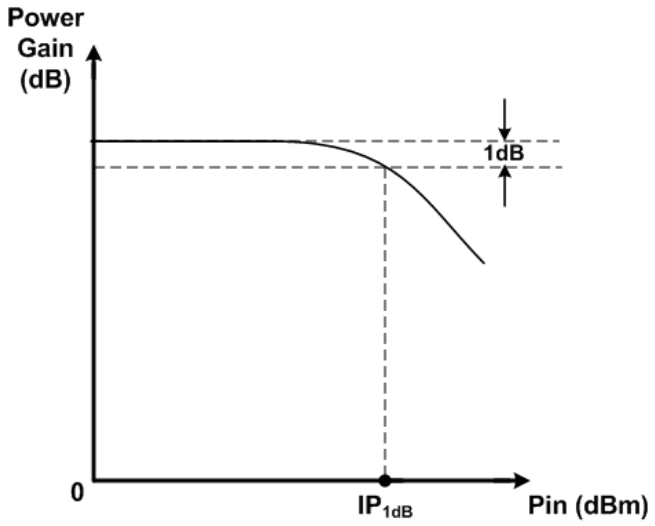


Fig. 2.3. The plots of power gain versus input power.

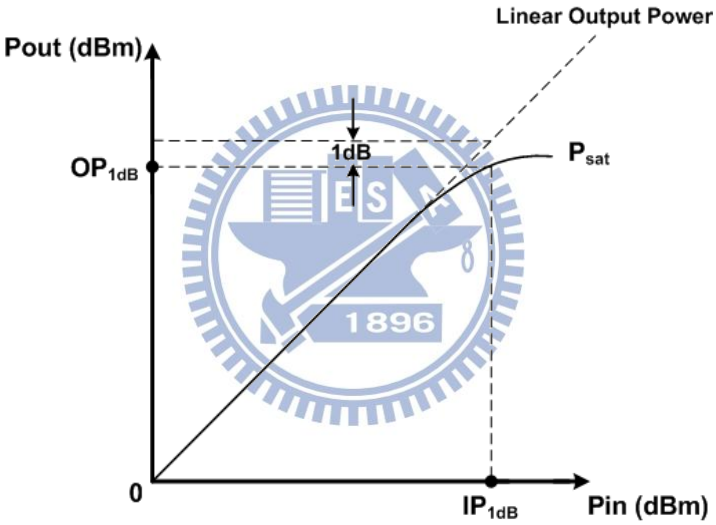


Fig. 2.4. The plots of output power versus input power.

2.2.2 Load-Line Theory and Load-Pull Characterization

A general PA is shown in Fig. 2.5. RFC represents an RF choke inductor used to feed DC power to the drain of the output transistor. DC block is a capacitor used to block from losing to the output load (R_L). Output matching network is used to transform the impedance of R_L to an optimal output impedance seen from the drain of the output transistor. With optimal output impedance, PA can deliver the maximum output power.

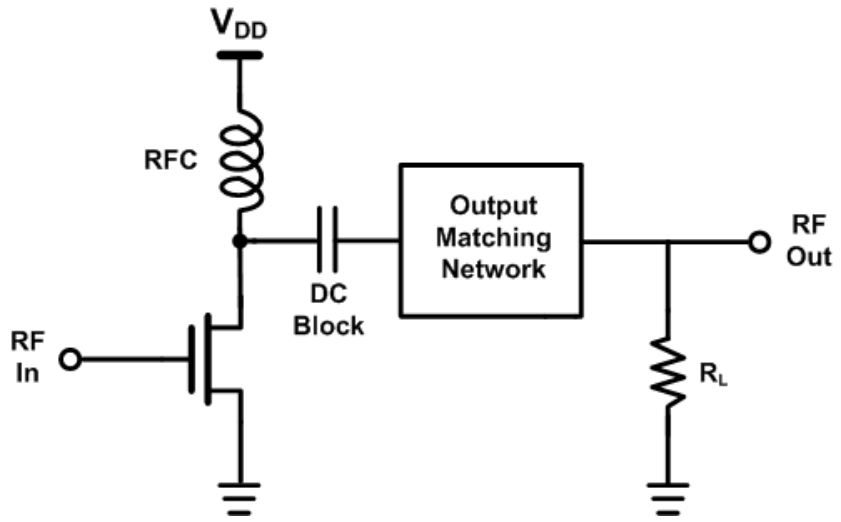


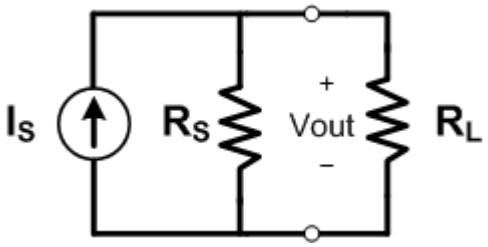
Fig. 2.5. Architecture of general RF power amplifier.

One evident difference between RF PA and linear RF amplifier such as LNA is the output matching design. Conjugate matching method, which is commonly used in RF amplifier, is no longer suitable for PA [11].

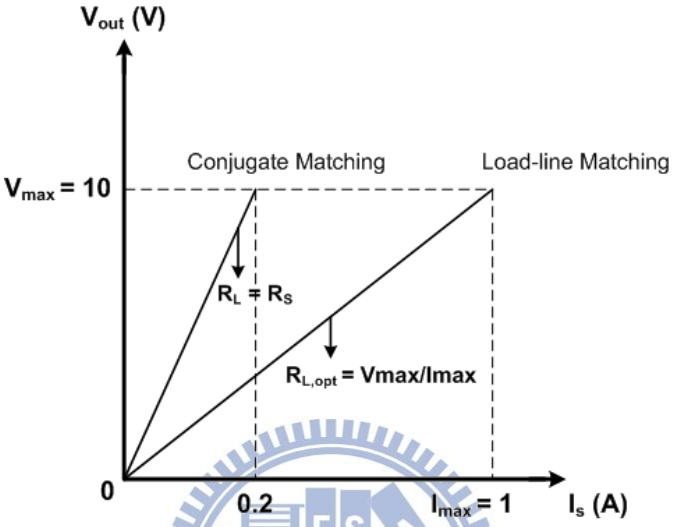
Fig. 2.6 (a) shows a simple current generator. The generator, for example, has a maximum output current of 1 A and an output resistance (R_S) of 100 Ω. According to the conjugate matching theory, the load resistance (R_L) should be chosen as 100 Ω. However, the voltage across the terminals of the generator would be 50 V. If the current generator is the output MOS transistor of a PA, the voltage would exceed the maximum output voltage of the output transistor, which is assumed to be 10 V here. For such physical restriction, another matching method named "load-line match" is selected to acquire maximum output power for PA. With this method, the optimal load resistor ($R_{L,opt}$) is chosen as

$$R_{L,opt} = \frac{V_{\max}}{I_{\max}} = 10\Omega \tag{2.19}$$

where it has been assumed that $R_S >> R_{L,opt}$. Fig. 2.6 (b) shows the comparison between conjugate match and load-line match. Load-line match is necessary for PA to provide maximum output power with the RF voltage swing still being kept within specified limits.



(a)



(b)

Fig. 2.6. (a) A simple current generator and (b) the comparison of its two output matching methods.

To obtain the optimal output impedance of PA, load-pull measurement is an accurate method which has been commonly used. A simple architecture of load-pull measurement is shown in Fig. 2.7. The device or amplifier under test (DUT) is set between an input tuner and an output tuner. The first step is to find the optimal output impedance which can be utilized to acquire the maximum output power. This forms the center point of the load-pull loci on Smith Chart. Next, the output impedance is adjusted repeatedly to get a constant output power which is lower than the maximum output power by 1 dB. A constant power contour will be presented on Smith Chart, too. This procedure is repeated many times and a set of constant output power contours are generated and shown on Smith Chart, as shown in Fig. 2.8. For PAE, this procedure needs to be done again, since the optimal output impedance for

maximum output power is different from the optimal output impedance for maximum PAE. Finally, two sets of contour are shown on Smith Chart, as shown in Fig. 2.9. The optimal output impedance for a well balance between output power and PAE can be chosen with the load-pull system.

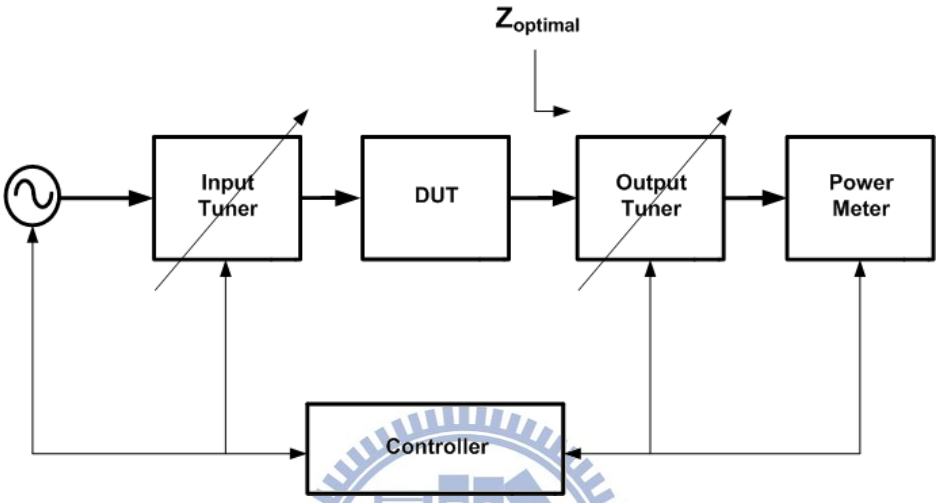


Fig. 2.7. Typical Load-pull system.

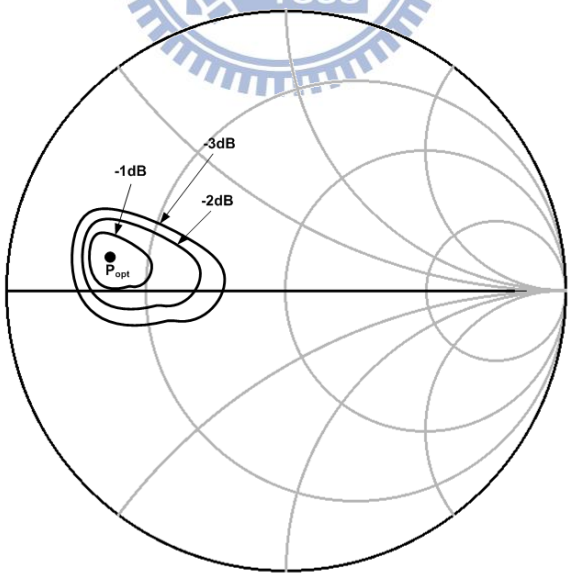


Fig. 2.8. Load-pull contour – delivered power contour.

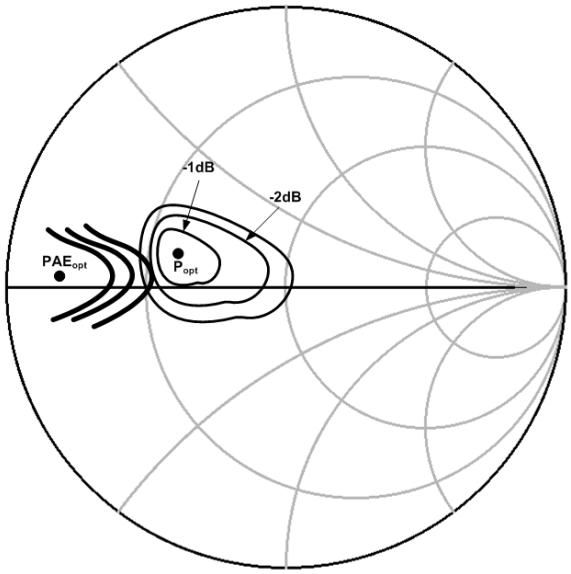


Fig. 2.9. Load-pull contours – delivered power contour and PAE contour.

2.2.3 Classes of Conventional Linear PA

There are four types of linear PA which are distinguished primarily with bias conditions. In class A type, the bias levels are chosen so that the output transistors can operate in the active region at all time, and it is clear that the transistors always dissipate power. The maximum drain efficiency of class A operation is 50 %. This is undoubtedly a theoretical number, since the variation of bias conditions, inevitable losses, and other non-ideal effects always exist. Class A PA provides good linearity but poor efficiency.

In class B type, the bias levels are chosen to shot off the output transistors half of every cycle. The product of the drain voltage and current of class B operation is not always positive, and the power dissipation would diminish in comparison with that of class A operation. The theoretical maximum drain efficiency is 78 %. Class B PA has worse linearity in exchange of better efficiency.

In class AB type, the bias levels are chosen so that the amplifier conducts between 50 % and 100 % cycle. Thus, class AB amplifier has better efficiency than class A amplifier, and better linearity than class B amplifier. Class AB operation can be considered as a compromise between class A and class B operation.

In class C type, the bias levels are chosen to make the output transistor conduct less than half cycle. As the conduction angle decreases to zero, the efficiency can achieve toward 100 %, but the gain and output power decrease to zero. Though the efficiency of class C amplifier is pretty high, the linearity is lost.

The difference among different types of PA is the bias point. Fig. 2.10 shows different bias points and their corresponding types of PA on MOS I-V curves. I_{max} represents the maximum output current of a transistor, V_{max} represents the maximum voltage drops across the drain and the source of the transistor, and V_{knee} represents the knee voltage of the transistor. The center point of the dashed line is the bias point of class A operation. The other bias points of class AB, class B, and class C are also shown, respectively.

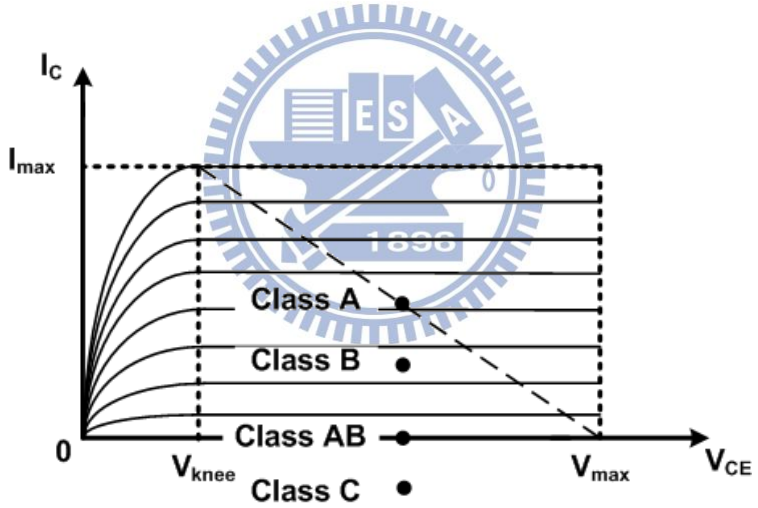


Fig. 2.10. Comparison among different bias points and there corresponding types of PA.

2.3 Conventional ESD Protection Design

2.3.1 Architecture of Conventional Whole-Chip ESD Protection Design

Fig. 2.11 shows a whole-chip ESD protection design which can provide effective ESD protection for CMOS ICs [2]. The typical design consists of a pair of ESD protection devices inserted beside the I/O pad and a power-rail ESD clamp circuit placed between the V_{DD} and

V_{SS} power lines. The pair of ESD protection devices is used to clamp ESD stress and provide ESD discharge paths among I/O pad and power lines. The power-rail ESD clamp circuit is used to clamp the V_{DD}-to-V_{SS} ESD stress and provide an ESD discharge path between V_{DD} and V_{SS} power lines.

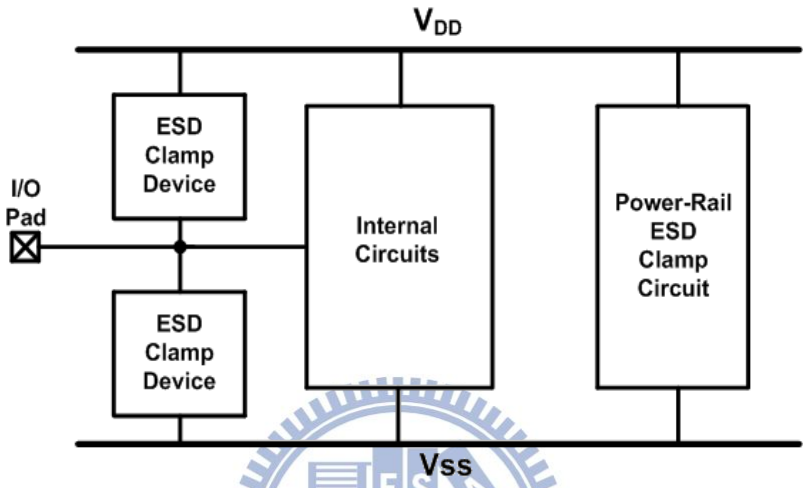


Fig. 2.11. Architecture of whole-chip ESD protection design.

2.3.2 Power-Rail ESD Clamp Circuit and I/O ESD Clamp Device

A typical power-rail ESD clamp circuit, which is shown in Fig. 2.12, consists of an ESD-transient detection circuit and an NMOS (M_{ESD}) used as a V_{DD}-to-V_{SS} ESD clamp device. The ESD-transient detection circuit is expected to detect ESD stress and then turn on the ESD clamp device to provide an ESD discharge path right after ESD events occur, while turn off the ESD clamp device under normal power-on conditions.

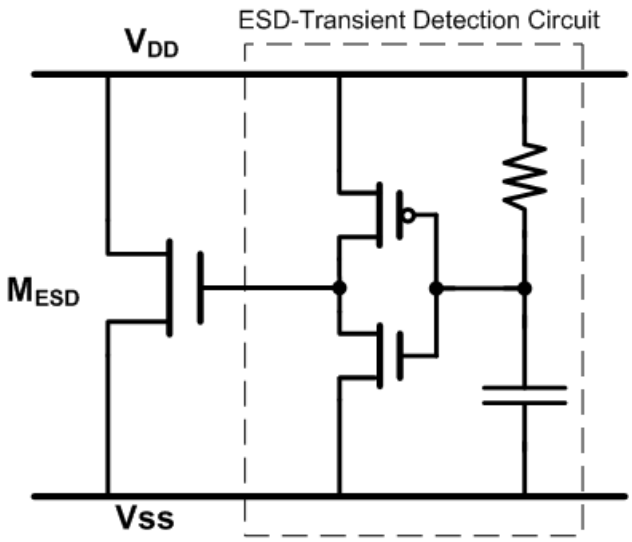


Fig. 2.12. Typical power-rail ESD clamp circuit.

A conventional ESD-transient detection circuit is an RC-detector. Since the pulse rise time of ESD events is on the order of nanosecond but that of the normal power-on events is on the order of millisecond. The RC time constant of the RC-detector should be designed to be on the order of microsecond, so the RC-detector is able to distinguish ESD events from normal power-on events.

M_{ESD} is used as a main ESD clamp device. It provides a low-impedance path for ESD current and clamps the ESD voltage between V_{DD} and V_{SS} power lines when it is triggered on by the ESD-transient detection circuit.

The pair of ESD protection devices inserted beside the I/O pad is expected to provide low-impedance ESD discharge paths among the I/O pad and power lines. A practical solution is a pair of diodes. Diode can endure a large amount of current with small device dimension. Furthermore, diode can clamp the voltage of I/O at about 0.7V when it is forward biased to discharge ESD current. The low clamping voltage is beneficial to protecting MOS devices used in the internal circuits from being damaged by ESD stress.

In conclusion, a typical and conventional whole-chip ESD protection design is shown in Fig. 2.13. Since this ESD protection design provides proper ESD discharge paths under every

ESD zapping mode, inclusive of positive-to-V_{DD} mode (PD-mode), positive-to-V_{SS} mode (PS-mode), negative-to-V_{DD} mode (ND-mode), negative-to-V_{SS} mode (NS-mode), V_{DD}-to-V_{SS} mode, and V_{SS}-to-V_{DD} mode, well ESD robustness is guaranteed. All the ESD discharge paths are shown in Fig. 2.14.

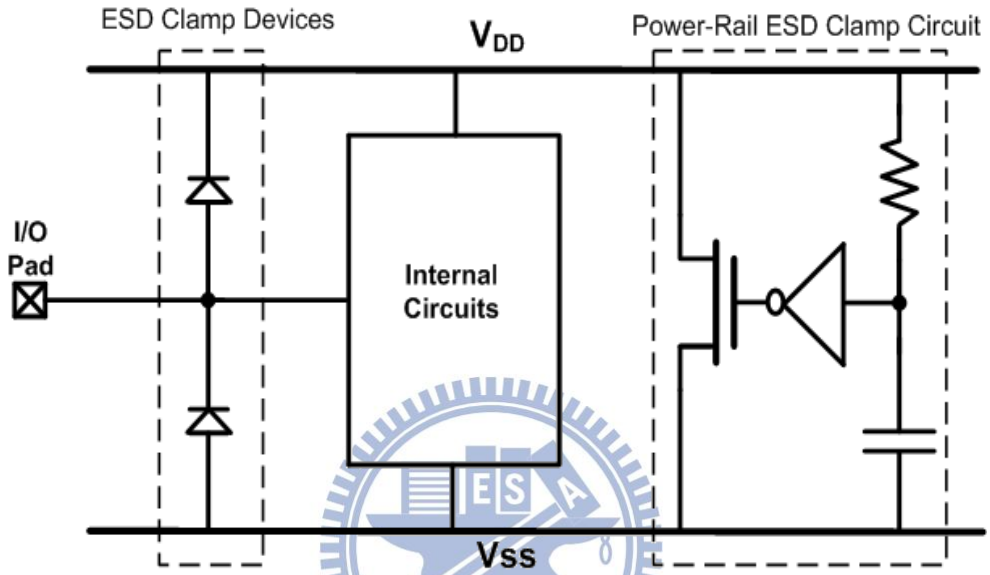
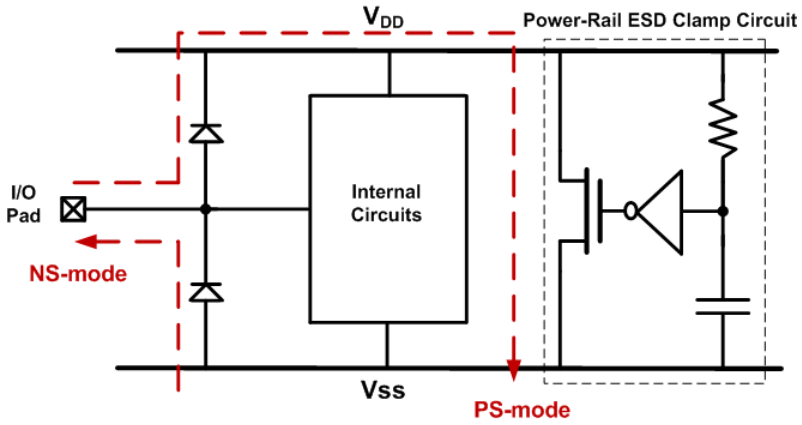
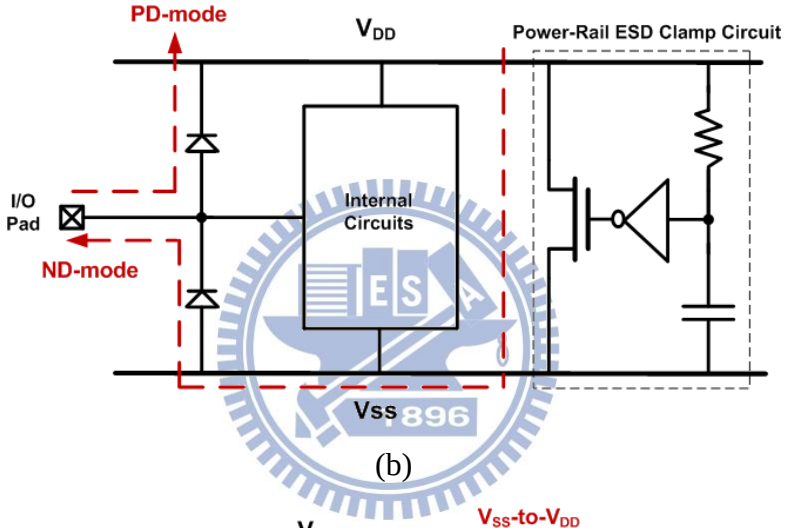


Fig. 2.13. Conventional whole-chip ESD protection design.



(a)



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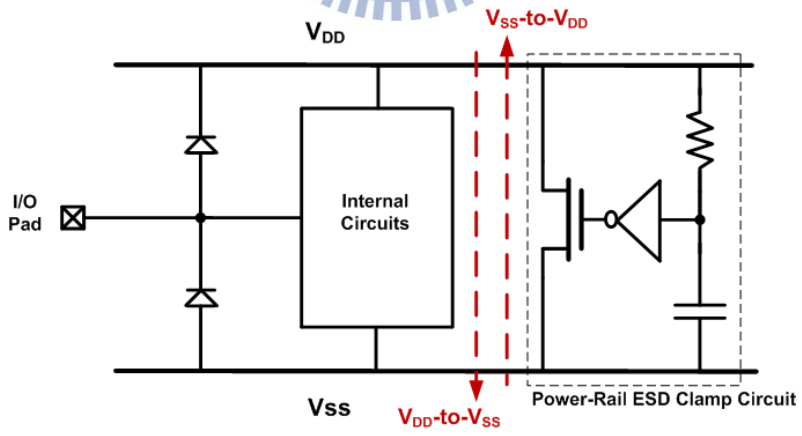


(c)

Fig. 2.14. ESD-discharge paths under (a) PS-mode and NS-mode, (b) PD-mode and ND-mode, and (c) V_{DD}-to-V_{SS} mode and V_{SS}-to-V_{DD} mode.

2.4 Issues of RF ESD Protection Design

2.4.1 Impacts of ESD Protection Design on RF Performance

The simple and effective ESD protection architecture in Fig. 2.13 would cause negative impacts while being applied to RF circuits. It is mainly because of the RF performance degradation caused by the parasitic capacitances of diodes.

To investigate the negative impacts caused by ESD protection diodes, some calculations with the concepts of S-parameters can help us. A conventional double-diode ESD protection design with a power-rail ESD clamp circuit for LNA is shown in Fig. 2.15.

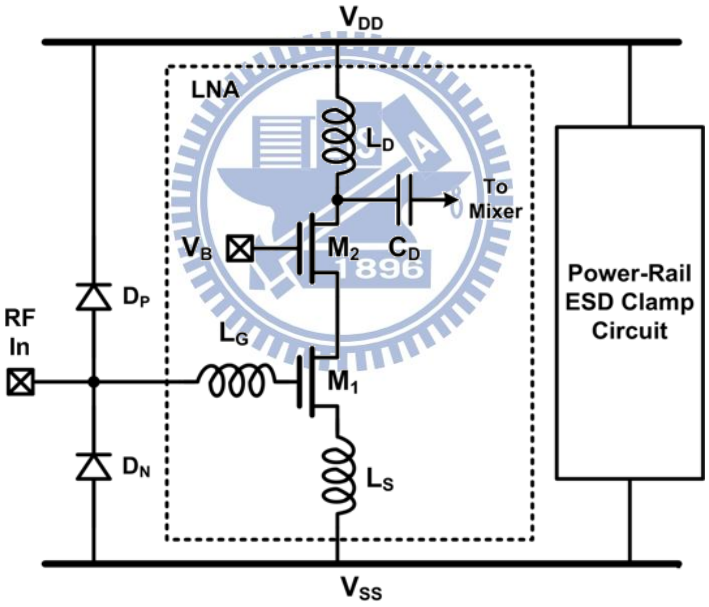


Fig. 2.15. Conventional ESD protection design with double diodes and a power-rail ESD clamp circuit for LNA.

In the circuit in Fig. 2.15, the parasitic effects of ESD protection diodes, D_P and D_N, cause RF performance degradation. Some equations can be calculated to describe the impact [9]. The insertion loss of ESD protection diodes can be expressed as

$$IL_{ESD} = \left|1 + \frac{Z_0}{2Z_{ESD}}\right| = \left|\frac{1}{S_{21,\,ESD}}\right| \tag{2.20}$$

where Z_0 is the 50-Ω normalization impedance, and Z_{ESD} is the parasitic impedance of ESD protection diodes at the input node. Using the expression in dB, the insertion loss (IL_{ESD}) is equal to the absolute value of S_{21} parameter ($S_{21,\,ESD}$).

The power gain of an RF LNA with ESD protection devices can be calculated from its schematic circuit diagram, as shown in Fig. 2.16. A simple expression of the input impedance (Z_{in}, LNA) of LNA at resonance is [12]

$$Z_{in,\,LNA} = s(L_s + L_g) + \frac{1}{sC_{gs}} + (\frac{gm}{C_{gs}})L_s \approx \omega_T L_s = Z_0 \tag{2.21}$$

where ω_T is the unity-gain frequency of the MOS transistor. The overall input impedance (Z_{in}) of the LNA with ESD protection diodes is

$$Z_{in} = Z_{ESD} // Z_{in,\,LNA} \approx Z_{ESD} // Z_0 \tag{2.22}$$

Therefore, the overall transconductance (G_m) of the LNA is

$$G_m = \frac{Z_{ESD}}{Z_{ESD} + Z_0} \frac{\omega_T}{s(Z_0 + Z_{in})} = \frac{\omega_T}{sZ_0} \frac{1}{2 + \frac{Z_0}{Z_{ESD}}} \tag{2.23}$$

The transducer power gain of the LNA can also be calculated. In order to simplify the calculation, the feedback capacitor C_{gd} of the MOS transistor was neglected first, and the input and output were assumed to be conjugately matched. The transducer power gain (G_T) is

$$G_T = \frac{P_L}{P_{avs}} = \frac{\frac{1}{8}\left|V_s G_m\right|^2 \left(R_o // Z_0\right)}{\frac{1}{8}\frac{\left|V_s\right|^2}{Z_0}} = \frac{\omega_T^2 \left(R_o // Z_0\right)}{4\omega_0^2 Z_0 IL_{ESD}^{\ 2}} \tag{2.24}$$

where P_L is the average power delivered to the load, P_{avs} is the average power available from the source, R_o is the output impedance of the cascoded NMOS transistors, and ω_0 is the operating frequency of input RF signal.

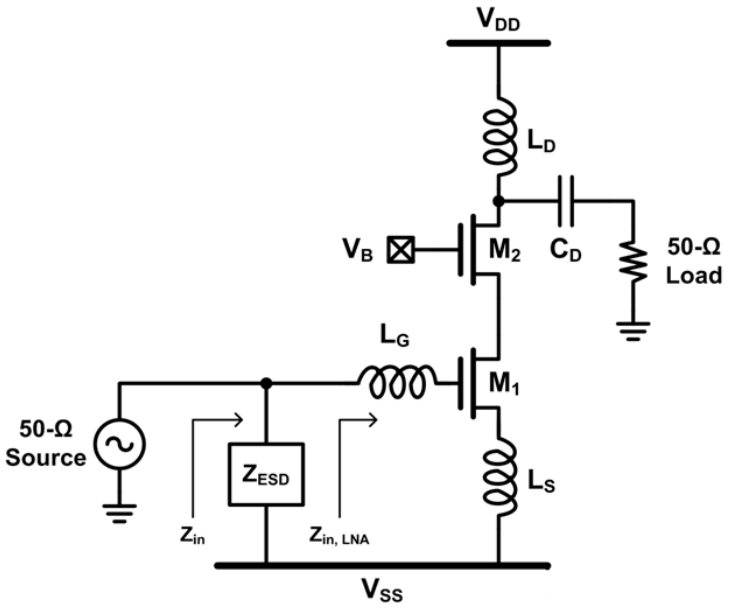


Fig. 2.16. LNA with parasitic impedance of input pad and ESD protection diodes for calculating the power gain.

The calculations demonstrate the disadvantages to the transducer power gain of LNA. It is caused by the insertion loss of ESD protection diodes. If the parasitic impedance of ESD protection diodes (Z_{ESD}) can be increased to infinite, the transducer power gain of LNA in Fig. 2.16 would converge to that of an LNA without any ESD protection diode. Therefore, ESD protection device with high parasitic impedance, namely, low insertion loss, is needed for RF ESD protection.

2.4.2 Challenges of RF ESD Protection Design

Once the parasitic impedance of ESD protection diodes can be increased, the degradation of RF performance of LNA would be improved. Reducing the device dimensions of ESD protection diodes can increase (decrease) the parasitic impedance (capacitance). Hence, the RF performance degradation caused by ESD protection diodes would be reduced. Unfortunately, such demand is on the opposite side of the demand of ESD robustness. The device dimensions of ESD protection diodes cannot be shrunk unlimitedly in consideration of

ESD robustness. Moreover, the Z_{ESD} will further decrease as the operating frequency of RF circuits increases. Designing an effective ESD protection design for RF circuits operating in higher frequency with minimum RF performance degradation is a terrible dilemma.

2.4.3 Conventional RF ESD protection designs

To overcome these problems, many RF ESD protection designs have been developed. One method is trying to cancel or isolate the parasitic capacitances from RF circuits, such as "ESD cancellation" and "ESD isolation"; other method is trying to fundamentally reduce the parasitic capacitances of ESD protection devices in order to minimize the influence on RF performance [13] [14]. Some of these methods will be briefly introduced in this section.

"ESD isolation" is a method to protect RF circuits under ESD events, and "isolate" the parasitic capacitances of ESD protection devices from RF circuits under normal operating conditions. Well designed "ESD isolation" can provide enough ESD robustness without serious RF performance degradation. An example is using LC-tanks, as shown in Fig. 2.17 [6]. The impedance of LC-tank is infinite when LC-tank operates at its resonant frequency. For this reason, the pair of LC-tanks can be designed to resonate at the operating frequency of the internal RF circuit, and the RF input port will see infinite impedance through ESD clamp devices with the LC-tank, ideally. Therefore, the parasitic effects of ESD protection devices would not influence the RF circuit under normal operating conditions. The resonant frequency of LC-tanks is

$$\omega_0 = \frac{1}{\sqrt{L_P C_P}} = \frac{1}{\sqrt{L_N C_N}} \tag{2.25}$$

The inductances and capacitances of LC-tanks can be chosen with (2.25).

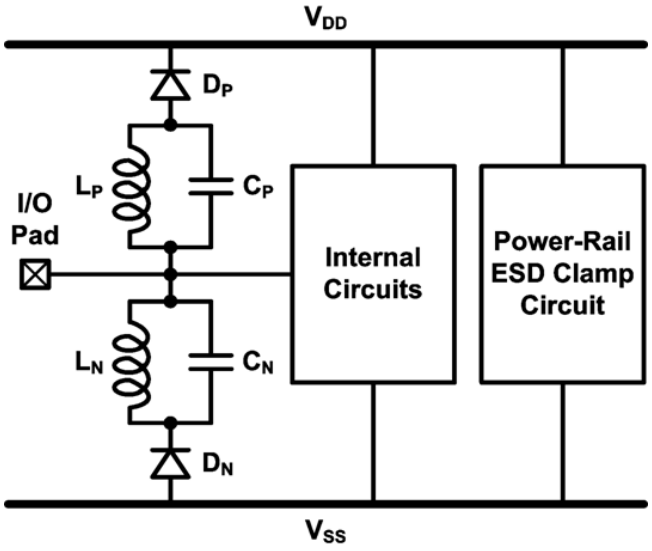


Fig. 2.17. ESD protection design with LC-tanks for RF circuits.

Another method is using series inductor and diode as ESD protection device, as shown in Fig. 2.18 [5]. The diode can be considered as a capacitor because of its parasitic effect. The impedance of the series inductor and diode is extremely small when the two devices operate at their resonant frequency, but extremely high when the two devices operate at frequencies above the resonant frequency. The resonant frequency of the series inductor and capacitor is the same as (2.9). Choose the resonant frequency of the series inductor and diode far away from the operating frequency of the RF circuit, and therefore the RF input port can see infinite impedance through the series inductor and diode under normal operating conditions. Thus, the parasitic effects of ESD protection devices would not influence the RF circuit. Of course, the diode serves the same function as an ESD clamp device does.

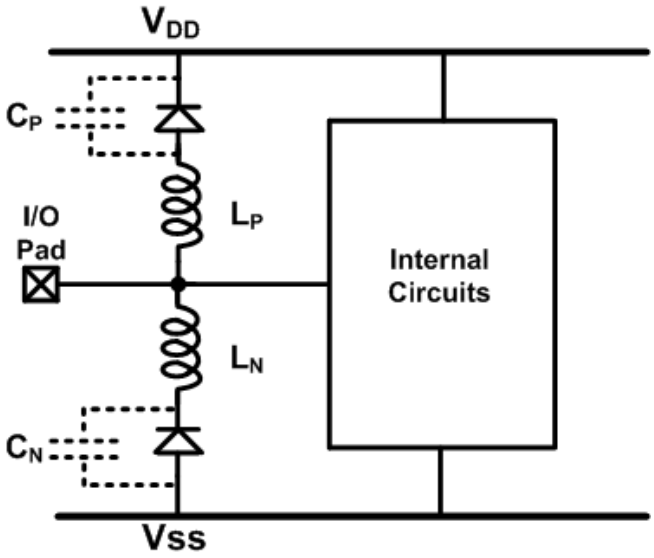


Fig. 2.18. ESD protection design with series diodes and inductors for RF circuits.

"ESD cancellation" is a method to turn ESD protection devices into a part of RF circuit so as to "cancel" the parasitic capacitances introduced by ESD protection devices.

A commonly used method is considering ESD protection devices as parts of matching network [15]. If an ESD protection device is simply added in front of an RF circuit, the parasitic capacitance of the ESD protection device might change the input matching condition. Merging the ESD protection device into the input matching network can minimize the influence. Fig. 2.19 shows this method. $C_{P,ESD}$ is the parasitic capacitance of an ESD protection device which changes the input matching condition. By adding extra capacitor C_C and inductor L_G, the input impedance of the internal RF circuit can be changed from Zi_1 to Zi_2 of 50Ω. Hiding ESD protection devices in input matching network can cancel the RF performance degradation caused by the parasitic capacitance of ESD protection devices.

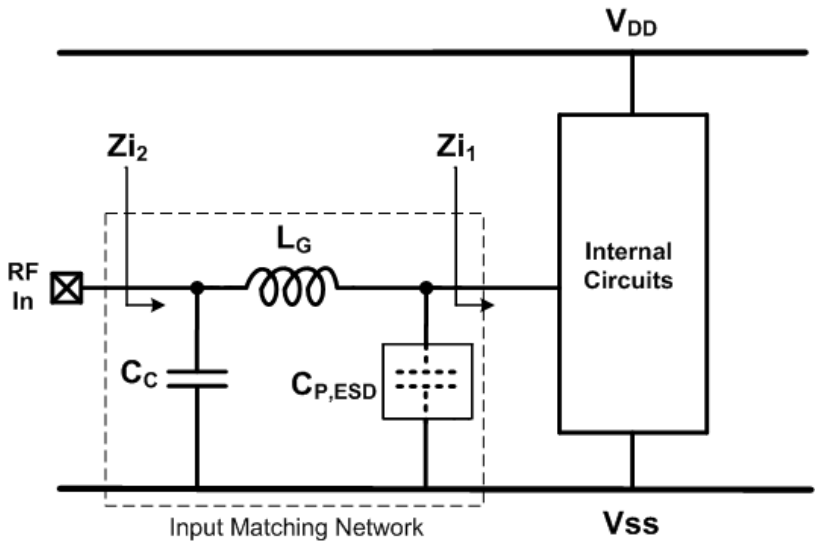


Fig. 2.19. Input matching co-design of RF circuits with ESD protection devices.

In addition, this method can be extended to broadband RF applications [16], as shown in Fig. 2.20. The ESD protection devices, which are diodes here, are allocated with decreasing size from the I/O pad to the internal RF circuit. The ESD protection devices are divided into several small devices rather than one large device for broad-band RF performance. For ESD robustness, dividing the ESD protection devices into decreasing size is better than dividing them into equal size, since a larger ESD protection device inserted right beside the I/O pad is beneficial to providing a high-current-tolerant ESD discharge path under ESD events. Z_0 represents the impedance of transmission lines, coplanar waveguides, or inductors which are used to do input matching. This architecture successfully combines ESD protection devices with input matching network, and it can provide enough ESD robustness without serious RF performance degradation.

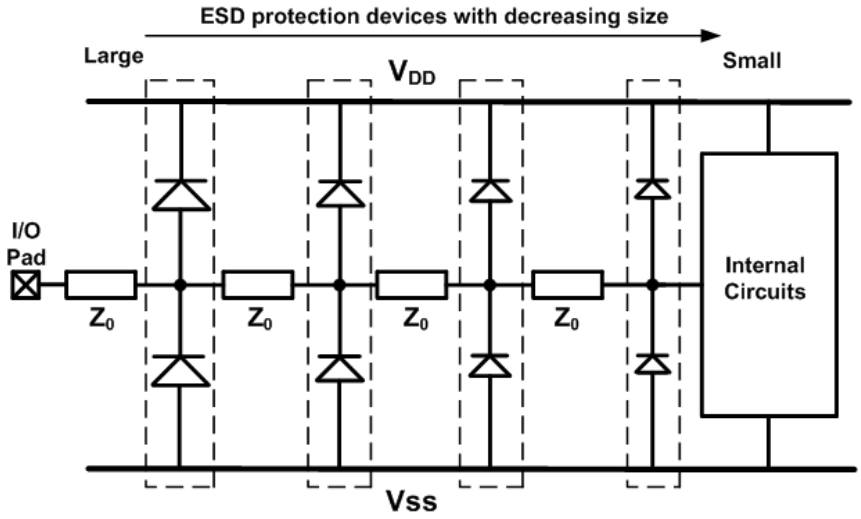
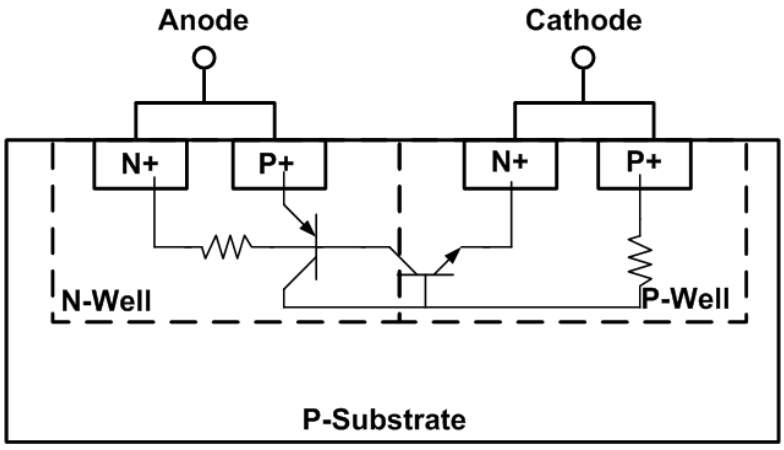


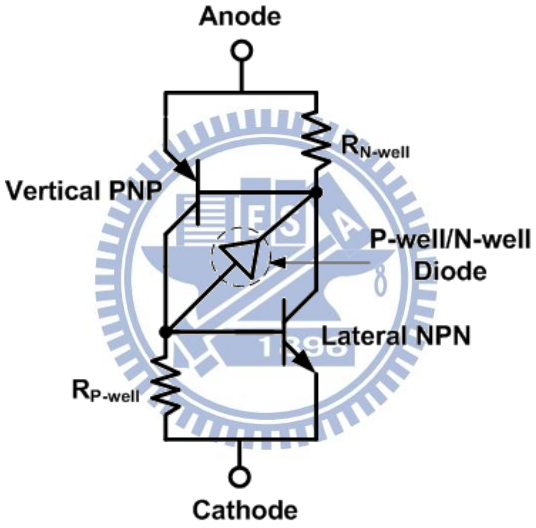
Fig. 2.20. ESD protection devices with decreasing size for broad-band RF circuits.

The methods mentioned above are a little complex to RF circuit designers since ESD protection circuits have to be co-designed with RF circuits. Considering ESD protection designs throughout RF design phase needs more effort. Therefore, a more straightforward direction is to fundamentally decrease the parasitic capacitances of ESD protection devices. RF designers can therefore easily add low-C ESD protection devices to RF circuits without complex co-design methodology. To meet these requirements, silicon-controlled rectifier (SCR) can serve. With well ESD robustness within a small layout area and lower parasitic capacitance, SCR is useful to RF ESD protection design [8].

Fig. 2.21 shows the cross-section view and the equivalent circuit of a typical SCR. The SCR structure consists of P-plus (P+) diffusion, N-well, P-well, and N-plus (N+) diffusion, as shown in Fig. 2.21 (a). This four-layer structure can be regarded as a two-terminal device consists of a lateral NPN and a vertical PNP bipolar transistor, as shown in Fig. 2.21 (b).



(a)



(b)

Fig. 2.21. The (a) cross-section view and (b) equivalent circuit of a typical SCR.

The DC I–V characteristics of SCR under ESD stress is shown in Fig. 2.22. Assume that positive ESD stress is applied to the anode of SCR and its cathode is relatively grounded. At the beginning, the voltage applied to the anode is less than the breakdown voltage of the N-well/P-well junction, so SCR acts like an open circuit. When the voltage applied to the anode is greater than the breakdown voltage, avalanche breakdown mechanism starts to work. Hole current flows through the P-well to the P+ diffusion connected to ground, and

meanwhile electron current flows through the N-well to the N+ diffusion connected to the anode. Once the voltage drops across the P-well resistor ($R_{P\text{-well}}$) (N-well resistor ($R_{N\text{-well}}$)) is larger than 0.7 V, the parasitic NPN (PNP) transistor will be turned on. Furthermore, the parasitic NPN (PNP) transistor injects electron (hole) current to bias the PNP (NPN) transistor, and then the positive-feedback regenerative mechanism helps SCR to be successfully triggered into its latching state and have a low holding voltage (V_{hold}) ~1.5 V.

Next, assume that negative ESD stress is applied to the anode of SCR and its cathode is relatively grounded. This negative voltage drops across the parasitic diode, which consists of the P-well/N-well junction, in SCR. As long as the parasitic diode is forward biased, ESD current can be discharged and the negative voltage will be clamped at the low cut-in voltage of the parasitic diode.

SCR provides suitable ESD discharging ability under every ESD stress condition, as described above. It can provide high ESD protection level within a small layout area. A smaller layout area introduces less parasitic capacitance, and therefore is beneficial to RF ESD protection.

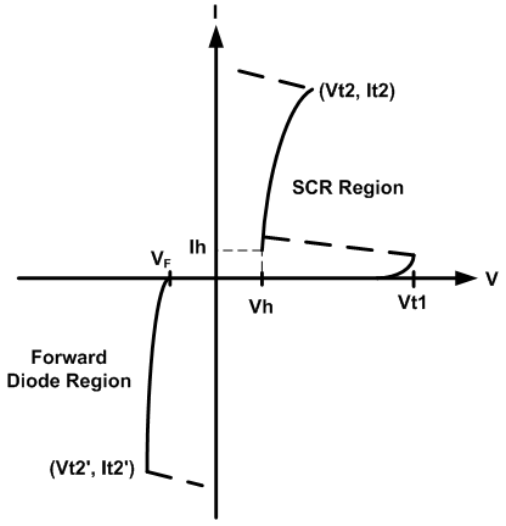


Fig. 2.22. I–V characteristics of SCR device under positive and negative voltage biases.

Chapter 3

ESD Protection Design for 60 GHz RF Circuits

3.1 Challenges of ESD Protection Design for 60 GHz RF Circuits

To design an ESD protection design for 60 GHz RF Circuits, a crucial problem needs to be concerned. The impedance of an ESD protection device can be expressed as

$$Z_{ESD} = \frac{1}{sC_{ESD}} \tag{3.1}$$

The higher the operating frequency is, the lower the impedance of ESD protection device is. Low impedance causes large signal loss, and therefore causes serious RF performance degradation. Since the operating frequency of 60 GHz RF circuits is pretty high, the parasitic capacitance of ESD protection device needs to be extremely suppressed. However, extremely suppressing the parasitic capacitances of ESD protection devices such as SCR to fit the requirement of 60 GHz RF circuits is difficult. Thus, low-C ESD protection device may not be a good option.

ESD isolation would be a proper method, since the limitation of the parasitic capacitance of ESD protection device is not that tough, and it would not increase the design complexity of RF circuits. Nevertheless, the drawback of the ESD isolation method shown in Fig. 2.17 is its high clamping voltage. The clamping voltage of the ESD protection design under ESD stress conditions is the sum of the clamping voltages of LC-tank and ESD protection diode. It is better to lower the clamping voltage so as to enhance its ESD protection ability.

3.2 Architecture of The Proposed ESD Protection Designs

Fig. 3.1 shows the circuit of one proposed ESD protection design for 60 GHz RF circuits. The ESD protection design A, which consists of a pair of ESD protection diodes (D_P and D_N), a series inductor and capacitor (L_N and C_N), and a supplement capacitor (C_S), is placed beside the I/O pad. The diodes provide ESD discharge paths from the input pad to V_{DD} / V_{SS}. In addition, a power-rail ESD clamp circuit is placed between V_{DD} and V_{SS} power lines so as to provide a discharge path between V_{DD} and V_{SS}.

The inductor in series with the capacitor can block the dc leakage path from input pad to V_{SS} under normal operating conditions. The equivalent inductance of the series inductor and capacitor (L_{eq}) can be expressed as

$$L_{eq} = L_N - \frac{1}{\omega^2 C_N} \tag{3.2}$$

L_{eq} can be used to eliminate the parasitic capacitance of ESD protection diodes (C_{Diodes}) at the operating frequency of the RF circuit by careful design. The resonant frequency of the parallel L_{eq} and C_{Diodes} is designed to be equal to the operating frequency of the RF circuit. Under this condition, the RF input port will see a large impedance from the ESD protection circuit (Z_{ESD}), where the parasitic capacitance (C_{Diodes}) has been eliminated, and the parasitic resistance (R_{Diodes}) remains large.

The resonant frequency of parallel L_{eq} and C_{Diodes} can be calculated by

$$\omega_0 = \frac{1}{\sqrt{L_{eq} C_{Diodes}}} \tag{3.3}$$

From Eq. (3.2) and (3.3), another equation is obtained as

$$\omega_0^2 L_N - \frac{1}{C_N} = \frac{1}{C_{Diodes}} \tag{3.4}$$

If the operating frequency of the RF circuit and the device dimensions of ESD diodes are

determined, (3.4) can be used to find the required inductance and capacitance. Besides, the resonant frequency of the series inductor and capacitor should be far away from the operating frequency, since the impedance would be extremely small at its resonant frequency. The resonant frequency of L_N and C_N (ω_{Series}) can be calculated as

$$\omega_{Series} = \frac{1}{\sqrt{L_N C_N}} \tag{3.5}$$

To investigate the ESD robustness of ESD protection designs with different sizes of ESD protection diodes, several splits with D_N and D_P in different sizes are studied. Since the C_{Diodes} varies with the size of ESD protection diode, a supplement capacitor (C_S) is added between RF input and V_{SS} to keep the total capacitance of C_{Diodes} and C_S. Therefore, the sizes of L_N and C_N can maintain the same, and the layout area can also maintain the same. Consider C_{Diodes} and C_S as one capacitor, and (3.4) turns out to be

$$\omega_0^2 L_N - \frac{1}{C_N} = \frac{1}{C_{ESD}} \tag{3.6}$$

where C_{ESD} is

$$C_{ESD} = C_{Diodes} + C_S \tag{3.7}$$

The power-rail ESD clamp circuit consists of an RC-detector, a CMOS inverter, and an RC-inverter-triggered NMOS. The RC-detector is designed to distinguish ESD transients from normal operating conditions. The R_1 (~10 kΩ) and C_1 (~10 pF) with time constant of 0.1 μs ~ 1 μs can meet such requirement, since the rise time of turn-on events are on the order of millisecond whereas that of ESD events are on the order of nanosecond. The NMOS (M_{ESD}) with ~2000-μm width is used as an ESD clamp device.

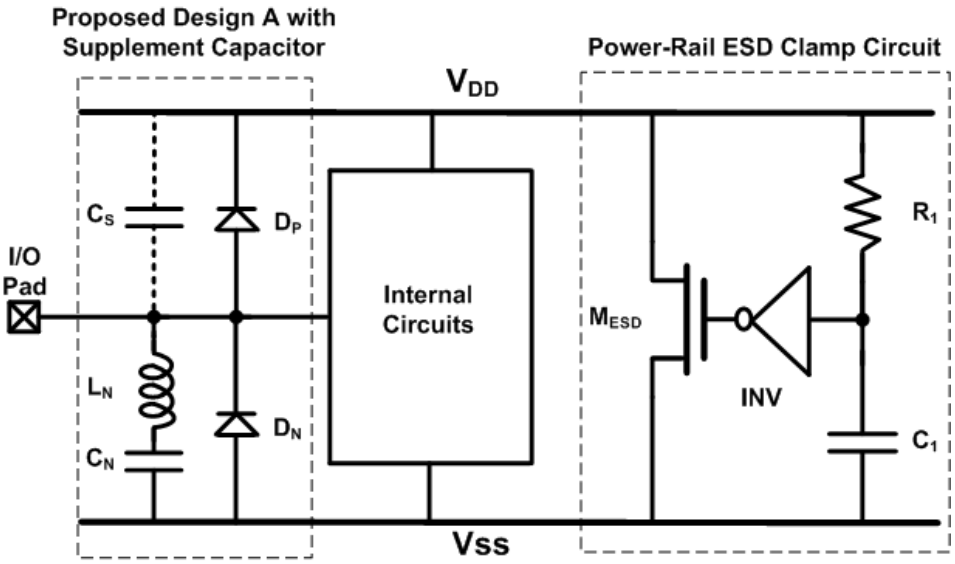


Fig. 3.1. Proposed ESD protection design A with supplement capacitor and power-rail ESD clamp circuit.

Another proposed ESD protection design is shown in Fig. 3.2. The ESD protection design B also consists of a pair of ESD protection diodes (D_P and D_N), but the series inductor and capacitor (L_P and C_P) are placed between RF input and V_{DD}. The operation of design B is similar to design A, and the design parameters can be calculated with (3.2) by replacing the L_N by L_P.

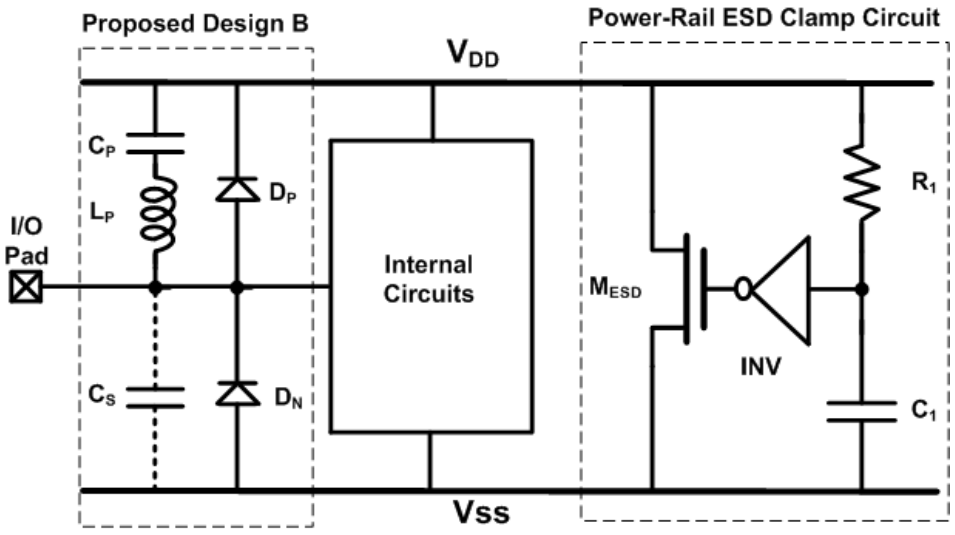


Fig. 3.2. Proposed ESD protection design B and power-rail ESD clamp circuit.

3.3 ESD Discharge Paths of the Proposed ESD Protection Designs

With this architecture, proper ESD discharge paths under every ESD zapping mode are guaranteed. For PS-mode, the ESD current first goes through D_P, and then it is discharged through the power-rail ESD clamp circuit. For PD-mode, the ESD current is discharged through D_P. For NS-mode, the ESD current is discharged through D_N. For ND-mode, the ESD current is first shunted from V_{DD} to V_{SS} through the power-rail ESD clamp circuit and then discharged through D_N. For V_{DD}-to-V_{SS} and V_{SS}-to-V_{DD} mode, the power-rail ESD clamp circuit can provide ESD discharge paths. All the ESD discharge paths are shown in Figs. 3.3 to 3.7. The proposed designs A and B have the same ESD discharge paths.

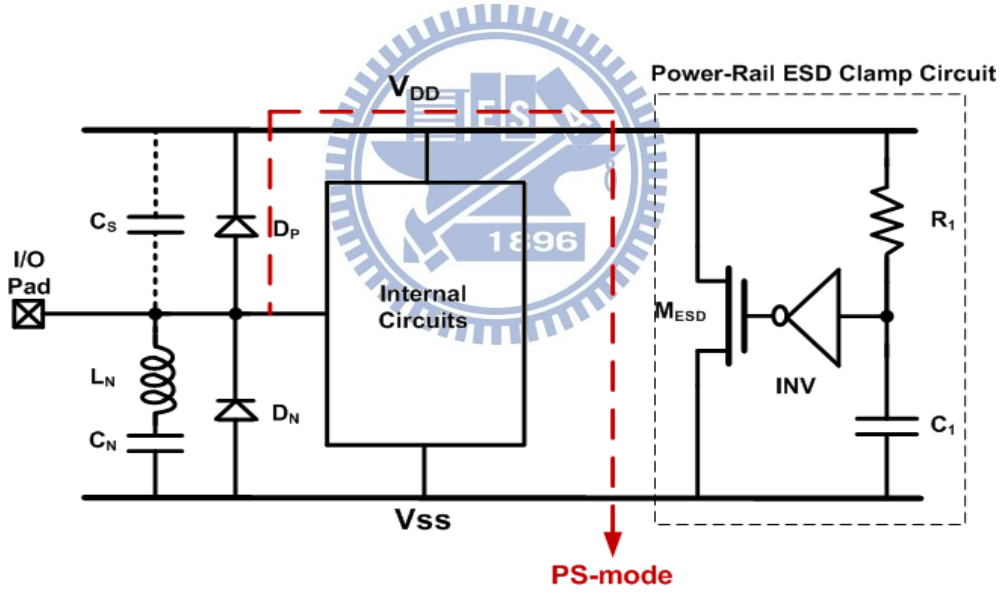


Fig. 3.3. ESD discharge path of the proposed design A under PS-mode.

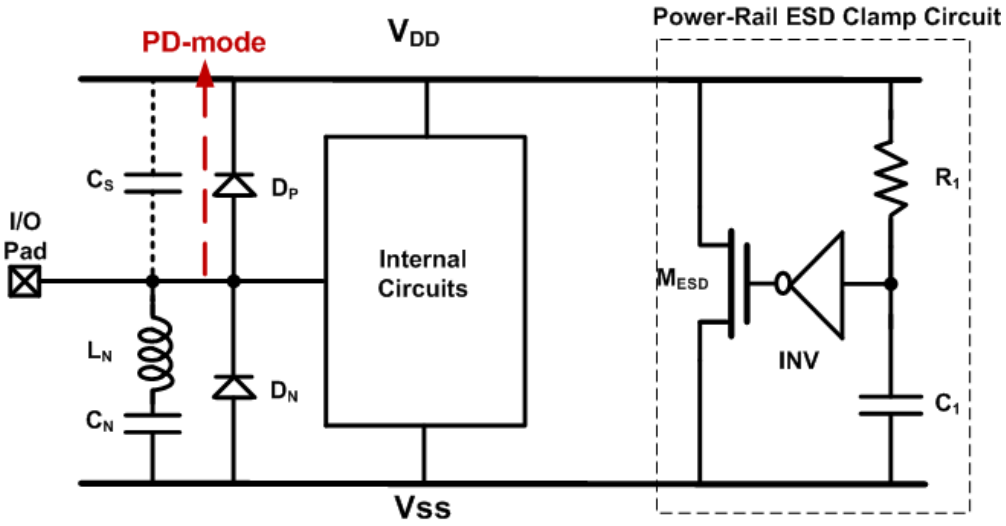


Fig. 3.4. ESD discharge path of the proposed design A under PD-mode.

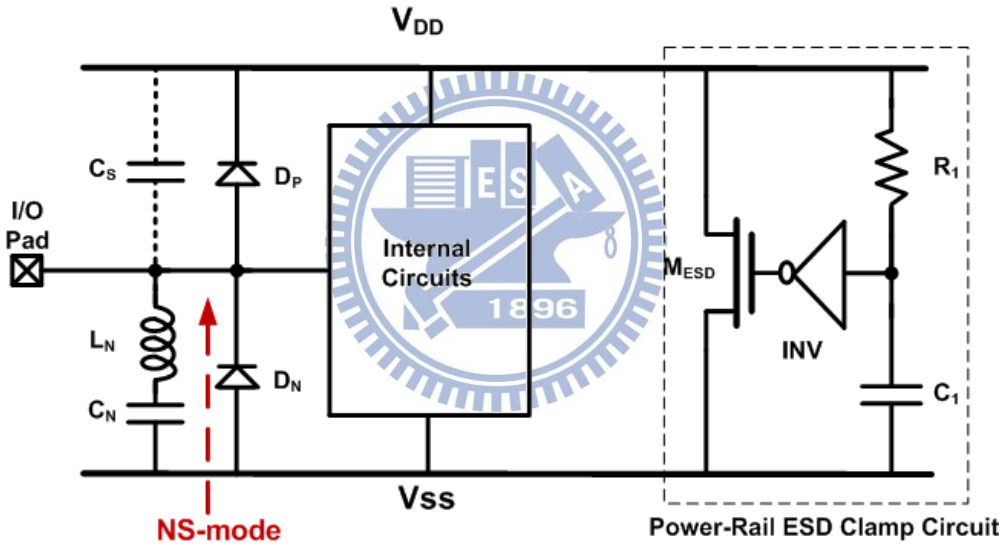


Fig. 3.5. ESD discharge path of the proposed design A under NS-mode.

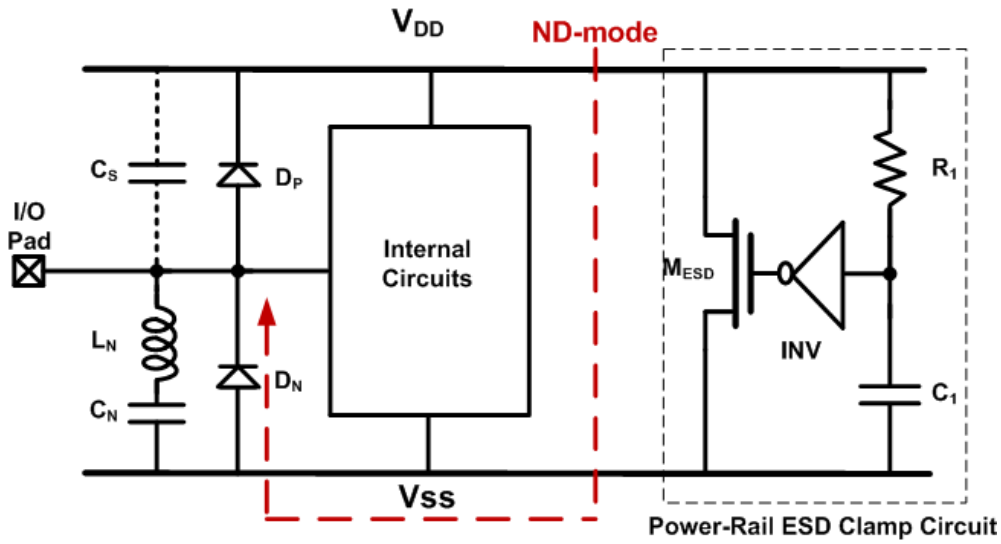


Fig. 3.6. ESD discharge path of the proposed design A under ND-mode.

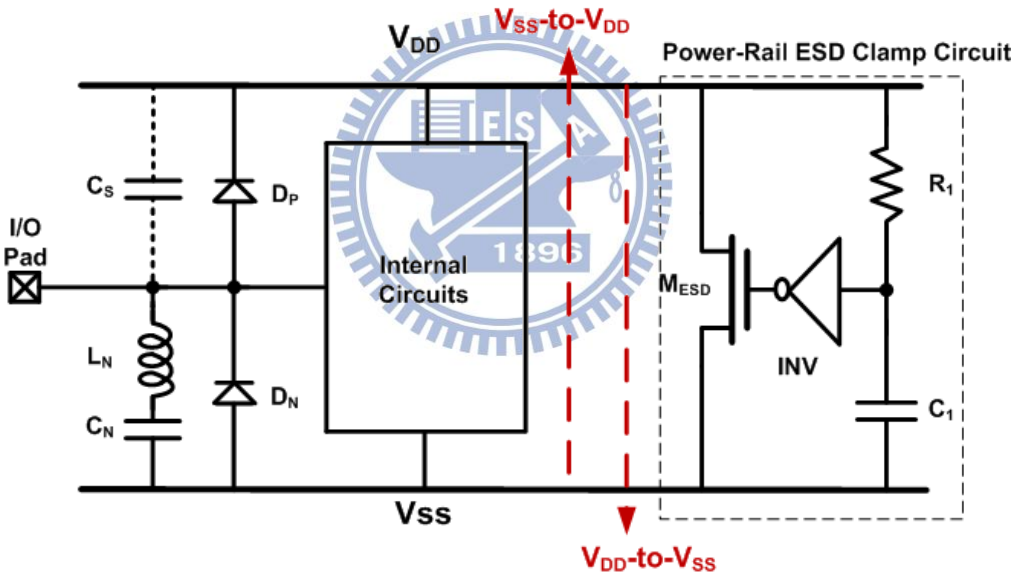


Fig. 3.7. ESD discharge path of the proposed design A under V_{DD}-to-V_{SS} and V_{SS}-to-V_{DD} mode.

Since the ESD current is discharged through only one diode from I/O pad to power lines, the clamping voltage under ESD stress conditions is lower than that of the structure shown in Fig. 2.17. It is beneficial to its ESD protection ability.

3.4 Simulation Results

The proposed designs are simulated by using ideal lumped devices. A 0.11-nH inductor and a 300-fF capacitor are used as the series inductor (L_N) and capacitor (C_N). The diodes D_N and D_P are simplified to an ideal capacitor model, C_{Diodes}. The sum of C_{Diodes} and C_S, that is, C_{ESD} in (3.6), is chosen as an 80-fF capacitor. Since ideal devices are used, the proposed designs A and B have the same simulation results. The simulated S_{21} parameter ($S_{21,\,ESD}$) of the proposed design is shown in Fig. 3.8. The S_{21} value at 60 GHz can be designed to be 0 dB, which means that insertion loss from ESD protection circuit is also 0 dB.

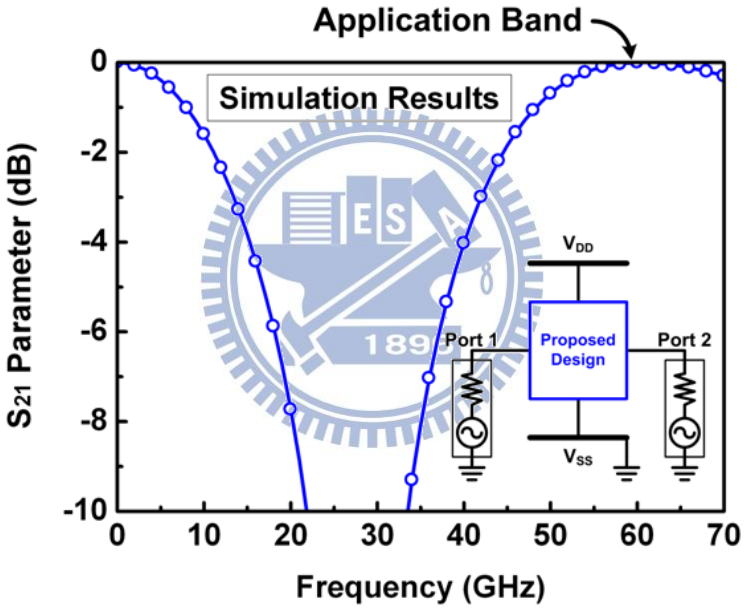


Fig. 3.8. Simulated S_{21} parameter of the proposed design.

3.5 Experimental Results

3.5.1 Test Circuits

Increasing device sizes of ESD protection diodes provides better ESD robustness but worse RF performance, and decreasing device sizes of ESD protection diodes makes opposite results. In order to find a well balance between ESD robustness and RF performance, both

designs are split into 4 test circuits with different sizes of ESD protection diodes. The test circuits of the proposed ESD protection designs have been fabricated in a 65-nm CMOS process. All device sizes are listed in Table 3.1. The width of D_P or D_N in test circuits A1 (B1), A2 (B2), A3 (B3), and A4 (B4) are 8 μm, 15 μm, 23 μm, and 30 μm, respectively, while the length of D_P or D_N are kept at 0.6 μm. The $C_{Diodeds}$ of test circuits A1 (B1), A2 (B2), A3 (B3), and A4 (B4) are 21 fF, 40 fF, 61 fF, and 80 fF, respectively. The L_N and L_P are chosen as 0.11 nH for designs A and B, and the C_N and C_P are designed as 300 fF. Besides, the C_S with 60 fF, 40 fF, and 20 fF are added to the test circuits A1 (B1), A2 (B2), and A3 (B3), respectively. To facilitate the on-wafer RF measurement, these test circuits are arranged with G-S-G style in layout. Part of the layout top view of the test circuit A4 is shown in Fig. 3.9. In other splits, C_S was added beside D_N. Every test circuit has the same layout area, 130×100 μm^2, as A4 does, since almost the same components are used in every test circuit.

Table 3.1
Device Parameters of Proposed ESD Protection Designs

Test Circuit	**Proposed Design A**				**Proposed Design B**			
	A1	**A2**	**A3**	**A4**	**B1**	**B2**	**B3**	**B4**
L_P	N/A	N/A	N/A	N/A	0.11 nH	0.11 nH	0.11 nH	0.11 nH
C_P	N/A	N/A	N/A	N/A	300 fF	300 fF	300 fF	300 fF
D_P	8 μm × 0.6 μm (9 fF)	15 μm × 0.6 μm (18 fF)	23 μm × 0.6 μm (27 fF)	30 μm × 0.6 μm (36 fF)	8 μm × 0.6 μm (9 fF)	15 μm × 0.6 μm (18 fF)	23 μm × 0.6 μm (27 fF)	30 μm × 0.6 μm (36 fF)
L_N	0.11 nH	0.11 nH	0.11 nH	0.11 nH	N/A	N/A	N/A	N/A
C_N	300 fF	300 fF	300 fF	300 fF	N/A	N/A	N/A	N/A
D_N	8 μm × 0.6 μm (12 fF)	15 μm × 0.6 μm (22 fF)	23 μm × 0.6 μm (34 fF)	30 μm × 0.6 μm (44 fF)	8 μm × 0.6 μm (12 fF)	15 μm × 0.6 μm (22 fF)	23 μm × 0.6 μm (34 fF)	30 μm × 0.6 μm (44 fF)
C_S	60 fF	40 fF	20 fF	N/A	60 fF	40 fF	20 fF	N/A

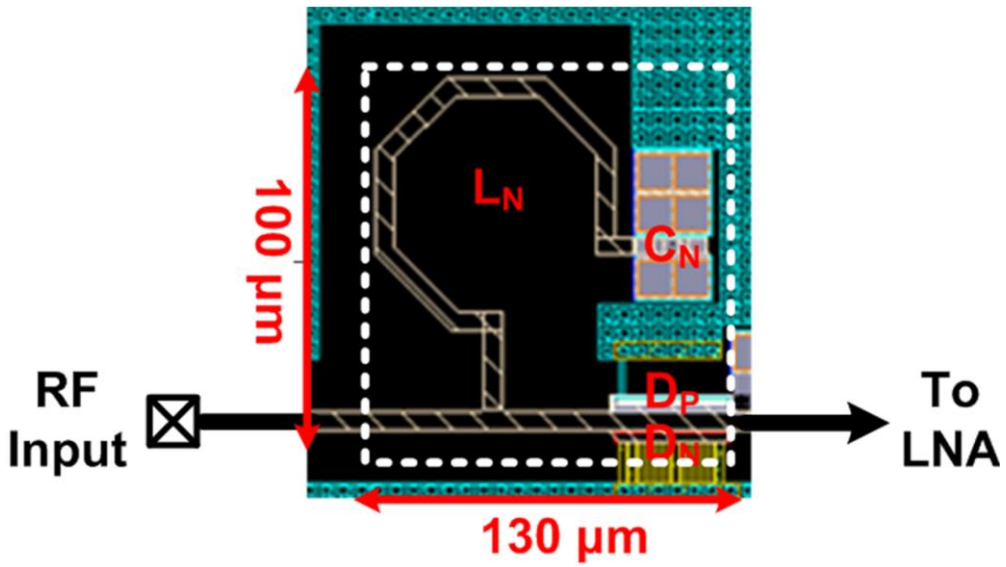


Fig. 3.9. Layout top view of the test circuit A4.

3.5.2 Measured RF Performance

The two-port S-parameters of the test circuits from 0 to 67 GHz were measured by using the vector network analyzer. During the S-parameter measurement, the port 1 and port 2 were biased at 0.5 V, which is $V_{DD}/2$ in the given 65-nm CMOS process. The dc bias of 1-V V_{DD} was also supplied to the test circuits. In order to extract the intrinsic characteristics of the test circuits in high frequencies, the parasitic effects of the G-S-G pads had been removed by using the de-embedding technique [17]. The source and load resistances to the test circuits were kept at 50 Ω.

The measured S_{21} parameters of the test circuits are shown in Figs. 3.10 and 3.11. For the proposed design A, the test circuits A1, A2, A3, and A4 have about 1.3-dB, 1.4-dB, 1.6-dB, and 1.8-dB insertion loss, respectively, at 60-GHz. For the proposed design B, the test circuits B1, B2, B3, and B4 have about 1.4-dB, 1.6-dB, 2.0-dB, and 2.3-dB insertion loss, respectively, at 60 GHz. Since the diodes used in simulation are simplified to ideal equivalent capacitor models rather than real diode models, the measured signal loss were larger than the simulated signal loss. The insertion loss of the proposed design B seems a little bit larger than the proposed design A. This is perhaps because of the more complex metal routing in layout. The

noise figures are also measured at 60 GHz. For design A, the test circuits A1, A2, A3, and A4 have 0.9-dB, 1.2-dB, 1.6-dB, and 2-dB noise figures, respectively. For design B, the test circuits B1, B2, B3, and B4 have 0.9-dB, 1.3-dB, 1.7-dB, and 2.2-dB noise figures, respectively.

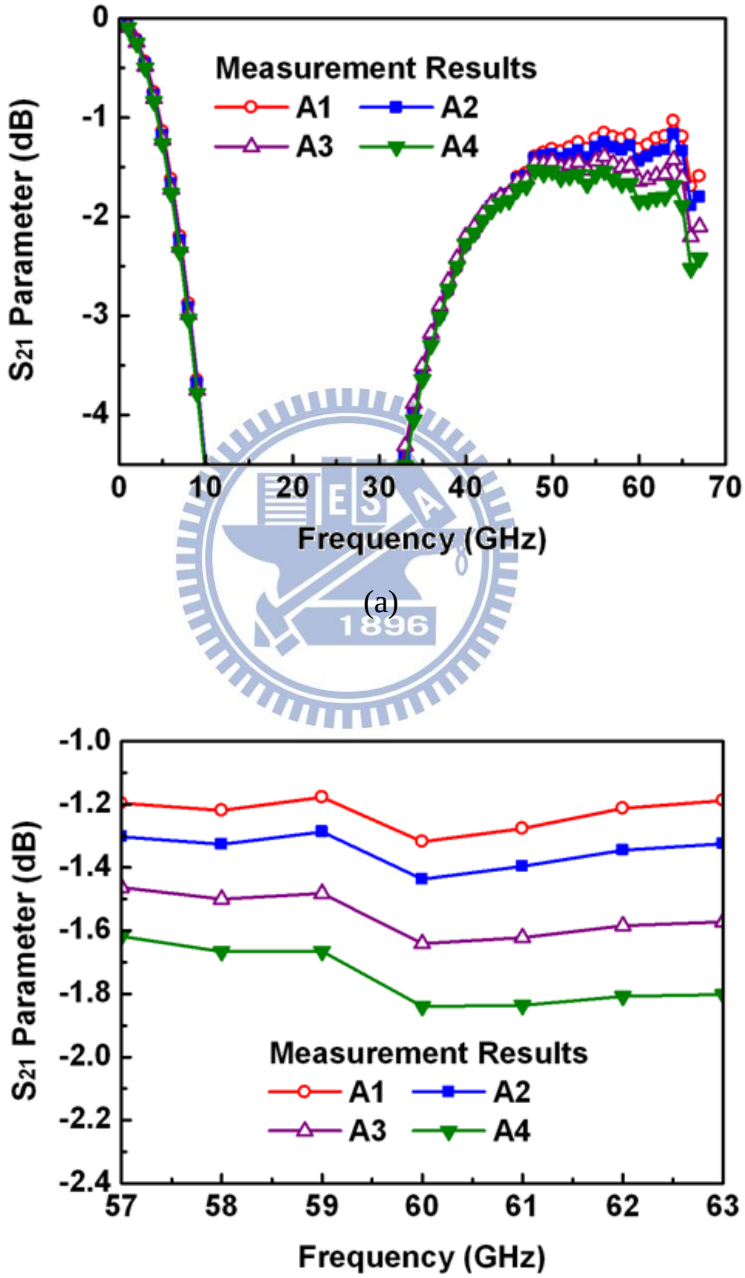
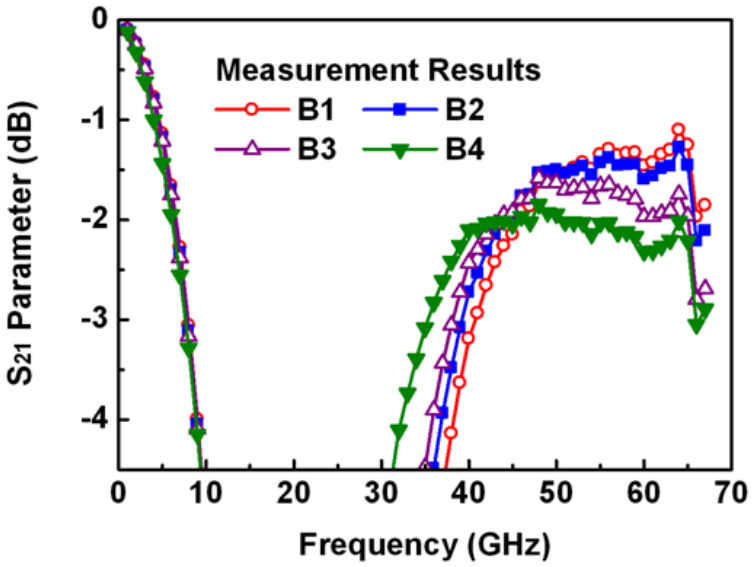
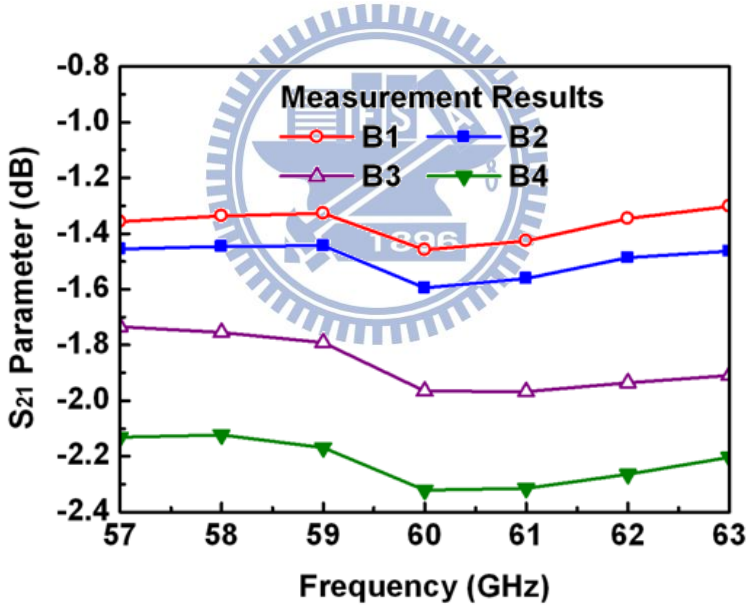


Fig. 3.10. Measured S_{21} parameters of proposed design A within (a) 0~67 GHz and (b) 57~63 GHz.



(a)



(b)

Fig. 3.11. Measured S_{21} parameters of proposed design B within (a) 0~67 GHz and (b) 57~63 GHz.

3.5.3 Measured ESD Robustness

ESD robustness of every ESD test circuit is evaluated by ESD tester. For the HBM ESD robustness, each test circuit is zapped by ESD pulses under PS-mode, PD-mode, NS-mode, and ND-mode ESD stress conditions. The failure criterion is defined as the I-V characteristics seen at RF input shifting over 30% from its original curve. The PS-mode, PD-mode, NS-mode, and ND-mode HBM ESD robustness of all ESD test circuits are measured, as listed in Table 3.2. According to the test results, the HBM ESD robustness of the proposed designs can be obtained from the lowest level of the robustness of the four modes. For the proposed design A, the test circuits A1, A2, A3, and A4 have 0.25-kV, 1.25-kV, 1.75-kV, and 2-kV HBM ESD robustness, respectively. For the proposed design B, the test circuits B1, B2, B3, and B4 have 0.25-kV, 1.25-kV, 1.75-kV, and 2.25-kV HBM ESD robustness, respectively. The measurement results of RF performance are also summarized in Table 3.2, inclusive of the measured S_{11} parameters. The measured S_{11} parameters show that all test circuits exhibit good input matching (S_{11} < -15 dB) at 60 GHz.

Table 3.2
Comparisons of Experimental Results Among ESD Protection Circuits in Silicon

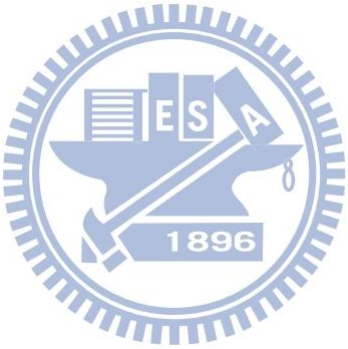
	Proposed Design A				**Proposed Design B**				**[18]**
	A1	**A2**	**A3**	**A4**	**B1**	**B2**	**B3**	**B4**	
S_{11} Parameters at 60 GHz	-16 dB	-17 dB	-19 dB	-21 dB	-22 dB	-29 dB	-26 dB	-26 dB	-22 dB
S_{21} Parameters at 60 GHz	-1.3 dB	-1.4 dB	-1.6 dB	-1.8 dB	-1.4 dB	-1.6 dB	-2.0 dB	-2.3 dB	-2.1 dB
Noise Figures at 60 GHz	0.9 dB	1.2 dB	1.6 dB	2.0 dB	0.9 dB	1.3 dB	1.7 dB	2.2 dB	-
PS-Mode HBM ESD Robustness	0.25 kV	1.5 kV	1.75 kV	2 kV	0.25 kV	1 kV	1.75 kV	2.25 kV	2.5 kV
PD-Mode HBM ESD Robustness	0.25 kV	1.5 kV	2.25 kV	2.5 kV	0.25 kV	1.5 kV	2.25 kV	2.5 kV	3.5 kV
NS-Mode HBM ESD Robustness	0.5 kV	1.25 kV	2 kV	2.25 kV	0.5 kV	1 kV	1.75 kV	2.25 kV	2.75 kV
ND-Mode HBM ESD Robustness	0.25 kV	1.25 kV	2 kV	2.25 kV	0.25 kV	1 kV	1.75 kV	2.25 kV	2.75 kV
Layout Area	100×130 μm^2	100×130 μm^2	100×130 μm^2	100×130 μm^2	100×130 μm^2	100×130 μm^2	100×130 μm^2	100×130 μm^2	110×220 μm^2

3.5.4 Comparison and Discussion

The HBM ESD robustness and the measured S_{21} parameters at 60 GHz of the proposed ESD protection designs A and B are compared in Table 3.2. Among the splits of the proposed designs A and B, the test circuit A4 (B4) can achieve 2-kV HBM ESD robustness with 1.8-dB (2.3-dB) insertion loss. Since the signal loss of B4 is a little higher than that of A4, A4 is the suitable ESD protection design for 60 GHz RF circuits in these splits.

There is another reference ESD protection design, which is also applied on 60 GHz RF circuits and had been verified in a 65-nm CMOS process, is compared with the proposed designs in Table 3.2 [18]. The reference ESD protection design also consists of some simple

passive devices - two diodes and two inductors. The drawback is its large layout area. Compared with the reference design, the layout area of the proposed designs can be reduced from 110×220 μm^2 to 100×130 μm^2. Moreover, the test circuit A4 can provide the required 2-kV HBM ESD robustness with lower insertion loss. Therefore, the compact ESD protection circuit for 60 GHz RF circuits can be realized by using the test circuit A4. The proposed design can easily be used for 60 GHz RF circuits.



Chapter 4

ESD Protection Design for 2.4 GHz CMOS RF PA

4.1 Traditional ESD Protection Design for PA

To design an ESD protection circuit or device which is suitable for PA, the characteristics of PA should be involved in the ESD protection design concept. Fig. 4.1 shows a traditional ESD protection design for PA [19]. The ESD protection design consists of a power-rail ESD clamp circuit, a diode connected between RF output pad and V_{SS}, and a diode string between V_{DD} and RF output pad. The voltage at the output of a PA would swing to more than twice of V_{DD} under normal operating conditions. In order not to cause signal loss, stacking several diodes between V_{DD} and RF output pad is needed. However, the clamping voltage of the diode string would be high when ESD current is discharged through the diode string, and it is disadvantageous to ESD protection. Moreover, the diode string and the power-rail ESD clamp circuit make up the longest ESD discharge path, which is also disadvantageous to ESD protection.

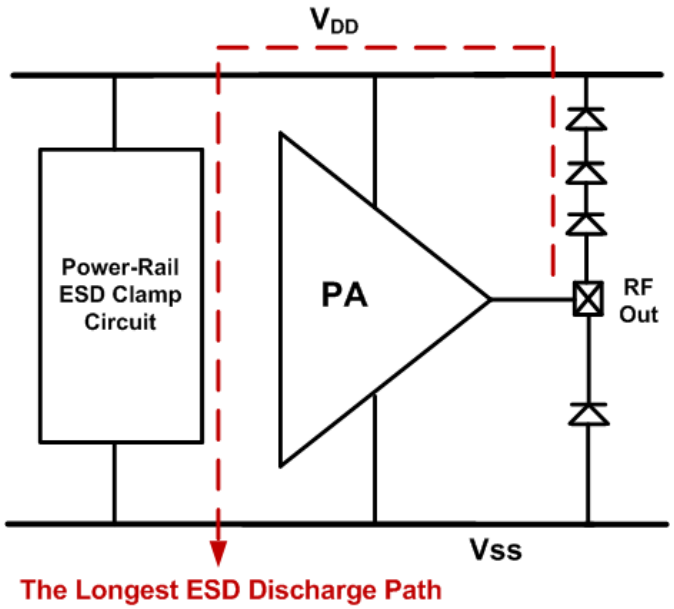


Fig. 4.1. Traditional ESD protection design for PA and its longest ESD discharge path.

4.2 Proposed ESD Protection Design for PA

To shorten ESD discharge paths and lower the clamping voltage, SCR is a proper choice. SCR is a bilateral-conduction ESD protection device, so it can provide shorter ESD discharge paths. Besides, SCR has lower holding voltage than diode string. Another advantage of SCR is its low capacitance with small layout area. Thus, SCR with proper trigger mechanism would be a suitable choice.

Fig. 4.2 shows the proposed practical ESD protection design which is suitable for PA. The ESD protection design consists of a power-rail ESD clamp circuit, an SCR with an ESD detection circuit which acts as a trigger circuit, and a pair of diodes, D_N and D_P.

The ESD detection circuit is used to detect ESD stress in order to send trigger message to the SCR and help turning it on. Since high trigger voltage is a drawback of typical SCR, extra trigger mechanism is needed to lower the trigger voltage. The ESD level would boost with lower trigger voltage. Considering the high voltage swing at the output node of PA, the ESD

detection circuit should be high-voltage-tolerant to avoid being damaged under normal operating conditions.

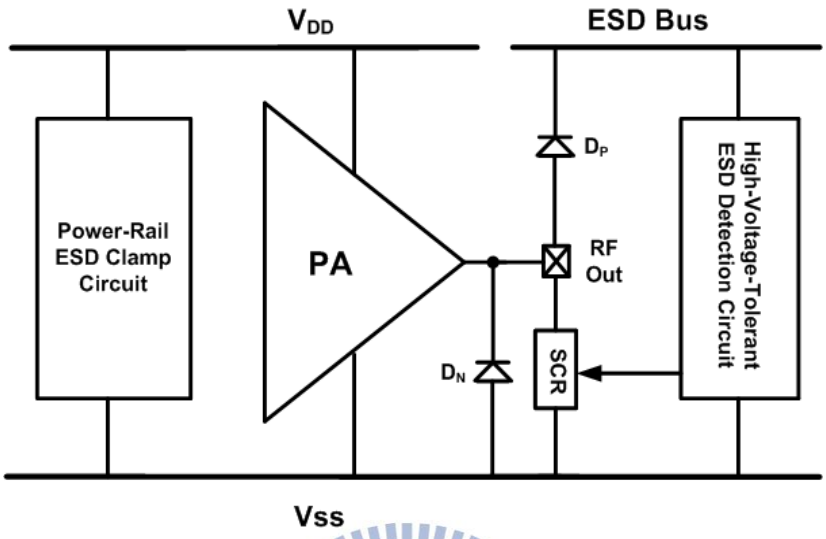


Fig. 4.2. The proposed ESD protection design for PA.

An implementation of this ESD protection design is shown in Fig. 4.3. The ESD protection design utilizes a Zener diode (D_Z) as a high-voltage-tolerant ESD detection circuit. The breakdown voltage of D_Z should be low enough so D_Z can be quickly turned on to trigger the SCR under ESD stress conditions. On the other hand, the breakdown voltage of D_Z should be high enough so that it would not be turned on to mistrigger the SCR under normal operating conditions. A diode D_p is placed between RF output pad and ESD bus in order to keep the ESD bus at high voltage level to avoid signal loss under normal operating conditions. A diode D_N is placed between RF output pad and V_{SS} to provide an ESD discharge path extra from the SCR. The used power-rail ESD clamp circuit is the same as that used in section 3.2.

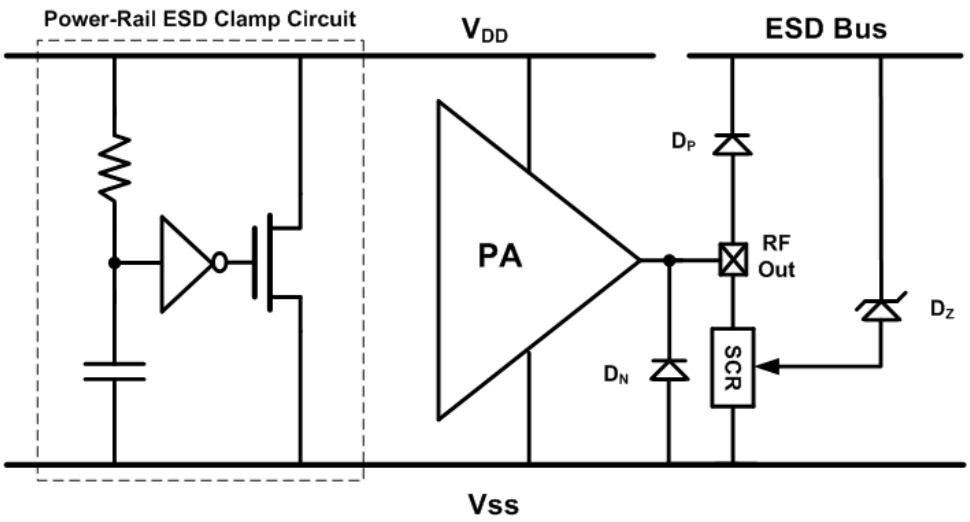


Fig. 4.3. The proposed ESD protection design with a Zener diode as the trigger circuit of the SCR.

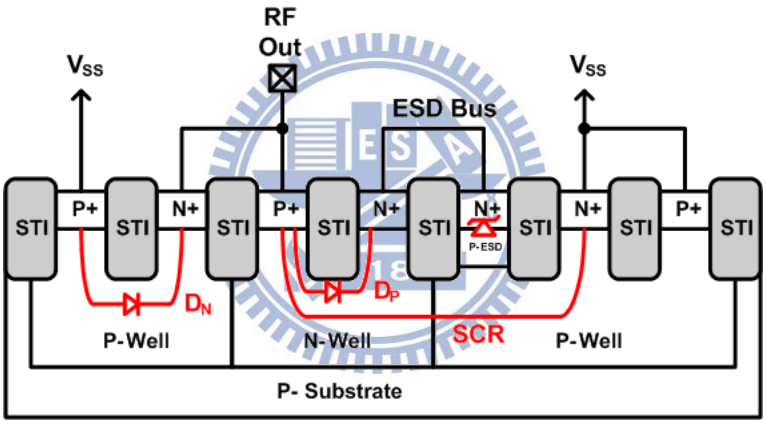
Fig. 4.4 (a) shows the proposed ESD protection device which implements this architecture, and Fig. 4.4 (b) shows its equivalent circuit. The P-ESD is a diffusion area which has higher doping concentration than P-sub but lower doping concentration than P+. The junction N+/P-ESD acts as a Zener diode embedded in the SCR and has lower breakdown voltage compared with P-well/N-well junction. D_P consists of P+/N-Well junction. D_N, which consists of P-well/N+ junction, is combined with the SCR for the consideration of layout area. The Zener-diode-triggered SCR (ZTSCR) is an ESD protection device designed for RF PA.

Assume that positive ESD stress is applied to the node which will be added to the RF output pad. At the beginning, the voltage applied to the anode is less than the breakdown voltages of D_Z as well as the N-well/P-well junction on the SCR path, so the ZTSCR acts like an open circuit. When the voltage applied to the anode is greater than the breakdown voltage of D_Z, the trigger current starts to flow from D_Z through P-well to P+ diffusion connected to V_{SS}. Once the voltage drops across the P-well resistor ($R_{P\text{-well}}$) is large enough, the parasitic NPN transistor will be turned on. The parasitic NPN transistor starts to inject electron current to bias the PNP transistor, and then the positive-feedback regenerative mechanism helps the

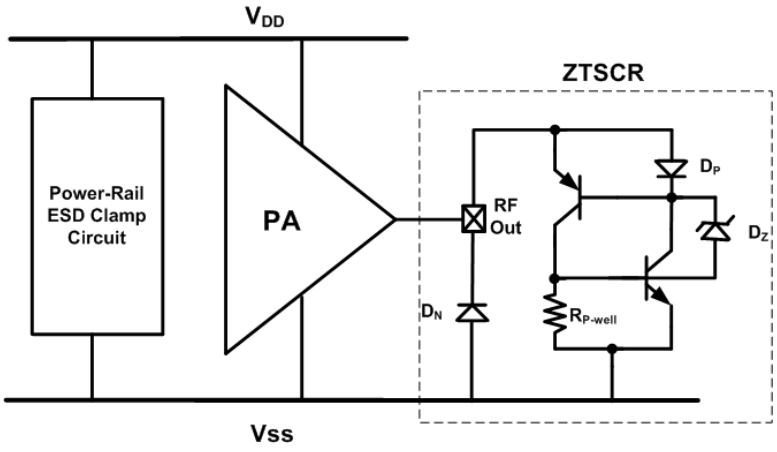
SCR be successfully triggered into its latching state.

The trigger voltage of the ZTSCR would be lower than the typical SCR described in chapter 2. Since the breakdown voltage of D_Z is lower than that of the N-well/P-well junction, the trigger current would more rapidly flow through $R_{P\text{-well}}$ to turn on the parasitic NPN transistor.

Next assume that negative ESD stress is applied to the node which will be added to the RF output pad. This negative voltage drops across D_N. As long as D_N diode is forward biased, the ESD current can be discharged and the negative voltage will be clamped at the low cut-in voltage of D_N.



(a)



(b)

Fig. 4.4. The (a) cross-section view and (b) the equivalent circuit of the ZTSCR.

Figs. 4.5 to 4.9 show the ESD discharge paths of ZTSCR under ESD stress conditions. For PS-mode, the ESD current first goes through D_P and then turned on the Zener diode to trigger the SCR. After the SCR is turned on, the ESD current can be discharged through the SCR path. For NS-mode, the ESD current is discharged through D_N. For PD-mode, the ESD current is discharged through the SCR path and the power-rail ESD clamp circuit. For ND-mode, the ESD current is first shunted from V_{DD} to V_{SS} through the power-rail ESD clamp circuit and then discharged through D_N. For V_{DD}-to-V_{SS} and V_{SS}-to-V_{DD} mode, the power-rail ESD clamp circuit provides ESD discharge paths.

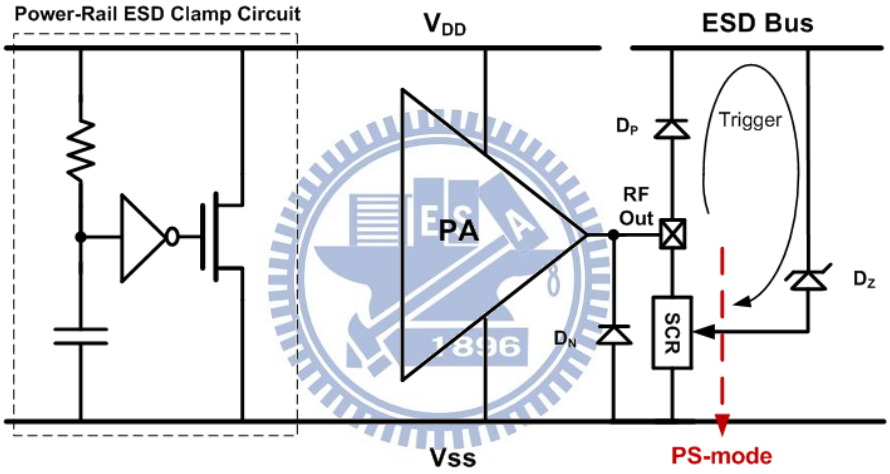


Fig. 4.5. ESD discharge path of the ZTSCR under PS-mode.

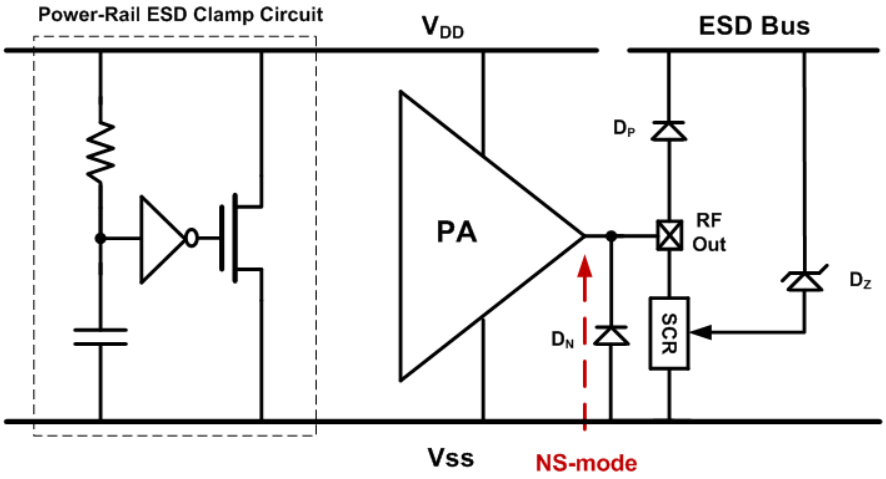


Fig. 4.6. ESD discharge path of the ZTSCR under NS-mode.

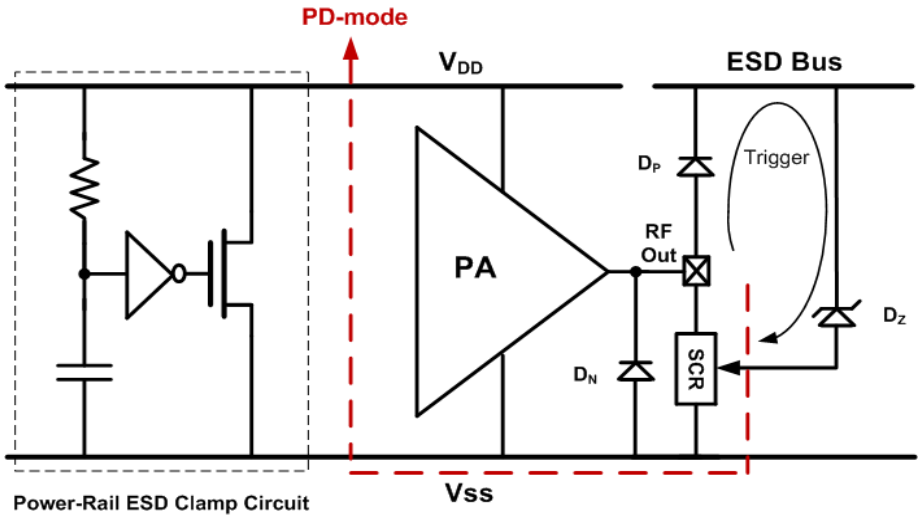
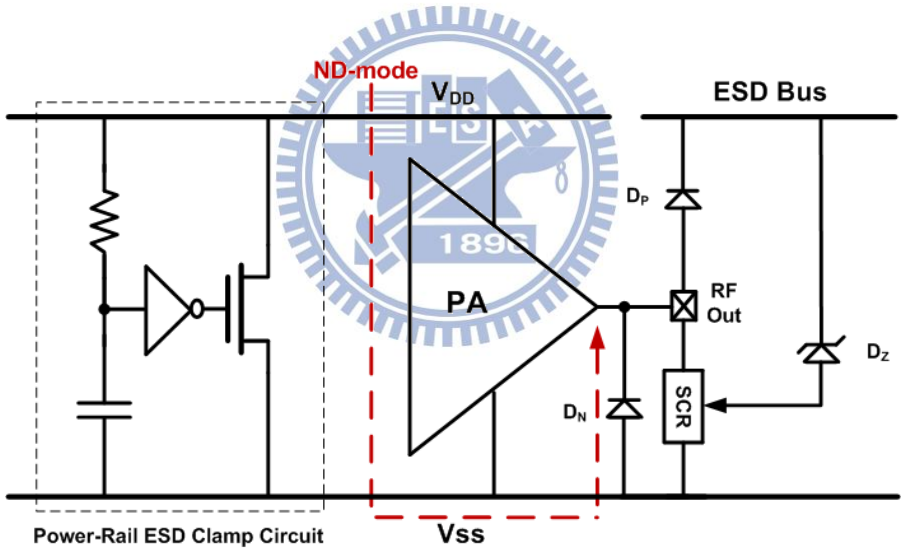


Fig. 4.7. ESD discharge path of the ZTSCR under PD-mode.



(d)

Fig. 4.8. ESD discharge path of the ZTSCR under ND-mode.

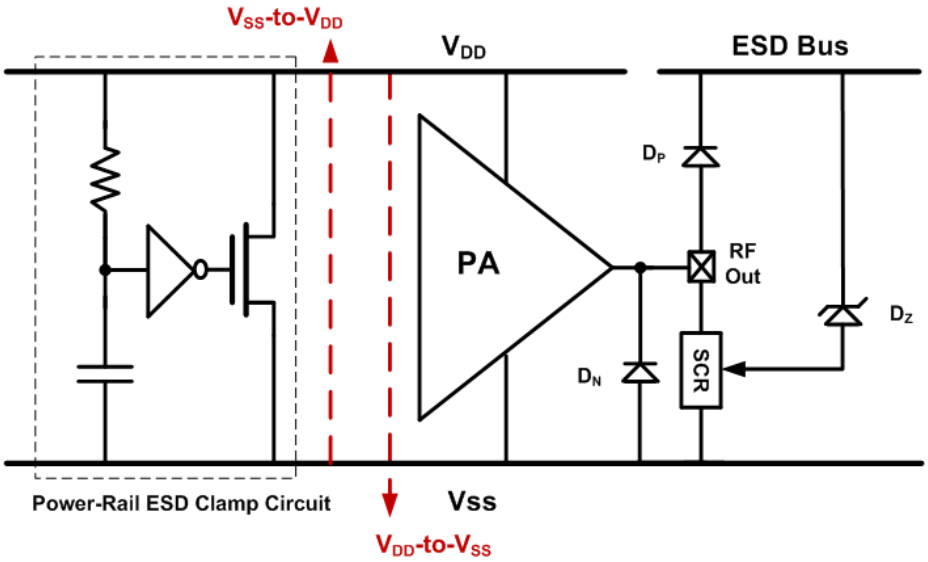


Fig. 4.9. ESD discharge path of the ZTSCR under V_{DD}-to-V_{SS} mode and V_{SS}-to-V_{DD} mode.

4.3 Experimental Results of ZTSCR

4.3.1 Test Devices

The length of each junction of the ZTSCR may influence the device characteristics. For this reason, the ZTSCR was split into 9 test devices with different junction length. The test devices of the proposed ZTSCR had been fabricated in a 65-nm CMOS process. All the junction dimensions are listed in Table 4.1, and the corresponding junction names are shown in Fig. 4.10. Every test device has the same width of 40 μm. All the junctions AW are on the ESD current paths, so they remain relatively large. Junction A represents the distance between D_N and ZTSCR. Junction B may influence the length of the SCR path and the parasitic resistance of the P+/N-well junction, so it may influence holding voltage and trigger voltage of ZTSCR. Changing junction C, D and E would change the length of the SCR path, and it may influence holding voltage and trigger voltage. The larger the junction F is, the bigger the $R_{P\text{-well}}$ is, vice versa. Large $R_{P\text{-well}}$ would lower trigger voltage and holding voltage of ZTSCR.

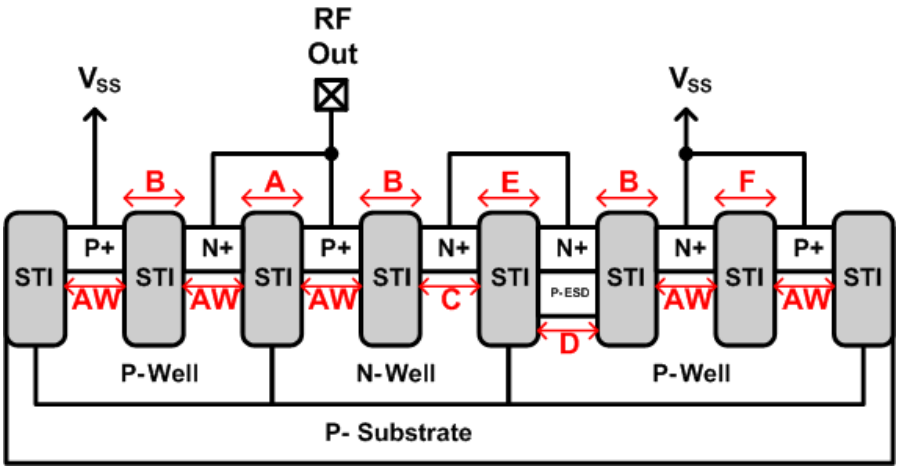


Fig. 4.10. Cross-section view of ZTSCR with several junctions which are used to do splits**.**

Table 4.1
Junction Dimensions of Each Split of ZTSCR

Split	AW (μm)	A (μm)	B (μm)	C (μm)	D (μm)	E (μm)	F (μm)
1-1	0.8	0.3	0.3	0.2	0.4	0.3	1.0
1-2		1.0					
1-3		0.3	1.0				
1-4			0.3	1.0			
1-5				0.2	1.0		
1-6					0.4	1.0	
1-7						0.3	0.5
1-8							2.0
1-9							3.0

4.3.2 Experimental Results

The layout top view of one of the test devices, split 1-6, is shown in Fig. 4.11. The width of every split is 40 μm, and the length varies with different splits. For RF measurements, the two-port network parameters of the 9 test splits were measured by using network analyzer from 0 to 20 GHz, and the parasitic capacitance of the 9 splits could be extracted from the measured two-port network parameters. During the two-port network parameters

measurement, the port 1 and port 2 were biased at 1.25 V, which is $V_{DD}/2$ in the given 65-nm CMOS process. The source and load resistances to the test circuits were kept at 50 Ω.

The ESD robustness of every split was evaluated by the HBM ESD tester. Each test device was zapped by positive and negative ESD pulses at the node which would be connected to the RF output pad. The failure criterion was defined as the I-V characteristic shifting over 30% from its original value after ESD stressed at every ESD test level. The HBM ESD levels of all ESD test devices are the tested levels under positive HBM ESD stress, and the results are listed in Table 4.2.

To investigate the turn-on behavior of each test device under ESD stress conditions, the transmission line pulsing (TLP) system with 10-ns rise time and a 100-ns pulse width was used. The secondary breakdown current (I_{t2}), which indicates the current-handling ability, and the trigger voltage, which indicates the turn-on speed, of each test device could be obtained from the measurement results. DC holding voltage of each test device was measured with Tek 370. All the measurement results of I_{t2}, trigger voltage, capacitance, and DC holding voltage of each test device are also summarized in Table 4.2.

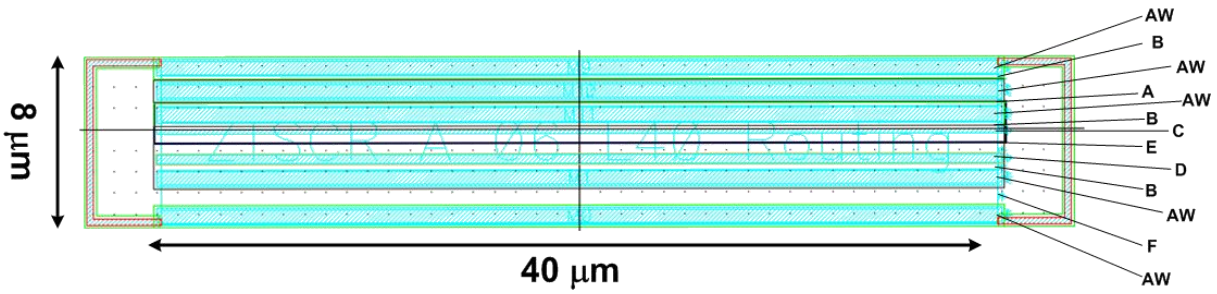


Fig. 4.11. Layout top view of split 1-6 of ZTSCR.

Table 4.2
Measurement Results of Each Split of ZTSCR

Split	C @ 2.4 GHz (fF)	DC Holding Voltage (V)	TLP-Measured Trigger Voltage (V)	TLP-Measured Secondary Breakdown Current (A)	HBM ESD Robustness (kV)
1-1	75.7	2.52	8.04	1.76	3.25
1-2	73.4	2.37	8.08	1.76	3.25
1-3	74.6	3.11	8.65	1.82	3.25
1-4	75.3	3.61	8.25	1.66	3.00
1-5	77.6	3.07	7.97	1.69	3.00
1-6	74.8	3.10	7.99	1.73	3.25
1-7	75.3	2.79	8.18	1.64	3.00
1-8	75.3	2.30	7.87	1.82	3.25
1-9	75.4	2.12	7.92	1.83	3.50

To apply the ZTSCR on an RF PA, there are something need to be carefully concerned. The first one is the DC holding voltage of the ZTSCR. Since the V_{DD} of PA circuit is set to be 2.5 V, the DC holding voltage of the ZTSCR should be higher than V_{DD} to avoid latch-up issues. The second one is its trigger voltage. Considering the output voltage of PA which would swing to more than $2 \times V_{DD}$, the trigger voltage of the ZTSCR should be higher than the maximum output voltage of PA. Because the ZTSCR will be added at the output of the PA, too low trigger voltage would cause mistriggering of the ZTSCR under normal operating conditions.

The spilt 1-6 is then selected, since the DC holding voltage is 3.10 V, which is higher than $1.2 \times V_{DD}$. Though the high operating temperature of PA circuit may decrease the DC holding voltage of SCR device [20], there exists buffer to prevent from latch up issues. In addition, it has relatively low trigger voltage (but high enough to avoid being mistriggered under normal operating conditions) and high HBM ESD robustness. Thus, spilt 1-6 would be suitable for a CMOS RF PA with supply voltage of 2.5 V. Fig. 4.12 shows the TLP-measured I-V curve of

the split 1-6. Fig. 4.13 shows the measured DC I-V curve.

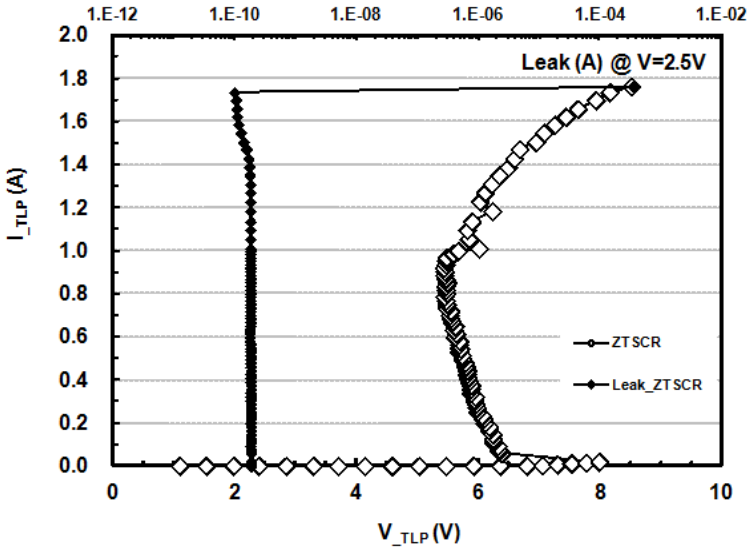


Fig. 4.12. TLP-measured I-V characteristics of split 1-6.

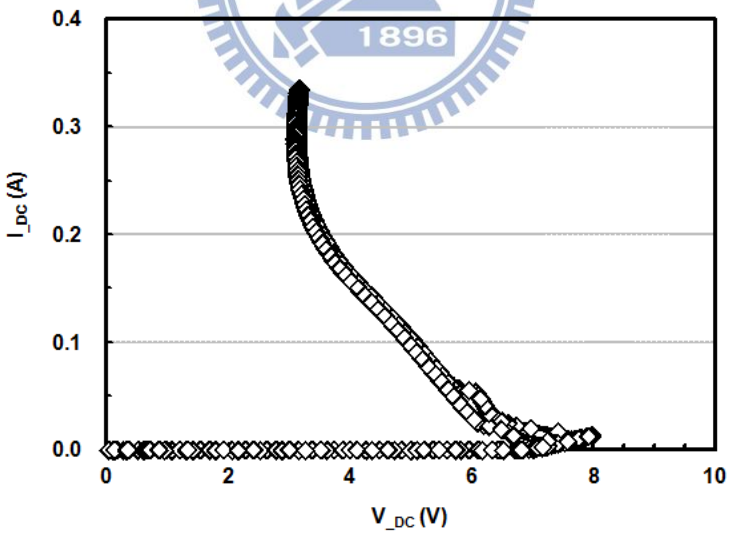


Fig. 4.13. Tek370-measured DC I-V characteristics of split 1-6.

4.4 Circuit Design of 2.4 GHz CMOS RF PA

4.4.1 Circuit Design

To more accurately investigate the ESD protection ability of the proposed ZTSCR, a 2.4 GHz CMOS RF PA is designed and fabricated. The ZTSCR would be added to the PA circuit so as to verify its ESD level.

In order to design a CMOS PA with high linearity, enough output power, and well efficiency, two-stage architecture was chosen. A simple two-stage PA is shown in Fig. 4.14. The power stage should be able to drive the output load, and the drive stage is used to drive the power stage of PA. A two-stage PA can provide required output power level.

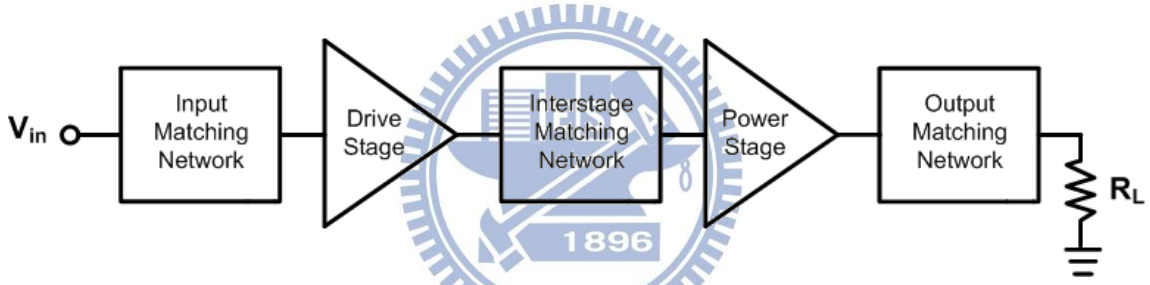


Fig. 4.14. Simple architecture of a two-stage power amplifier.

The structure of the power stage was chosen as self-biased cascode structure [21]. The second step is to choose transistor sizes and bias point. The required maximum output power is 26 dBm, and the required maximum output current is calculated as 800 mA. According to the DC I-V curve of the used NMOS, all the MOS transistor sizes of the power stage is determined with total width = 3072 μm and channel length = 0.28 μm. The power stage is chosen as class AB operation and the bias voltage is 0.9 V.

The structure of the driver stage is the same as the power stage, and the MOS transistor sizes are determined to provide enough power gain for pre-amplification. All the transistor sizes of the power stage are determined with total width = 512 μm and channel length

= 0.28 μm. The bias condition is also chosen as class AB operation for the consideration of moderate linearity and efficiency. The power stage is chosen as class AB operation and the bias voltage is 0.9 V, too. The used MOS devices are all 2.5 V devices so that the PA circuit can sustain the output voltage of $2 \times V_{DD}$.

Both input and inter-stage matching networks are π-matching for conjugate match, and the output matching network is designed with load-pull simulation of ADS. Fig. 4.15 shows the circuit diagram of the 2.4 GHz CMOS PA.

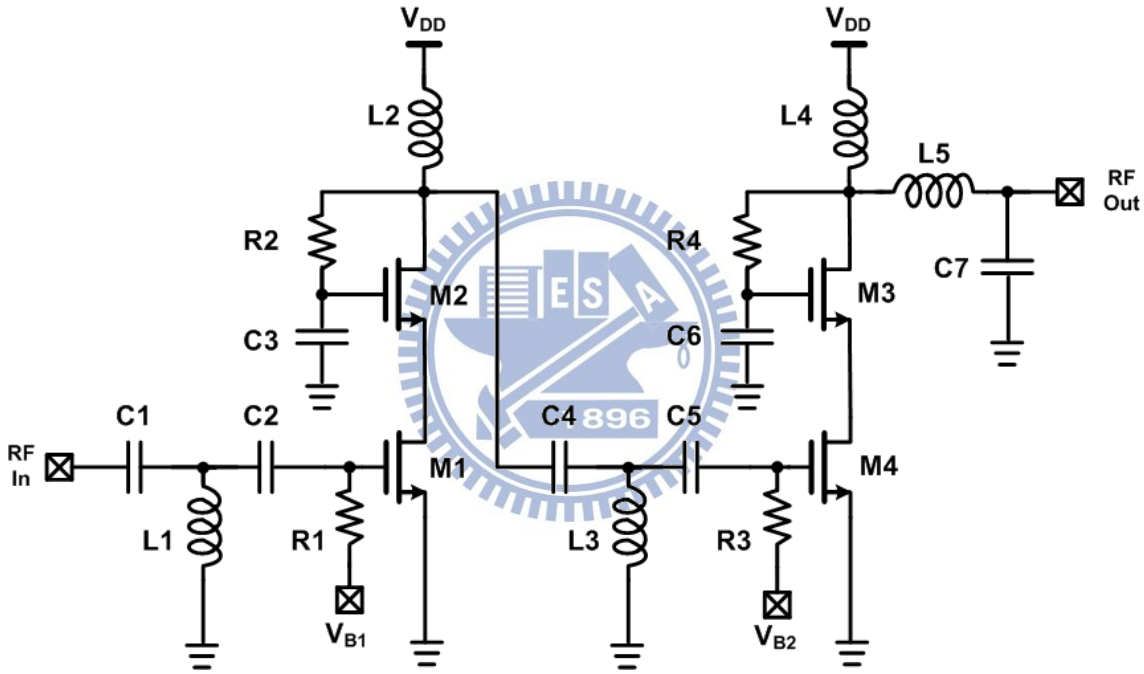


Fig. 4.15. The circuit diagram of the 2.4 GHz two-stage CMOS PA.

4.4.2 Post-Simulation Results

The post-simulation results of the 2.4 GHz CMOS PA is presented in this section. The PA is designed in a 65-nm 1P6M CMOS process with 2.5 V supply voltage and simulated with ADS. The corresponding device parameters are organized in Table 4.3. The post-simulation results are illustrated in Figs. 4.16 to 4.19. Fig. 4.16 shows the simulated S_{11} parameter and S_{21} parameter. Fig. 4.17, Fig. 4.18, and Fig. 4.19 show the simulated power

gain, output power (Po), and PAE versus input power (Pin), respectively. The simulated results are summarized in Table 4.4

Table 4.3
Component values and device dimensions of the 2.4 GHz CMOS PA

Parameter	Value
M1、M2	512 μm/0.28 μm
M3、M4	3072 μm/0.28 μm
R1、R3	5 kΩ
R2、R4	2.50 kΩ
L1	5.62 nH
L2	2.80 nH
L3	1.32 nH
L4	3.32 nH
L5	1.67 nH
C1、C2	0.32 pF
C3、C6	2.41 pF
C4	0.60 pF
C5	3.33 pF
C7	2.25 pF

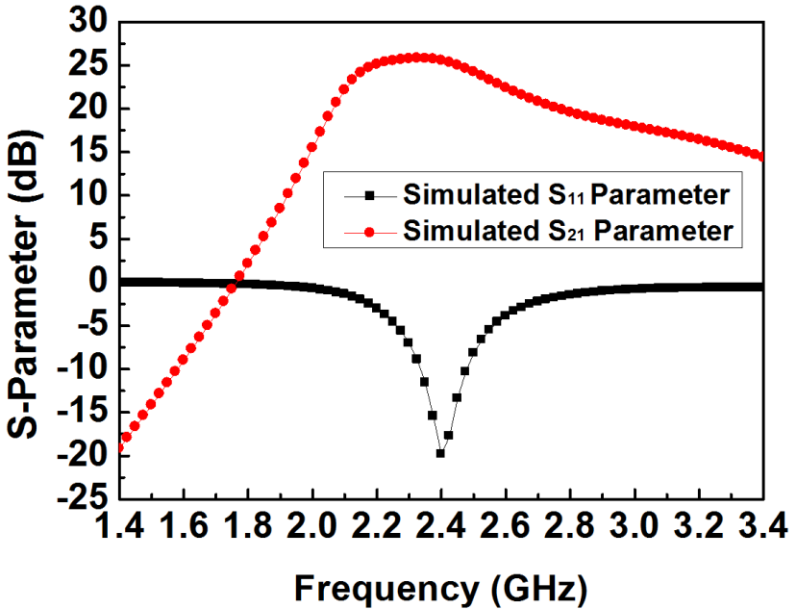


Fig. 4.16. Simulated S-parameters of the 2.4 GHz CMOS PA.

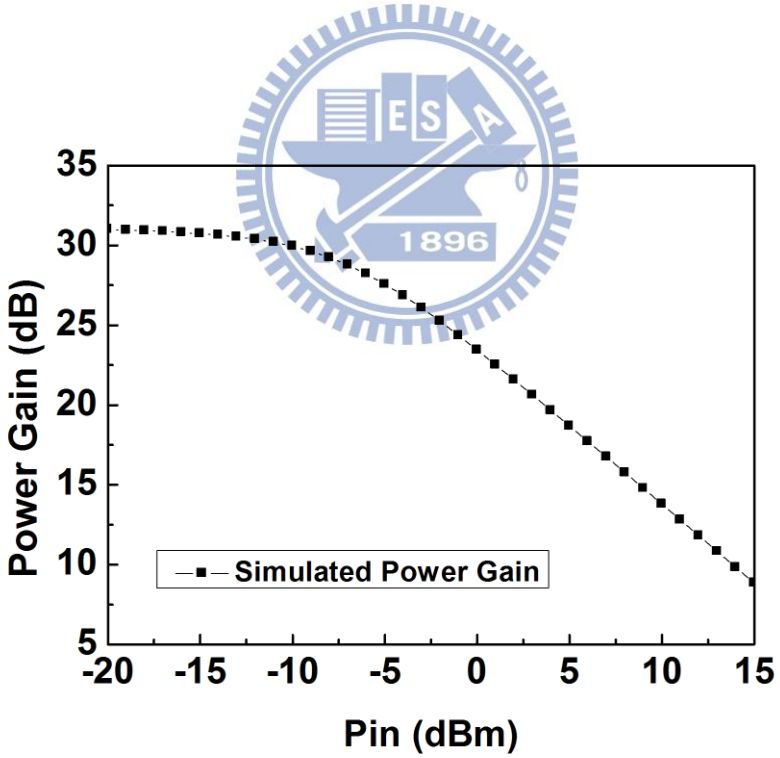


Fig. 4.17. Simulated power gain of the 2.4 GHz CMOS PA.

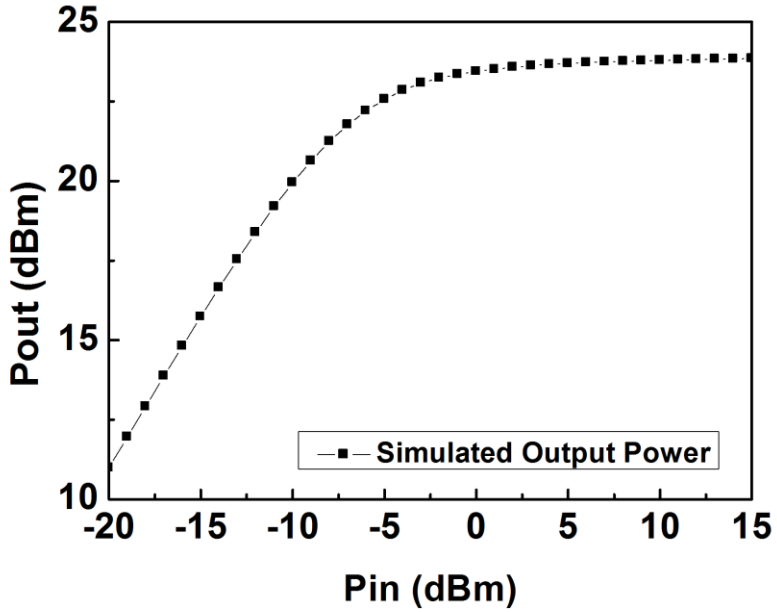


Fig. 4.18. Simulated output power of the 2.4 GHz CMOS PA.

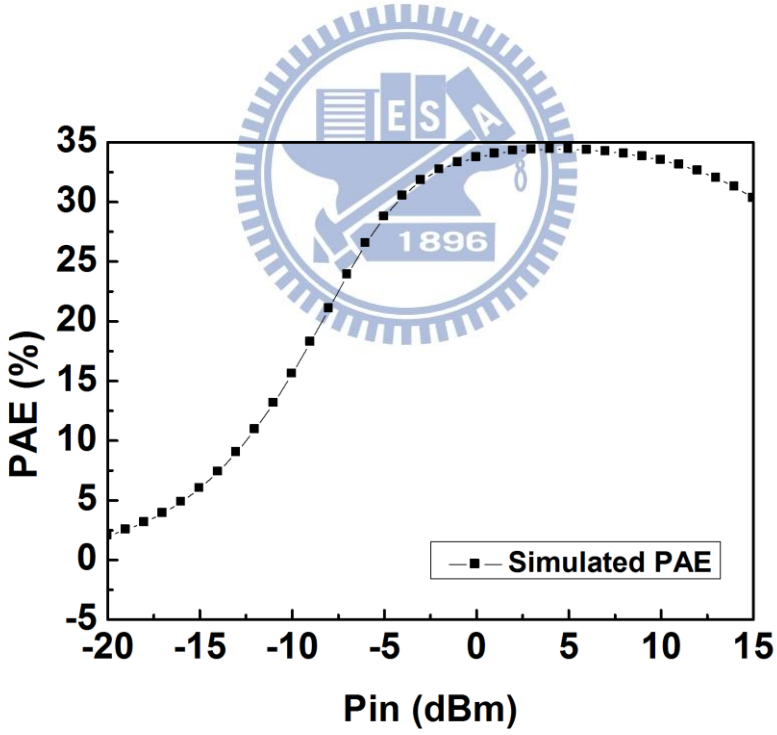


Fig. 4.19. Simulated PAE of the 2.4 GHz CMOS PA.

Table 4.4
Summary of the post-simulation results of the 2.4 GHz CMOS PA

Technology	**TSMC 65-nm 1P6M CMOS**
V_{DD}	2.5 V
V_{B1}	0.9 V
V_{B2}	0.9 V
Frequency	2.4 GHz
Maximum Output Power	23.84 dBm
Power Gain	30.95 dB
P_{1dB}	20.63 dBm
Maximum PAE	34.42 %
PAE at P1dB	18.26 %

4.5 Experimental Results of 2.4 GHz CMOS PA with ZTSCR

4.5.1 The Layout Description of Unprotected PA and ESD-protected PA

Three test circuits have been designed and fabricated in a 65-nm CMOS process. The first one is unprotected PA, as shown in Fig. 4.20. The output matching network, which consists of L5 and C7, is removed from the test circuit. Since the MOS transistors in the power stage of the PA would directly suffer ESD zapping under ESD stress conditions when the inductor L5 is not on-chip, the ESD level of the worst case can be verified.

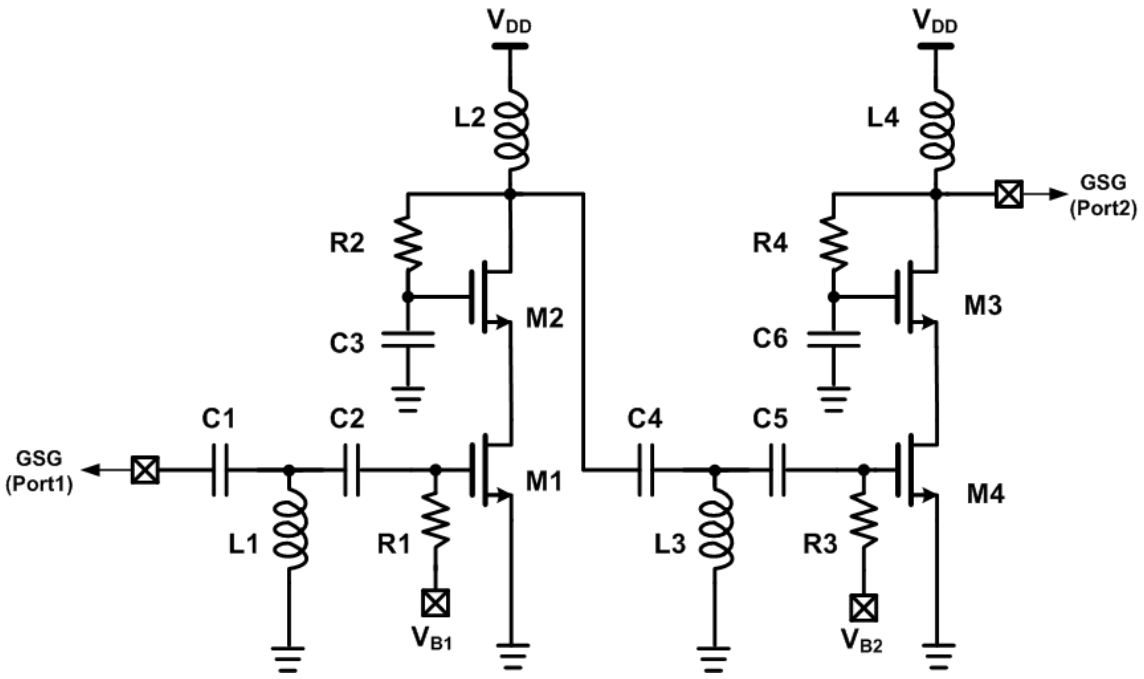


Fig. 4.20. Unprotected PA without the output matching network.

The others are ESD-protected PA. In some RF applications, the RF choke inductor of the output stage of PA is off-chip while the others are on-chip. In some other applications, all the RF choke inductors are off-chip. These two applications remain pads that may suffer ESD stress. For comprehensive consideration, both applications should be involved in the ESD level test. Therefore, the layouts of ESD-protected PA are split into two types. Type I is for an ESD-protected PA with an off-chip RF choke inductor at the output stage, and type II is for an ESD-protected PA with both RF choke inductors off-chip. Both types will be illustrated here. The output matching networks are also removed from the test circuits of the two types of PA. The used power-rail ESD clamp circuit is the same as that used in section 3.2.

Type I:

Fig. 4.21 shows the architecture of the type I. The V_{DD} pads of the PA are separated. A ZTSCR is added at the output pad, and a power-rail ESD clamp circuit is placed between the V_{DD} pad of the drive stage and V_{SS}. Under ESD test conditions, ESD pulse will be zapped among the output pad, V_{SS}, and the V_{DD} pad of the drive stage. Meanwhile, the V_{DD} pad of the

power stage will be floating so as to consider it to be off-chip.

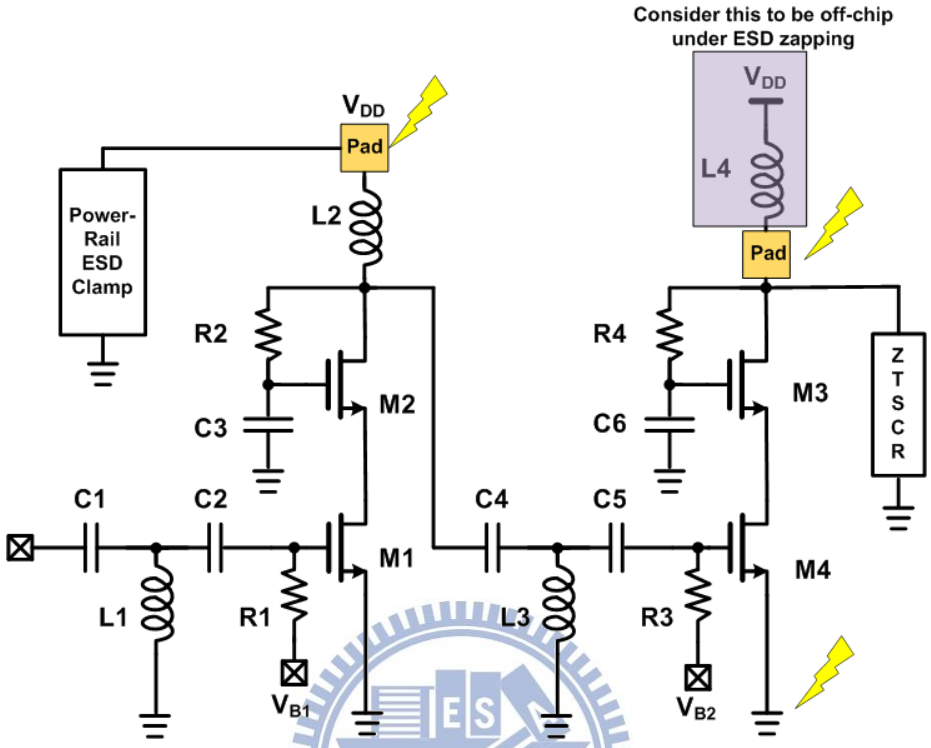


Fig. 4.21. Type I of the ESD-protected PA.

Type II:

Fig. 4.22 shows the architecture of the type II. Two pads, E2 and E3, are added between the two stages and the two RF choke inductors. These two pads are used for ESD test without any RF consideration. Besides, two ZTSCRs are added to E2 and E3, and a power-rail ESD clamp circuit is placed between an independent pad (E1) and V_{SS}. E2 and E3 represent the bonding pads of PA. E1 represents the V_{DD} pad of other circuits in transmitter. Under ESD test conditions, ESD pulse will be zapped among the E1, E2, V_{SS}, and E3. Meanwhile, V_{DD} of the PA circuit will be floating so as to consider it to be off-chip.

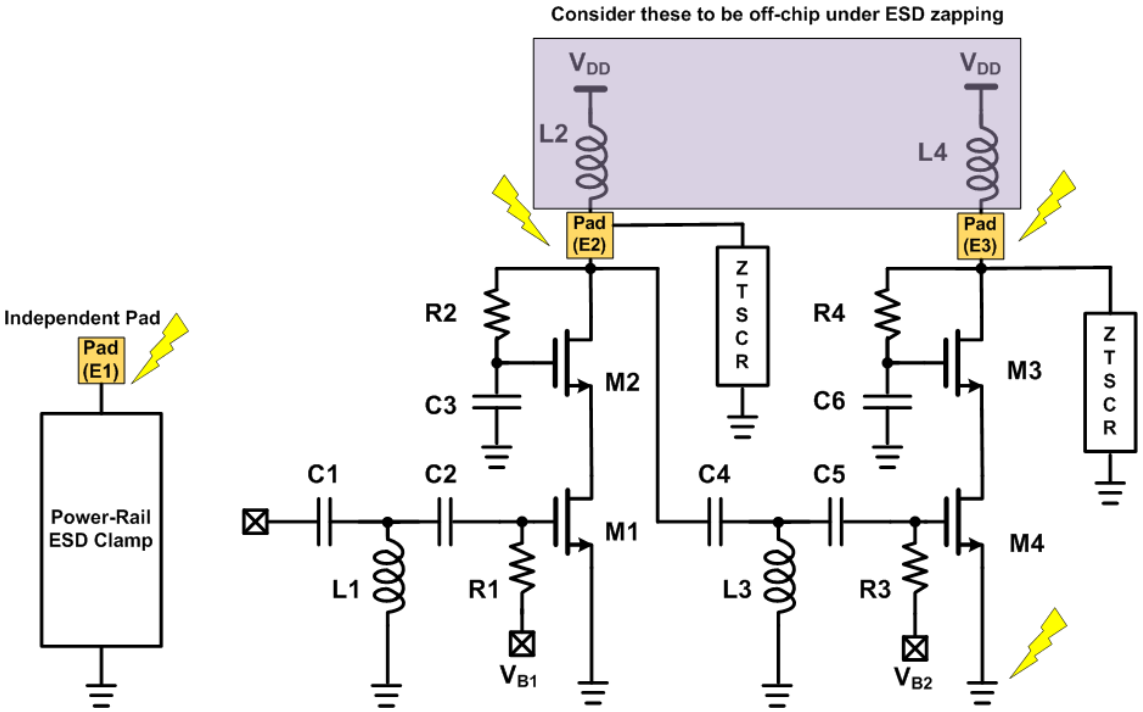


Fig. 4.22. Type II of the ESD-protected PA.

4.5.2 ESD Levels Measured with HBM ESD Tester

Fig. 4.23 shows the die photo of the un-protected PA. Fig. 4.24 shows the type I of ESD-protected PA, and Fig. 4.25 shows the type II of ESD-protected PA. The ESD robustness of the three test circuits is first tested with HBM ESD pulse by using Agilent HCE-5000. For the unprotected PA and the type I of ESD-protected PA, PS-mode, PD-mode, NS-mode, and ND-mode ESD stresses were applied among the RF output pad, V_{DD}, and ground pad. For type II, PS-mode, PD-mode, NS-mode, and ND-mode ESD stresses were applied among E1, E2, E3, and V_{SS}. Besides, pin-to-pin ESD stress was applied to the E2 pad and E3 pad. The failure criterion is defined as the I-V characteristics seen at RF input shifting over 30% from its original curve. The ESD robustness of each mode of every split is summarized in Table 4.5.

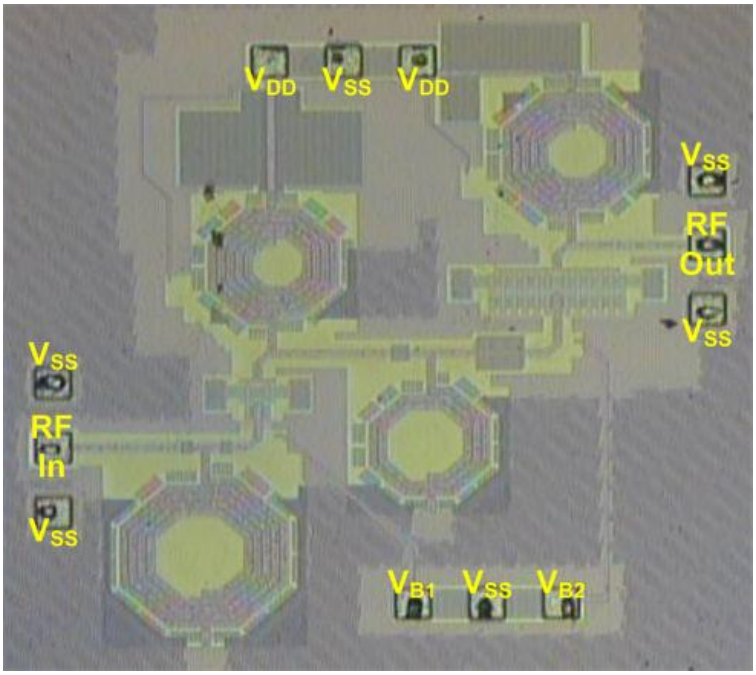


Fig. 4.23. Die photo of the unprotected PA.

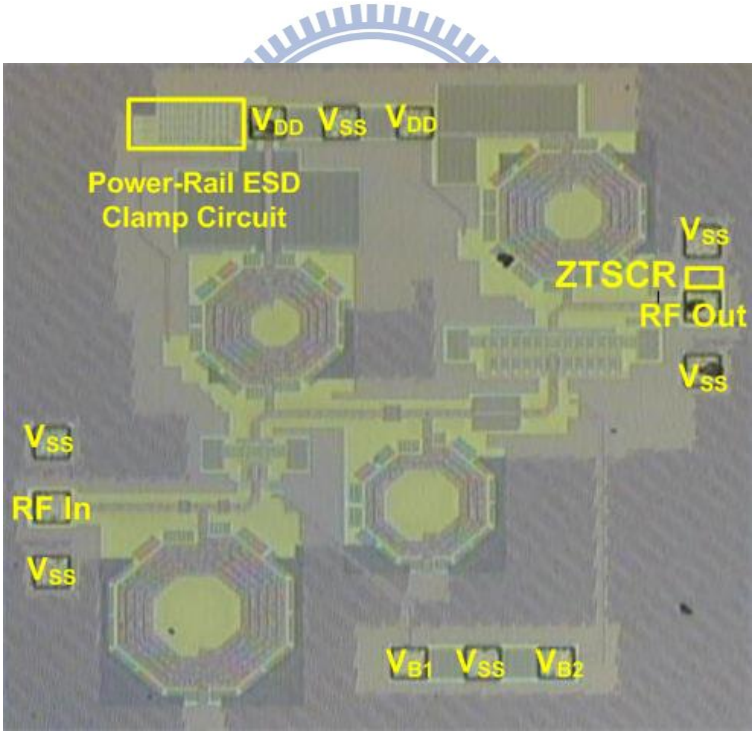


Fig. 4.24. Die photo of type I of the ESD-protected PA.

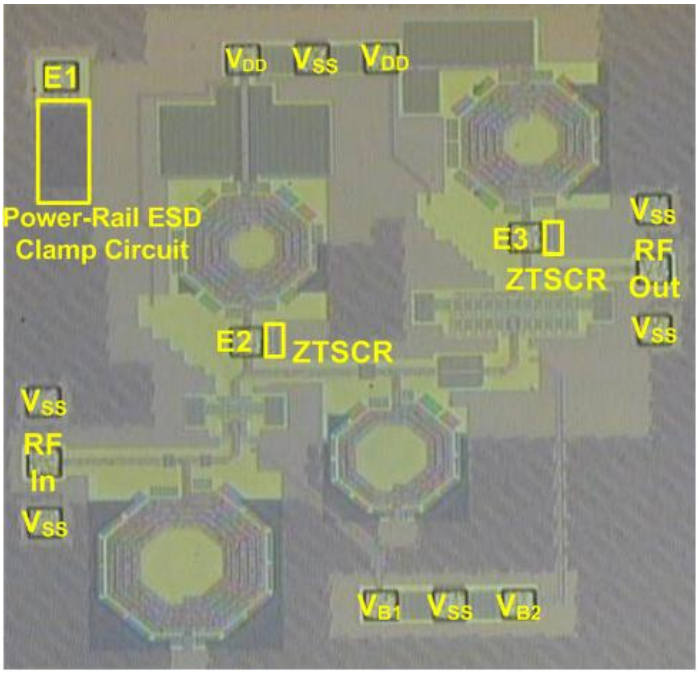


Fig. 4.25. Die photo of type II of the ESD-protected PA.

Table 4.5
Measured ESD level of each zapping mode with HBM tester

Cell Name	Unprotected PA	Type I	Type II	
			E2	E3
PS	500 V	4 kV	3 kV	4 kV
PD	500 V	4 kV	3 kV	4 kV
NS	>8 kV	>8 kV	5.5 kV	>8 kV
ND	>8 kV	>8 kV	5 kV	>8 kV
Pin to Pin (E2 to E3)	N/A	N/A	3 kV	
Pin to Pin (E3 to E2)	N/A	N/A	4 kV	

4.5.3 Measured RF Performance of the Unprotected PA

The two-port S-parameters of the unprotected PA were measured by using the vector network analyzer. Besides, the large signal characteristics were extracted with load-pull RF measurement system. With the help of the load-pull system, the optimal output impedance was found, and the maximum PAE, output power, and P1dB were measured.

The measurement results of the unprotected PA are illustrated in Figs. 4.26 to Fig. 4.30. Fig. 4.26 shows the measured S_{11} parameter, and Fig. 4.27 shows the measured S_{21} parameter. Fig. 4.28, Fig. 4.29, and Fig. 4.30 show the measured power gain, output power (Po), and PAE versus input power (Pin), respectively. The measurement results are summarized in Table 4.6

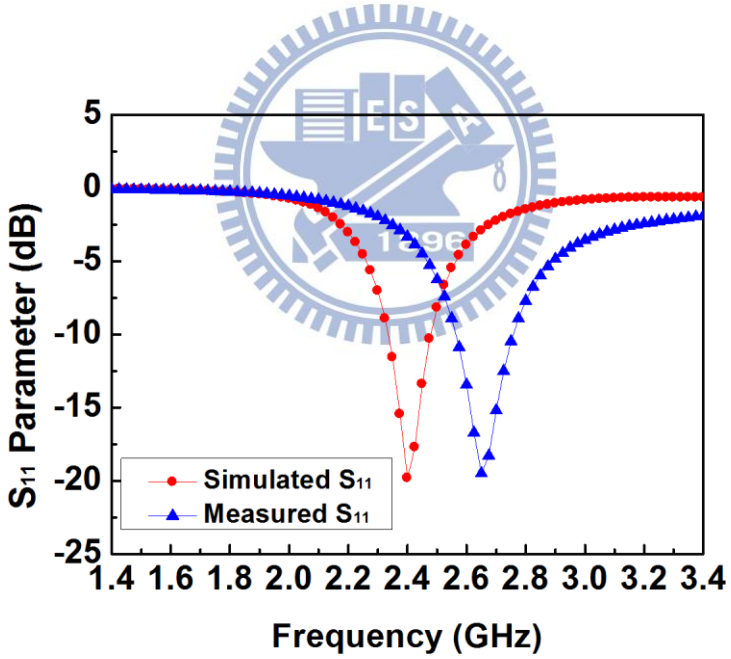


Fig. 4.26. Measured S_{11} parameter of the unprotected PA.

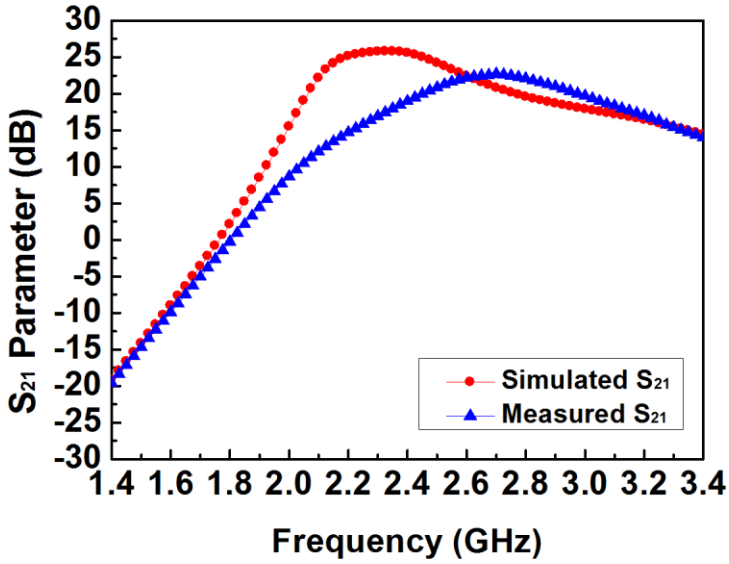


Fig. 4.27. Measured S_{21} parameter of the unprotected PA.

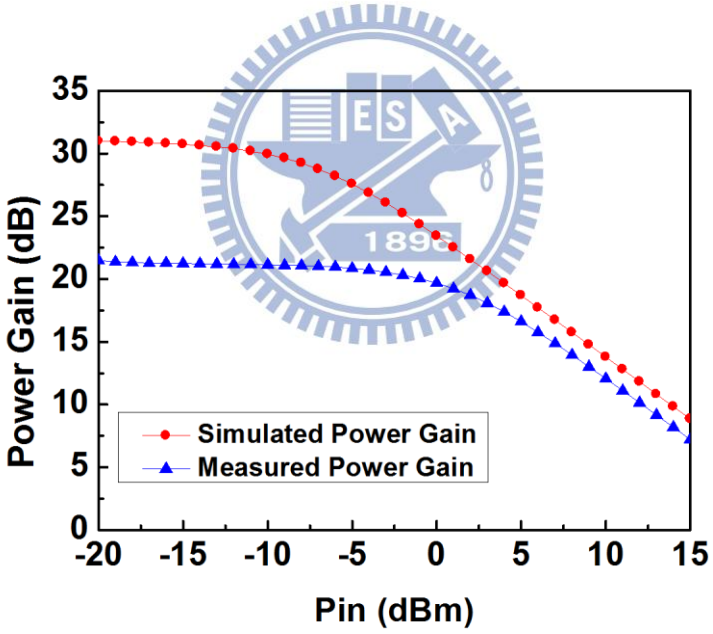


Fig. 4.28. Measured power gain of the unprotected PA.

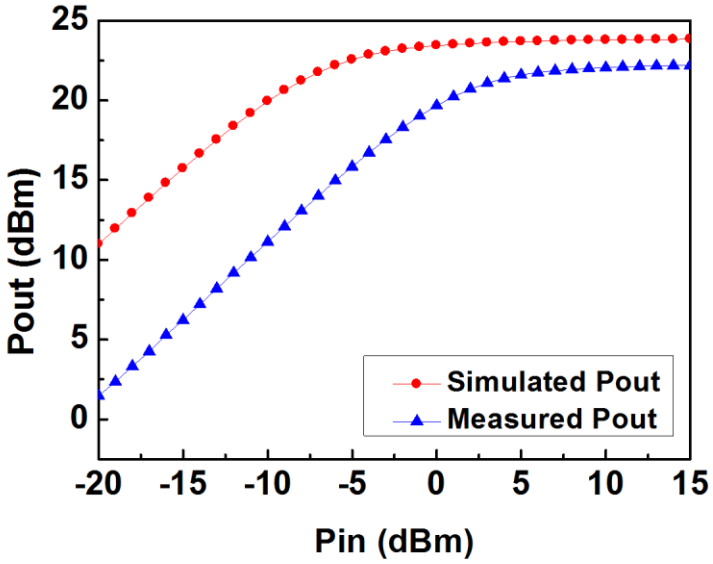


Fig. 4.29. Measured output power of the unprotected PA.

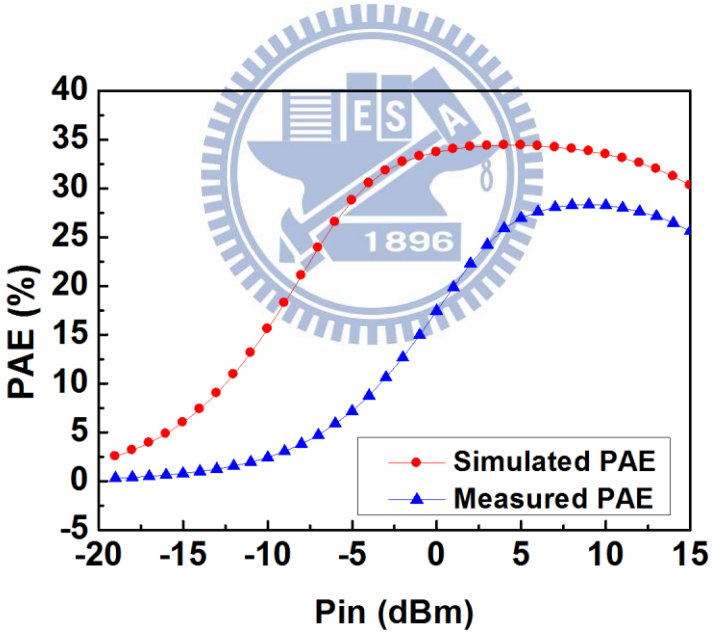


Fig. 4.30. Measured PAE of the unprotected PA.

Table 4.6
Summary of the measurement results of the 2.4 GHz CMOS PA

	Simulation	**Measurement**
Technology	TSMC 65-nm 1P6M CMOS Process	
V_{DD}	2.5 V	2.5 V
Frequency	2.4 GHz	2.65 GHz
Maximum Output Power	23.84 dBm	22.20 dBm
Power Gain	30.95 dB	21.47 dB
P_{1dB}	20.63 dBm	19.04 dBm
Maximum PAE	34.42 %	28.32 %
PAE at P1dB	18.26 %	14.98 %

4.5.4 Comparison of RF Performance before ESD Stress

Since the ZTSCR is an extra device to PA, it is necessary to investigate the influence on the RF performance of PA caused by the ZTSCR. Fig. 4.31 and Fig. 4.32 show the comparisons of S-parameters among the three test circuits. Fig. 4.33, Fig. 4.34, and Fig. 4.35 show the comparisons of power gain, output power, and PAE versus input power among the three test circuits, respectively. The large signal characteristics of each test circuit were measured based on the same optimal output impedance extracted with load-pull system.

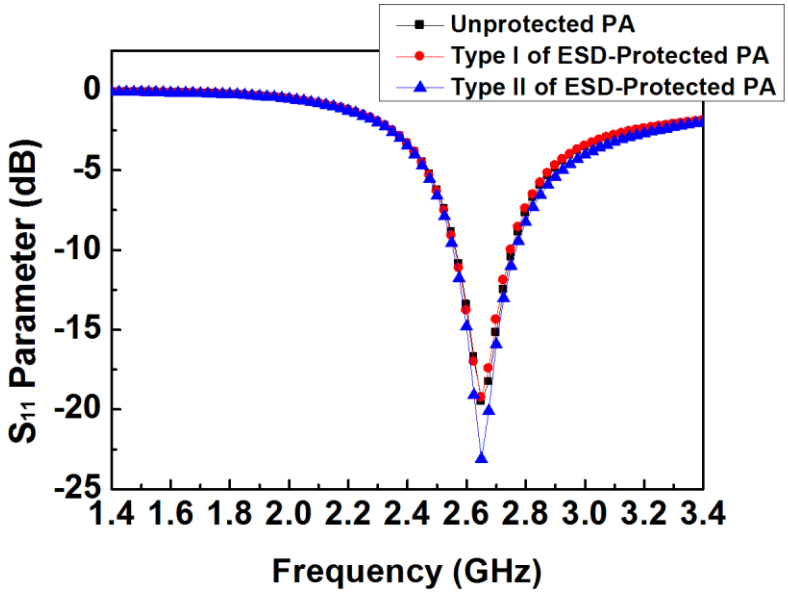


Fig. 4.31. Comparison of S_{11} Parameter of the unprotected PA and the ESD-protected PA.

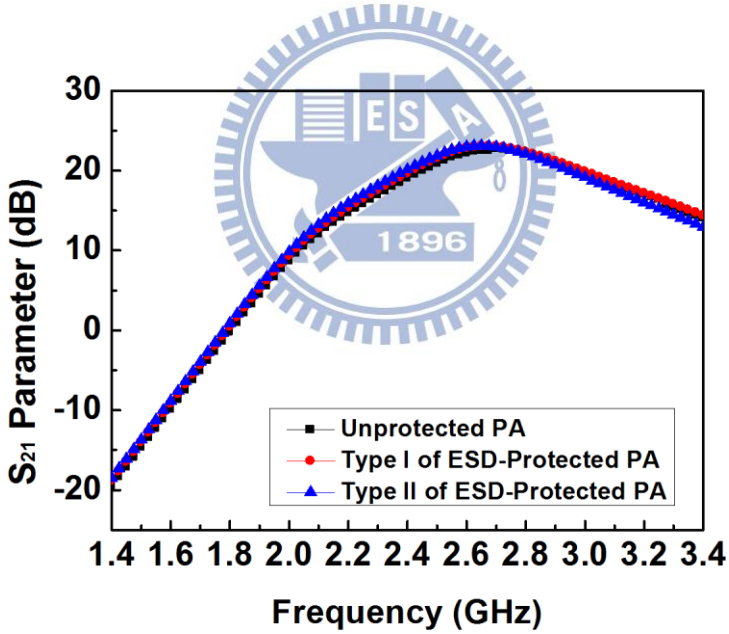


Fig. 4.32. Comparison of S_{21} Parameter of the unprotected PA and the ESD-protected PA.

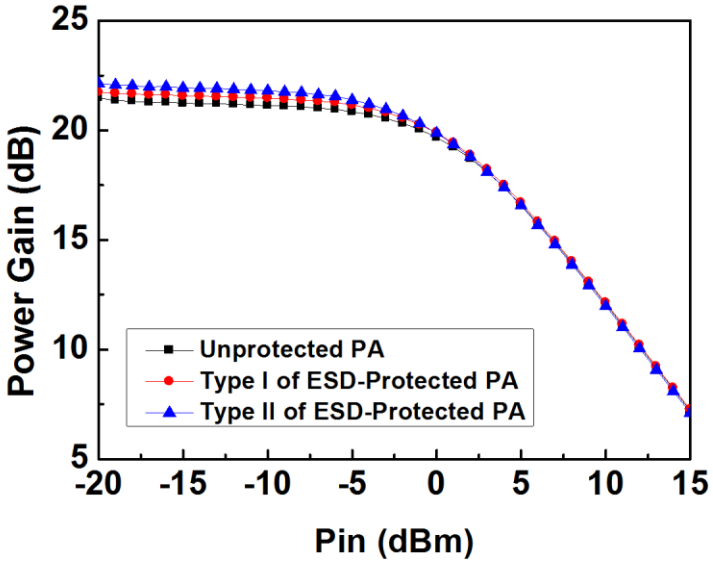


Fig. 4.33. Comparison of power gain of the unprotected PA and the ESD-protected PA.

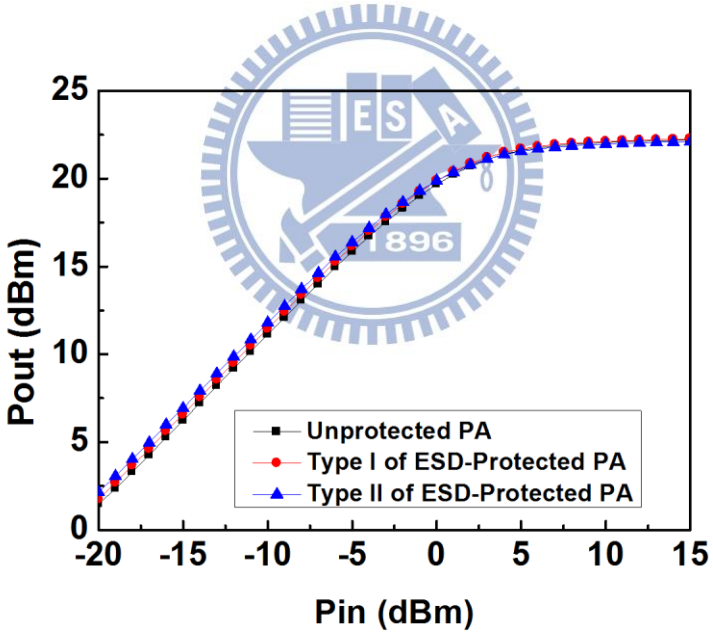


Fig. 4.34. Comparison of output power of the unprotected PA and the ESD-protected PA.

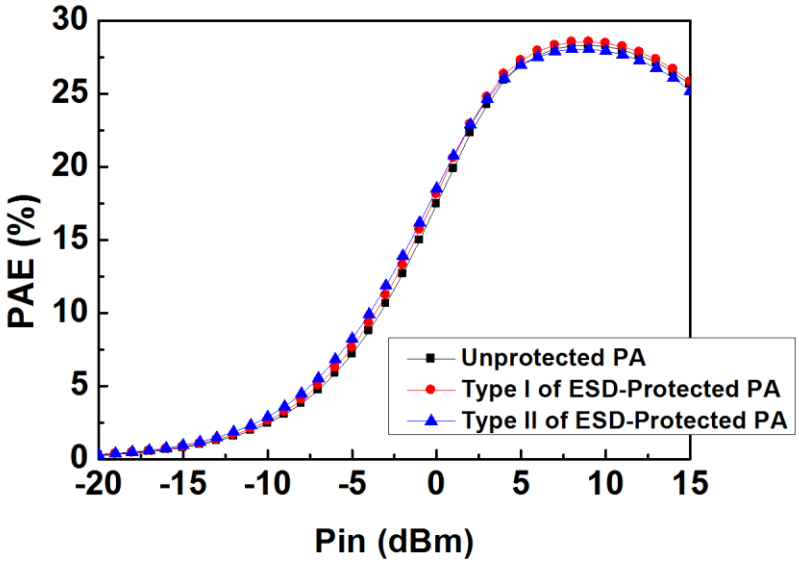


Fig. 4.35. Comparison of PAE of the unprotected PA and the ESD-protected PA.

4.5.5 Comparison of RF Performance after ESD Stress

To investigate the ESD protection ability of the ZTSCR, all the three test circuits were tested by HBM ESD zapping with every mode mentioned in section 4.5.2. The large signal characteristics of ESD-protected PAs were extracted with load-pull system by using the same optimal output impedance found for the unprotected PA. Figs. 4.36 to 4.38 show the RF performance of the unprotected PA after HBM ESD zapping. Figs. 4.39 to 4.41 show the RF performance of the type I of ESD-protected PA after HBM ESD zapping. Figs. 4.42 to 4.44 show the RF performance of the type II of ESD-protected PA after HBM ESD zapping. The measurement results are summarized in Table 4.7.

To investigate the failure mechanism of type II of the ESD-protected PA, emission microscope (EMMI) can be utilized to find the failure location. Fig. 4.45 shows the EMMI picture of type II of the ESD-protected PA after 4-kV HBM ESD zapping of every mode. The failure location is the ZTSCR added to E2 pad. Furthermore, the scanning electron microscope (SEM) picture is shown in Fig. 4.46. It is clear that the ZTSCR has been damaged. This failure mechanism indicates that the failed function of PA after HBM ESD zapping is

caused by the damaged ZTSCR. Since the ZTSCR is damaged earlier than the MOS transistor used in PA, trigger speed and clamp voltage of the ZTSCR is tolerable to the used MOS transistor when ZTSCR is applied to PA. Therefore, the ESD level of ZTSCR itself becomes crucial. If the ESD level of ZTSCR can be boosted, the ESD level of ESD-protected PA with ZTSCR would further enhance. One method is to enlarge the width of ZTSCR.

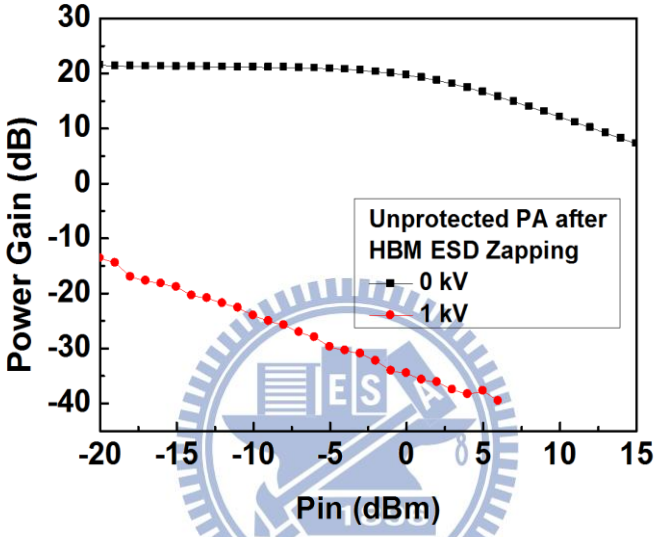


Fig. 4.36. Power gain of the unprotected PA after HBM ESD zapping.

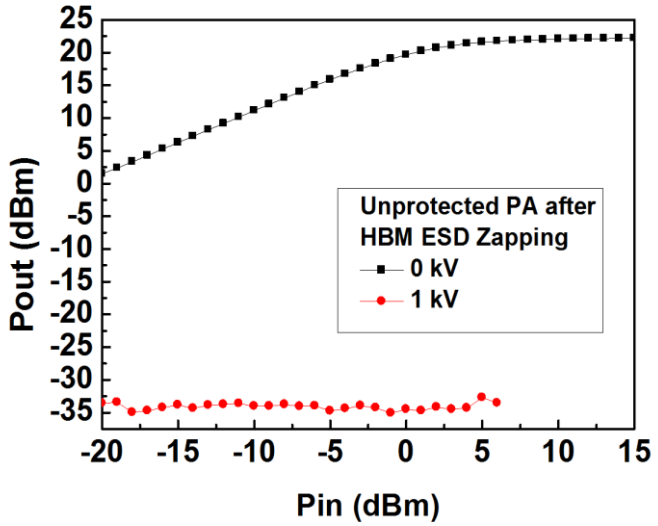


Fig. 4.37. Output power of the unprotected PA after HBM ESD zapping.

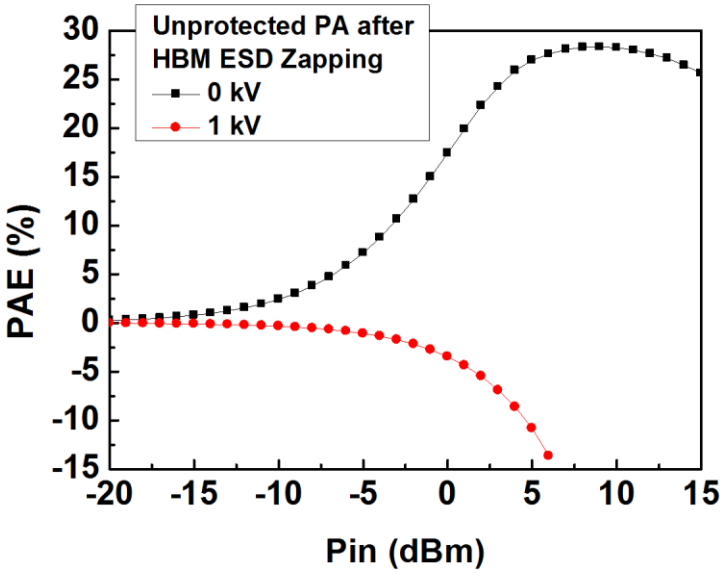


Fig. 4.38. PAE of the unprotected PA after HBM ESD zapping.

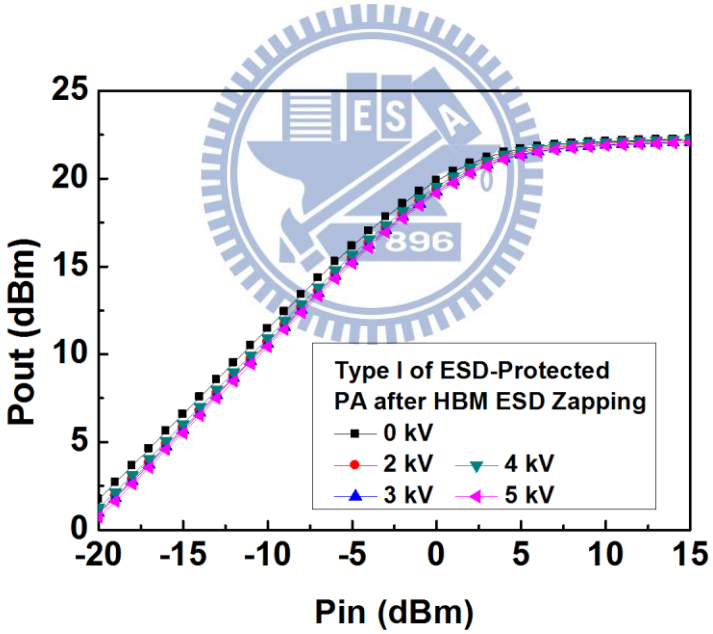
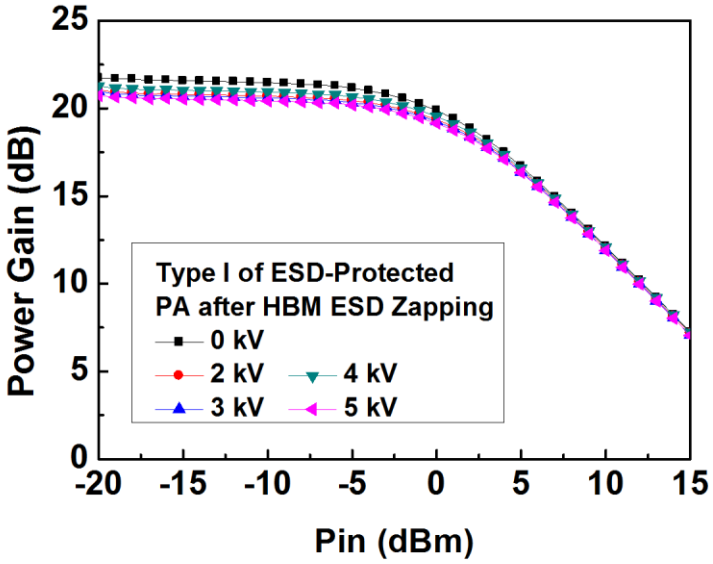
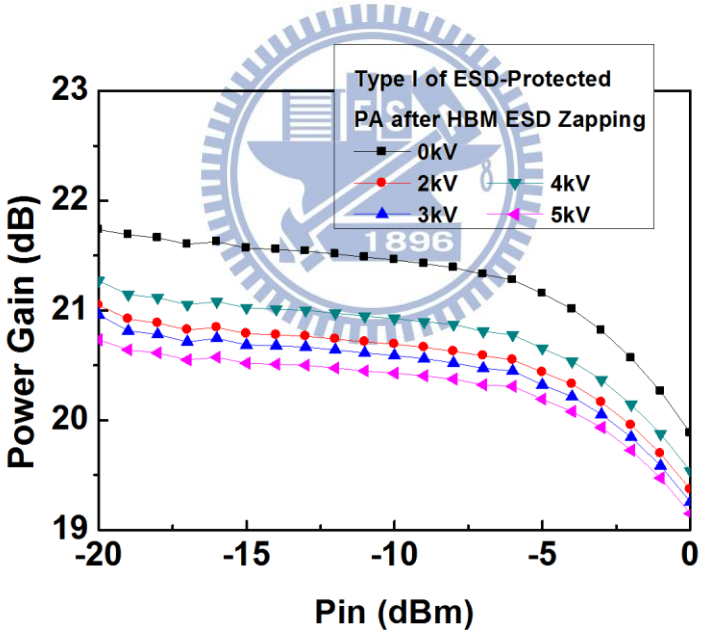


Fig. 4.39. Output power of type I of the ESD-protected PA after HBM ESD zapping.

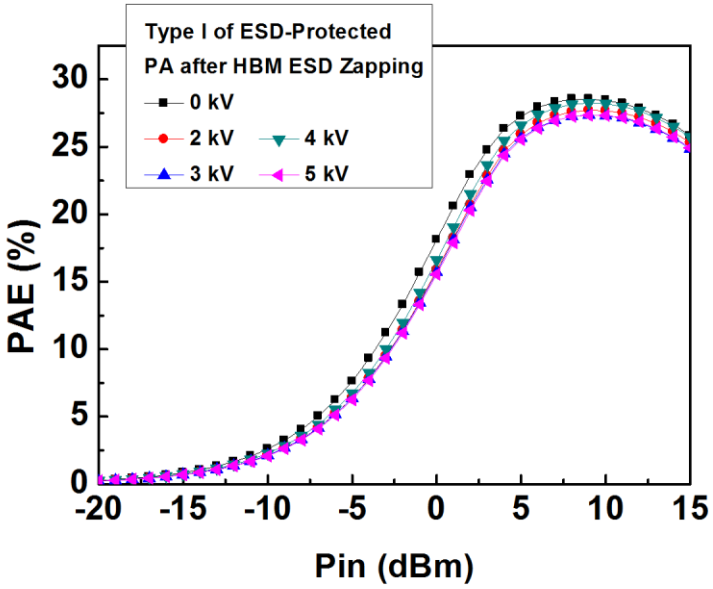


(a)

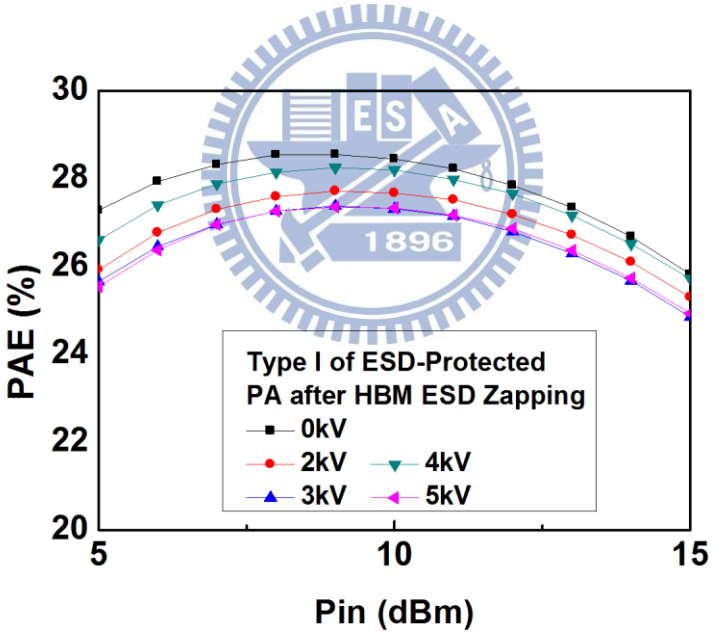


(b)

Fig. 4.40. Power gain of type I of the ESD-protected PA after HBM ESD zapping with input power ranging from (a) -20 dBm to 15 dBm and (b) -20 dBm to 0 dBm.

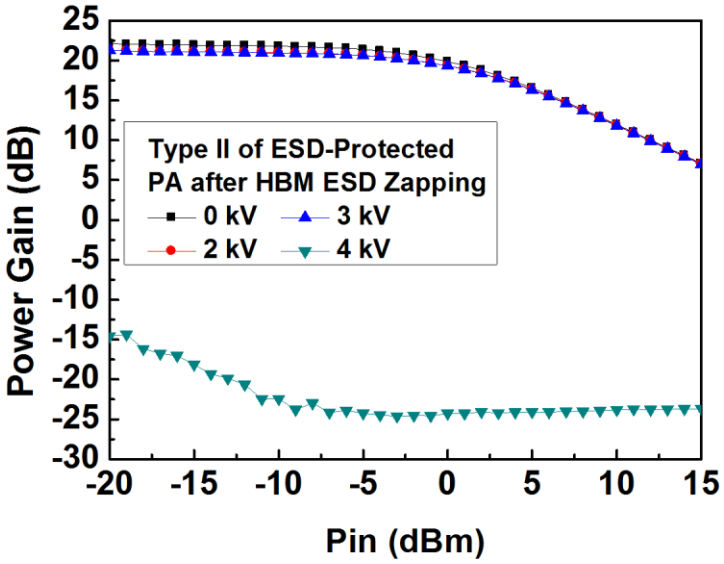


(a)

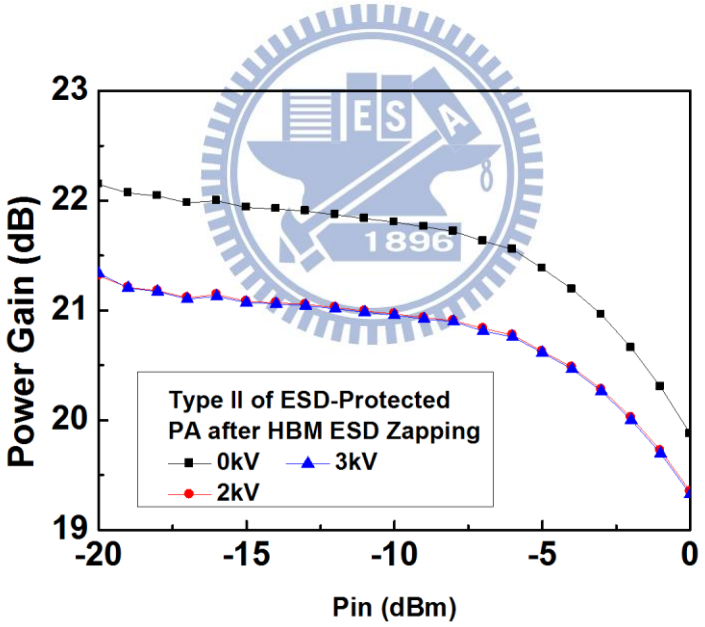


(b)

Fig. 4.41. PAE of type I of the ESD-protected PA after HBM ESD zapping with input power ranging from (a) -20 dBm to 15 dBm and (b) 5 dBm to 15 dBm.

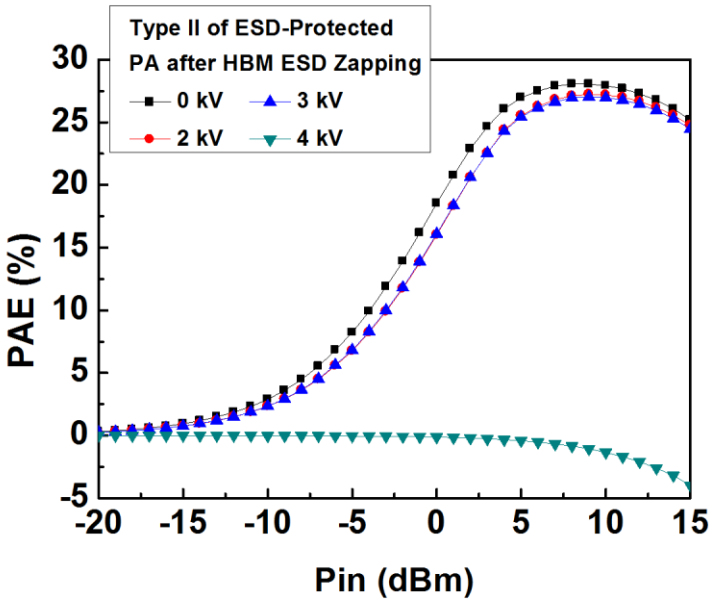


(a)

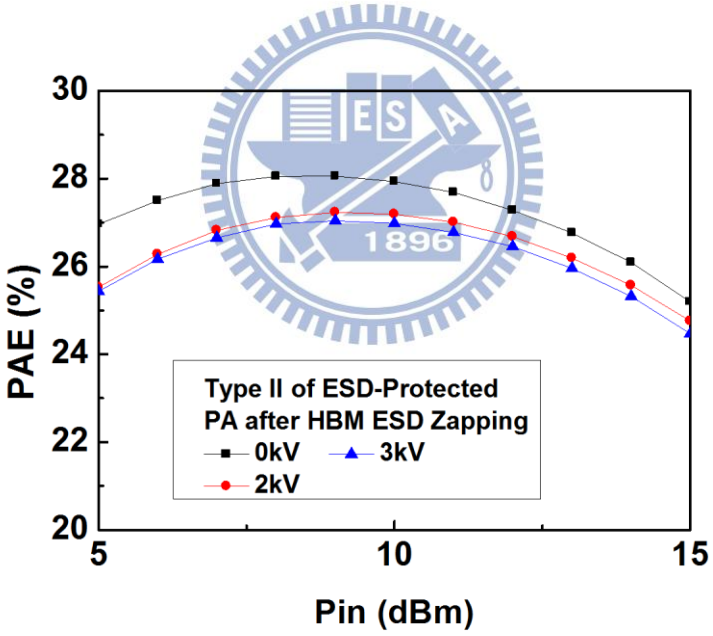


(b)

Fig. 4.42. Power gain of type II of the ESD-protected PA after HBM ESD zapping with input power ranging from (a) -20 dBm to 15 dBm and (b) -20 dBm to 0 dBm.



(a)



(b)

Fig. 4.43. PAE of type II of the ESD-protected PA after HBM ESD zapping with input power ranging from (a) -20 dBm to 15 dBm and (b) -20 dBm to 0 dBm.

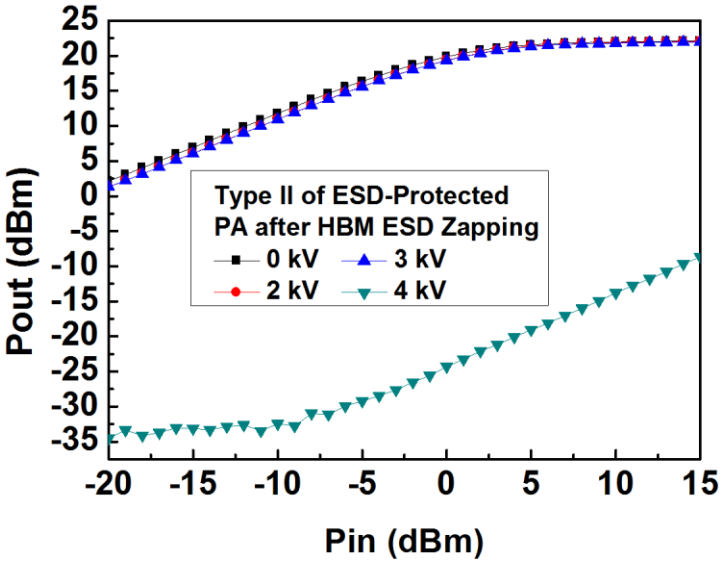


Fig. 4.44. Output power of type II of the ESD-protected PA after HBM ESD zapping.

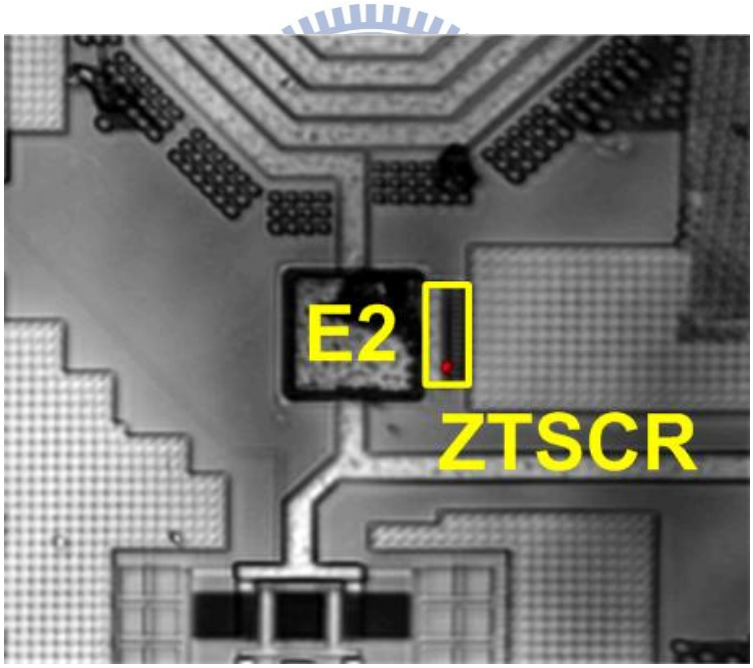


Fig. 4.45. EMMI picture of type II of the ESD-protected PA after 4-kV HBM zapping of every mode. The failure location is at the ZTSCR added to E2 pad.

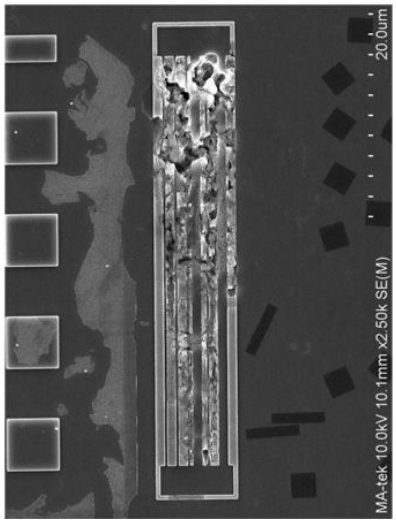


Fig. 4.46. SEM picture of type II of the ESD-protected PA after 4-kV HBM zapping of every mode.

Table 4.7
Summary of RF performance of the unprotected PA and the ESD-protected PA after HBM ESD zapping

		After HBM ESD Zapping					
		0 kV	**1 kV**	**2 kV**	**3 kV**	**4 kV**	**5 kV**
Maximum Output Power (dBm)	**Unprotected PA**	22.20	-33.57				
	Type I	22.26		22.16	22.08	22.2	22.05
	Type II	22.11		22.03	21.97	-8.67	
P1dB (dBm)	**Unprotected PA**	19.03	failed				
	Type I	18.57		18.70	18.59	18.14	18.47
	Type II	17.96		18.02	18.00	failed	
Maximum PAE (%)	**Unprotected PA**	28.32	-0.03				
	Type I	28.55		27.72	27.38	28.25	27.33
	Type II	28.06		27.23	27.04	0	
PAE at P1dB (%)	**Unprotected PA**	14.98	failed				
	Type I	13.30		13.54	13.46	11.96	13.31
	Type II	11.87		11.74	11.82	failed	

4.6 Discussion

Briefly, there are two targets to a successful RF ESD protection design. One is that the RF performance of circuits should not be degraded after the ESD protection design is added. Another one is that the ESD-protected RF circuits should have enough ESD robustness.

For PA circuits, the commonly used figures of merit are power gain, output power, P1dB, PAE, and so on. It is not easy to estimate the RF performance degradation of PA circuit caused by ESD protection device by purely measuring the parasitic capacitance or S-parameters of ESD protection device. Therefore, full-functional RF testing is needed for ESD-protected PA circuits to verify the effect caused by ESD protection device before being zapped by ESD stress. To verify the ESD level of ESD-protected PA circuits, there are two failure criteria after being zapped by ESD stress. One is 30% shifting in the I-V characteristic, another one is RF function failure. It has been demonstrated in [22] that the second method is more suitable and accurate for RF circuits.

The two types of ESD-protected PA were therefore being verified with full-functional RF testing before and after ESD stress. The measurement results before ESD stress show that the proposed ZTSCR would not cause serious RF performances degradation, and the measurement results after ESD stress show that the ESD-protected PA with ZTSCR have enough HBM ESD robustness.

The failure analysis of type II of the ESD-protected PA shows that the ESD level depends on ZTSCR as well as the MOS width used in PA. If the used MOS width is pretty large, the HBM ESD robustness of PA circuit may exceed that of ZTSCR itself. If the used MOS width is small, ZTSCR still provide about 3-kV HBM ESD robustness for PA circuit, which is approximately equal to the ESD robustness of ZTSCR itself. In conclusion, the size of ZTSCR should be chosen depends on the used MOS width of the stage it added to.

4.7 PA ESD Protection Design Consists of RF Choke Inductor and Power-Rail ESD Clamp Circuit

The above sections present ESD protection design for PA with an off-chip RF choke inductor at the output stage and PA with all RF choke inductors off-chip. In some other applications, the RF choke inductor at the output stage of PA may be on-chip. For this kind of applications, a probable ESD protection design is shown in Fig. 4.47.

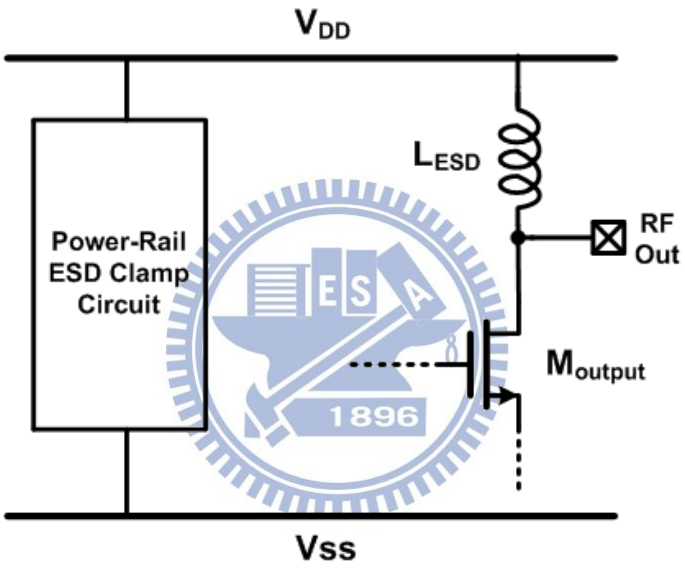


Fig. 4.47. ESD protection strategy for PA with the RF choke inductor L_{ESD} and a power-rail ESD clamp circuit.

Fig. 4.47 shows a simple structure of a PA with an on-chip inductor at the output stage and a power-rail ESD clamp circuit between V_{DD} and V_{SS} power lines. The M_{output} represents the transistor at the output stage of the PA. L_{ESD} is an RF choke inductor used to feed DC power to the PA circuit, which exhibits very low impedance at low frequency, and therefore can also be treated as a low-impedance path to ESD current under ESD events. Since PA is used to deliver large power, the RF choke inductor at the output stage needs to be designed with large metal width so as to sustain large current density. This characteristic is also

beneficial to treating the RF choke inductor as an ESD discharge path. In addition, a power-rail ESD clamp circuit is inserted between V_{DD} and V_{SS} power lines to provide ESD paths.

Fig. 4.48 and Fig. 4.49 show ESD discharge paths under every discharge mode. For PS-mode, the ESD current first goes through L_{ESD} and then be discharged through the power-rail ESD clamp circuit. For NS mode, the ESD current is discharged through the power-rail ESD clamp circuit and then goes through L_{ESD}. For PD-mode, the ESD current is discharged from the output pad to V_{DD} through L_{ESD}. For ND-mode, the discharge path is in an opposite direction. The ESD protection design merely consists of an on-chip RF choke inductor at the output stage of PA and a power-rail ESD clamp circuit, and contributes no parasitic capacitances to the RF output. Without extra ESD protection devices, the design complexity of RF circuit is greatly reduced.

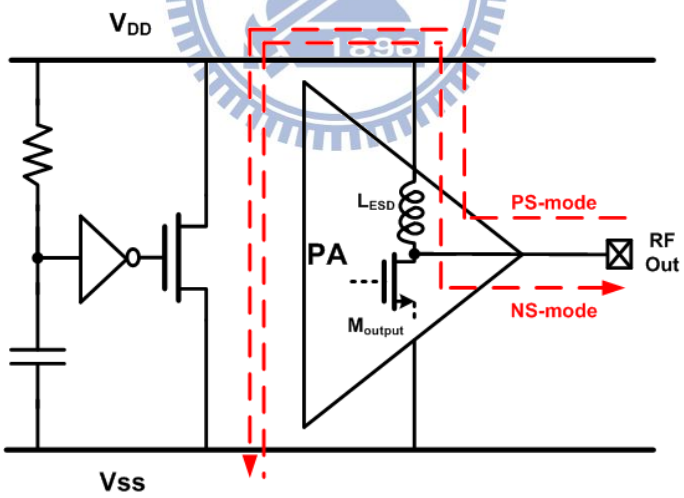


Fig. 4.48. ESD discharge paths under PS-mode and NS-mode ESD stress.

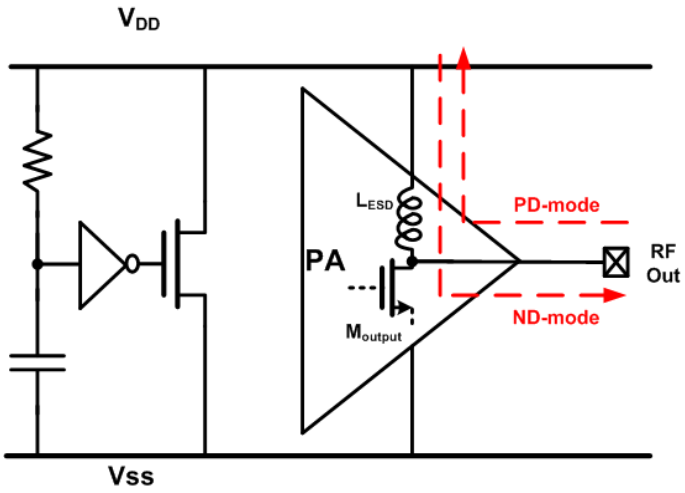


Fig. 4.49. ESD discharge paths under PD-mode and ND-mode ESD stress.

To implement this ESD protection design, a 2.4 GHz CMOS PA circuit which is shown in Fig. 4.50 has been designed as an ESD-protected PA. The output matching network was also removed from the test circuit for the same reason mentioned above. The used power-rail ESD clamp circuit is the same as that used in chapter 3.

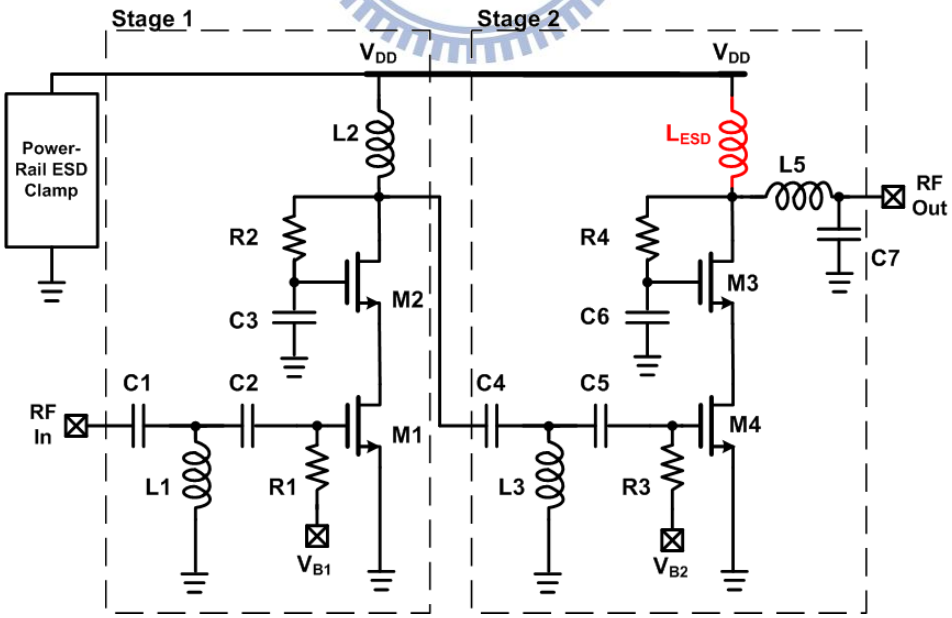


Fig. 4.50. Circuit diagram of the ESD-protected PA circuit.

This ESD protection design has been designed and fabricated in a 65-nm CMOS process.

Fig. 4.51 shows the die photo of the ESD-protected PA. The PS-mode, PD-mode, NS-mode, and ND-mode 4-kV ESD stresses were applied to the output pad of the ESD-protected PA. To investigate the ESD robustness, the S-parameters of ESD-protected PA before and after ESD zapping were measured with the vector network analyzer. The measured S_{21} parameters of the ESD-protected PA before and after 4-kV HBM ESD zapping of every mode mentioned above are shown in Fig. 4.52. According to Fig. 4.52, the S_{21} parameter still maintains well.

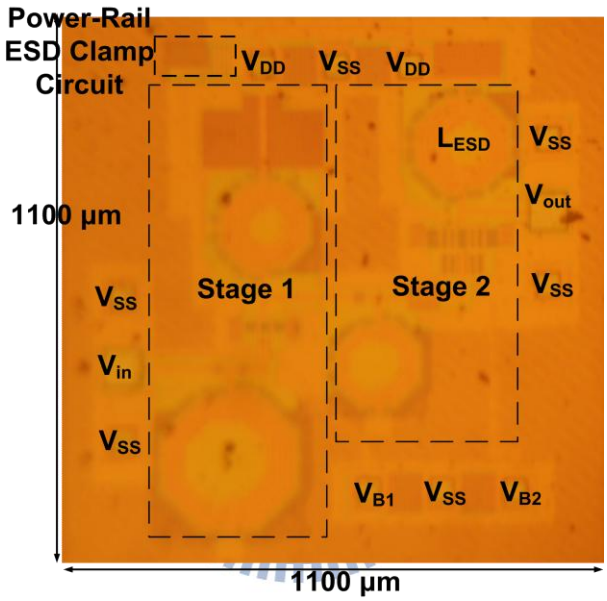


Fig. 4.51. Die photo of the ESD-protected PA.

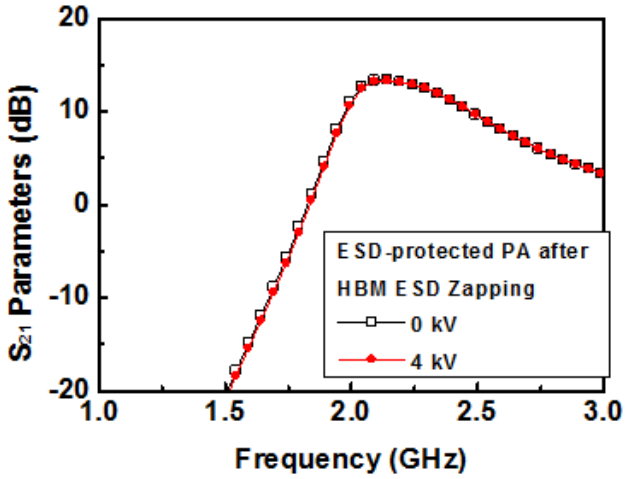
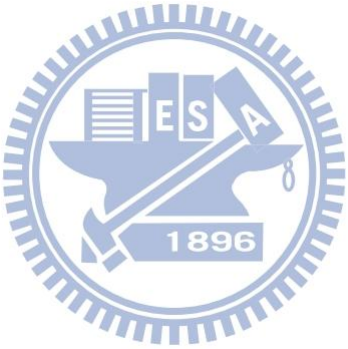


Fig. 4.52. Measured S_{21} parameters of the ESD-protected PA before and after HBM ESD stress of 4 kV.

The ESD protection strategy for PA with on-chip choke inductor at the output stage has been successfully verified in a 65-nm CMOS process. According to the measurement results, the S_{21} parameter of the ESD-protected PA after 4-kV HBM ESD zapping still maintains well. This ESD protection strategy merely utilizes an RF choke inductor of the PA circuits and a power-rail ESD clamp circuit, but can provide at least 4-kV HBM ESD robustness and decrease the complexity of RF circuits design.



Chapter 5
Conclusions and Future Works

5.1 Conclusions

In this thesis, the issues of RF ESD protection design are presented. The parasitic effects of ESD protection devices may cause signal loss, change input matching conditions, and induce other undesired RF performance degradation. Designing RF ESD protection devices or circuits with good ESD level and less influence on RF performance is quite a challenge. Two RF ESD protection design are proposed to advance this goal.

One is for 60 GHz RF circuits. Since the circuit operating frequency of 60 GHz RF applications is quite high, the parasitic capacitance of ESD protection design is greatly limited. The ESD protection design for 60 GHz RF circuits has been proposed, fabricated, and examined in a 65-nm CMOS process. The proposed ESD protection design simply consists of a pair of diodes, a supplement capacitor, and a series inductor and capacitor. The pair of diodes acts as ESD clamp device. The series inductor and capacitor are used to tune out the parasitic capacitances of ESD protection diodes. In addition, the supplement capacitor is added to lower the layout area. The proposed ESD protection design has small layout area and required 2-kV HBM ESD robustness with 1.8dB insertion loss at 60 GHz. Therefore, the compact ESD protection design for 60 GHz RF circuits can provide enough ESD level with tiny influence on RF performance. The proposed compact ESD protection design can be used for 60 GHz RF ESD protection.

Another one is for RF CMOS PA. PA plays an important role in RF ICs, but the ESD protection designs for CMOS PA have not been widely investigated. The ESD protection design for RF CMOS PA, named ZTSCR, has also been proposed, fabricated, and examined

in a 65-nm CMOS process. The ZTSCR is a Zener-diode-triggered SCR. With the well designed trigger mechanism, the ZTSCR is suitable for CMOS PA since the characteristics of PA has been involved in the design phase. Besides, a 2.4 GHz CMOS PA is also designed to verify the ESD protection ability of the ZTSCR. Three experimental circuits, including unprotected PA and two ESD-protected PA are fabricated in a 65-nm CMOS process. One ESD-protected PA is design for PA circuits with off-chip RF choke inductor at the output stage. Another one is for PA circuits with every RF choke inductor off-chip. The experimental results show that the unprotected PA has terrible ESD level, while the two types of ESD-protected PA have enough HBM ESD level. Moreover, the measurement results before ESD stress also show that the ZTSCR would not influence the RF performances of PA under normal operating conditions. The experimental results reveal the truth that the ZTSCR indeed do its work. Therefore, the proposed ZTSCR for PA ESD protection can provide enough ESD level without serious PA performances degradation. Besides, an ESD protection design for PA with on-chip RF choke inductor at the output stage is also fabricated and verified in a 65-nm CMOS process. For such kind of PA applications, the simple ESD protection strategy consists of an on-chip RF choke inductor and a power-rail ESD clamp circuit can provide enough HBM ESD level without serious PA performance degradation.

5.2 Future Works

The proposed ZTSCR is for PA with output voltage swing higher than $2 \times V_{DD}$. However, it may not be suitable for class-E PA. Since the output voltage swing of a class-E PA would higher than $3.6 \times V_{DD}$, the trigger voltage of the proposed ZTSCR is too low to avoid being mistriggered. Unfortunately, boosting the trigger voltage of SCR will decrease its ESD level. In order to apply the ZTSCR to class-E PA, the ZTSCR still needs some modification.

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Vita

姓　　名：蔡　翔　宇

學　　歷：

台北市立建國高級中學　　(91 年 9 月~94 年 6 月)

國立交通大學電子工程學系　　(94 年 9 月~99 年 6 月)

國立交通大學電子研究所碩士班　　(99 年 9 月~101 年 9 月)

研究所修習課程：

類比積體電路	吳介琮 教授
數位積體電路	周世傑 教授
積體電路之靜電放電防護設計特論	柯明道 教授
類比濾波器設計	陳巍仁 教授
半導體物理及元件(一)	汪大暉 教授
射頻積體電路	郭建男 教授
數位通訊	林大衛 教授
奈米電子元件	荊鳳德 教授

永久地址：新北市板橋區國慶路 149 巷 10 號 3 樓

Email：kplus.ee94@nctu.edu.tw

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(A) Referred Journal Paper:

[1] C.-Y. Lin, L.-W. Chu, **Shiang-Yu Tsai**, and M.-D. Ker, "Design of compact ESD protection circuit for V-band RF applications in a 65-nm CMOS technology," *IEEE Trans. Device Mater. Reliab.*, vol. 12, no. 3, pp. 554-561, Sep. 2012.

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(B) International Conference Papers:

[1] C-Y. Lin, L.-W. Chu, **Shiang-Yu Tsai**, M.-D. Ker, T.-H. Lu, T.-L. Hsu, P.-F. Hung, M.-H. Song, J.-C. Tseng, T.-H. Chang, and M.-H. Tsai, "Modified LC-tank ESD protection design for 60-GHz RF applications," in *Proc. European Conf. Circuit Theory and Design*, 2011, pp. 57-60.

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(C) Local Conference Paper:

[1] 竹立煒、林群祐、**蔡翔宇**、柯明道、盧澤華、許村來、洪彬舫、宋明相、曾仁洲、張子恒、蔡銘憲,"以改良式電感電容共振腔實現之60-GHz射頻靜電放電防護電路," in *Proc. Taiwan ESD and Reliability Conference*, 2011, pp. 50-53.

(D) Patent:

[1] L.-W. Chu, C.-Y. Lin, **Shiang-Yu Tsai**, M.-D. Ker, M.-H. Tsai, T.-L. Hsu, C.-P. Jou, "ESD protection design for high-speed interfaces," U.S. and R.O.C. patent pending.