國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩 士 論 文

單晶片微加速度計與可調式靈敏度讀出電路整合設計

Design of a Monolithic Micro-accelerometer with a Readout Circuit of Tunable Sensitivity

研 究 生：林易達　　Yi-Da Lin

指導教授：溫瓌岸 博士　　Dr. Kuei-Ann Wen

中 華 民 國 一0一 年 9 月

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摘　要

本論文提出一單晶片微加速度計與可調式靈敏度讀出電路整合設計，此感測系統在標準 0.18um 製程下製作。藉由讀出電路可調增益的功能可以使此感測系統更廣泛的應用在各種不同的加速度環境。

本論文的低雜訊可調增益前置放大器採取開迴路的連續時間電壓感測並採取二次截波穩定搭配雙相關取樣解調功能以達到抑制低頻雜訊和直流偏移誤差的目的，最後經由三角積分類比數位轉換器將訊號數位化。根據模擬結果，可調靈敏度範圍從 324.8 mV/fF 到 17425.47 mV/fF，訊號對雜訊諧波失真比 80dB，有效位元 12 位元。根據量測結果, 前置放大器電路的等效輸入加速度雜訊可以被抑制到 29.41ug/√Hz，總功耗 1.043mW。

Design of a Monolithic Micro-accelerometer with a Readout Circuit of Tunable Sensitivity

Student: Yi-Da Lin Advisor: Dr. Kuei-Ann Wen

Department of Electronic Engineering

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Abstract

The accelerometer is fabricated in 0.18μm ASIC-compatible CMOS MEMS technology and, with the assistant of low noise gain tunable interface being combined with 2nd Sigma-Delta Modulator (SDM) A/D converter in the proposed work. The linear decibel variable gain amplifier (VGA) can regulate the output signal level between sensor signals and external forces. It makes the newly proposed monolithic CMOS MEMS accelerometer with low noise gain tunable interface more applicable to various applications.

The new approach of the low noise preamplifier combines the Dual-Chopper amplifier (DCA) and Correlated Double Sampling (CDS) demodulation technologies to alleviate 1/f noise and DC offset. According to the simulation results, the tunable sensitivity can be adjusted from 324.8mV/fF to 17425.47mV/fF in differential mode. SNDR is 80dB, ENOB is 12bit. According to the measurement results, The circuits noise equivalent acceleration (CNEA) is 29.41ug/$\sqrt{}$Hz. The total power consumption is limited to 1.043mW.

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林易達

2012 年 9 月

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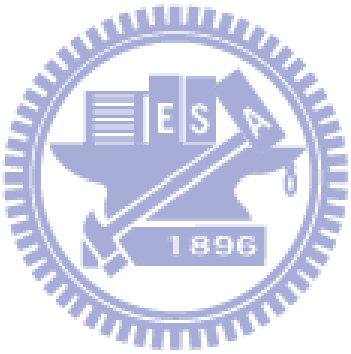

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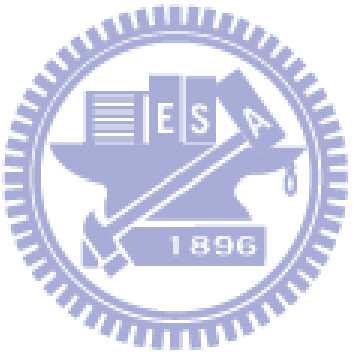


Chapter 1

Introduction

Over the past thirty years, advance in micro-fabrication have enabled the integration of multiple miniaturized sensors and actuators with analog and digital microelectronic circuits to create micro-electromechanical-systems (MEMS). Among these kinds of MEMS products, the inertial sensor is one of the useful devise to detect the force (acceleration) from external environment. It is so called accelerometer. It has been used on most automotive like Air-Bag, Electronic Stability Control, conventionally. The more applications of accelerometer has developed such as consumer electronics, sports, health care, and military industry. Especially, high-sensitivity accelerometers are crucial components in inertial navigation system (INS), seismometers for oil exploration, earthquake prediction, and microgravity measurements. In order to adapt the all kinds of the application, the universal sensing system must be developed.

There are many different types' inertial sensors in micromechanical devices. 1. Piezoelectric accelerometers, most piezoelectric accelerometers have the piezoelectric material. When the accelerometer is subjected to vibration, a force is generated which acts on the piezoelectric element (quartz, Lead-Zirconate-Titanate, and so on). This force is equal to the product of the acceleration and the mass. Due to the piezoelectric effect a charge output proportional to the applied force is generated.

The prices of these products are usually much higher because of the special materials. 2. Piezoresistive accelerometer uses semiconductor material which responses mechanical stress with changing resistivity. But Piezoresistive sensing has inferior

performance due to intrinsic resistor thermal noise and strong temperature dependence. 3. Tunneling devices require an extremely small gap between tip and electrode (< 10 Angstrom) and high voltage (>10V), they are very expensive to fabricate and difficult to integrate. 4. Capacitor sensing system composes of a mass, spring with inter-digital electrode fingers. The deviation of the inter-digital fingers are produced by the moving proof mass, then base on the charge conservation theorem, the charge transfers to voltage signal or current signal. Moreover, the characters of low temperature coefficients and insensitive to the external environment increase the reliability when the ICs are working. This is why the capacitance sensing accelerometer plays a leading role in the 3C products.

In terms of process, Micro-fabrication methods are generally classified into two main categories: *surface* micromachining and *bulk* micromachining. In bulk micro-machined, micro-structure is carved from the silicon substrate by the methods used in IC fabrication, and defines structures by selectively etching inside a substrate (wafer), surface micromachining creates structures on top of a substrate by using a succession of thin film deposition and selective etching. Thus, it features a large proof mass and large capacitor area that lead to higher sensitivity and higher resolution approaching micro-gravity (μg). But the applications are limited by its cost and package size. Different from bulk micro-machining, surface micromachining builds the microstructures by deposition and etching of different structural layers on top of the silicon substrate. The added layers are generally very thin with their size varying several micro meters, hence the proof mass is small on the order of 10^{-9} Kg, resulting in limitations on the performance of the accelerometer such as large Brownian noise and

low sensitivity.

Despite the congenital conditions are inferior to bulk micro-machined, the advantages of CMOS MEMS in *surface* micromachining are still attractive on the commercial considerations. In conclusion, the CMOS MEMS capacitance accelerometer in *surface* micromachining can be fabricated with minor add-on post processes and have high compatibility with VLSI technology, so the low cost much easier achieved compared to the other types accelerometer. Therefore, the enormous efforts on high performance readout front-end has outstanding achievements in many literatures [2][3][4][5], that confirm the feasibility of CMOS MEMS accelerometer in *surface* micromachining. Base on that, the thesis focuses on CMOS MEMS accelerometer and completes a design flow with the CoventorWare advanced software MEMS+. In the MEMS+, the accelerometer device is a parametric model which could be directly simulated with CMOS circuits in Cadence SpectreRF.

1-1 Motivation

The low mass accelerometers always suffer from large Brownian noise, which interferences the signal accuracy. The rough solution is to increase the weight of the proof mass, but it also increases cost on large area of the MEMS structure. By means of careful design between the readout circuit architecture and sensor structure stiffness will be more feasible. The Brownian noise can be suppressed compared to [5], which is in the same post process. Besides, the vacuum package is another methodology to reduce Brownian noise.

In the readout circuit part, the CMOS circuits are implemented by voltage control

field effect transistor (FET), thus the inherent low frequency noise (flicker noise or 1/f noise) and thermal noise both are bound to be suppressed. Besides, the process variation always causes the mismatch between transistors pair, the DC offset will be the significant problem on the circuit normal operation. The chopper stabilized amplifier and correlated double sampling are the most powerful techniques to deal with the non-ideal effect of the CMOS circuits.

The CMOS MEMS structures after post process always appears the undesired phenomenon due to thermal effect and residual stress such as the structure out-plane curling (warping stress), the structure in-plane curling (position deviation of sensing finger). They always decrease the sensitivity of accelerometer, introduce more non-linear terms, and produce unnecessary signal in noise rejection readout circuits such as Chopper Stabilized Amplifier (CHS), Correlated Double Sampling (CDS).

In order to fulfill high performance universal circuit for different application, the proposed work inherits low noise low power circuit technique with the assistant of voltage control linear Variable Gain Amplifier (VGA) and includes three methodologies to overcome the non-ideal phenomenon after post process. A universal readout interface is suitable for different applications of the acceleration detection, and the applications for different acceleration range detections are listed in the table 1.1.

Table 1.1: Acceleration applications

Applications	**Acceleration**
Drop protection	±1G
Handheld device	±3G
Human dynamics (walking, jogging)	±4G
Abrupt activities (gaming)	±8G
Electronic stability program(ESP)	±10G

1-2 Mixed-signal CMOS MEMS Accelerometers

1-2.1 CMOS MEMS Process

In order to achieve the goal of integration of the system-on-chip (SOC), the accelerometer is fabricated in National Chip Implementation Center (CIC) 0.18μm mixed -signal/RF one-poly six-metal (1P6M) with CMOS readout interface. By way of a sequence of deposit, stacking, etching, a multilayer structure is formed in the standard 0.18μm CMOS IC process as shown in Figure 1-2.1(a). The multilayer structure facilitates the complex signal routing. The PAD region is defined as a MEMS structure, and the passivation layer provides a protection on the other CMOS circuits during the MEMS process.

The post process only requires an additional RLS mask. This is used to identify the etching region on oxide and silicon substrate. To facilitate MEMS device movements, the depth of etching hole usually up to 12 um above. And the main etching technology provided by CIC is the dry etching, which is much easier to obtain a high aspect ratio micro-structure.

After the COMS processing done, an anisotropic CHF_3 reactive ion etch (RIE) is the first steps to etch away SiO_2 where are not Coated with photoresist, resulting in vertical sidewalls, as shown in Figure 1-2.1(b).

In order to obtain a complete vacant structure, the final step is isotropic (SF_6) etching as shown in Figure 1-2.1(c), which is used to etch the silicon substrate and release the microstructures.

The minimum etching width and two metal layers are separated at least 4 um in design rule as shown in Figure 1-2.1(d) [8].

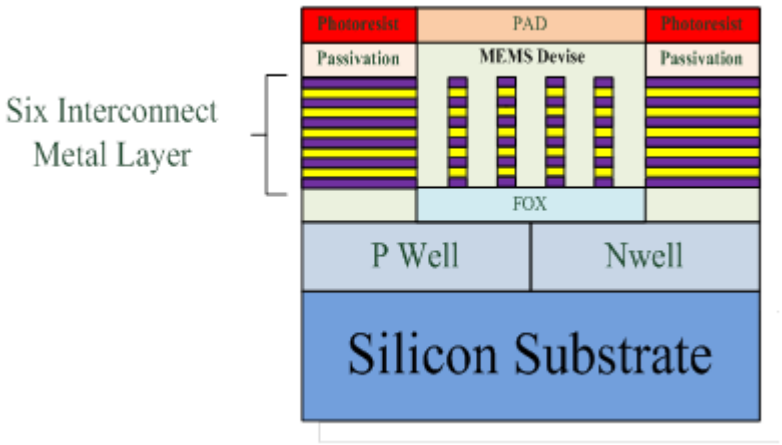


Figure 1-2.1(a): The cross-section view of 1P6M IC structure

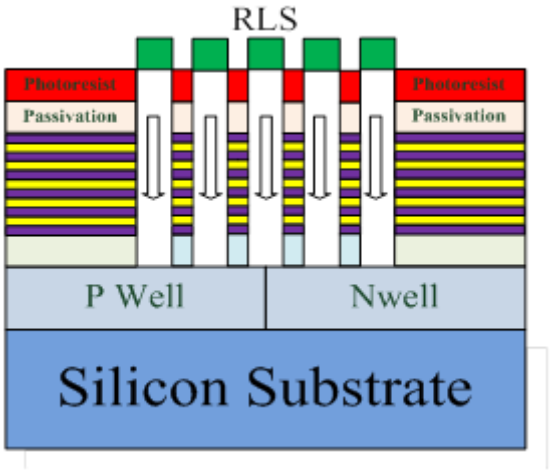


Figure 1-2.1(b): Photoresist protective coating and the oxide layer anisotropic etching

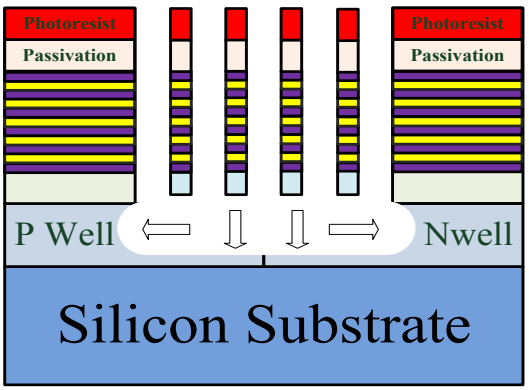


Figure 1-2.1(c): Isotropic etching

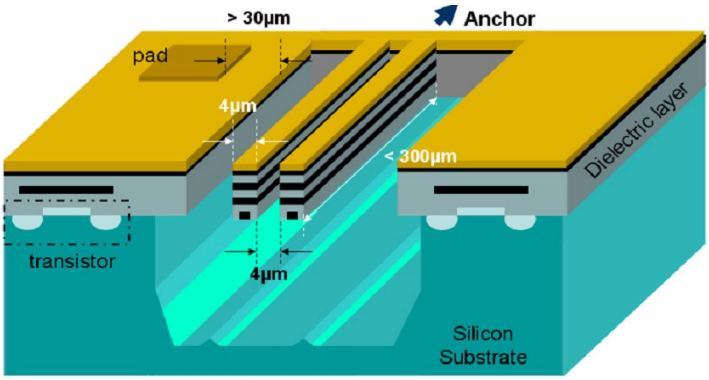


Figure 1-2.1(d): CMOS MEMS design rule

1-2.2 CMOS MEMS Accelerometer Model

Mechanical Model

The typical capacitive sensing accelerometer consists of proof-mass, folded springs, anchors, and inter-digital comb fingers as shown in Figure 1-2.2(a). When the accelerometer subject to the external acceleration, the proof-mass moves parallel to the external acceleration and press the folded springs with a force ma_{in} according to "Newton's second law of motion" where m is the weight of the proof mass, a_{in} is the external acceleration. At the same time, the moving changes the distance between movable finger and fixed fingers. And then the capacitances vary in differential mode if the sensing capacitors are perfect symmetry. A lumped-parameter schematic of the mass-damper system is shown in Figure 1-2.2(b).

The specifications of the proposed accelerometer depends on the physical characters such as the weight of the proof mass, the length of the comb fingers, turns number of the folded spring, and so on.

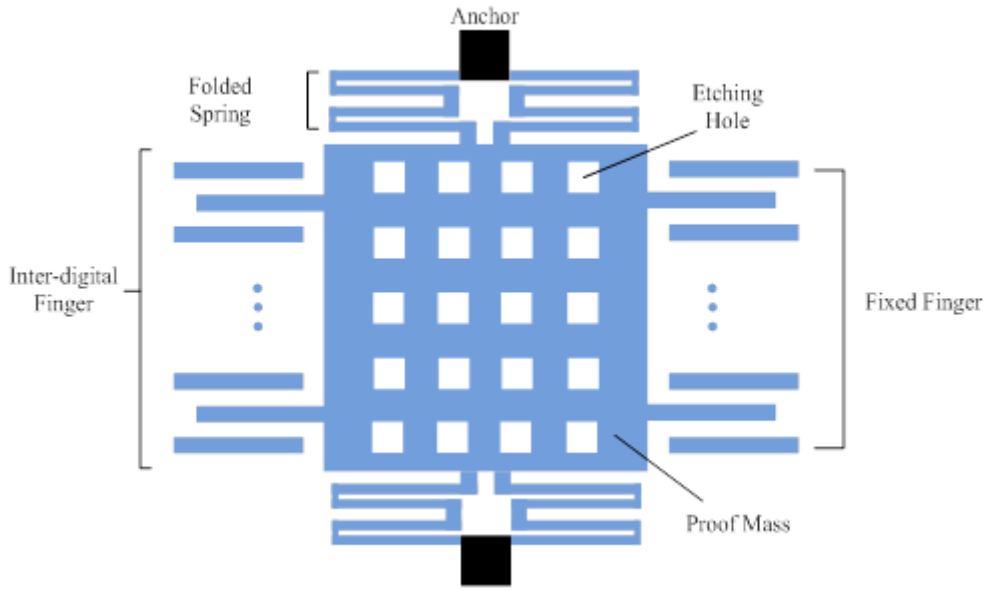


Figure 1-2.2(a): The typical capacitive sensing accelerometer schematic

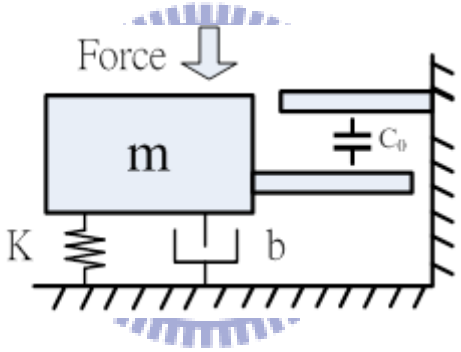


Figure 1-2.2(b): Accelerometer mechanical lump models

The motion equations of the accelerometer can be described in second order differential equation as follow:

$$\mathrm{m}\frac{d^2x}{d^2t} + b\frac{dx}{dt} + kx = \mathrm{m}a_{in} \qquad (1\text{-}2\text{-}1)$$

Where m is the weight of the proof mass, b is the damping coefficient, x is the displacement, and k is the spring constant. By the Laplace transformation, the differential equation can be transformed into the s-domain. The transfer function of the accelerometer is given by:

$$T(s) = \frac{X(s)}{a_{in}} = \frac{1}{s^2 + \frac{w_n}{Q}s + w_n^2} \quad (1\text{-}2.2)$$

Where W_n is the natural frequency, if the operational frequency is always much lower than it's natural frequency, the natural frequency can be approximated to

$$W_n = \sqrt{\frac{k}{m}} \quad (1\text{-}2.3)$$

The system settling time directly relates with the mechanical quality factor as:

$$Q = \frac{\sqrt{Km}}{b} \quad (1\text{-}2.4)$$

b is the damping coefficient. A device is said to be under-damped if Q>0.5, critically damped if Q=0.5, and over-damped if Q<0.5.

Spring

The folded beam springs are used to maintain system equilibrium after sense acceleration. The spring constant decides the natural frequency, sensitivity, and quality factor, so its character parameters include width, length of beam, and turn number, as shown in Figure 1-2.2(c). The spring constant in the Y-axis is given by:

$$k_y \propto Et\left(\frac{w}{L}\right)^3 / N \quad (1\text{-}2.5)$$

The spring constant of a folded-beams in the sensing axis and the out-plane axis relates to (1-2.5) and (1-2.6) respectively with the cross-axis rejection ratio described in (1-2.7).

$$k_z \propto Ew\left(\frac{t}{L}\right)^3 / N \quad (1\text{-}2.6)$$

$$k_z / k_y \propto \left(\frac{t}{w}\right)^2 \quad (1\text{-}2.7)$$

Where E is multilayer structure effective young's modulus of elasticity, and w, l, and t

are the beam width and length and thickness, respectively. (1-2.7) implies that high aspect ratio of the spring structure offers good cross axis rejection ratio.

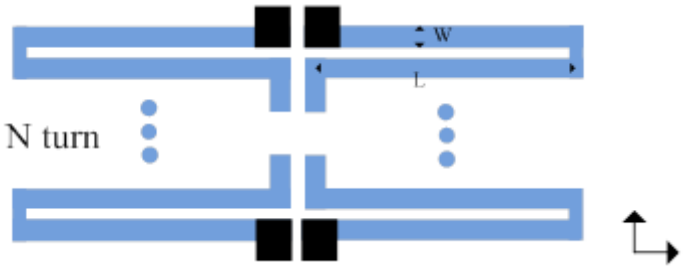


Figure 1-2.2(c): Multi-turn folded-beam spring

Sensing Capacitor

The sensing capacitor consists of the moveable fingers on the edge of proof mass and fixed fingers are connected with silicon substrate. The sensing comb fingers in the 1P6M process are connected with each other by tungsten via. The schematic diagram is shown in Figure 1-2.2(d). The single sensing capacitance is calculated in the simplest form, neglected fringe field effect:

$$C_0 = \varepsilon_0 \varepsilon_r \frac{L_{ov} t_0}{d_0} \tag{1-2.8}$$

Where ϵ_0, and ϵ_r are air electrical permittivity and oxide relative permittivity, d_0, L_{ov}, and t_0 are the air gap width, length and thickness of the metal stack

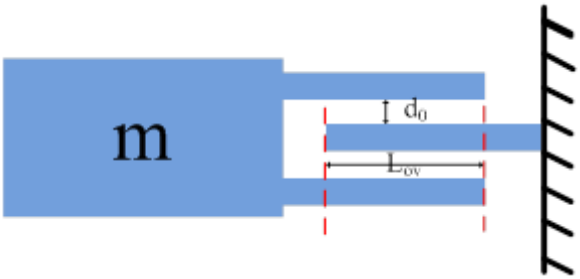


Figure 1-2.2(d): Accelerometer lumped model

Squeezed Film Damping

The damping factor comes from the friction between the vibration objects and the air. The dominant damping mechanism in X-Y plane is the squeezed-film damping and the squeezed-film damping can be molded as:

$$b \approx 7.2N\frac{\mu L_{ov} t^3}{d^3} \tag{1-2.9}$$

N is number of the comb fingers. $\mu(1.85 \times 10^{-5}\, N \cdot \frac{s}{m^2})$ is the viscosity of the air under atmospheric pressure at room temperature. L_{ov} is the finger overlapped length, t is the finger thickness, and d is the air gap width.

Brownian Noise

Mechanical in the fluid always has the random Brownian motion by air damping, it causes a random force in the sensing system. The power spectral density (PSD) of the Brownian noise is molded as follow:

$$\overline{A_n^2} = \frac{4k_B Tb}{9.8^2 m^2}\, G^2/Hz \tag{1-2.10}$$

Where K_B is Boltzmann's constant (1.38×10^{-23} J/K), T is temperature, b is damping factor and m is the weight of proof mass in kg.

It is also viewed as a kind of input-referred noise for readout circuit. And the Brownian noise equivalent acceleration (BNEA) is expressed as:

$$BNEA = \frac{\sqrt{4K_B\, Tb}}{9.8m}\, G/\sqrt{Hz} \tag{1-2.11}$$

1-2.3 Non-ideal Effect on CMOS MEMS Accelerometer

Structure Out-plane Curling

During the post-process, because of the different thermal expansion coefficients in

six metal–dielectric stacked structure, the sensing fingers always tend to curl in opposing directions (out-plane-curling) as shown in Figure 1-2.3(a), and the sidewall sensing capacitance will be significantly reduced. With proper design as shown in Figure 1-2.3(b) which takes advantage of good local matching of curl to solve the problem of indeterminate sidewall capacitor [9]. The stator and proof-mass fingers are fixed along with a common axis, with the stator connected to a cantilevered frame that is rigid compared with the proof-mass suspension. As a result, the inter-digital fingers will curl in line and provide maximum sidewall capacitor.

In the consequence, the curling effect decreases the stationary capacitance and the sensitivity of the sensing readout. Moreover, the output will be introduced more non-linear terms.

The enclosure at the edge of the accelerometer is called “rigid frame”. And a rigid frame of the accelerometer structure is also adopted to match the out-plane curling in this work.

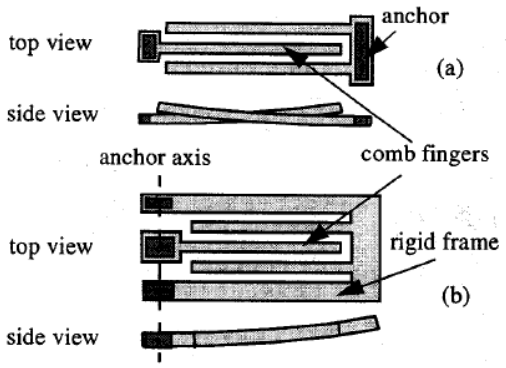


Figure 1-2.3(a): Comb fingers without curling matching; (b): with curling matching [9]

Structure In-plane Curling (Position Offset)

Due to the manufacturing misalignment of the embedded metal layers that creates

stress gradient, so the sensing fingers could be not so straight in line. The situation is a little different from “Out-plane curling”, the movable fingers at the edge of proof-mass bend upward or downward to the anchored fingers in the two dimensions plane (X-Y axis), and leading to imbalance in fully bridge stationary capacitor as shown in Figure 1-2.3(c). It is also called sensor position offset.

In the consequence, the capacitance deviation will exist in fully bridge stationary capacitor when the external acceleration is zero. The asymmetry sensing capacitances are viewed as the acceleration which is applied at the system input continuously for readout circuit. In other words, the position offset produces an undesired acceleration signal in the readout circuit, the unnecessary signal can be large enough to block the useful signal. Since the offset is dynamic as an AC signal in most readout interface such as CHS and CDS, it is also called “AC offset in [2].

Since the AC offset and the detected signal are modulated (or sampled in SC circuit) at the same clock frequency, they are almost impossible to be separated only by filter or to be blocked by ac coupling or to use offset storage technique as DC offset in CMOS circuit. The sensor offset could only be removed by trimming or calibration, the pros and cons of them will be discussed with readout interface architecture.

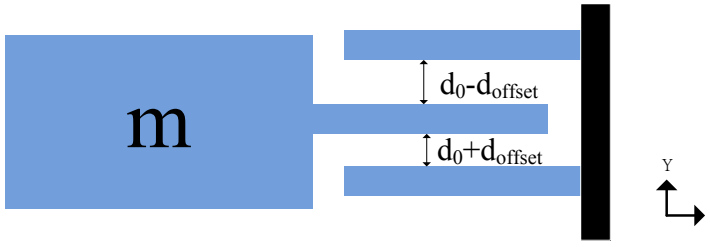


Figure 1-2.3(c): The position offset of the sensing capacitance

1-3 Front-end Pre-amplifier Survey

The whole sensing system includes a low noise gain tunable pre-amplifier and a second order Sigma-Delta Modulation (SDM) analog-to-digital converter (A/D). By using the oversampling and noise shaping (it will be discussed in next chapter), the higher resolution can be easier achieved than conventional Nyquist A/D in the same limited chip area. However, the noise shaping can't deal with the noise at the SDM input, a low noise pre-amplifier must be designed for the weak signal of the CMOS accelerometer.

Besides, the weak signals from CMOS MEMS accelerometer are susceptible to be interfered from any other noise source from circuit part such as flicker noise from CMOS transistor, thermal noise in data sampling switches, resistors, and capacitors. How to reduce the noise source as possible becomes a critical issue for high resolution sensing system currently. Follow the developments of low noise pre-amplifier step by step, a low noise gain tunable pre-amplifier is improved in our approach. First, realize the operation principle of the accelerometer. Second, distinguish the different configuration of diversification readout circuits.

1-3.1 Capacitive Accelerometers Operation Principle

Figure 1-3.1(a) shows the variation of sensing capacitance as an external acceleration is subjected to the sensing system. V_{mp} and V_{mn} are the modulation signals, d_0 is the gap of the comb fingers, and C_0 is the sensing capacitance when the movable inner plate is at the center. Δd is very small compared to d_0 , so the sensed voltage at the sensing node can be approximated as:

$$V_{sense} = \frac{2C_0}{2C_0+C_p}\frac{\Delta d}{d_0}V_m \quad (1\text{-}3.1)$$

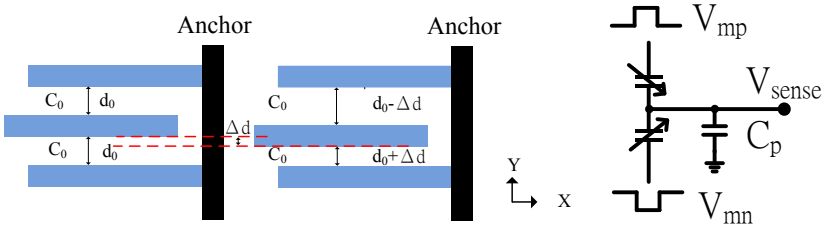


Figure 1-3.1(a): The schematic of the capacitance variation

Besides, the acceleration bandwidth is limited by the nature resonate frequency ω_0, and the transducer sensitivity is related to the nature resonate frequency as:

$$S = \frac{\vec{\Delta d}}{\vec{a}} = \frac{1}{{\omega_0}^2} \quad (1\text{-}3.2)$$

Where Δd is the displacement, a is the acceleration. Combining (1-3.1) and (1-3.2) , the transducer sensitivity of the accelerometer is given by:

$$S = \frac{V_{sense}}{a} = \frac{2C_0}{2C_0+C_p}\frac{V_m}{d_0}\frac{1}{{\omega_0}^2} \quad (1\text{-}3.3)$$

1-3.2 Capacitive Pre-amplifier

Flicker Noise and DC Offset Reduction Pre-amplifier

For CMOS circuit, the main noise source is the flicker noise which is inversely proportional to frequency and makes sensing system noisy in the baseband, so it is also called 1/f noise. Moreover, the CMOS circuits like differential amplifiers always require the perfect matching to suppress the common mode signals as possible, however the unknown process variation and layout style may cause mismatch in the transistor pairs. In the consequence, with the same DC bias, there is a voltage deviation at the differential

output. The phenomenon reduces the circuit operation dynamic range, and decrease the common mode rejection ratio (CMRR). An extra voltage is added at the input to null the deviation at the output DC level, it is called “DC offset voltage”. A high performance of CMOS readout interface purposes to suppress the DC offset and flicker noise.

There are three main types of noise rejection circuits in reference [10]. Such as Auto-zeroing (AZ), Correlate Double Sampling (CDS) which is a special case of AZ, chopper stabilization (CHS) technique is widely used in precision circuits to reduce DC offset and flicker noise.

The conventional techniques as above are distinguished by continuous-time sensing and discrete-time sensing. The CHS is usually applied to continuous-time sensing, while the CDS is used in discrete time sensing circuits.

Base on the above noise reduction concepts, the capacitive sensing circuits have been developed to many configurations. In continuous-time sensing, the capacitance variation can be transduced to current (CTC) with trans-impedance amplifier (TIA) [12] [13], and can be transduced to voltage (CTV). The capacitance to voltage (CTV) also can be divided into capacitive feedback architecture (TCA close-loop) and open-loop architecture. In discrete time, the charge sensing readout circuits is always designed with CDS or AZ. The comparisons of conventional architectures were discussed in reference [11]. And the architecture is classified into a tree diagram as follow:

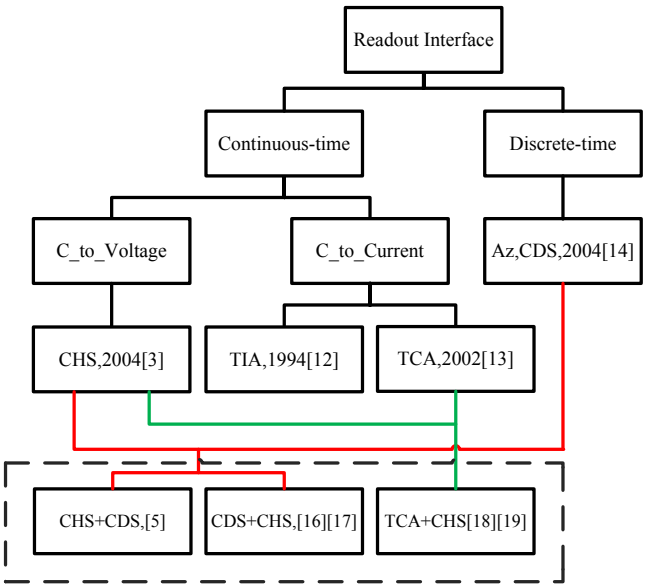


Figure 1-3.2(a): Tree diagram of the conventional techniques

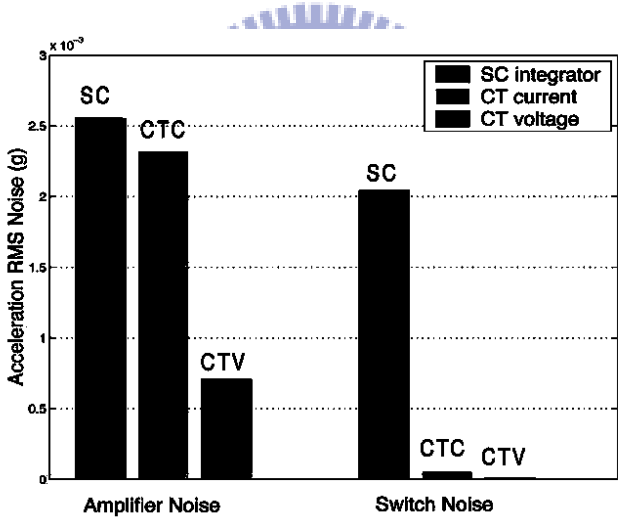


Figure 1-3.2(b): Noise contribution in the conventional architectures [2]

The noise contribution is the critical problem for CMOS MEMS accelerometer, the discrete time sensing composites of the switching capacitors, which suffers from much more thermal noise by switch on-resistors, capacitors. Besides, the noise folding will occur during sampling process [10]. Its applications are more suitable for larger signal generator like bulk-devise. And the noise comparisons between continuous time sensing

and discrete time sensing can be found in Figure 1-3.2(b) [2]. Its applications are more suitable for larger signal generator like bulk-devise.

Nowadays, in order to obtain high performance readout circuits in all respects like low noise, low power, accuracy gain, and high linearity. Single architecture has been unable to fulfill the demands. In recent years, capture the advantages of variety of those architectures to satisfy the higher performance readout circuits has become a popular design method as marked in dash line in Figure 1-3.2(a) . For example, the CHS is often combined with CDS to give consideration to noise, power, and linearity. The next section will discuss the pros and cons of them.

1-3.3 Combinational Architecture

CDS with CHS

In reference [16], the CDS is adopted as capacitance to voltage converter (CVC) and the CHS is adopted as a gain enhancement at next stage. The main advantage of the CDS at first stage is insensitivity to parasitic capacitor at sensing node and completes the sampling process to eliminate the DC offset and flicker noise. For the weak signal of the CMOS MEMS accelerometer, one drawback of this topology is that a preamp is needed after the charge integration amplifier. Especially in the reference [16], the CHS at the next stage consumes much more power because of the high modulation frequency. The drawback also exists in reference [17], the whole SC amplifier architecture requires high data sampling rate (at least two times signal frequency) to enlarge high modulation frequency. So it also dissipates more power.

Besides, in the switching capacitor circuits, because the circuit bandwidth must be

several times higher than the sampling rate to allow the circuit to settle properly, the noise folding causes the in-band noise to multiply. Assume that the bandwidth BW = N*f_s, where f_s is the sampling frequency. Then the SNR loss due to the noise folding is givens in [15]:

$$\frac{SNR_{sc}}{SNR_0} = \frac{1}{N} \qquad (1\text{-}3.4)$$

Where SNR_0 is the ideal case that the bandwidth is infinity, SNR_{sc} is the finite bandwidth. Thus, the SNR after sampling is decreased by the fact N. Base on the above reasons, this topology is not good enough to meet the low power low noise requirement.

CHS with Trans-Capacitance Amplifier (TCA)

Instead of adopting the discrete time sensing at the first stage, the continuous time topology is utilized in reference [18][19]. The CHS with TCA configuration not only improves the disadvantage of the single TCA topology [13], that only the AC capacitance change can be sensed, but is still insensitivity to parasitic capacitor like [16]. The robust DC bias is one of the most attractive features for designer; furthermore the band pass function is formed to filter out the flicker noise and DC offset by a feedback capacitor and a large resistor. Without thermal noises from switching capacitors, The CHS with TCA could save much power compared to SC circuits. The robust DC bias in close loop configuration requires a large bandwidth to obtain an AC virtual ground at the modulation frequency [15]. And the more offset decrease the CMRR by the extra feedback capacitors and resistors

Besides, the full close loop architectures are always combined with the digital controlled resistive ratio variable gain amplifier (VGA) and it consume much more power and areas if wider tunable range is required.

CHS with CDS

The first stage adopts the open loop architecture with CHS and the demodulation stage is combined with CDS function in order to cancel out the DC offset and flicker noise from the open loop stage [7]. Reducing the noise source at signal path as possible is the main ideal in this configuration. Base on the idea, the amplifier specifications can be relaxed significantly. The high gain, high slew rate op-amp are not required in this configuration, so it saves most power although the high modulation frequency is utilized. After demodulation, the close loop is configured to linearly enlarge the signal. The power consumption of the close loop op-amp can be maintained as low as possible due to the low speed demodulated signal. For low noise low power applications, this topology had already implemented with CMOS MEMS accelerometer in [5].

Besides, the noise folding effect on SC circuit and continuous-time voltage sensing is compared in [15]. Assume BW = (2N-1)*f_m, where f_m is the modulation frequency. The SNR loss is given in [15]:

$$\frac{\mathrm{SNR}_{\mathrm{open-loop}}}{\mathrm{SNR}_0} = \frac{\left\{\frac{8}{\pi}\sum_{n=1}^{N}\frac{1}{(2n-1)^2}\right\}^2}{\frac{16}{\pi^2}\sum_{n=1}^{N}\frac{1}{(2n-1)^2}} \qquad (1\text{-}3.5)$$

The experimental results show that the SNR loss in continuous time topology is more insensitive to op-amp bandwidth. In contrast of SC circuit, the continuous time sensing approach has the best noise performance with the same power consumption.

The comparison of the above popular configurations is shown in Figure 1-3.3(a)

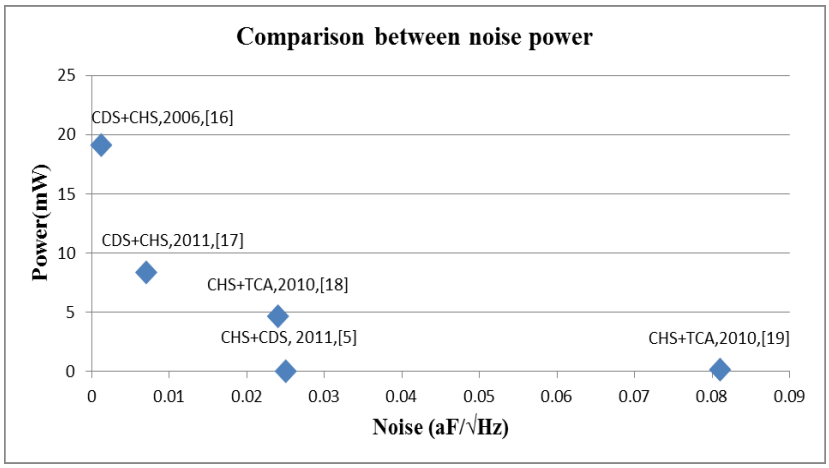


Figure 1-3.3(a): Noise and power consumption of the latest configurations

1-4 Back-End Sigma-Delta modulation Analog-to –Digital Cconverter

The SDM is purpose of suppressing the quantization noise by the oversampling and noise shaping technique. Before design a high performance Sigma-Delta Modulator (SDM), we will introduce the theorem and specifications of SDM in order to realize the pros and cons of an A/D. In this chapter, a basic operation principle and specifications of the SDM are presented.

1-4.1 Quantization Noise

After comparing between the analog input signal V_{in} and V_{ref}, the analog input signal V_{in} is converted to the digital output D_{out} by an N-bit A/D as shown in Figure 1-4.1(a), and the analog input signal V_{in} can be described by a series of the digital output D_{out} as follow:

$$V_{in} = V_{ref}(b_1 * 2^{-1} + b_2 * 2^{-2} + \cdots + b_N * 2^{-N}) \pm V_{error} \qquad (1\text{-}4.1)$$

Where $-\frac{1}{2}V_{LSB} \leq V_{error} \leq \frac{1}{2}V_{LSB}$, V_{LSB} is the Least Significant Bit.

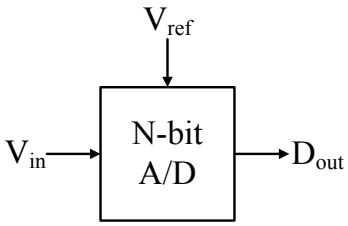


Figure 1-4.1(a): N bit A/D

The V_{error} is the so called Quantization Noise. It is an inherent error during the quantization processing. That makes the Digital codes D_{out} can't restore to V_{in}. And the distortion exists between the restored analog signal and original one. The analog signal V_{in} must be larger than the Quantization Noise in order to complete the A/D conversion and recover to the original signal. The definition of Quantization Noise can be explained by a 3-bit ADC as shown in Figure 1-4.1(b). And the quantization error can be calculated as:

$$V_Q = V_I - V_R \tag{1-4.2}$$

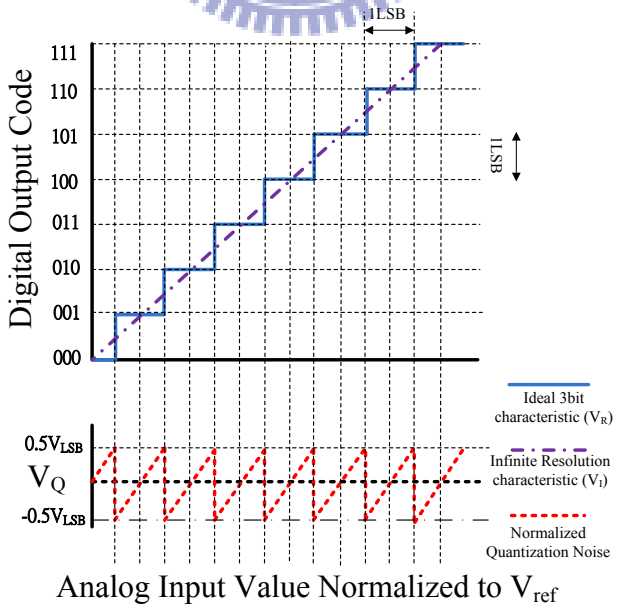


Figure 1-4.1(b): Ideal input-output characteristic of a 3-bit ADC

From above definition, the quantization noise can be viewed as a random white noise within $\pm\frac{1}{2}V_{LSB}$. A uniform distribution of the quantization error between $\pm\frac{1}{2}V_{LSB}$ is shown in Figure 1-4.1(c), $F_Q(X)$ is the probability density function of the quantization error. And the root means square value (RMS) of the quantization noise power can be calculated as follow:

$$V_{Q(RMS)} = \left[\int_{-0.5V_{LSB}}^{0.5V_{LSB}} x^2\ dx\right]^{1/2} = \frac{V_{LSB}}{\sqrt{12}} \qquad (1\text{-}4.3)$$

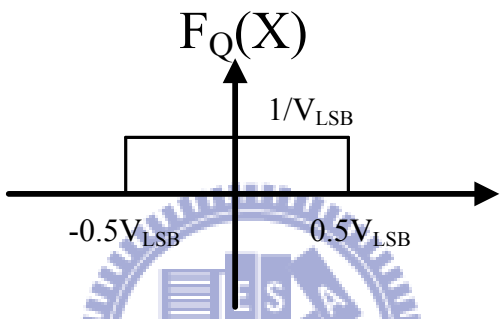


Figure 1-4.1(c): Probability density function

The sine wave is widely used to be the input signal to analysis the A/D converter and the signal to quantization noise ratio (SQNR) can be calculated as follow (assume that the amplitude of the sine wave is "A" and the $V_{LSB}=2A/2^N$):

$$SQNR = 20\log\left[\frac{V_{in(RMS)}}{V_{Q(RMS)}}\right] = 20\log\left[\frac{\frac{\sqrt{2}}{2}A}{\frac{A}{2^{N-1}\sqrt{12}}}\right] = 6.02N+1.76\ dB \qquad (1\text{-}4.4)$$

N is the resolution. If the designed A/D wants to be boosted one-bit, the SQNR must be increased six dB first. Further, the effective number of bits (ENOB) can be defined from above as:

$$ENOB = \frac{SQNR-1.76}{6.02} \qquad (1\text{-}4.5)$$

Take only the quantization noise into consideration here.

1-4.2 Oversampling Technique

Different from the Nyquist rate A/D (low sampling rate), as the name suggests, the sampling rate of the SDM is designed to be much higher than input frequency. The purpose of oversampling is to suppress the quantization noise by extending the bandwidth of the quantization noise. The quantization noise power can be divided by sampling frequency to calculate the noise power per unit bandwidth, called the power spectrum density (PSD). From Figure 1-4.2(a), the total amount of the quantization noise in the signal band of the interest (called the in-band noise power) for the high sampling rate case (F_{SB}) is smaller than that for the low sampling rate case (F_{SL}), F_B is the signal bandwidth.

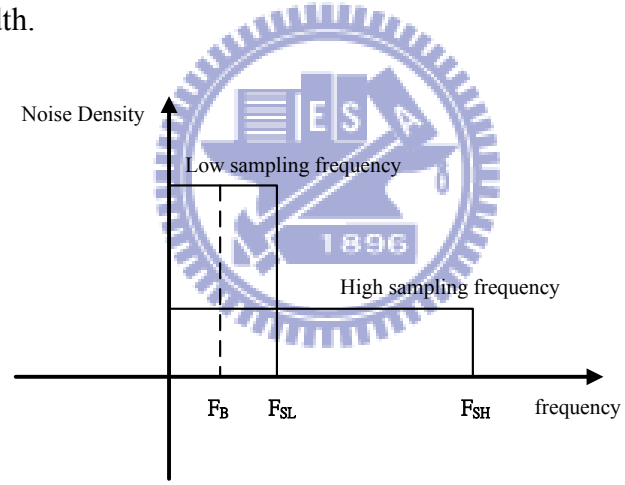


Figure 1-4.2(a): Quantization noise density with different sampling frequency

And the definition of the oversampling ratio (OSR) is convenient to analysis the performance of the SDM and the OSR is defined as follow:

$$\mathrm{OSR} = \frac{f_s}{2f_B} \tag{1-4.6}$$

f_s is the sampling frequency and the f_B is the signal bandwidth. The total quantization noise power is calculated to be $V_{LSB}/\sqrt{12}$ in section 1-4.1 and can be transformed to

frequency domain as the white noise, and plot the power spectrum density in Figure 1-4.2(b). The in-band quantization noise power (P_e) after oversampling technique can be calculated as follow:

$$P_e = \int_{-F_B}^{F_B} \frac{V_{Q(RMS)}}{F_S}\, df = \int_{-F_B}^{F_B} \frac{V_{LSB}}{12F_S}\, df = \frac{V_{LSB}^2}{12}\frac{1}{OSR} \qquad (1\text{-}4.7)$$

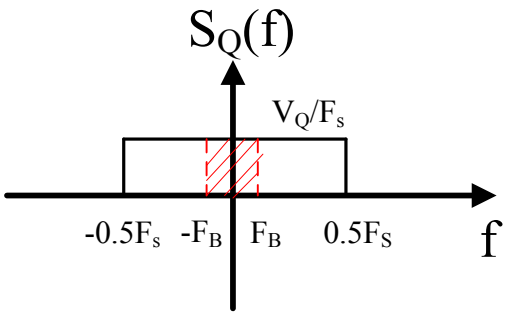


Figure 1-4.2(b): In-band quantization noise power spectrum

The SQNR after oversampling technique can be calculated as follow:

$$SQNR = 20\log\left[\frac{\frac{\sqrt{2}}{2}A}{\frac{A}{2^{N-1}\sqrt{12}}\sqrt{\frac{1}{OSR}}}\right] = 6.02N+1.76\ dB+10*\log(OSR) \qquad (1\text{-}4.8)$$

By oversampling, the SQNR of the A/D is boosted by the factor of 10*log(OSR), and the resolution is also boosted too.

1-4.3 Noise Shaping

The noise shaping can be realized by modeling the first order SDM as shown in Figure 1-4.3(a). The basic SDM consists of an integrator H(z), a quantizer, a D/A converter employed in the feedback path. The input signal subtracts the signal from D/A output. And the value after subtraction will be integrated by the integrator.

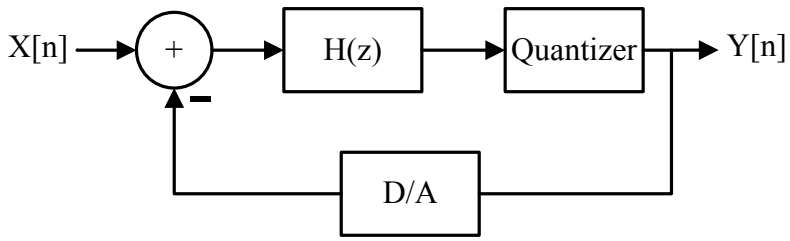


Figure 1-4.3(a): The first order SDM block diagram

The discrete time operation can be described in mathematical calculation by creating the corresponding linear model as shown in Figure 1-4.3(b).

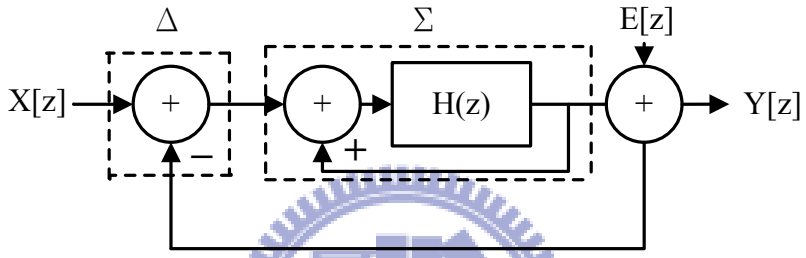


Figure 1-4.3(b): The first order SDM linear model

By observation from the linear model, the signal transfer function (STF) can be derived from signal X(z) to output Y(z) path and the quantization noise transfer function (NTF) can be derived from quantization noise E(z) to output Y(z) path, and they are given by:

$$\mathrm{STF} = \frac{\mathrm{X(z)}}{\mathrm{Y(z)}} = \frac{\mathrm{H(z)}}{1+\mathrm{H(z)}} \tag{1-4.9}$$

$$\mathrm{NTF} = \frac{\mathrm{E(z)}}{\mathrm{Y(z)}} = \frac{1}{1+\mathrm{H(z)}} \tag{1-4.10}$$

The system output is given by:

$$\mathrm{Y(z)} = \mathrm{STF} * \mathrm{X(z)} + \mathrm{NTF} * \mathrm{Y(z)} \tag{1-4.11}$$

The operation of the integrator can be described in discrete time calculation as follow:

$$\mathrm{H(z)} = \frac{1}{\mathrm{z}-1} \tag{1-4.12}$$

The system output is transformed to:

$$Y(z) = Z^{-1} * X(Z) + (1 - Z^{-1}) * E(Z) \quad (1\text{-}4.13)$$

By observation results from above equations, the quantization noise becomes a high pass function, and the in-band noise (low-frequency) can be suppressed after noise shaping.

1-4.4 Performance Prediction of The Second Order SDM

The linear model of the second order SDM is shown in Figure 1-4.4(a).

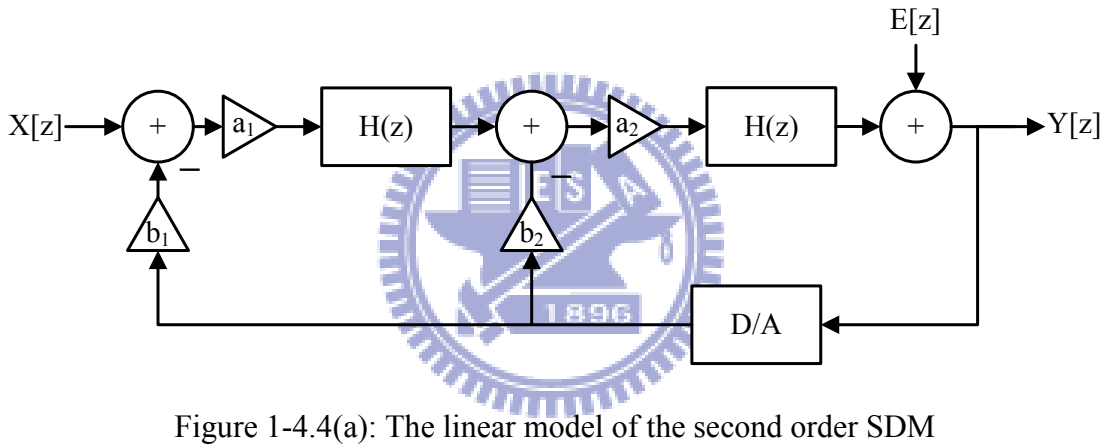


Figure 1-4.4(a): The linear model of the second order SDM

After hand calculation the STF and NTF can be written in a general form and they are given by:

$$STF = \frac{X(z)}{Y(z)} = \frac{a_1 a_2}{z^2 + (a_2 b_2 - 2)z + (1 - a_2 b_2 + a_1 a_2 b_1)} \quad (1\text{-}4.14)$$

$$NTF = \frac{X(z)}{Y(z)} = \frac{(1 - z^{-1})^2}{z^2 + (a_2 b_2 - 2)z + (1 - a_2 b_2 + a_1 a_2 b_1)} \quad (1\text{-}4.15)$$

In general, for simplifying the transfer function form, we choose the SDM's pole at z=0, and the parameters of the 2nd SDM is selected to be a_1=0.5, a_2=2, b_1=b_2=1, respectively. And the transfer function of SDM's output become to:

$$Y(z) = STF * X(Z) + NTF * E(Z) = Z^{-2} * X(Z) + (1 - Z^{-1})^2 * E(Z) \quad (1\text{-}4.16)$$

Next, replace z with $e^{j2\pi f/fs}$, and $\sin(x) = (e^{jx} - e^{-jx})/2j$. In the frequency domain, the squared magnitude of the NTF is given by:

$$|NTF(f)|^2 = \left(1 - e^{-\frac{j4\pi f}{fs}}\right) * \left(1 - e^{\frac{j4\pi f}{fs}}\right) = \left[4\sin^2\left(\frac{\pi f}{f_s}\right)\right]^2 \qquad (1\text{-}4.17)$$

In-band quantization noise power P_e can be calculated by using (1-4.3) and (1-4.17)

$$P_e = \int_{-F_B}^{F_B} \frac{V_{Q(RMS)}}{F_S}\left[4\sin^2\left(\frac{\pi f}{f_s}\right)\right]^2 df \approx \frac{\pi^4 {V_{LSB}}^2}{60OSR^5} \qquad (1\text{-}4.18)$$

After oversampling and noise shaping, the SQNR of the proposed 2nd SDM can be calculated as follow:

$$SQNR = 20\log\left[\frac{\frac{\sqrt{2}}{2}A}{\frac{A}{2^{N-1}}\frac{\pi^2}{\sqrt{60OSR^5}}}\right] = 6.02N+1.76\ dB-12.9+50\log(OSR) \qquad (1\text{-}4.19)$$

If the proposed SDM is one bit A/D, OSR is chosen to be 250 and the SQNR can be approach to be 114.77dB, the ENOB can be up to 18 bit resolution.

Approach

In order to get a high dynamic range for wider applications, the voltage control linear variable gain amplifier (VGA) is adopted with open-loop voltage sensing in the proposed work. In contract to the conventional open loop continuous time voltage sensing with CHS configurations, the dual CHS is utilized to overcome the residual offset and reduces the signal speed to save much power consumption. The VGA not only regulates the output signal level between sensor signals and external forces, but also acts as a gain enhancement stage.

For the accelerometer part, shorter sensing fingers introduce less non-ideal effect (residual stress) after post process. So, instead of using the long sensing fingers, the

multi turns long folded springs are adopted to increase the sensitivity of the proposed accelerometer.

In spite of the proposed accelerometer with short finger can reduce residual stress, and prevent from structure curling, the proposed work still utilize three methodologies to compensate the accelerometer non-ideal factor: 1. The extra fingers are configured as electrostatic actuator to adjust the position offset. 2. Curling matching with rigid frame. 3. The 1st low pass filter with differential difference amplifier (DDA) is used to filter out the high frequency noise and subtract the AC offset.

1-5 Organization

Chapter 1 discusses about the non-ideal factor and process flow of the CMOS MEMS capacitive accelerometers in *surface* micromachining and shows the comparison between several popular noise rejection readout interfaces is given. In chapter 2, a new design flow includes implementation and simulation with Cadence Analog Design Environment directly will be present. In chapter 3, the implementation and simulation of the low noise gain tunable interface and the 2nd SDM will be present. The measurement results are discussed in chapter 4. In chapter 5, we establish the single chopper architecture and simulate the noise performance. Besides, in order to emphasize the advantage of the DCA, we also simulate the noise and estimate power consumption without the DCA design. Finally, describe the future work for the author.

Chapter 2

CMOS MEMS Accelerometer Design and Simulation

2-1 Design Flow

A new approach to simulate the CMOS MEMS accelerometers with CMOS readout circuits in Cadence Analog Design Environment (ADE) is by using the ConventerWare advanced software MEMS+. In the MEMS+, the users provide two process information of the foundry service. 1. The material (silicon, oxide, Aluminum) database such as material density, atmospheric pressure, and Young's modulus. The aluminum material data is shown as Figure 2-1(a). 2. The process flow provides the thickness of metal layer and manufacturing steps as shown in Figure 2-1(b). And the structures could be created as a 3D model by the parameterized module. For example, the parameterized modules for accelerometer include the proof mass and etching hole, variety of springs, comb fingers and so on. The designers can assign the variables for the width and length of the structures. After create the 3D model, make sure that the mechanical connection and the electrical connection are both correct, and then the 3D model with structure variable can be imported into the Cadence as a Verilog-A model. The structure layout could be imported at the same time. The design flow with MEMS+ is shown as Figure 2-1(c).

Material Properties

Name	Value	Units
Visual Properties		
Color	Custom	
Transparency		
Material Orientation : Euler Angles		
Density	2.3e-15	kg/um^3
Elastic Constants : Isotropic		
Isotropic		
E	7000	MPa
nu	0.3	
PreStress : Anisotropic		
Anisotropic		
Stress Gradient in Z : In-plane Isotropic		
Thermal Coefficient of Expansion		
alpha	2.31e-05	1/K
Zero Stress Temperature	293.15	K
Thermal Conductivity	2.37e+08	pW/(um*K)
Specific Heat	8.98e+14	pJ/(kg*K)
Electrical Conductivity	3.69e+13	pS/um
Piezoelectric Coefficients : Stress Coefficien		
Relative Permittivity : Isotropic		
Isotropic		
er	0	
Piezoresistive Coefficients		
Relative Permeability	*undef*	
Coercivity	*undef*	A/m
Saturation Magnetization	*undef*	A/m

Figure 2-1(a): Aluminum material data

Sub	Substrate	Silicon		400	L3D0					
Planar Fill1	FieldOxide	Oxide		0.35					Front	
Planar Fill3	ILD2	Oxide		5.5					Front	
Planar Fill4	METAL1	Aluminum		4.99					Back	
Straight Cut2					METAL1	Positive	0	0	Front	46
Planar Fill5	IMD1	Oxide		0.85					Front	
Planar Fill6	METAL2	Aluminum		0.53					Front	
Straight Cut3					METAL2	Positive	0	0	Front	48
Planar Fill7	IMD2	Oxide		0.85					Front	
Planar Fill8	METAL3	Aluminum		0.53					Front	
Straight Cut4					METAL3	Positive	0	0	Front	50
Planar Fill9	IMD3	Oxide		0.85					Front	
Planar Fill10	METAL4	Aluminum		0.53					Front	
Straight Cut5					METAL4	Positive	0	0	Front	52
Planar Fill11	IMD4	Oxide		0.85					Front	
Planar Fill12	METAL5	Aluminum		0.53					Front	
Straight Cut6					METAL5	Positive	0	0	Front	54
Planar Fill13	IMD5	Oxide		1					Front	
Planar Fill14	METAL6	Aluminum		2.34					Front	
Planar Fill15	ILDtot	Oxide		5.5					Front	
Planar Fill2	METALtot	Aluminum		4.99					Front	
Straight Cut7					METAL6	Positive	0	0	Front	56
Straight Cut8					HM	Positive	0	0	Front	24
Straight Cut9					RLS	Negative	0	0	Front	20

Figure 2-1(b): Process flow

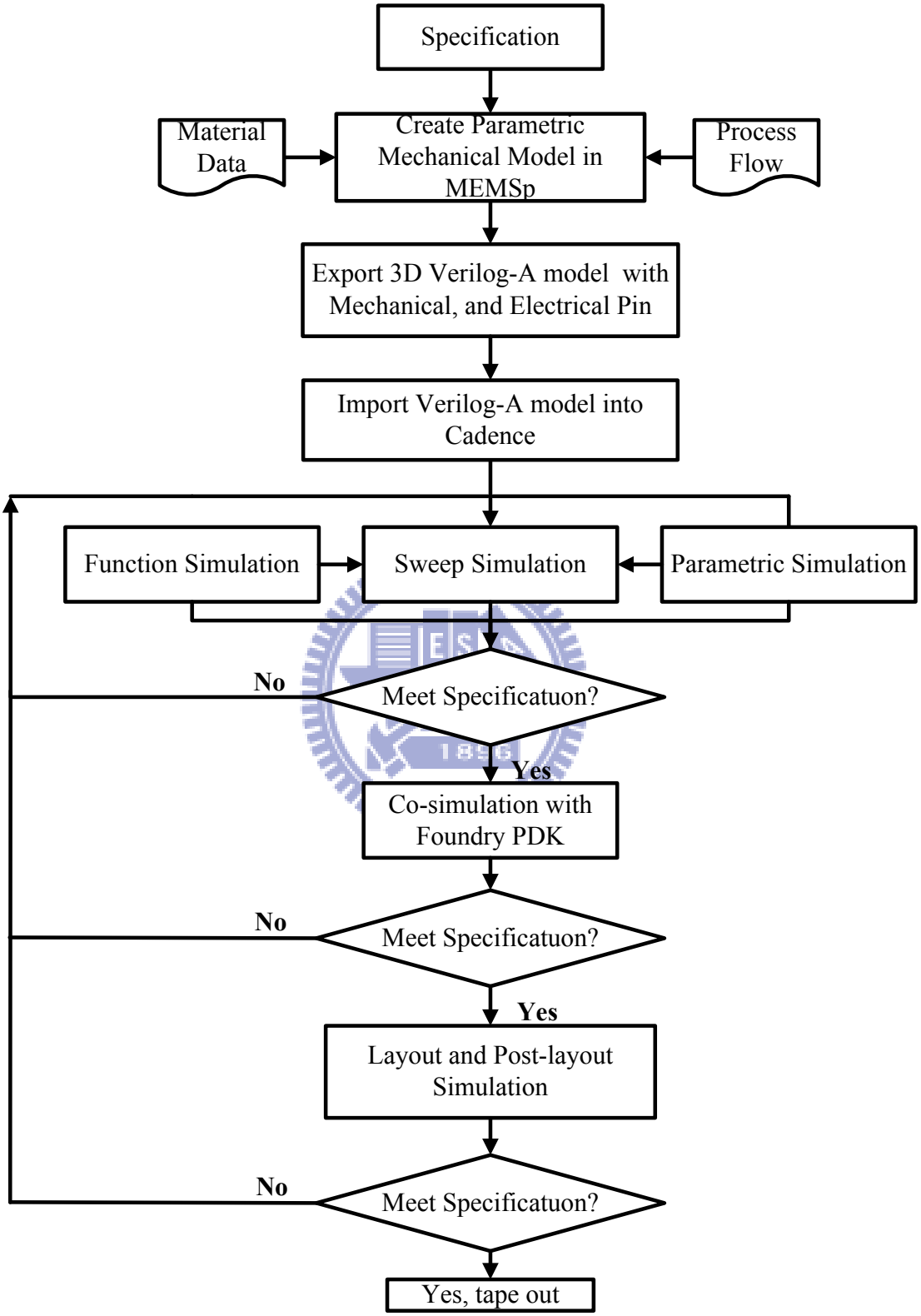


Figure 2-1(c): Design flow of MEMS+

2-2 Accelerometer Design

The parameterized accelerometer 3D model in MEMS+ is shown in Figure 2-2(a). Most of sensor area is occupied by the proof-mass, and the etching holes are spread over the proof mass with equal space to make sure that the proof-mass can be successfully released after post process, as shown in Figure 2-2(b).

The "H" shaped accelerometer has enough electrostatic actuator fingers to compensate the position deviation.

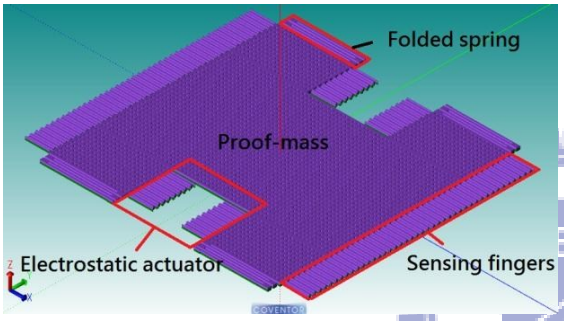


Figure 2-2(a): Accelerometer 3D model

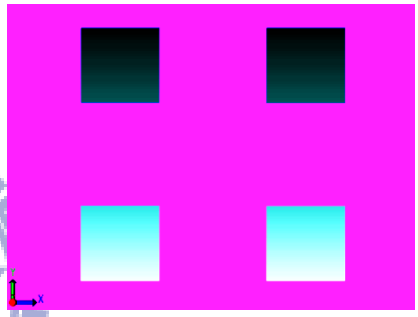


Figure 2-2(b): Etching hole

The sensing fingers are shown in Figure 2-2(c). In order to avoid electrical conflict by double sides sensing fingers, the metal layers in the sensing fingers must be slightly separated from proof mass. The oxide layers are used to connect with the proof-mass.

Due to the less structure curling effect on accelerometer performance, the folded springs are designed to maintain the sensitivity approximate to about 1mV/g. Thus, the shorter sensing fingers could be implemented with the less structure curling effect.

Figure 2-2(c): Sensing fingers

Figure 2-2(d): Folded spring

2-3 Accelerometer Simulation

2-3.1 Simulation Environments

The weight of proof mass can be directly derived in the MEMS+, and the damping coefficients must be simulated in the ConventerWare and filled into MEMS+ before simulation.

Moreover, before simulate the accelerometer in Cadence, the electrical pin and mechanical pin must be exported from MEMS+. The electrical pins are directly connected to the CMOS circuits, and accept the electronic signals. The mechanical pins include physical signals (acceleration and force) input and output (displacement and capacitance variation). The capacitance vibration is recorded in capacitance output. The accelerometer symbol in Cadence is shown in Figure 2-3.1(a).

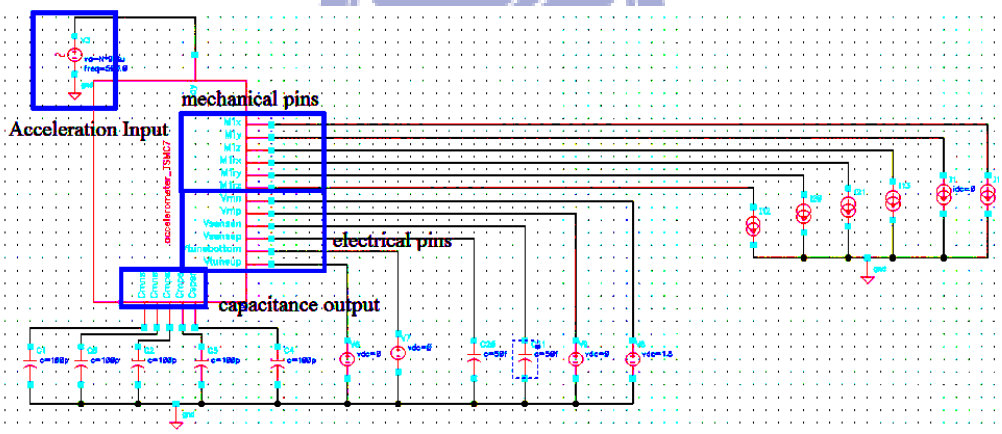


Figure 2-3.1(a): Accelerometer symbol in cadence

When the MEMS+ model is simulated in cadence ADE, the physical signals (acceleration, velocity, displacement, and force…) are expressed in the voltages and the currents. For example, 1 g acceleration equal to 9.8uV. And the unit scale factors are shown in Table 2-3.1.

Table 2-3.1: Unit scale factor

Physical units	Electronic unit
1 rad	1E-4V
1 m	1E6V
1 m/s	1E-2V
1 m/s^2	1E-6V
1 N	1E-3A

2-3.2 Sensing Capacitors

The rest capacitance values significantly affect the sensitivity and the thermal noise according to the formula in section 1-2.2. Due to the thin-film CMOS MEMS structure, the rest capacitance values are about several hundred femto farad. As the acceleration is subjected to the accelerometer, the capacitance variation is several femto farads even smaller in the shot sensing fingers.

In the simulation, the acceleration is subjected to the mechanical pins, and sweeps the acceleration to observe the sensing capacitances variation and displacement of proof mass. The stationary sensing capacitances are located on the zero acceleration. The simulation result is shown in Figure 2-3.2(a).

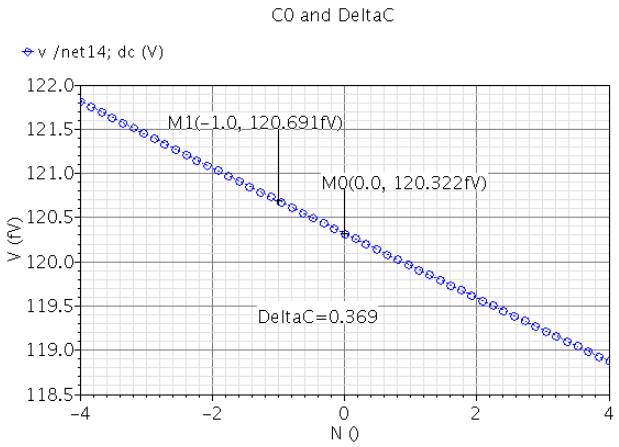


Figure 2-3.2(a): X-axis: acceleration Y-axis: capacitance variation

2-3.3 Nature Frequency

The nature frequency is simulated in AC analysis. Different from CMOS MEMS resonators, the operation frequency of accelerometer is smaller than the nature frequency. Besides, the nature frequency affects the sensitivity according to formula (1.3.3). The simulation in Figure 2-3.3(a) shows a large nature frequency, that makes the accelerometer far away from Brownie noise.

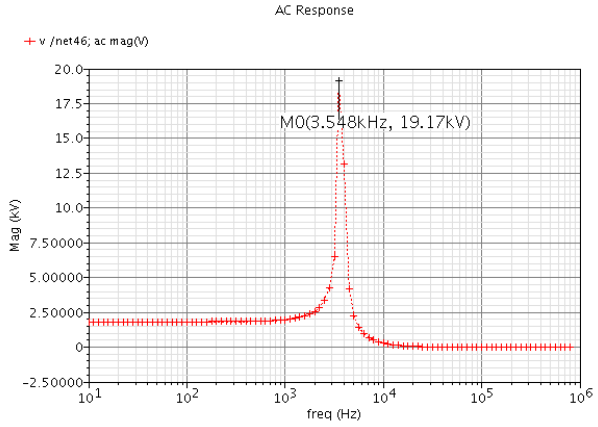
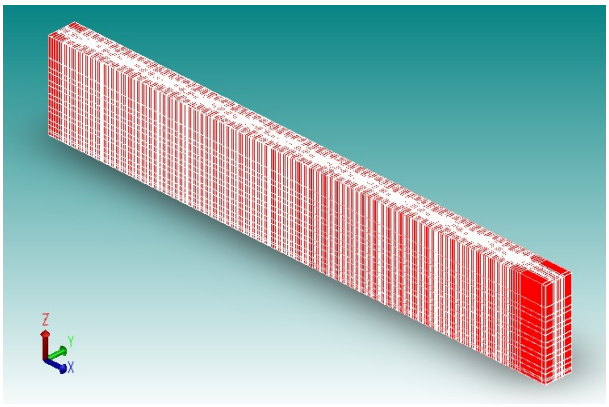


Figure 2-3.3(a): Accelerometer nature frequency

2-3.4 Damping Coefficient

The damping coefficient of the squeeze film of the inter-digital fingers decides the system Brownie noise and the quality factor described in section 1-2.2. And the damping coefficient is simulated in CoventorWare by using a single finger. Only a mesh single overlap region of the finger is calculated by DampingMM analysis in the simulation as shown in Figure 2-3.4(a). The frequency response of system damping is shown in Figure 2-3.4(b). And the Brownie noise is calculated with the damping simulation result, they are summarized in Table 2-3.4.



Damping Force Coefficient

	Frequency (Hz)	Damping Coefficient (N/(m/s))
point 1	10	5.091107E-08
point 2	2.782559E01	5.091107E-08
point 3	7.742637E01	5.091106E-08
point 4	2.154435E02	5.091107E-08
point 5	5.994843E02	5.091108E-08
point 6	1.668101E03	5.091107E-08
point 7	4.641589E03	5.091108E-08
point 8	1.29155E04	5.091107E-08
point 9	3.593814E04	5.091105E-08
point 10	1.0E05	5.091093E-08

OK

(a) (b)

Figure 2-3.4(a): Mesh model of single finger; (b): AC response of damping coefficient

Table 2-3.4: Damping coefficient and Brownie noise

	Simulation
Damping	11.81E-6
BNEA	4.2ug/√ Hz

2-3.5 Electrostatic Forces

The “H” shaped accelerometer has extra fingers to be applied the external voltage V. These extra fingers are used as electrostatic actuators. The external force is used to push the sensing fingers back to the center. The routing of the electrostatic actuators is shown in Figure 2-3.5(a).

As an electrical potential is applied across two plates of a capacitor, an attractive force is generated between two plates. The ideally electrostatic forces components in Y-axis are given by:

$$F_x = -\frac{1}{2}\frac{\partial C_0(x)}{\partial x}V^2 \qquad (2\text{-}3.1)$$

Where the negative sign indicates the force is attractive.

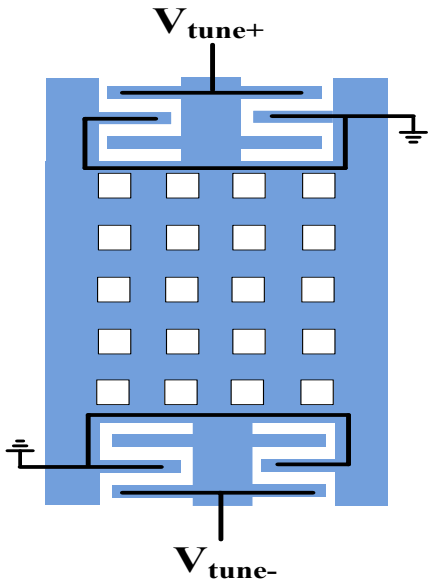


Figure 2-3.5(a): Electrostatic actuators connection

But take the non-ideal accelerometer capacitance fingers into account, the electrostatics actuator is a non-linear actuator. The simulation result in Figure 2-3.5(b) shows the capacitance variation by sweeping the external force from 0 V to 20V.

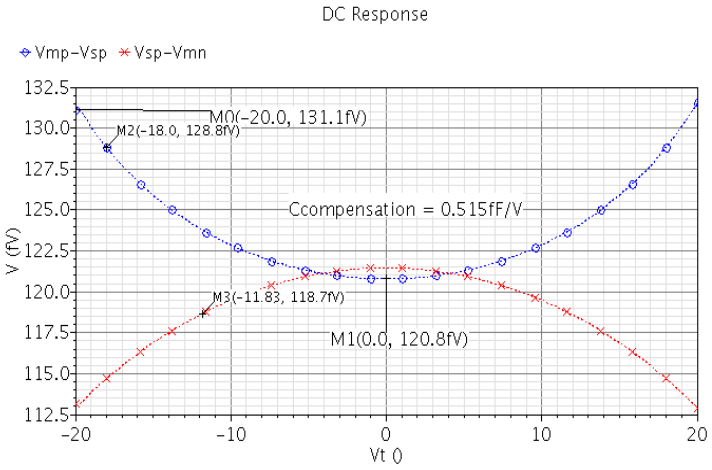


Figure 2-3.5(b): Capacitance variation with the electrostatic forces

Figure 2-3.5(b) shows the 20% sensor offset can be compensated with external voltage 20V.

2-4 Accelerometer Layout

In order to obtain the benefits of the fully differential architecture, the full bridge sensing capacitors is configured as Figure 2-4(a).

The symmetric layout style is employed to compensate cross-axis manufacturing gradients and to achieve better cross-axis rejection in the fully differential accelerometer as shown in Figure 2-4(b).

The symmetric rigid frame is also designed in the accelerometer to compensate the structure out-plane curling, described in section1-2.3.

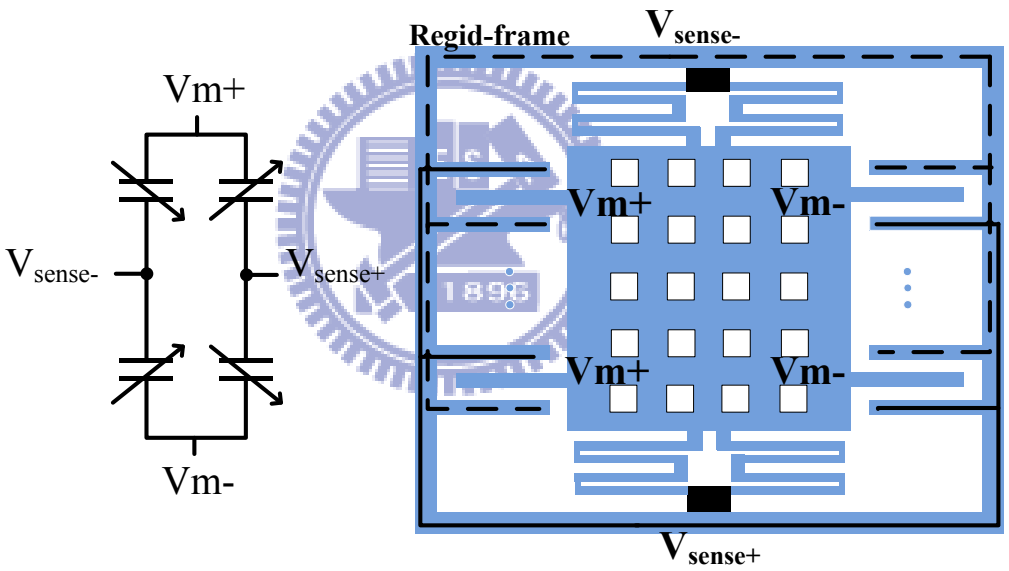


Figure 2-4(a): Full bridge sensing capacitors (left); (b): Symmetric layout (right)

The CMOS MEMS accelerometer is fabricated in TSMC Mixed-signal 0.18um and has the post process in APM. Because the field oxide and poly-silicon in CMOS process have larger residue stress, they are rarely used in CMOS MEMS accelerometer, the proposed accelerometer is only manufactured in six metal-oxides stacked alternately. The whole accelerometer layout is shown in Figure 2-4 (c) and the geometry parameters

are listed in Table 2-4.

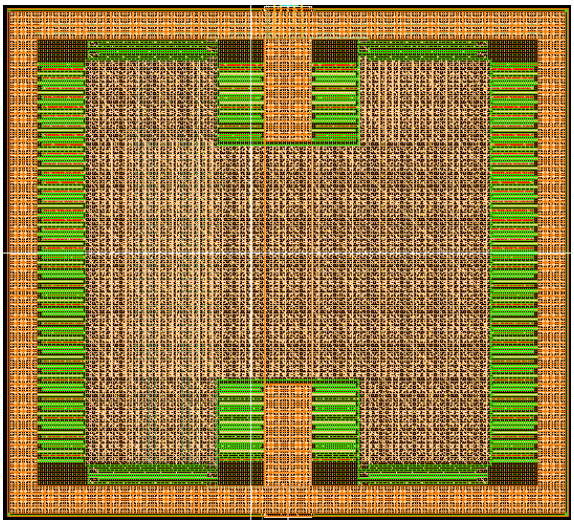


Figure 2-4(c): Accelerometer layout

Table 2-4: Physical parameter of the proposed accelerometer

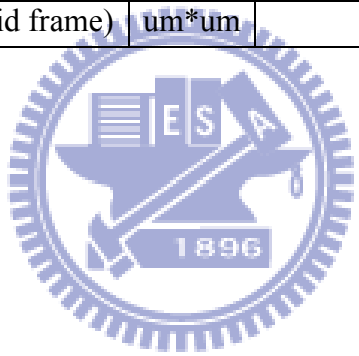
Parameter		Value	Unit
Proof-mass	Area	984*888	um^2
	Area of each holes	4.8*4.8	um^2
	Pitch of each holes	6.9	N/A
Comb-finger	No of comb cells	84	N/A
	Length of comb	76	um
	Width of comb	4	um
	Area of overlap	72*10.49	um^2
	gap	4	um
Folded-spring	No of beam	4	N/A
	Width of beam	4	um
	Length of beam	210	um
	gap	4	um

2-5 Summary

After a series of simulations, the performance of the proposed accelerometer can be simulated in Table 2-5.

Table 2-5: The proposed accelerometer performance

	Unit	**MEMS+ TSMC.18 Pro**
Mass	ug	9.4738
Displacement@1G	nm	17.95
Spring constant	N/m	5.15
C_0	fF	120.3
ΔC	fF/g	0.369
f0	KHz	3.548
BNEA	ug/√Hz	4.2
Area(include rigid frame)	um*um	984*888



Chapter 3

Circuit Design and Co-simulation

3-1 Architecture

The whole system is composed of the front-end pre-amplifier and the back-end Sigma-Delta Modulation (SDM) analog-to-digital converter as shown in Figure 3-1(a). The noise at the SDM input and different input amplitude will degrade the signal-to-noise and distortion ratio (SNDR or SINAD). The low noise pre-amplifier with gain tunable function is needed for a universal acceleration sensing system.

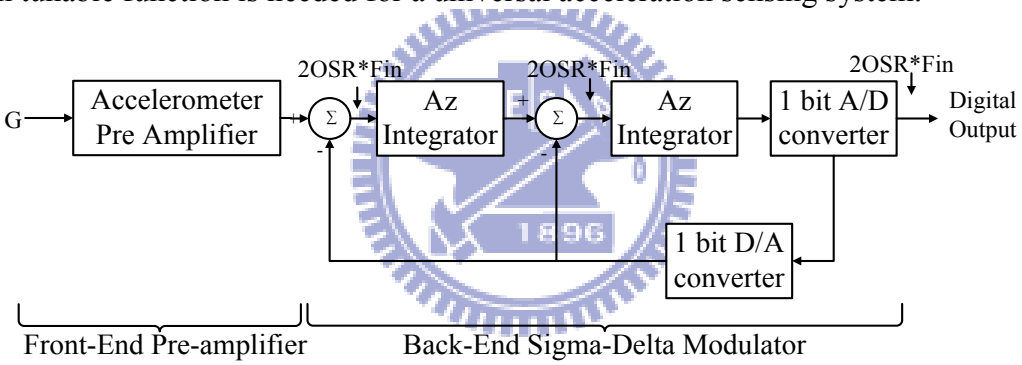


Figure 3-1(a): Universal acceleration sensing system

Front-end Pre-amplifier

A low noise pre-amplifier is based on the Dual-Chopper amplifier (DCA) [3] with embedded low bandwidth, high linearity Variable Gain Amplifier (VGA). Due to the considerations of low noise, high linearity, the whole DCA topology is composed of a low gain, high bandwidth pre-amplifier, the Gm-C filter, a VGA, CDS demodulator, and a first-order low pass filter with Differential Difference Amplifier (DDA) function.

The DCA is improved from conventional chopper amplifier. In the conventional

chopper amplifier, the modulation frequency is larger than the corner frequency of the flicker noise, only thermal noise of the circuit will contribute to the output noise. But the conventional chopper amplifiers always suffer from two drawbacks. First, the large power consumption is needed due to the high modulated signal. Second, the residual offset appears after demodulation due to non-ideal analog switch effect such as charge injection and clock feed-through, which explained in [17].

Different from conventional chopper amplifier, the DCA architecture employs two chopping clocks ϕ_H and ϕ_L, the fundamental principle is as the same as the nested chopper amplifier reported in [17]. In order to relax the low pass filter requirement and get less phase lag in multistage amplifiers topology, choose the clock $\phi_H >> \phi_L$ is needed. Thus the high order low pass filter is not required and the rest chip area can be saved.

In this configuration [17], the signal is modulated twice by ϕ_H and ϕ_L. and the double-modulated signal is first amplified by A1. A2 represent the VGA with the Gm-C filter as an open-loop gain enhancement stage and low pass filter. The off-chip LPF is also not required. The first order low pass filter can meet the requirements to smooth the amplified signal.

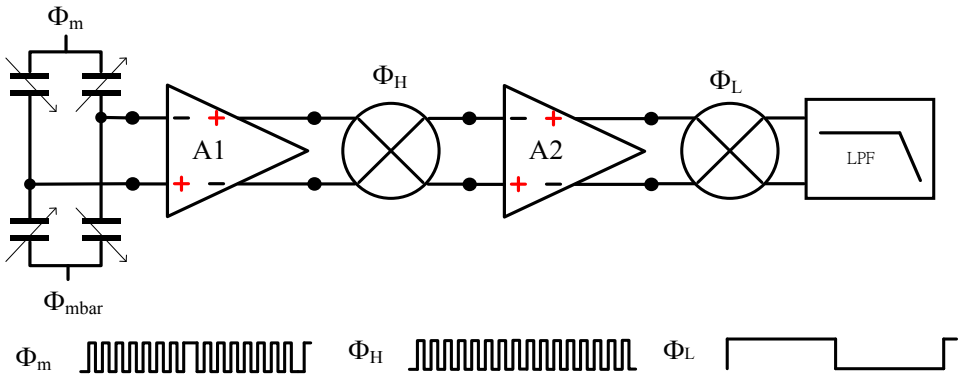
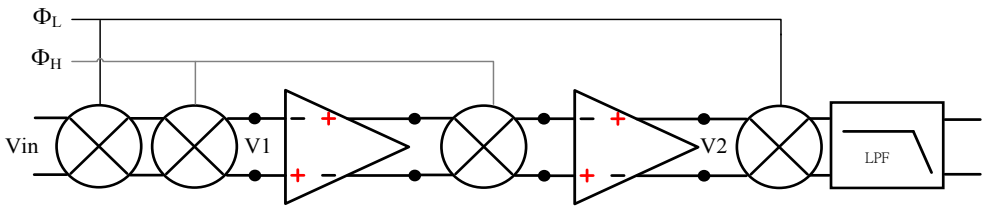
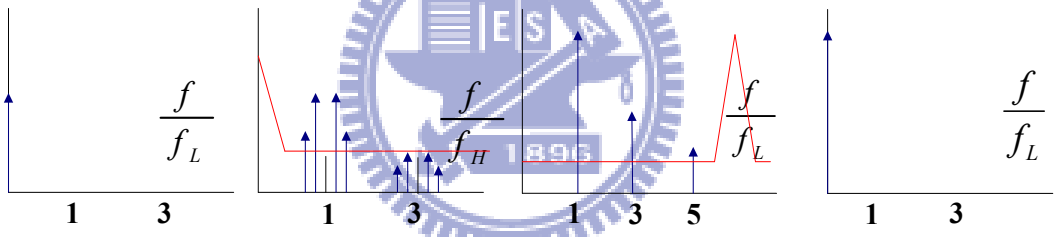


Figure 3-1(b): The DCA configuration

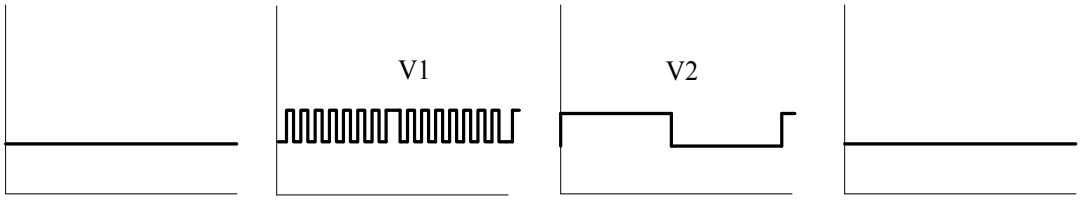
The operation principles of DCA in both frequency domain and time domain are also shown in Figure 3-1(c) ~ 3-1(e). After the two input modulation choppers, the signal is modulated to frequency mf_H+nf_L (m and n are the odd numbers) at the input of DCA, and after the first modulation chopper, the signal is down-converted to nf_L (n is odd). After the final demodulation chopper and low pass filter, the frequency of amplified signal is recovered to the original frequency.



(c)



(d)



(e)

Figure 3-1(c): DCA equivalent circuit; (d): Frequency domain; (e): Time domain

The function level schematic is shown in Figure 3-1(f). The accelerometer bias utilizes the switching bias with reset phase. And the chopping frequency is selected to be 500K Hz, where is far away from the corner frequency. The low noise amplifier stage

focuses on blousing the noise suppression and the power consumption, besides it also maintains the linearity of amplified signal by low gain, high bandwidth architecture. The first demodulation moves the signal frequency to medium frequency band and boosts the DC offset and flicker noise of the first stage. And then a two pole overlapping by the open-loop Gm-C and VGA is adopted to filter out the DC offset and the flicker noise from the first stage. In addition, the linear variable gain amplifier is controlled by the external voltage. The CDS demodulation is most suitable for the open-loop configuration and it is operated in low chopper frequency to recover the original frequency and cancel out the DC offset and the flicker noise from the previous stage. Finally, the anti-aliasing filter with DDA function is designed to correct the DC error which is caused by sensor position offset.

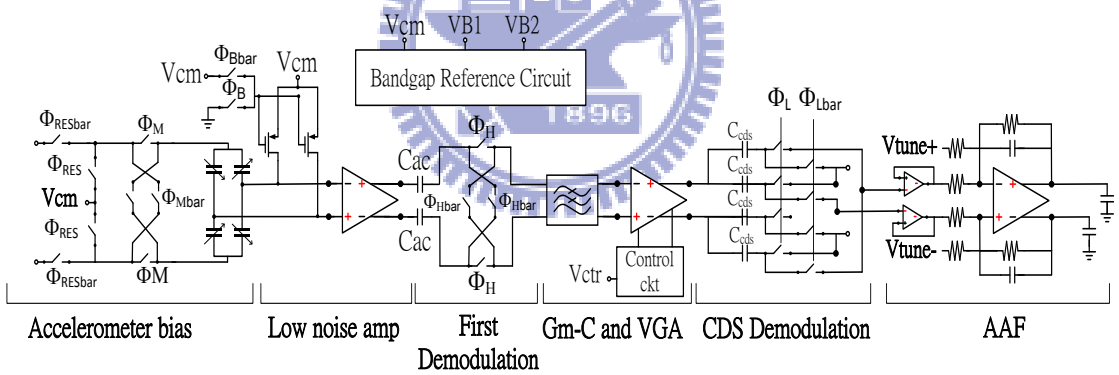


Figure 3-1(f): The schematic of accelerometer and pre-amplifier

Back-end Sigma-Delta Analog-to-Digital (A/D) converter

Compared to traditional Nyquist rate A/D converter, the sigma-delta modulators are suitable to implement A/D converter for low-speed high-resolution applications. The SDM not only maintains the circuits simple to achieve oversampling and noise shaping to obtain the high resolution but also saves much more chip area compared to Nyquist rate A/D converter if the same resolution is required. The designed SDM is a second

order modulator. It is advantages of high resolution high stability.

3-2 Accelerometer Bias

3-2.1 Design Concepts

Figure 3-2.1(a) shows the schematic of modulation and sensor bias. The robust switching bias method is proposed on [2]. Instead of using diodes and sub-threshold MOSFETs, the charge accumulation can be avoided in this topology. Every 16 clock reset cycles, and the reset switch is turned on and connects the input sensing nodes directly to a dc voltage source. The periodic reset scheme re-establishes the dc bias voltage periodically and prevents charge accumulation.

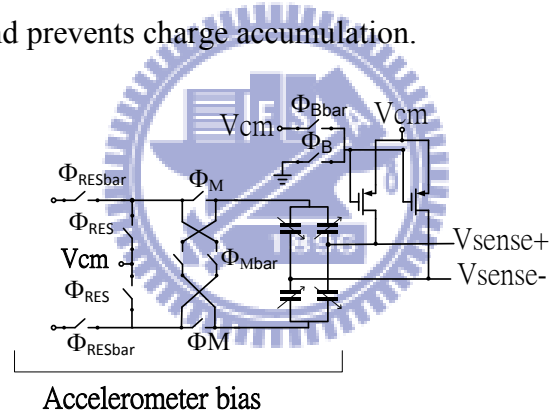


Figure 3-2.1(a): Accelerometer switching bias and modulation

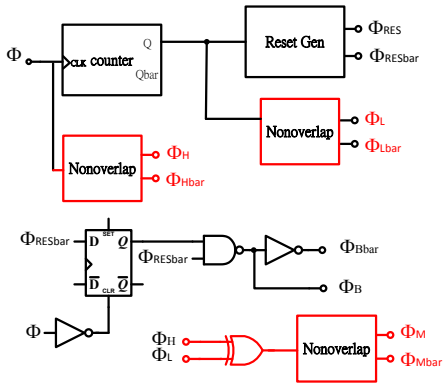


Figure 3-2.1(b): Clock generator

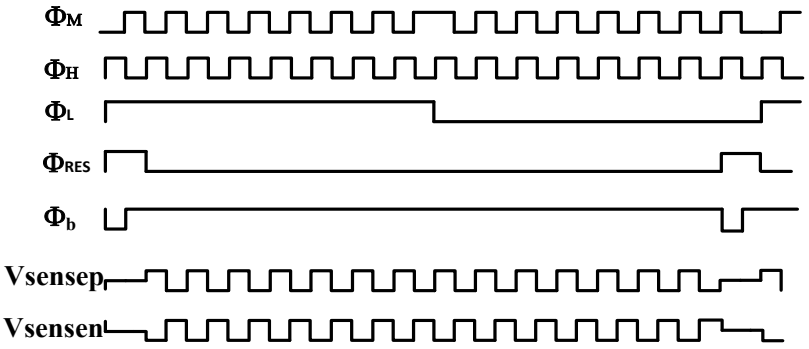


Figure 3-2.1(c): Timing diagram of the control clock

Before exploring the function of switching bias with reset phase, analyzing of the drawbacks of switching bias without reset phase is needed.

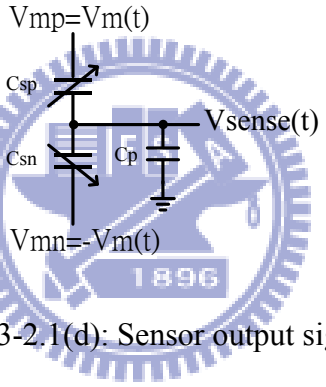


Figure 3-2.1(d): Sensor output signal

According to charge conservation, the output signal in Figure 3-2.1(d) can be written as:

$$\mathrm{Vsense(t)} = \mathrm{V}_b + \frac{C_{sp}-C_{sn}}{C_{sp}+C_{sn}+C_p}\mathrm{V}_m(t) + \frac{Q_t(t)}{C_p+C_n+C_p} \qquad (3\text{-}2.1)$$

Where $\mathrm{V_b}$ is the dc level, $\mathrm{C_{sp}}$ and $\mathrm{C_{sn}}$ is the sensing capacitance, $\mathrm{V_m(t)}$ is the ac modulation signal, $\mathrm{Q_t(t)}$ is any possible undesired charging. The undesired charging is not only produced by charge injection error, but also has the signal-dependent error in a non-perfectly balanced capacitive bridge. When the reset has settled, and the reset switches and the modulation are still on, the total error charge can be described as follow:

$$\mathrm{Q_t(t) = Q_r + Q_i = C_{sp}(V_b - V_{mp}) + C_{sn}(V_b - V_{mn}) + V_b C_p + Q_i} \qquad (3\text{-}2.2)$$

Where Q_r is the signal-dependent error, Q_i is the charge injection from the bias switches. Figure 3-2.1(e) depicts the two types error voltage occurring procedures.

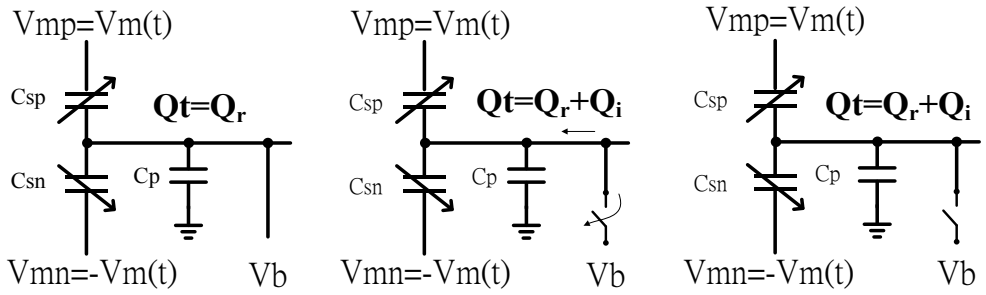


Figure 3-2.1(e): Charge at the sensing node before, at and after the reset is turned off [2].

The signal-dependent reset error can be eliminated by disabling the modulation during the resident turning the modulation back on after the reset [2]. And substitute the modulation by reset phase and synchronously follow the bias switches, the signal-dependent reset error can be eliminated. The voltages after reset are given as:

$$V_{mp} = V_{mn} = V_{sensep} = V_{sensen} = V_b \qquad (3\text{-}2.2)$$

In addition, NMOS transistors could have relatively large leakage current in the N-well process, because its base is the substrate that is fixed at the ground. The PMOS transistors are utilized as the bias switches. And the size is designed with minimum size for two reasons: to reduce the temperature-dependent parasitic capacitance, and to reduce the junction area hence the junction leakage. The cross-section view of the switch structures is shown in Figure 3-2.1(f), body, source and drain are all biased at the same voltage, and there is approximately zero potential between the drain and body.

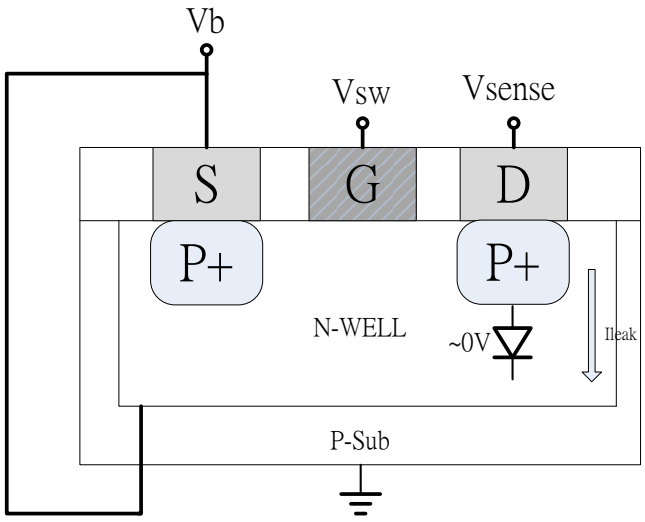


Figure 3-2.1(f): Cross-section view of the PMOS switch

3-2.2 Post-layout Simulation of the Control Clocks

The clock generator is simulated in Figure 3-2.2(a). There is only at TT corner,1.8V, and 27℃ . Other corners show a little drift, but they are still acceptable.

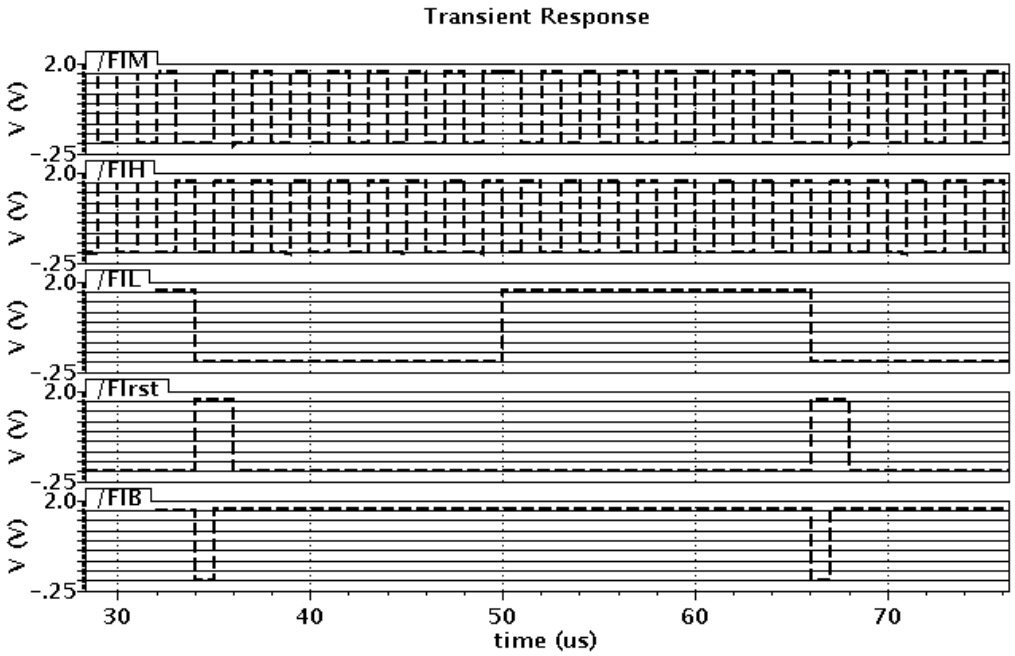


Figure 3-2.2(a): The control clocks (top to bottom: ϕ_M, ϕ_H, ϕ_L, ϕ_{RES}, ϕ_B)

3-3 Open-loop Pre-amplifier

3-3.1 Low Noise Amplifier

The open-loop pre-amplifier is much easier to do optimization between noise and power at the first stage in [2][5]. The schematic of the open-loop pre-amplifier is shown in Figure 3-3.1(a).

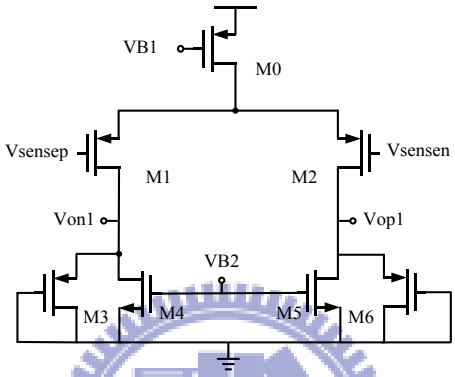


Figure 3-3.1(a): The schematic of the open-loop pre-amp

The design target on this preamp is focused on low noise, low gain, and high-bandwidth. The open-loop pre-amplifier dominates the whole system noise performance according to the theorem of noise figure in multi cascaded amplifier. The formula is approximated as follow:

$$\overline{V_{n-DCA}}^2 = \sqrt{V_{n1}^2 + \left(\frac{V_{n2}}{A_1^*}\right)^2} \qquad (3\text{-}3.1)$$

V_{n1} is the input-referred noise (IRN) from A1, the V_{n2} is the input-referred noise (IRN) from later stage. The gain is boosted enough to suppress the noise from later stage, but can't be too large for two reasons: Increase Miller's effect will degrade the sensitivity in this parasitic sensitivity architecture and the more distortion will be induced into the amplified signal. The gain can be calculated as (3-3.2)

$$A_v = \frac{gm_1}{gm_3} \tag{3-3.2}$$

g_m is the trans-conductance. M3 and M6 share the current from g_{m1} to boost the gain.

The IRN can be modeled in Figure 3-3.1(b) and calculated in (3-3.3). The noise level is decided by thermal noise in CHS technique. And the IRN can be suppressed by trans-conductance of the input pair of the amplifier.

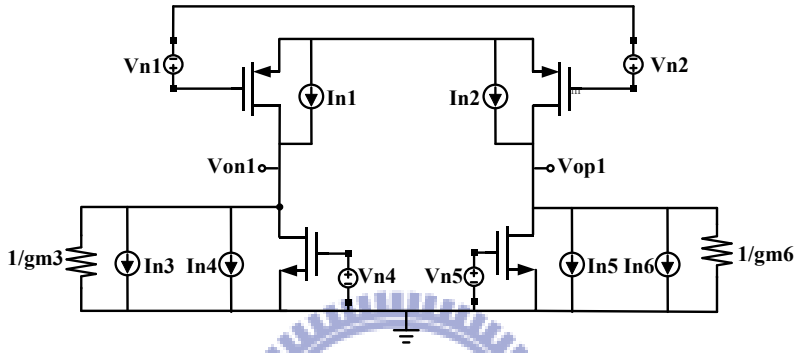
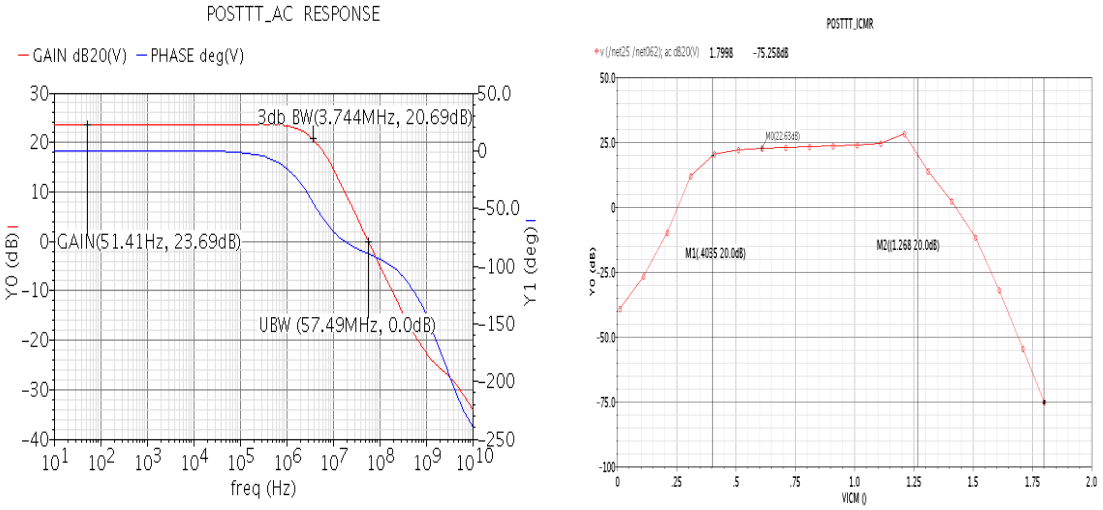


Figure 3-3.1(b): The noise model of the open-loop pre-amp

$$IRN = \overline{V_{ckt,in}^2} = 2\left[\frac{8}{3}KT\left(\frac{1}{gm_1} + \frac{gm_3}{gm_1^2} + \frac{gm_4}{gm_1^2}\right) + \frac{1}{C_{oxf}}\left(\frac{K_{p1}}{(WL)_1} + \frac{K_{p3}}{(WL)_3} + \frac{K_{n4}}{(WL)_4}\right)\right] \tag{3-3.3}$$

3-3.2 Low Noise Amplifier Post-layout Simulation

In the simulation, the amplifier noise, gain, bandwidth and input common range will be simulated. The input common range can be viewed as a toleration of voltage drift in the sensing node, the wider range the better toleration. And the noise spectrum is focused at 500K Hz, because the modulation architecture will remove the flicker noise and will retain the thermal noise. The modulation frequency is selected to be 500K Hz that is far away from the corner frequency of the Op-amp. Figure 3-3.2(c) ~ Figure 3-3.2(e) show the simulation result in TT corner, 1.8V, and 27℃. Other corners are listed in Table 3-3.2.



(c) (d)

Figure 3-3.2(c): AC response of the pre-amp; (d): Input range of the pre-amp

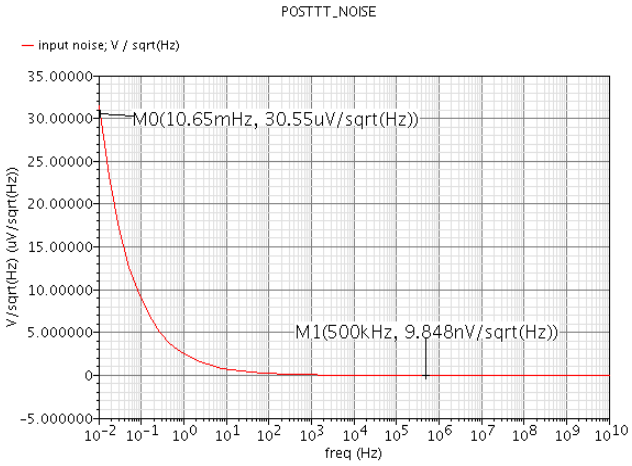


Figure 3-3.2(e): Noise spectrum of the pre-amp

Table 3-3.2: The corners simulation results of the pre-amp

	Unit	**TT**	**SS**	**FF**
DC Gain	dB	23.69	23.34	22.59
UGB	M Hz	57.49	48.48	69.25
3db BW	M Hz	3.744	3.228	5.041
ICMR	Volt	0.4~1.268	0.383~1.24	0.4813~1.35
Noise	nV/sqrt(Hz)(@500k)	9.848	10.31	9.517

3-4 Gm-C Filter and Linear Gain Tunable Interface

3-4.1 Gm-C Filter

The schematic of Gm_C filter is shown in Figure 3-4.1(a). The Gm_C filter is suitable for small input signal in the range of several millivolts. It is a first-order low-pass filters with a cut-off frequency about 40K and a linear input range of 200mV. The DC gain is 1. The low pass capacitor C_L has a value of 12pF.

The 3db bandwidth of the Gm-C filter is equal to the next VGA stage, and the two pole overlapping is formed. Thus, they have a powerful filtering capability. The first demodulation and the low pass filter can filter out the DC offset, flicker noise and charge injection error from first stage.

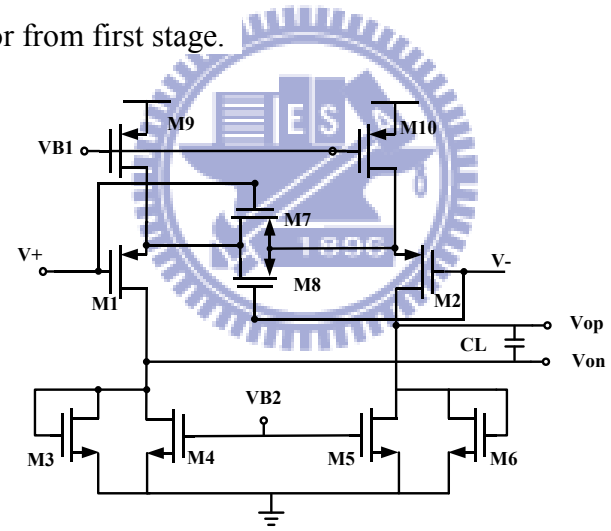


Figure 3-4.1(a): The schematic of the Gm_C filter

3-4.2 Gm-C Filter Post-layout Simulation

The AC simulation in TT corner, 1.8V, and 27℃ result show in Figure 3-4.2(a). And the high frequency signal decade to -19.79 dB at 500K Hz.

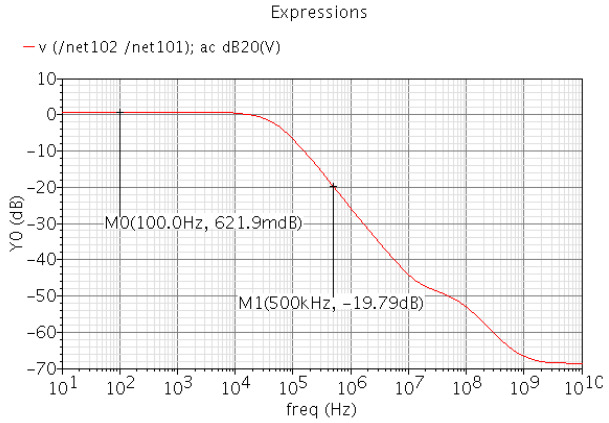


Figure 3-4.2(a): AC response of the Gm_C filter

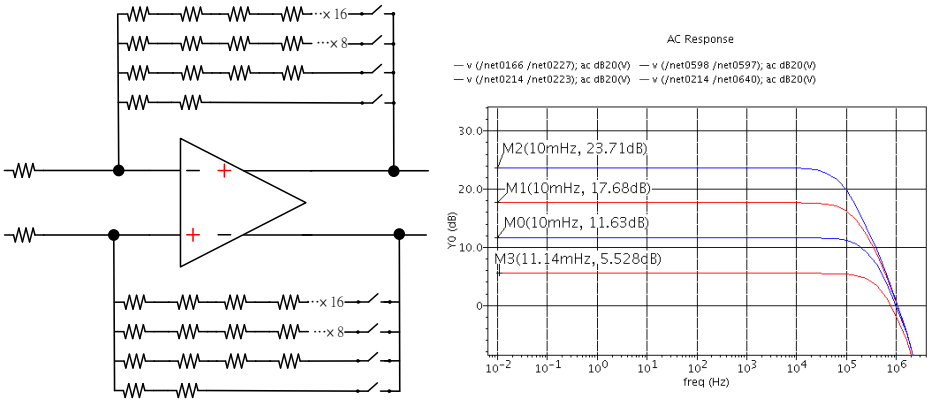
Table 3-4.2: Other corner simulation results of the Gm_C filter

	Unit	TT	SS	FF
DC Gain	(mdB)	621.6	869.7	859.8
Decade	@500k(dB)	-19.79	-21.12	-16.51

3-4.3 Linear Variable Gain Amplifier (VGA)

The digital control resistive VGA is utilized in most applications. Figure 3-4.3(a) and Figure 3-4.3(b) show the digital control resistive VGA and AC simulation. Although the digital control resistive VGA has the benefit in gain accuracy and has linear variation, but it occupies large area in resistors array to obtain the wider linear gain variation.

Instead of using the digital control resistive VGA, the open-loop linear VGA has been developed in [6]. The pure CMOS transistors are utilized in this topology. Like the digital control resistive VGA, the open-loop linear VGA also performs a decibel linear gain variation with an external control voltage.



(a) (b)

Figure 3-4.3(a): Digital control resistive VGA; (b): Simulation result

The V-I converter circuit is utilized to approximate the pseudo-exponential function, and it has a linear range when k is small enough, as shown in Figure 3-4.3(c). The function is described as follow:

$$e^{2ax} = \frac{e^{ax}}{e^{-ax}} \cong \frac{k+(1+ax)^2}{k+(1-ax)^2} \qquad (3\text{-}4.1)$$

K and a are the constants. (3-4.1) is valid for 2ax << 1. X is the independent variable. Here K is selected to be 0.15, a is selected to be 0.1.

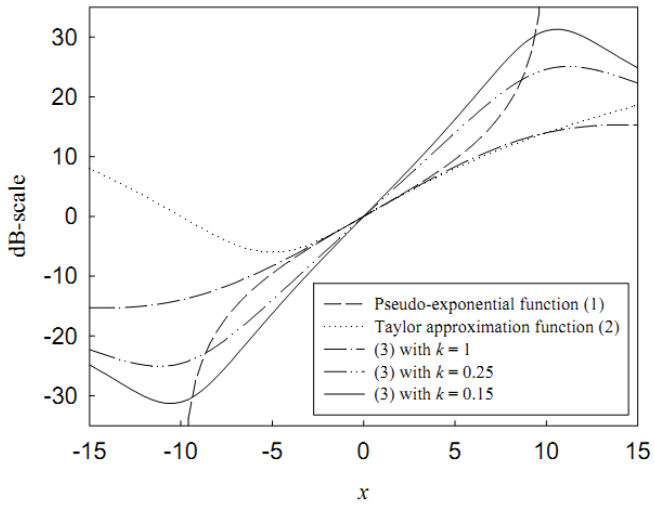


Figure 3-4.3(c): Plots of various functions on dB-scale [6]

Design the currents (Ic1 and Ic2) of a V-I converter in Figure 3-4.3(d) to meet the k and a in following equation:

$$e^{2ax} = \frac{e^{ax}}{e^{-ax}} \cong \frac{k+(1+ax)^2}{k+(1-ax)^2} = \frac{I_{c2}}{I_{c1}} = \frac{\frac{I_0}{K(V_{dd}-|V_{th}|)^2}+\left[1+\frac{V_c}{(V_{dd}-|V_{th}|)}\right]^2}{\frac{I_0}{K(V_{dd}-|V_{th}|)^2}+\left[1+\frac{V_c}{(V_{dd}-|V_{th}|)}\right]^2} \qquad (3\text{-}4.2)$$

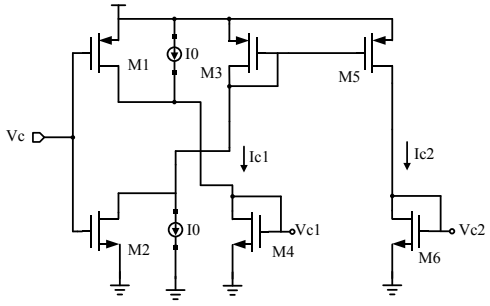


Figure 3-4.3(d): The schematic of the V-I converter

Figure 3-4.3(e) shows the proposed VGA. The VGA is composed of an input source-coupled pair (M2 and M5) and diode-connected loads (M3 and M4). The tail currents of M0 and M1are mirrored from M4 and M6 of the V-I converter. The sum of currents through input pair and loads is equal to that of the upper PMOS current sources (M7 and M8). The open loop gain is given as:

$$\text{Gain} = \sqrt{\frac{(W/L)_{2,5}\times I_{C2}}{(W/L)_{3,4}\times I_{C1}}} \qquad (3\text{-}4.3)$$

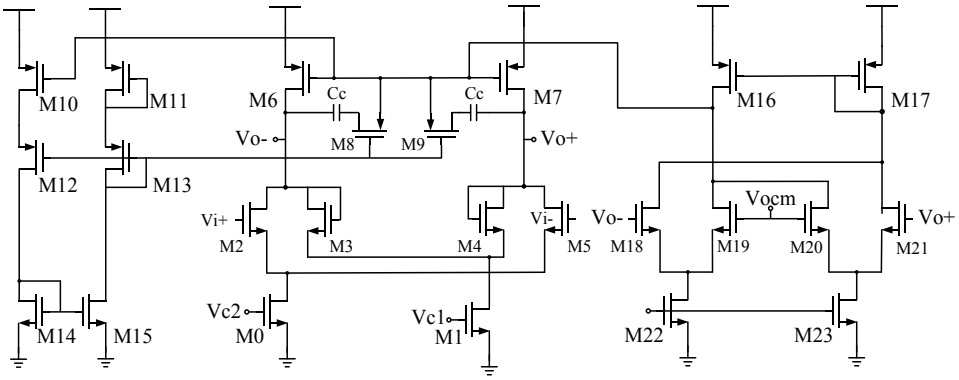


Figure 3-4.3(e): The schematic of the VGA

For the common mode feedback (CMFB) loop (M16~M23), the stability in the feedback loop is the design key point. Thus, understand the poles and zeros locations are the necessary tasks. The zero of CMFB loops is given by:

$$\omega_z \approx \frac{1}{C_C(g_{m6,7}{}^{-1} - R_z)} \tag{3-4.4}$$

G_m is the trans-conductance of M6, M7. R_z is the MOS resistors M8, M9.

The second pole of CMFB is given by:

$$\omega_{p2} \approx \frac{-g_{m7}}{C_L + C_{g7}} \tag{3-4.5}$$

C_L is the loading capacitor. C_{g7} is the total capacitance in the gate of M7.

The large loop gain (T) of the CMFB corrects the output voltage to output common mode voltage which is given by:

$$|T| = g_{m18} \times (r_{o16} // r_{o19}) \times g_{m7} \times \frac{1}{g_{m4}} \tag{3-4.6}$$

3-4.4 VGA Post-layout Simulation

Figure 3-4.4(a) is the AC gain variation with the control voltage Vc. In TT corner, 1.8V, and 27℃, the Vc is swept from 0.4V to 1.4V. Other corners simulation results are listed in Table 3-4.4 and plotted in Figure 3-4.4(b).

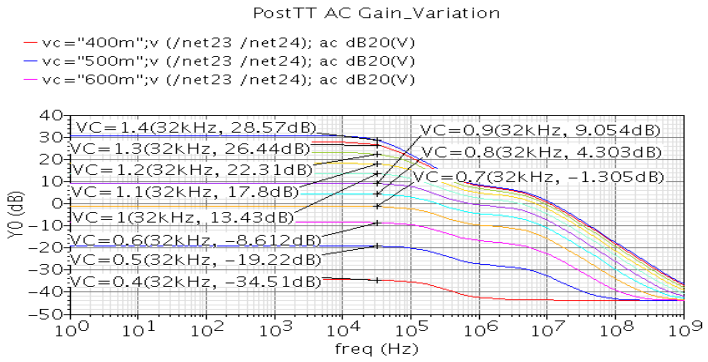


Figure 3-4.4(a): AC gain sweep of the VGA(TT, VDD=1.8V, T=27℃)

Table 3-4.4: AC gain sweep data of the VGA (VDD=1.8V, T=27℃)

Vc	0.4	0.5	0.6	0.7	0.8	0.9	1	1.1	1.2	1.3	1.4
gain(tt)	-34.51	-19.22	-8.612	-1.305	4.303	9.054	13.43	17.8	22.31	26.44	28.57
gain(ff)	-29.12	-15.41	-6.156	0.364	5.451	9.761	13.69	17.51	21.4	25.14	27.54
gain(ss)	-39.17	-22.86	-11.05	-2.999	3.057	8.162	12.88	17.62	22.42	26.22	28.79

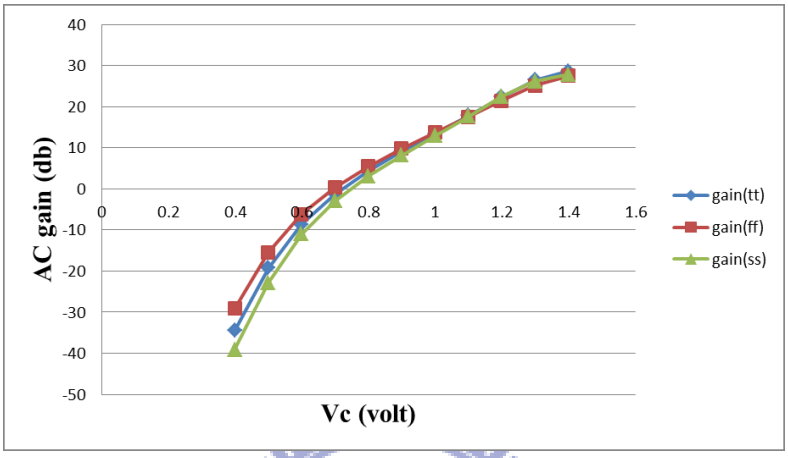


Figure 3-4.4(b): AC gain sweep data of the VGA (VDD=1.8V, T=27℃)

The stability of the CMFB is simulated in Figure 3-4.4(c) with different Vc in TT corner, 1.8V, and 27℃. Other corners simulation results are plotted in Figure 3-4.4(d).

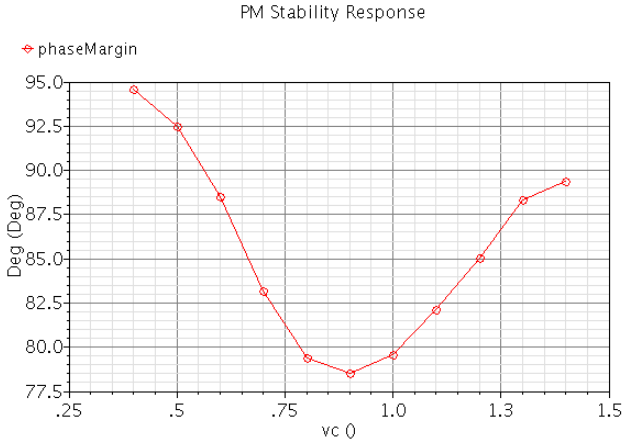


Figure 3-4.4(c): CMFB stability response of the VGA (TT, VDD=1.8V, T=27℃)

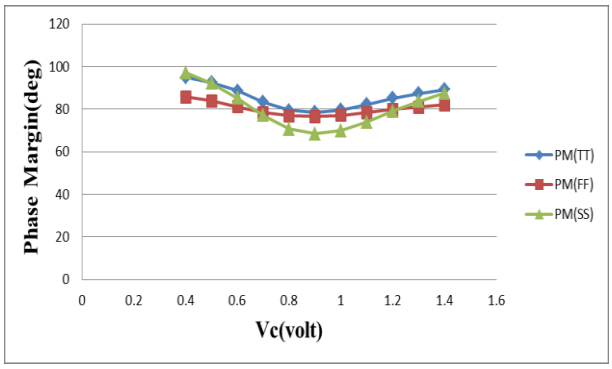


Figure 3-4.4(d): Stability response of the VGA CMFB (VDD=1.8V, T=27℃)

The loop gain is plotted in Figure 3-4.4(e) with 1.8V, and 27℃.

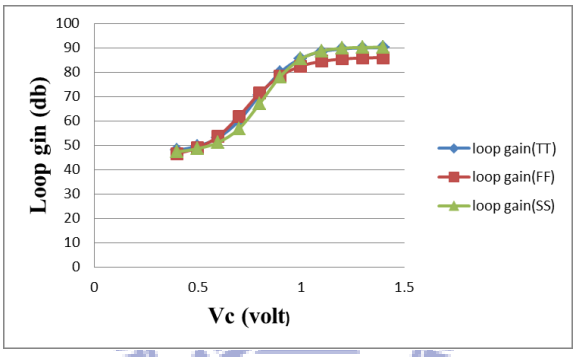
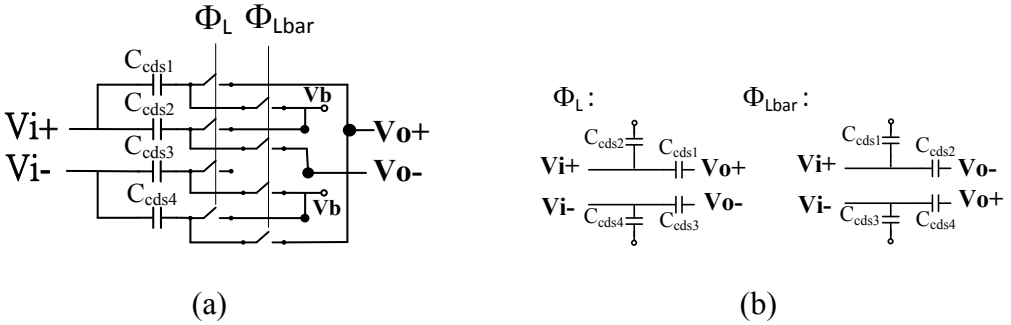


Figure 3-4.4(e): Loop gain of the VGA CMFB (VDD=1.8V, T=27℃)

3-5 Correlated Double Sampling (CDS) Demodulation

In reference [5], The CDS is combined with demodulation function. Different from conventional CDS, the new approach stores the flicker noise and DC offset in C_{CDS} in two phases, samples the differential signals at the same time. In the next phase, the differential signals and error voltage will be subtracted. Thus, the flicker noise and DC offset will be canceled and the signal will become two times. Figure 3.5(a) shows the CDS schematic



(a) (b)

Figure 3.5(a): The schematic of the CDS; (b): CDS operation principle

In Figure 3.5(b), the CDS can complete the noise and the offset cancelation by two steps operations. At the operation principle can be described as follow:

At ϕ1, the voltage stored in $C_{cds2,\,4}$ is given by:

$$V_{i+}(1)=V_i+V_{error} \tag{3-5.1}$$

$$V_{i-}(1)=-V_i+V_{error} \tag{3-5.2}$$

At ϕ2, the voltage stored in $C_{cds1,\,3}$ is given by:

$$V_{i+}(2)=-(V_i+V_{error}) \tag{3-5.3}$$

$$V_{i-}(2)=-(-V_i+V_{error}) \tag{3-5.4}$$

The V_{error} is the DC offset and flicker noise of the Gm-C filter and the VGA. After the two operation steps, the output voltage can be calculated as follow:

$$Vo_+=V_{i-}(2)+V_{i+}(1)\approx 2V_i \tag{3-5.5}$$

The calculation result shows that the error voltage can be subtracted by the CDS.

3-6 Low Pass Filter (LPF)

3-6.1 Op-amp Design

In the contribution to the architecture of DCA and CDS demodulation, the first

order low pass filter is good enough to filter out the high frequency noise. Besides, the first order low pass filter with differential difference amplifier (DDA) is designed in the last stage. Because the sensor offset is a DC deviation after demodulation. The DDA is utilized to correct the sensor offset and DC offset in this stage. In order to obtain the linear amplified signal, the close loop configuration is adopted in the low pass filter. And the Op-amp design considerations are the linearity and gain requirement in this stage. The demodulated signal relaxes the slew rate and band width. The folded cascade op has high gain, high output swing as shown in Figure 3-6.1(a). In continuous time applications, the CMFB loop with source degeneration resistor (M17~M20) increases the linearity.

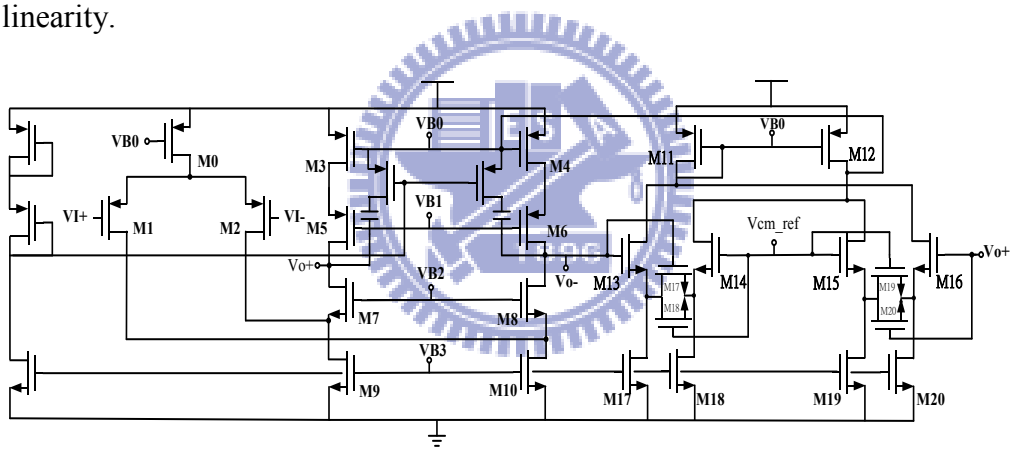


Figure 3-6.1(a): The schematic of the folded cascode op

3-6.2 Op-amp and LPF Post-layout Simulation

In TT corner, 1.8V, and 27℃, Figure 3-6.2(a) shows the DC gain up to 66.13dB, phase margin 89.86 (deg), bandwidth 434.8K Hz.

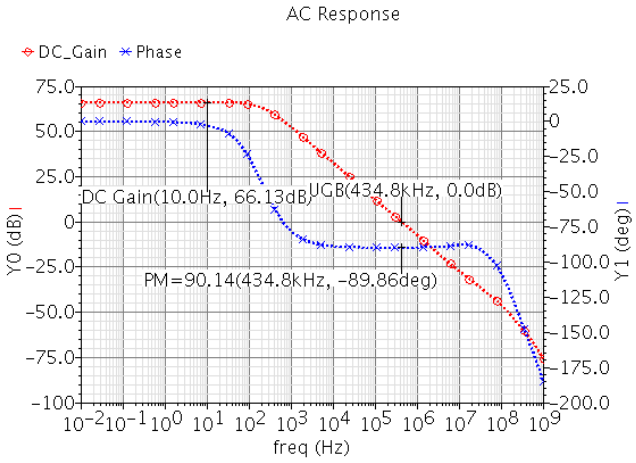


Figure 3-6.2(a): AC response of the continuous time folded cascade op

Figure 3-6.2(b) shows the input common mode range (ICMR) from 0V ~ 1.2 V.

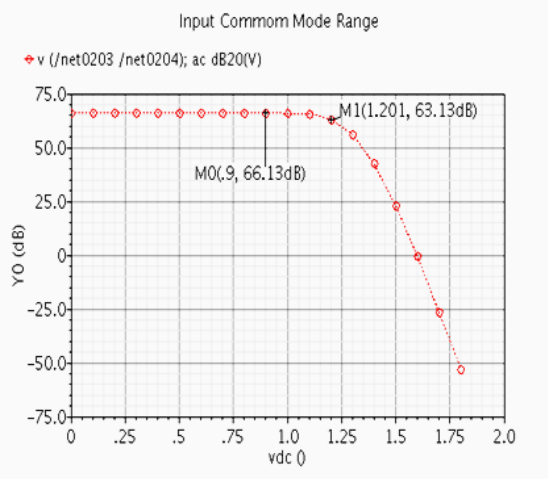


Figure 3-6.2(b): ICMR of the folded cascade op

Other corners simulation results are arranged in Table 3-6.2(a).

Table 3-6.2(a): Other corners simulation of the continuous time folded cascade op

	Unit	**TT**	**SS**	**FF**
DC gain	dB	66.13	66.43	63.15
PM	Deg	90.14	90.21	90.09
3db-BW	Hz	591	504	703
ICMR(V)	Volt	0~1.2	0~1.156	0~1.232

The AC response in close loop configuration is shown in Figure 3-6.2(c). Figure 3-6.2(d) shows the slew rate and output swing in transient response.

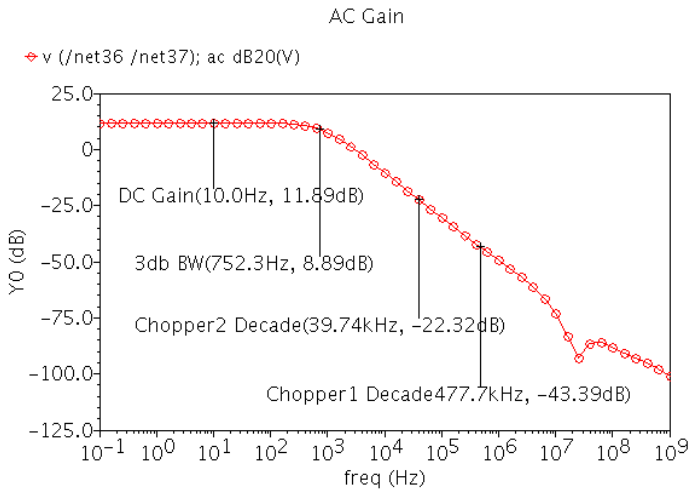


Figure 3-6.2(c): AC response in close loop configuration

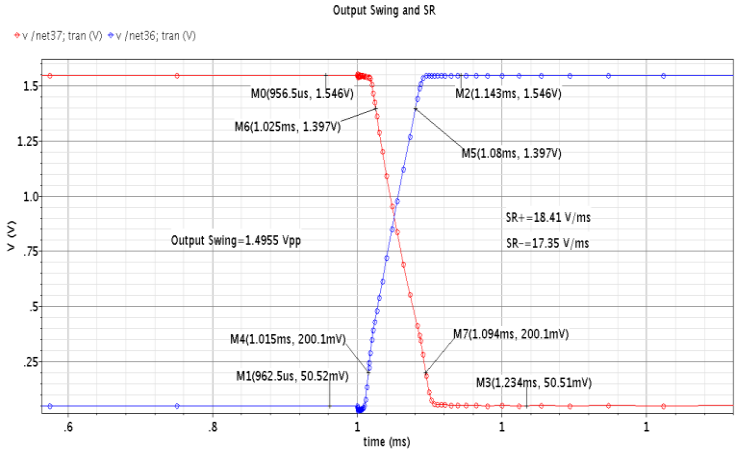


Figure 3-6.2(d): Slew rate and output range in close loop configuration

Other corners simulation results are listed in Table 3-6.2(b).

Table 3-6.2(b): Other corners in close loop configuration

	Unit	TT	SS	FF
DC gain	@10Hz(dB)	11.89	11.98	11.87
SR+	(V/ms)	18.44	12.14	25.1
SR-	(V/ms)	17.12	10.03	23.24
Output Range	Volt	1.4983Vpp	1.51Vpp	1.5022Vpp

3-7 Bandgap Reference (BGR) Circuit

3-7.1 Low Voltage BGR

The bandgap reference (BGR) provides the currents and reference voltage for the whole circuits. The circuit topology of the designed BGR is shown in Figure 3-7.1(a). The BGR consists of start-up circuit (M1~M3), high open loop gain single end op, the diode connect PNP. The start-up circuit is utilized to avoid the null operation point. It must be close (M1 off) after op settled. The high open loop gain op based on negative feedback topology force its input at the same dc level. In order to layout in common centroid style, the PNP of Q1 and Q2 is programed in the ratio 1:8. The BGR provide a reference voltage which is the sum of negative temperature coefficient (V_{EB1}) and positive temperature coefficient (ΔV_{BE}). The BGR produces a negative temperature coefficient by V_{EB1},

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4+m)V_T - E_g/q}{T} \approx -2mV \qquad (3\text{-}7.1)$$

Where $m \cong -3/2$, Eg is the Energy Bands of silicon, q = 1.6E-19 Coulomb, V_T is the thermal voltage. T is absolute temperature ° K. And the positive temperature coefficient ΔV_{BE} is given by:

$$\frac{\partial V_{BE}}{\partial T} = \frac{K}{T} \ln n \qquad (3\text{-}7.2)$$

K is the Boltzmann constant. N is the ratio of Q_1 and Q_2. The reference voltage is given by:

$$V_{ref} = \frac{R_3}{R_2 + R_3} \times (V_{BE3} + I_{M3} \times R_2) \qquad (3\text{-}7.3)$$

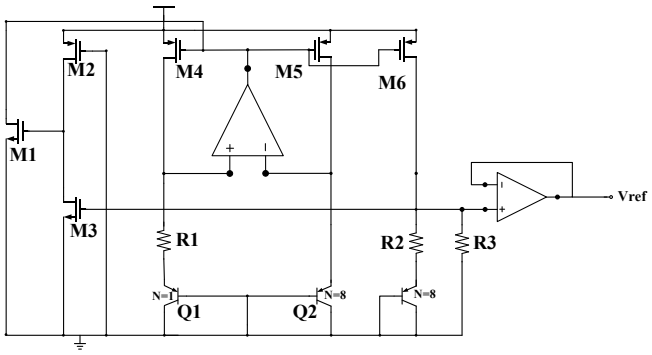


Figure 3-7.1(a): The schematic of BGR

3-7.2 BGR Post-layout Simulation

First, we sweep the temperature from -100℃ to 100℃ in different corners and the simulation results are shown in Figure 3-7.2(a) ~ Figure 3-7.2(c).

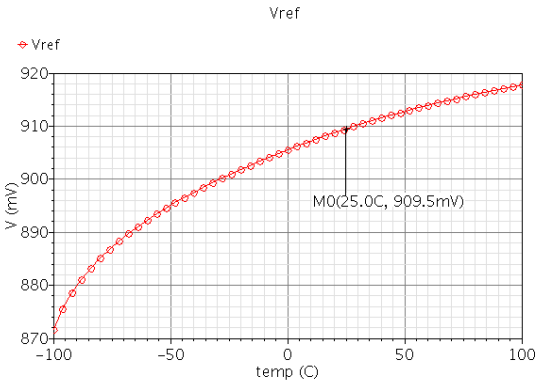


Figure 3-7.2(a): Sweep temperature (TT)

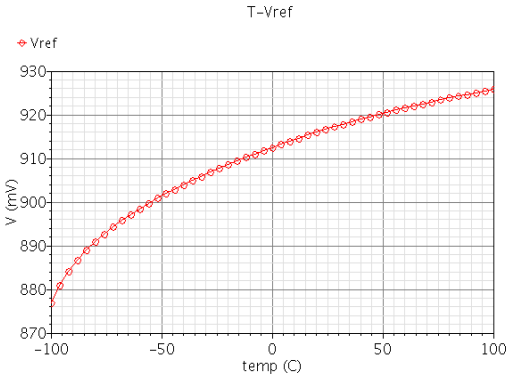


Figure 3-7.2(b): Sweep temperature (SS)

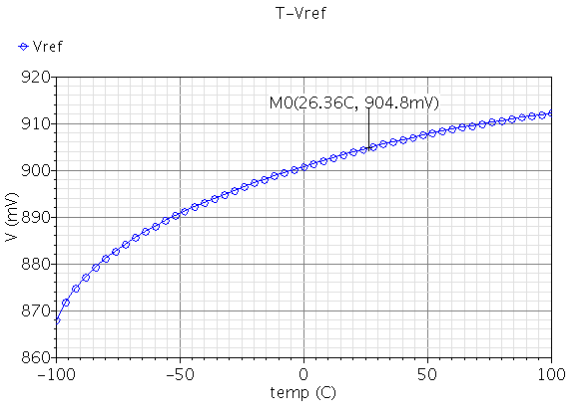


Figure 3-7.2(c): Sweep temperature (FF)

Second, we sweep the power supply from 0V to 3V in different corners and the simulation results are shown in Figure 3-7.2(d) ~ Figure 3-7.2(f).

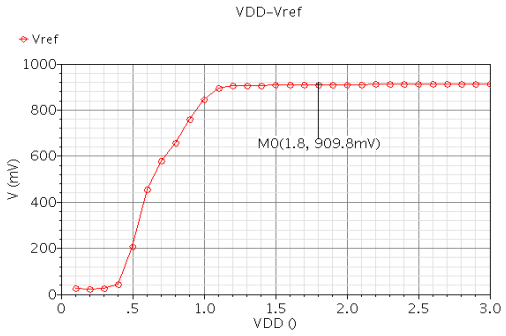


Figure 3-7.2(d): Sweep VDD (TT)

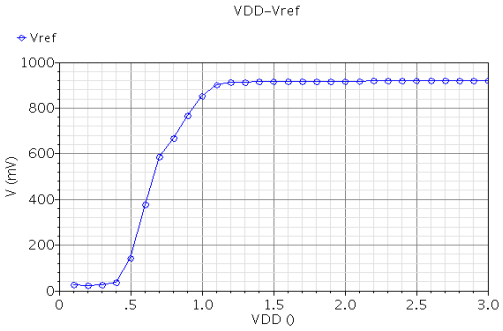


Figure 3-7.2(e): Sweep VDD (SS)

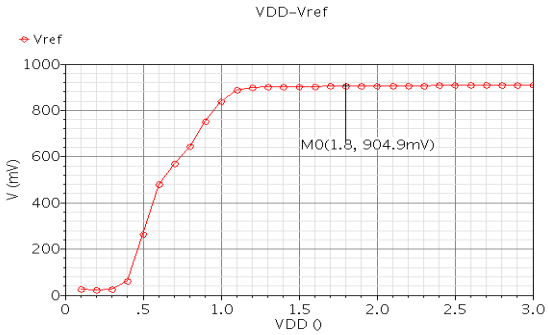


Figure 3-7.2(f): Sweep VDD (FF)

Third, the startup function at the M1 gate is shown in Figure 3-7.2(g) ~ Figure 3-7.2(i). The power supply is given by a ramp.

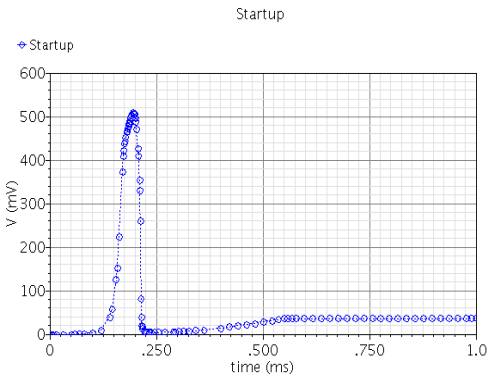


Figure 3-7.2(g): Startup function (TT)

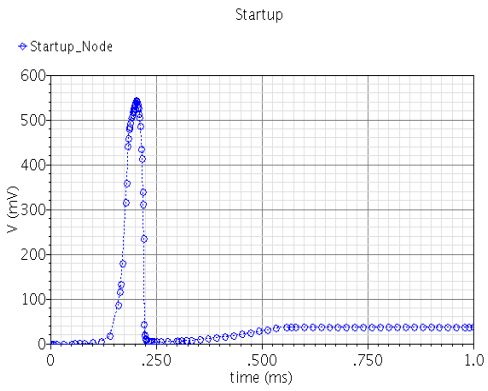


Figure 3-7.2(h): Startup function (SS)

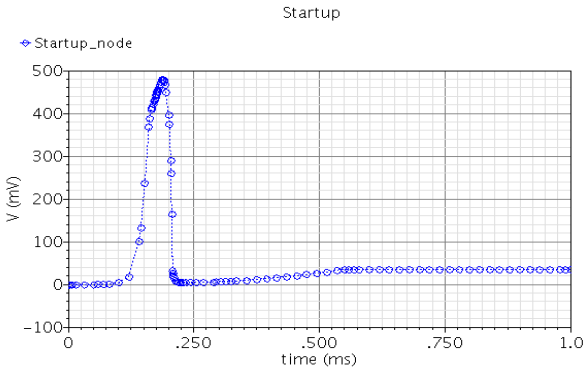


Figure 3-7.2(i): Startup function (FF)

3-8 Preamp System Simulation

3-8.1 System Noise Contribution

In the system simulation, we focused on the total noise contribution and linearity of output signal. For noise simulation, the DCA with CDS demodulation architecture is simulated with PSS and Pnoise functions in SpectreRF. In order to facilitate convergence during simulation, the superposition principle is adopted in the analysis. The system equivalent circuit is shown in Figure 3-8.1(a). The system equivalent circuit can be separated by high chopper equivalent circuit and low chopper equivalent circuit as shown in Figure 3-8.1(b).

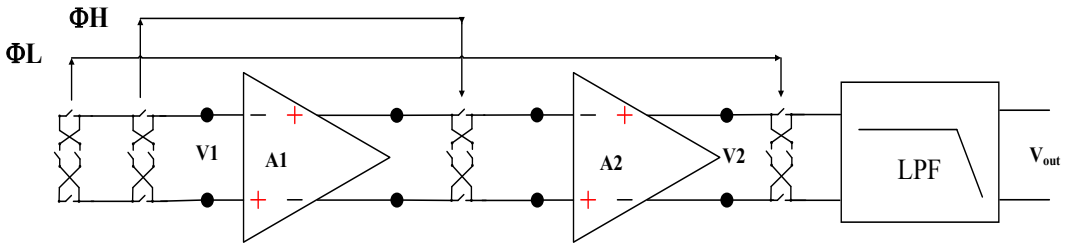


Figure 3-8.1(a): DCA equivalent circuit

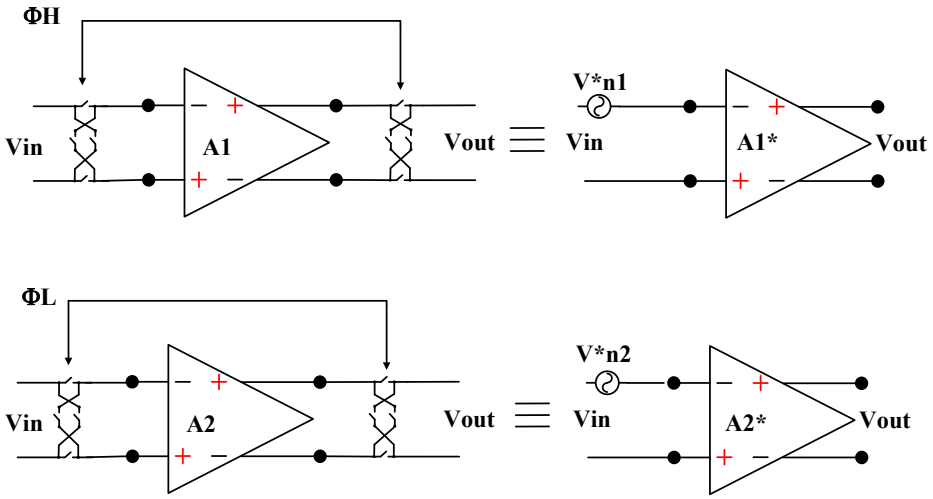


Figure 3-8.1(b): High frequency and low frequency chopper equivalent circuits

First, we obtain the noise contribution at the first demodulation output by simulating the high frequency chopper equivalent circuits. Figure 3-8.1(c) shows the input referred noise (IRN) of the high chopper frequency. The IRN of the high frequency chopper is 5.59nV/$\sqrt{}$Hz within 500Hz. Figure 3-8.1(d) shows the input referred noise (IRN) for low frequency chopper. The IRN of low frequency chopper is 172.5nV/$\sqrt{}$Hz within 500Hz. The above simulation is the post-layout simulation is in TT corner, 1.8V, and 27° C.

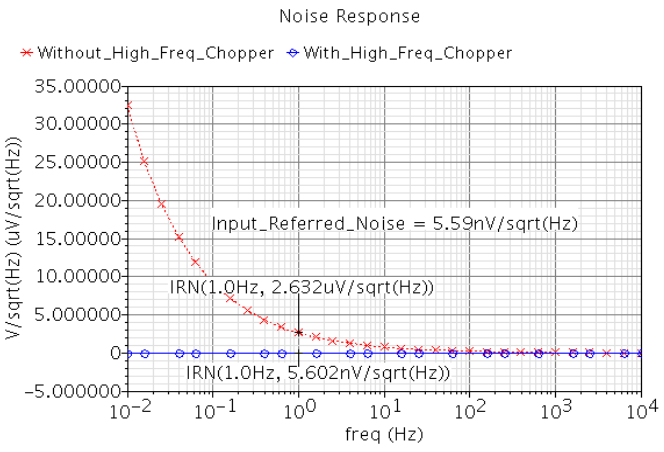


Figure 3-8.1(c): Input referred noise for high frequency chopper

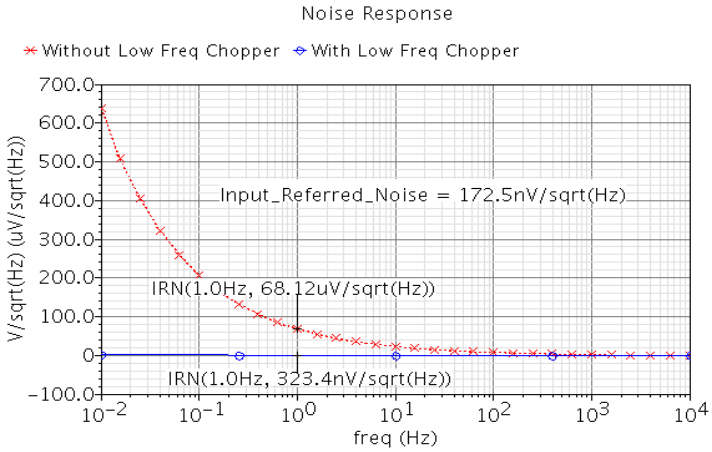


Figure 3-8.1(d): Input referred noise for low frequency chopper

Figure 3-8.1(a) is equivalent to Figure 3-8.1(e). Then, calculate the noise contribution in this configuration according to the noise figure formula in (3-3.1). We also can verify that the first stage dominates the system noise contribution. The system noise floor is 12.57nv/$\sqrt{}$Hz within 500Hz in TT corner, 1.8V,

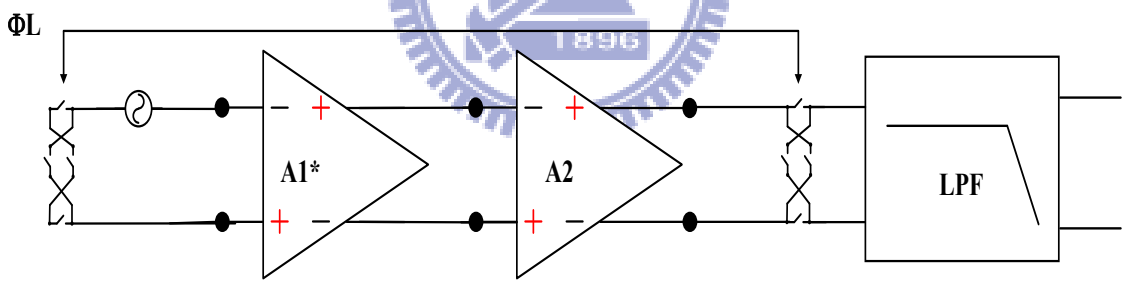


Figure 3-8.1(e): Figure 3-8.1(a) equivalent circuit

Other corner simulation results are listed in Table 3-8.1

Table 3-8.1: System noise floor

	Unit	TT	SS	FF
Noise Floor	nV/sqrt(Hz)	12.57	13.48	11.68

3-8.2 Preamp Output Signal Transient Simulation

Figure 3-8.2(a) ~ Figure 3-8.2(d) show the transient results at all stage single output nodes in TT corner, 1.8V, 27℃. The system sensitivity is set to be in the 4g mode.

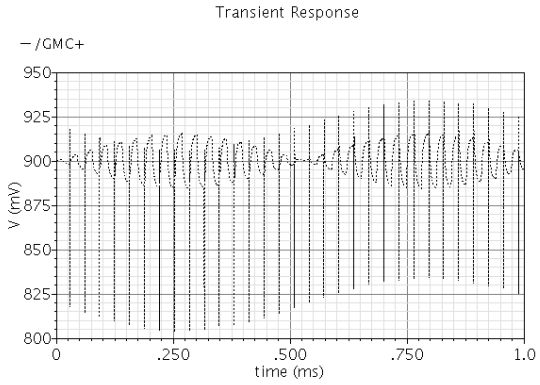


Figure 3-8.2(a): The Gm_C output

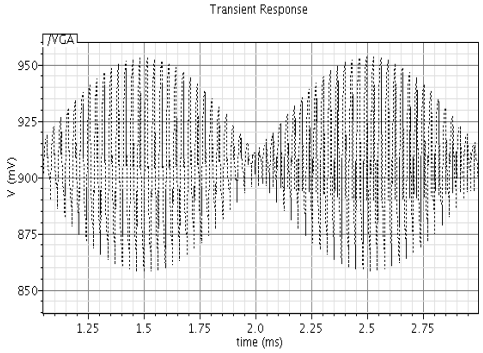


Figure 3-8.2(b): The VGA output

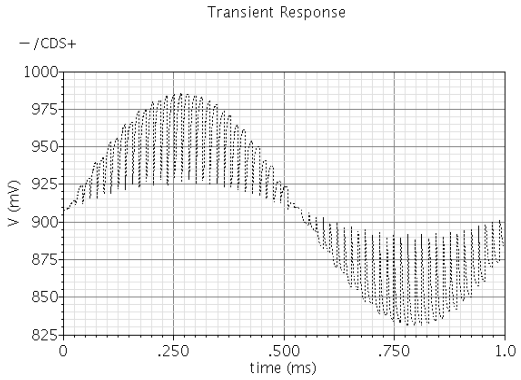


Figure 3-8.2(c): The CDS output

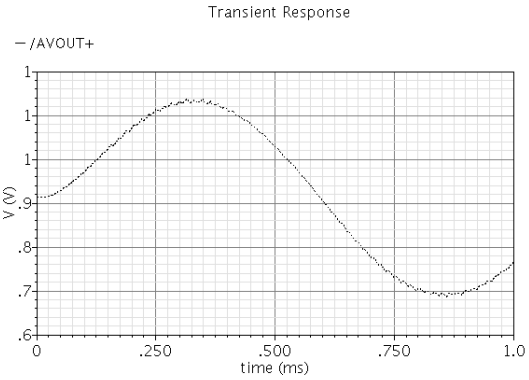


Figure 3-8.2(d): The AAF output

The amplified signals has a good linearity in TT corner, 1.8V, 27℃.

3-9 Preamp System Specifications

3-9.1 Sensitivity

By varying the VGA from -6dB to 28.57dB, the tunable sensitivity can be adjusted from 324.8mV/fF ~ 17425.47mV/fF (differential output) in TT corner, 1.8V, 27℃. But the practical operation range is -6dB~20dB for $\pm 1 \sim \pm 10g$ applications.

3-9.2 Noise

The circuit noise contribution and Brownie noise are simulated in section 3-8.1 and section 2-3.4, 12.57nV/√Hz and 4.2ug/√Hz respectively. The circuit equivalent noise can be viewed as a circuit noise equivalent acceleration (CNEA) that depends on the voltage resolution of the interface circuit V_{noise} and sensitivity (S) of the accelerometer ($S = \Delta V/a_{in}$), the sensitivity of the proposed accelerometer is 0.98mV/g, and the CNEA can be calculated as following equation:

$$\mathrm{CNEA} = \frac{V_{noise}}{S} \qquad \left[\frac{m/s^2}{\sqrt{Hz}}\right] \tag{3-9.1}$$

V_{noise} equals to 12.57nV/√Hz. CNEA is 12.82ug/√Hz. And the total noise equivalent acceleration (TNEA) can be calculated in the following equation:

$$\mathrm{TNEA} = \sqrt{\mathrm{CNEA}^2 + \mathrm{BNEA}^2} \qquad \left[\frac{m/s^2}{\sqrt{Hz}}\right] \tag{3-9.2}$$

TNEA equals to 13.49ug/√Hz in TT corner, 1.8V, 27℃. The TNEA can be multiplied by the sensitivity $S_{\Delta C}$ (ΔC/g) to obtain the noise floor in capacitance scale (F/√Hz).

3-9.3 Dynamic Range (DR)

The definition of dynamic range is the ratio of maximum detectable acceleration and minimum detectable acceleration in logarithmic scale, which is given by:

$$\mathrm{DR}_{(db)} = 20\log(\frac{a_{max}}{a_{min}}) \quad (3\text{-}9.3)$$

a_{max} is 10g, a_{min} is the product of TNEA and signal bandwidth. TNEA equals to 13.49ug/$\sqrt{}$Hz. The signal bandwidth equals to 500 Hz. And the DR can be calculated to be 90.41 dB. In TT corner, 1.8V, 27℃, other corner simulation results are listed in Table 3-9. The sensitivity shows the differential output voltage.

Table 3-9: System specifications (BNEA =4.2ug/$\sqrt{}$Hz)

	Unit	TT	FF	SS
Sensitivity (max)	mV/fF	17425.47	17258.5	17807.11
Sensitivity (min)	mV/fF	324.8	315.72	286.2
CNEA	ug/√Hz	12.82	12.2	13.75
TNEA	ug/√Hz	13.49	13.3	14.377
DR	dB	90.41	89.85	90.98
Power	uW	619.08	1183	556.24

3-10 2nd SDM Behavioral Simulation

3-10.1 Ideal Model Simulation

Before implementing a 2nd SDM in transistor level, the behavioral simulation must be done, which is convenient to choose the parameters of a proposed 2nd SDM for designers and easily validates any changes on the system level. It can simplify the work on transistor-level design as it can predict the performance of the SDM on a higher level. Thus, create the ideal behavioral model in MATLAB Simulink as shown in Figure 3-10.1(a).

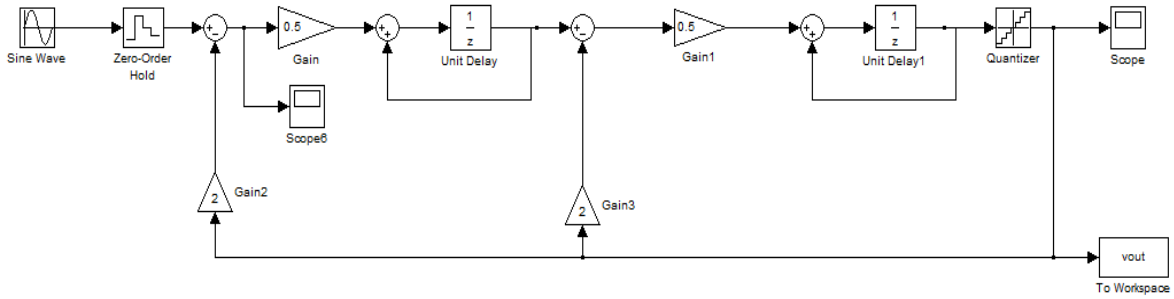


Figure 3-10.1(a): Ideal linear model of the 2nd SDM

The parameters are listed in Table 3-10.1. And the simulation result is almost the same as hand calculation in section 1-4.4 as shown in Figure 3-10.1(b).

Table 3-10.1: 2nd SDM parameters

Parameters	Variable
A/D bit number	1
OSR	250
Signal bandwidth	950Hz
a_1	0.5
a_1	2
b1	1
b2	1

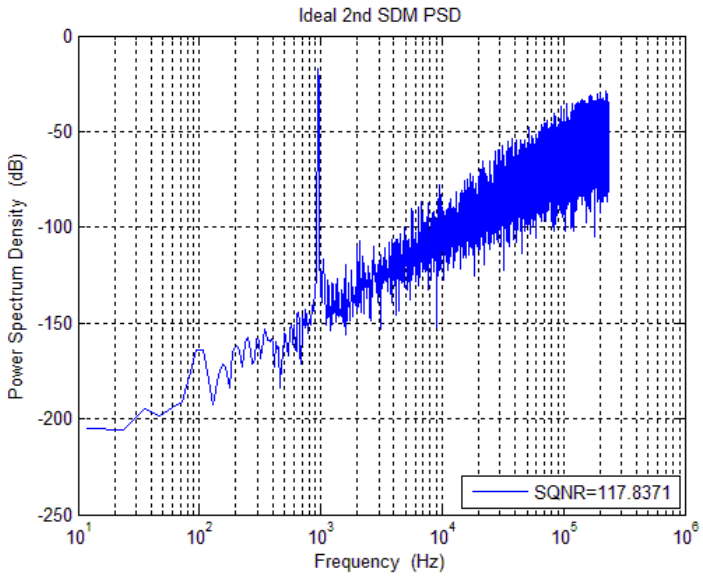


Figure 3-10.1(b): The simulation result of the ideal SDM behavioral model

3-10.2 Non-ideal Model

Base on the ideal model of the SDM in previous section, the non-ideal effect of the CMOS circuits such as clock jitter, switch thermal noise, OP noise, finite DC gain, bandwidth and slew rate must be taken into considerations.

Aperture Jitter

The clock jitter can occur from the main clock generator to the entire SDM, or relative jitter can occur between the circuit blocks of the SDM. The significant effect of the clock jitter on the SDM is the sample and hold, the front-end SDM. And the quantizer will have negligible effect, since the filter is designed to settle to a given accuracy within half the sampling period. Although the timing error occurs slightly early or late as shown in Figure 3-10.2(a), the output of the filter was fully settled, where ΔV is the same as noise. And the same arguments between the DAC and filter is similarly, too [22].

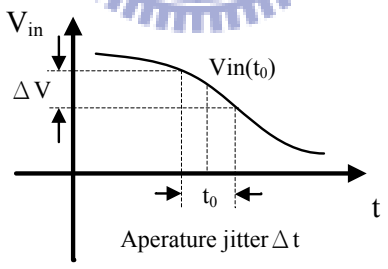


Figure 3-10.2(a): Aperture jitter

In the ideal operation, the SC circuits completes the charge transfers during the uniform non-overlap clocks, however sampling clock jitter results in non-uniform sampling time sequence. The error voltage will increase the total error power at the quantizer output and decrease the SQNR. The error voltages are introduced by a sine

wave input with amplitude A and frequency f_{in}, the error voltage occurs at the difference of the sampling timing Δt that is derived as follow:

$$V_{in}(t+\delta) - V_{in}(t) \approx 2\pi f_{in}\Delta t A\cos(2\pi f_{in}t) = \Delta t * \frac{d}{dt}V_{in}(t) \qquad (3\text{-}10.1)$$

The behavioral model is created in Figure 3-10.2(b). Both the input signal $V_{in}(t)$ and its derivative $\frac{dV_{in}(t)}{dt}$ are continuous-time signals, which are sampled with sampling period T_S by a zero-order hold. In the model, the sampling uncertainty Δt. Δt is assumed to be a Gaussian random process X(t) with standard deviation Δτ. The signal n(t) is implemented by a sequence of random numbers with Gaussian distribution, zero mean, and unity standard deviation.

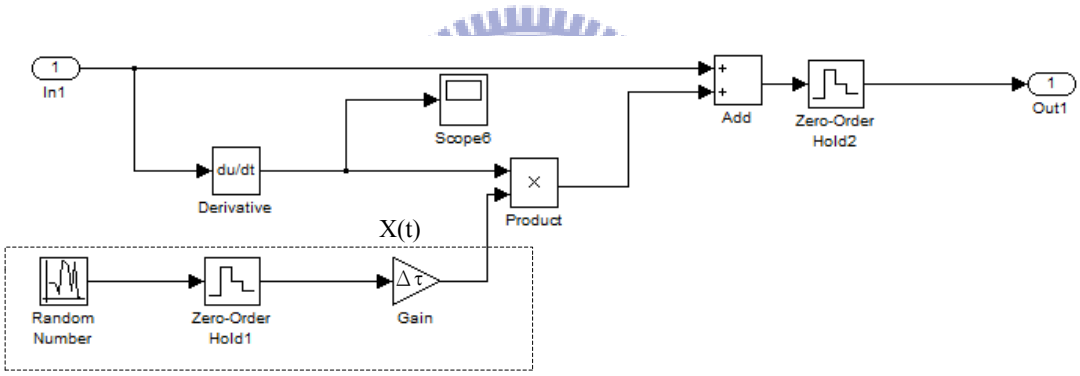


Figure 3-10.2(b): Aperture jitter behavioral model

Switch Thermal Noise

The switch thermal noise is contributed by the sampling phase and integration phase. At the sampling phase, the total noise power included the D/A (P_{NDA}) and two sampling capacitor (C_s, P_{NCAP}) at two input branch that uniform distributes in sampling frequency and integral in-band noise power as follow:

$$P_{NCAP} = \int_{-F_B}^{F_B} \frac{2KT}{C_s f_s} df = \frac{1}{OSR}\left(\frac{2KT}{C_s}\right) \qquad (3\text{-}10.2)$$

$$P_{NDA} = \int_{-F_B}^{F_B} \frac{[2\times(2^B-1)]^2 KT}{C_s f_s} df = \frac{1}{OSR}\left(\frac{4(2^B-1)^2 KT}{C_s}\right) \quad (3\text{-}10.3)$$

Where K is the Boltzmann's constant. T is the resistor's absolute temperature. The $[2*(2^B-1)]^2$ is the number of total switch of the D/A in fully differential configuration. Take the gain effect at the first integrator gain $[a_1/2*(2^B-1)]$ and second integrator gain b_1 into consideration, the noise power at output becomes to:

$$P_{NDAO} = P_{NDA} \times [a_1/2(2B-1)]^2 \times {b_1}^2 = \frac{1}{OSR}\left(\frac{4KT}{C_s}\right) \quad (3\text{-}10.4)$$

And the total noise power in sampling phase is calculated as follow:

$$P_{totS} = \frac{6}{OSR}\left(\frac{KT}{C_s}\right) \quad (3\text{-}10.5)$$

At the integration phase, it is calculated by the first order low pass filter transfer function and given by:

$$P_{totI} = \frac{5}{2OSR}\left(\frac{KT}{C_s}\right) \quad (3\text{-}10.6)$$

Since the thermal noises introduced during these two phases are uncorrelated, the total noise in SC integrator is calculated as follow:

$$P_{tot} = \frac{5}{2OSR}\left(\frac{KT}{C_s}\right) + \frac{6}{OSR}\left(\frac{KT}{C_s}\right) = \frac{17}{2OSR}\left(\frac{KT}{C_s}\right) \quad (3\text{-}10.7)$$

The switch thermal noise voltage is superimposed to the input voltage $V_{in}(t)$ leading to

$$V_{in}(t) - P_{tot}(t) = \left[V_{in} + \sqrt{\frac{17}{2OSR}\left(\frac{KT}{C_s}\right)}\, n(t)\right] \times b = \left[V_{in} + \sqrt{\frac{17}{2b*OSR}\left(\frac{KT}{C_f}\right)}\, n(t)\right] \times b \quad (3\text{-}10.8)$$

Where n(t) represents a Gaussian random process with unity standard deviation, b_n denotes the integrator gain C_S/C_f (C_f is the D/A capacitors). The model of the above calculation is shown in Figure 3-10.2(c). The integrator in Figure 3-10.2(c) includes two SC input branches and f_u equals to $\sqrt{\frac{17}{2bn*OSR}\left(\frac{KT}{C_f}\right)}$. Besides, the thermal noise model is

placed at front-end of the SDM, and the switch thermal noise at the second integrator will be filtered out by noise shaping in SDM feedback loop like the quantization noise at the quantizer input. So, it can be negligible at system simulation of the SDM.

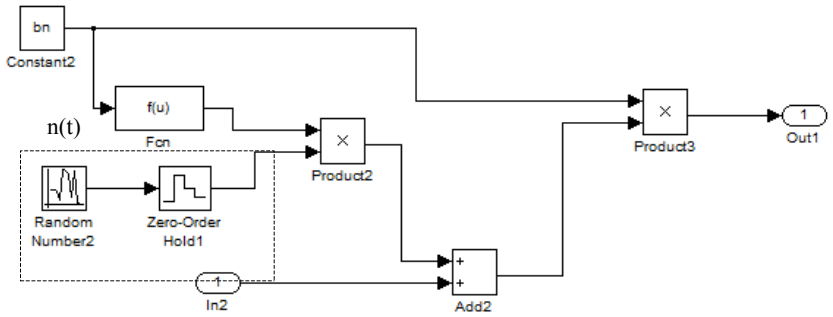


Figure 3-10.2(c): Switch thermal noise behavioral model

Pre-amplifier Noise

By means of the DCA and CDS technique the pre-amplifier noise is dominated by the active anti-aliasing filter. Moreover, the OP-amp noise at the first integrator cannot be filtered out by noise shaping, but the auto-zeroing technique is adopted at the first integrator. Therefore, the residual noise is the thermal noise and it is modeled in Figure 3-10.2(d). The V_n denotes the thermal noise of the OP and Pre-amp.

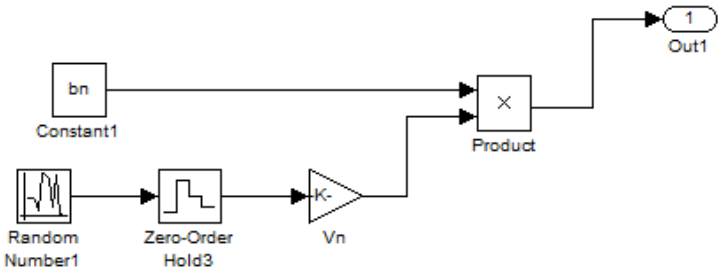


Figure 3-10.2(d): The OP thermal noise behavioral model

Finite Open-loop DC Gain

The finite DC gain results the "integrator leakage". The consequence of this integrator "leakage" is that the in-band noise is increased. And the transfer function of the integrator with the integrator leakage (α) is given by:

$$H(z) = \frac{z^{-1}}{1-\alpha z^{-1}} \tag{3-10.8}$$

So, the DC gain of the integrator H_0 becomes to be:

$$H(z = 1) = \frac{1}{1-\alpha} \tag{3-10.9}$$

Finite Bandwidth and Slew Rate

The effect of finite bandwidth and slew rate cause the settling error. They lead to a non-ideal transient response within each clock cycle, thus producing an incomplete or inaccurate charge transfer to the output at the end of the integration period. The settling error can be simplified into a single-end SC integrator as shown in Figure 3-10.1(d).

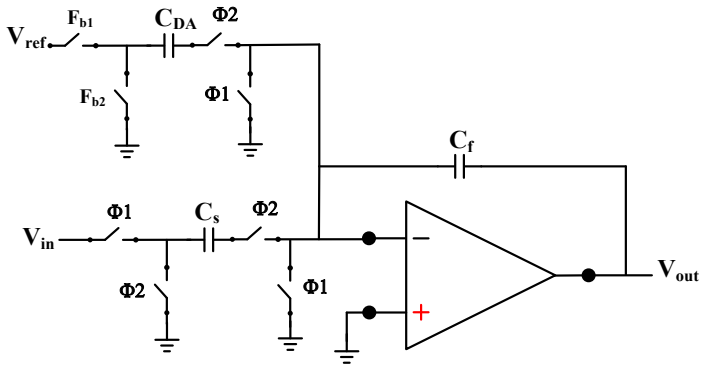


Figure 3-10.2(e): The single-end SC integrator

The operation of the output node during the integration interval of the output node (when ϕ2 is on, between $nT_s - T_s/2$ and nT_s) is given by:

$$V_o(t) = V_o(nT_s\text{-}T_s) + \alpha V_s(1 - e^{-t/\tau}) \tag{3-10.9}$$

Where, $V_s = V_{in}(nT_s\text{-}T_s)$, α is the integrator leakage which accounts for the operational amplifier finite gain A_0, α is calculated as follow:

$$\alpha = \frac{A_0 C_f}{A_0 C_f + C_s + C_{DA}} \tag{3-10.10}$$

And $\tau = 1/(2\pi * GBW)$ is the time constant and GBW is the unity gain frequency of the integrator loop-gain during the considered clock phase. The slope of this curve reaches its maximum value when t=0, resulting in:

$$\frac{d}{dt} Vo(t)\Big|_{max} = \alpha \frac{V_s}{\tau} \tag{3-10.11}$$

Two separate cases as follows should be taken into account.

- The value given by (3-10.11) is lower than the op-amp SR. In this case, there is no slew rate limitation and the evolution of V_0 is described by (3-10.9) during the whole clock period (until $t = T_S/2$).
- The value given by (3-10.11) is higher than SR. In this case, the op-amp is in slewing, thus the first part of the transient of V_0 ($t < t_0$) is linear with slope SR. The following equations hold (assuming $t_0 < T_S/2$):

$$t \le t_0 \qquad Vo(t) = V_o(nT_s\text{-}T_s) + SR \times t \tag{3-10.12}$$

$$t > t_0 \qquad Vo(t) = V_o(t_0) + (\alpha V_s + SR \times t)\left[1 - e^{-\frac{t-t_0}{\tau}}\right] \tag{3-10.13}$$

Imposing the condition for the continuity of the derivatives of (3-10.12) ~ (3-10.13), t_0 is derived:

$$t_0 = \frac{\alpha V_s}{SR} - \tau \tag{3-10.14}$$

3-10.3 Non-ideal Model Simulation

The non-ideal model of the 2nd SDM is created in Figure 3-10.3(a). The clock jitter accompanies with the input signal and is sampled by a zero-order hold. The switch thermal noise includes the two input branch of the first integrator without noise shaping. The pre-amplifier provides the noise contribution at front-end of the SDM.

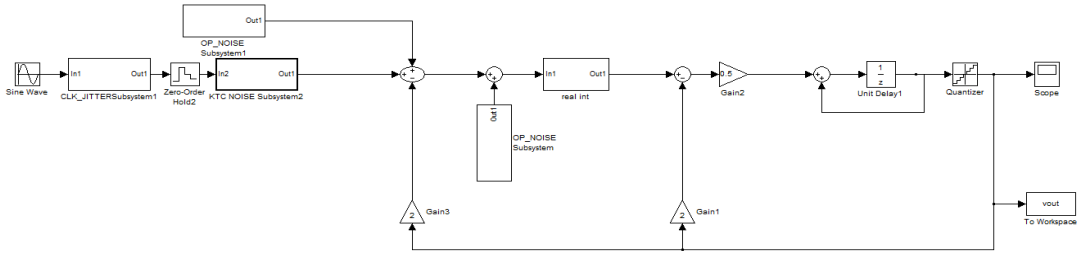


Figure 3-10.3(a): Non-ideal model of the 2nd SDM

For design a high performance 2nd SDM, take the layout matching and the feasible devices of the 0.18um CMOS technology into consideration is an important issue and the design coefficients of the proposed 2nd SDM are listed in Table 3-10.3(a). And the designed transfer function of the STF and NTF are given by:

$$\text{STF} = \frac{\text{X(z)}}{\text{Y(z)}} = \frac{0.25}{z^2 - 1z + 0.5} \tag{3-10.15}$$

$$\text{NTF} = \frac{\text{X(z)}}{\text{Y(z)}} = \frac{(1 - z^{-1})^2}{z^2 - 1z + 0.5} \tag{3-10.16}$$

Table 3-10.3(a): SDM design parameters

Parameter	Value
Signal amplitude	350mV
Signal bandwidth	950Hz
OSR	250
Feedback voltage	±225mV
Data point	10000
a_1	0.5
a_1	0.5
b_1	2
b_2	2

The specifications of the proposed circuits are listed in Table 3-10.3(b), and the simulation environment is set to be T=27℃, Boltzmann's constant K=1.38×10^{-23}.

Table 3-10.3(b): Specifications of the integrator

Specifications	**Value**
UGB	6MHz
Op-amp noise (RMS)	10uV/√Hz
Slew-rate	2.5V/us
Open-loop gain	1000
Integrator leakage (α)	0.996
C_f	4pF
b_n	2
Standard deviation Δτ	10ns

Before simulating the behavior non-ideal model, the stability of the high order SDM must be taken into consideration. According to transfer function of the STF and NTF, the stability simulation results of the 2nd SDM show a stable system that poles of the 2nd SDM are located within the unit circle as shown in Figure 3-10.3(b) and Figure 3-10.3(c) respectively.

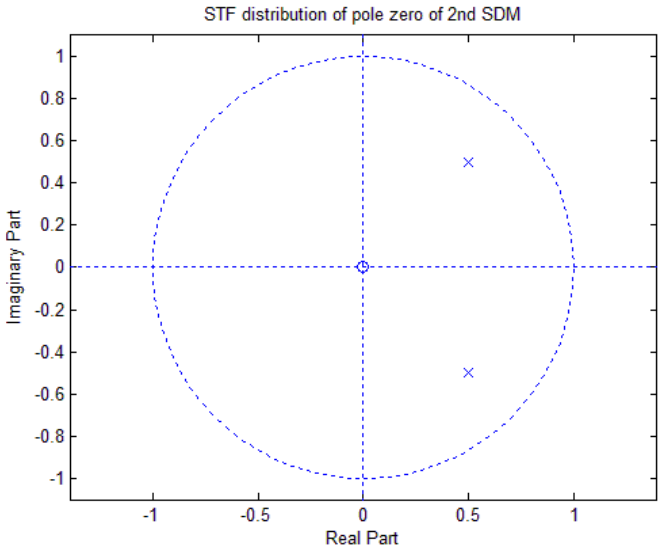


Figure 3-10.3(b): STF stability

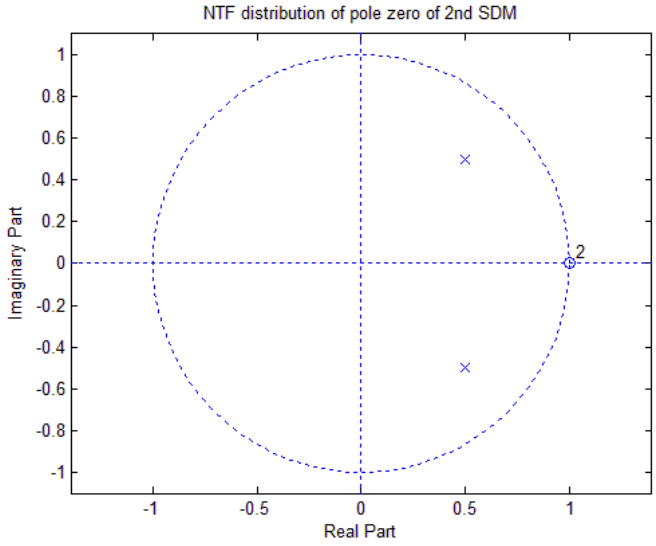


Figure 3-10.3(c): NTF stability

According to the above design parameters, the simulation result shows that the SQNR is 81.68dB as shown in Figure 3-10.3(d).

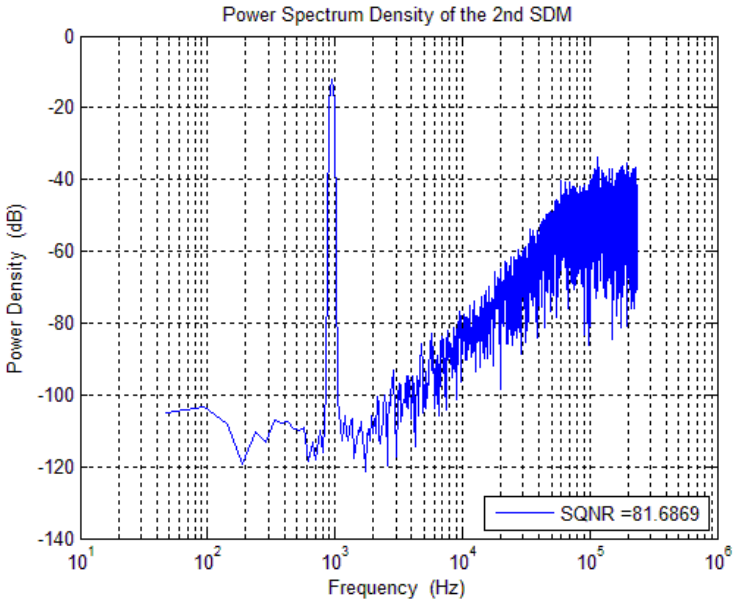


Figure 3-10.3(d): PSD of the 2nd SDM non-ideal model

The parameters of the proposed 2nd SDM are fixed and the performances of the 2nd SDM can be implemented with the above practical and feasible design coefficients.

Moreover, the other design consideration such as the noise of the pre-amplifier is uncertainty due to the different readout architectures and circuit design techniques. The relationship between the SQNR and the output noise of the preamplifier must be simulated and make sure that the noise contribution of the pre-amplifier cannot affect the SQNR significantly. Thus, sweep the pre-amplifier noise to observer the variation of the SQNR as shown in Figure 3-10.3(e).

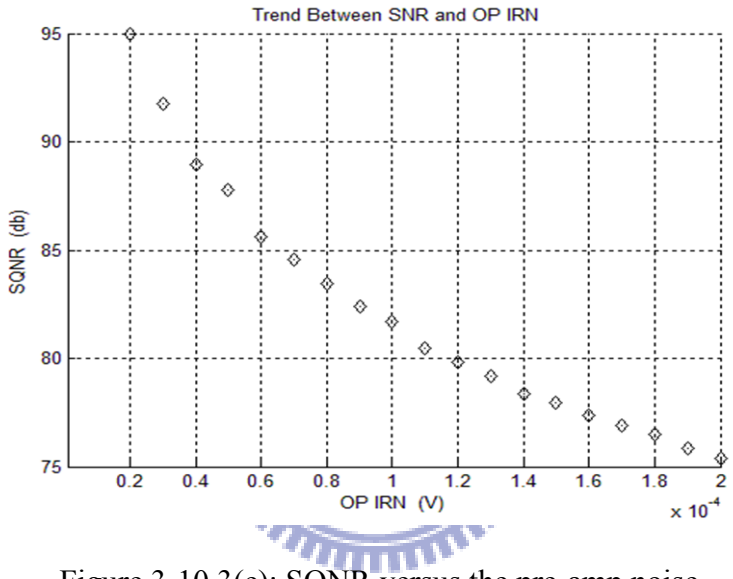


Figure 3-10.3(e): SQNR versus the pre-amp noise

From the simulation results, if the pre-amplifier noise voltage is lower than 120uV (RMS), the SQNR can be maintained more than 80dB. The equivalent input referred noise of the pre-amplifier is 43.865nV/√Hz for 500 Hz bandwidth of the pre-amp that is much larger than the proposed low noise amplifier design target IRN=12.58nV/√Hz in section 3-8.1.

3-11 Low Power Latch Comparators

3-11.1 Latch Comparators

The dynamic latch comparator is always used in discrete-time application. The comparator operates in two modes by controlling the clock ϕ1. As the ϕ1 OFF, the latch goes into the reset mode, the $M_{3,4}$ are turned off, there are no supply currents in drain of the $M_{9,10}$, the drain of the $M_{9,10}$ is pulled up to VDD. And the output is reset to ground by the two inverter buffers that record the output bit-stream from the following SR latch. As the ϕ1 ON, the latch goes into its regenerative mode, the regenerative mode is completed by two cross-coupled inverters M_5 ~ M_8, the pre-charged parasitic capacitances of the drain of the $M_{9,10}$ are discharged by transistor M_1 and M_2 respectively. The drain currents of the $M_{5,6}$ are steered to obtain the final state determined by the mismatch triode resistors of the $M_{1,2}$ which are given by:

$$\frac{1}{R_1} = K_1\left[\left(\frac{W}{L}\right)_1 (V_{i+} - V_t)\right] \qquad (3\text{-}11.1)$$

$$\frac{1}{R_2} = K_2\left[\left(\frac{W}{L}\right)_2 (V_{i-} - V_t)\right] \qquad (3\text{-}11.2)$$

Where V_t is the threshold voltage of the $M_{1,2.}$ From the above formula, the discharge rate depends on the input voltage that determinates the triode resistors, too.

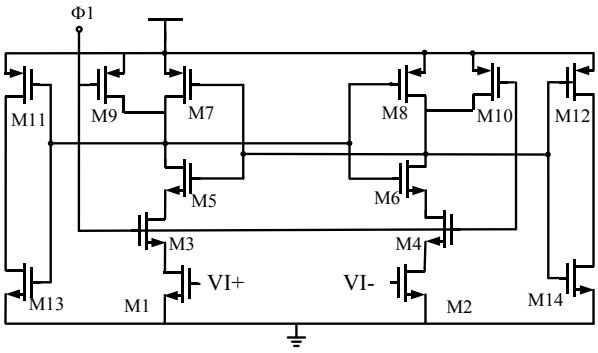


Figure 3-11.1(a): Latch comparator

Besides, in order to minimize the kickback noise, the comparator employs the cascode transistors (also called the isolation transistors) to separate the drain nodes of the input differential pair from the regeneration nodes during the regeneration process. The whole comparator is a purely dynamic circuit, which is quite power efficient. And the propagation delay is simulated to be about 2.1ns that is good enough for low speed SDM.

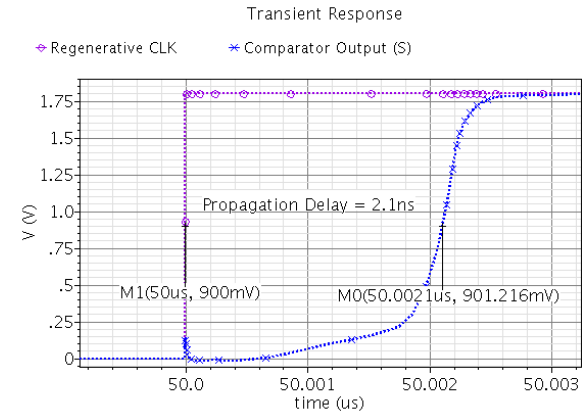


Figure 3-11.1(b): Propagation delay

3-11.2 Mote-Carlo Comparator Offset Extraction

Although the low speed 2nd SDM relaxes the requirement of the proposed SDM and suppresses the inherent non-ideal phenomenon of the comparator such as the comparator offset and hysteresis by noise shaping. The monte-carlo methodology is still adopted to extract the comparator offset for cautious. The test-bench for the comparators offset extraction is created in Figure 3-11.2(a), an ideal sample and hold (S/H) is described in Verilog-A and placed in front of the positive side of the comparator input. And a triangle wave with 1mV steps as the input is applied at the S/H input, and the sampled signal is compared with negative voltage which is 899mV continuously in 500K Hz. Since the

sampling period is designed to be 2us, the input triangle slope is selected to be 1mV/1us that is convenient to record the input-output amplitude.

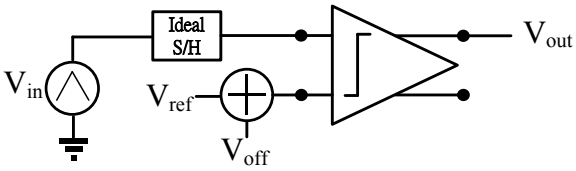


Figure 3-11.2(a): Test-bench of the comparators offset extraction

In the ideal operation, if the input signal is larger than the V_{ref}, the V_{out} is one. But once the offset voltage exists the V_{in} must be larger than $V_{ref}+V_{off}$. By means of the monte-carlo 500 runs, record the timings when the output alters from 0 to 1. The deviation of the output changed timing denotes offset voltage for this comparator in the TSMC 0.18um process. And the transient simulation result of input-output character is shown in Figure 3-11.2(b)

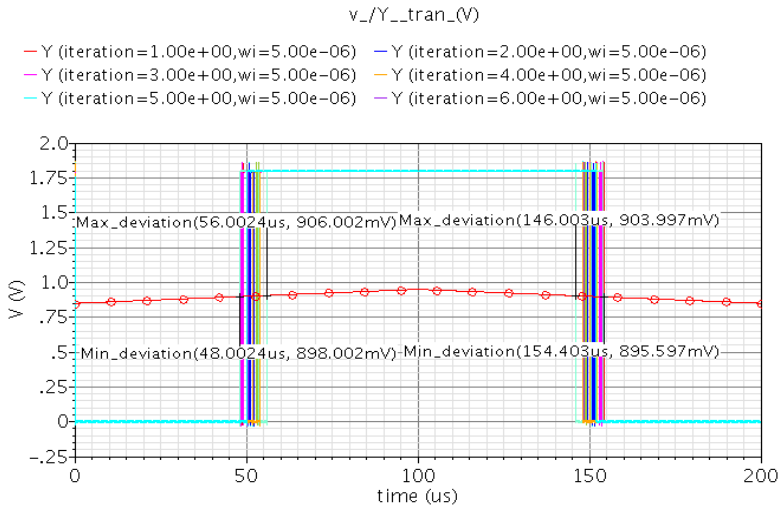


Figure 3-11.2(b): Input-output transfer curve by Monte-Carlo 500 runs

By recording the output changed timing, a subsequent post-processing (here is calculated in Matlab) for each ramp value the number of comparator output 1 is counted and normalized to the number of runs as shown in Figure 3-11.2(c).

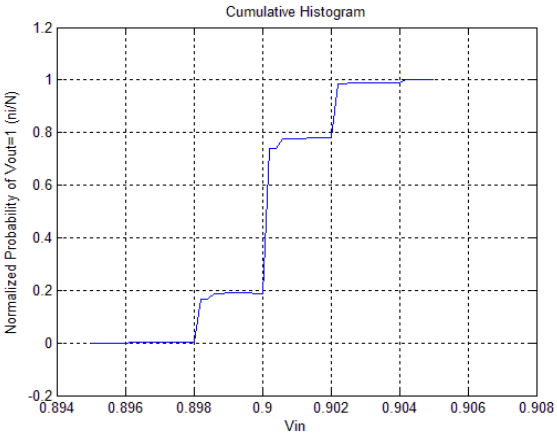


Figure 3-11.2(c): Cumulative histogram

From Figure 3-11.2(c), the comparator offset voltage is distributed from -1mV to +6mV related to V_{ref} (0.899V), and the 80% output is one if the input signal is larger than 0.9V. The simulation data of the rising slope have been plotted in a normal distribution plot as shown in Figure 3-11.2(d). It is seen that the result is to a good approximation a straight line. Hence, the offset of the comparator is normal distributed and its mean value as well its standard deviation can be calculated by Matlab function [24].

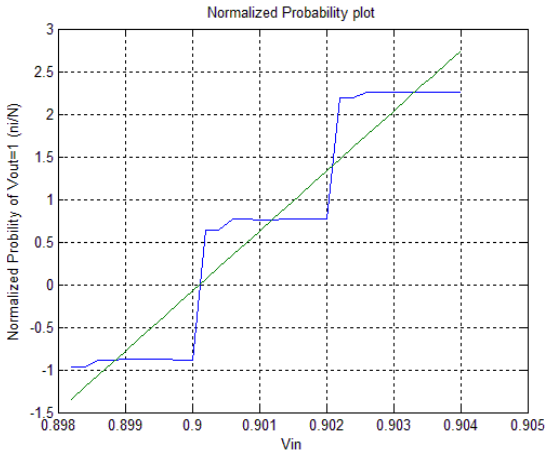


Figure 3-11.2(d): Normal probability plot

After calculation in Matlab, the mean value of the input voltage is 901mV for

output one. Thus the offset voltage could be estimated (901mV-0.889mV) to be 2mV and the other specifications of the low power latch comparator are listed in Table 3-11.2.

Table 3-11.2: Specifications of the latch comparator

Parameters	Value
Mean value	901mV
Standard deviation	1.4mV
Propagation delay	2.1ns

3-12 Discrete Time Op-amp and Post-layout Simulation

3-12.1 Discrete Time Op-amp

For SC-circuits, the Op-amp is improved from the folded cascode op with continuous time CMFB in section 3-6.1. An extra set of capacitance and an extra set of switches are used in the conventional SC_CMFB as shown in Figure 3-12.1(a). The clocks operate the switches in opposite phase, therefore, during every clock phase, the total loading on the differential loop is the same (C_1+C_2) [25]. The value of C_2 can be determined by making the CM loop bandwidth comparable to that of the differential loop. Then C_1 can be designed 5–10 times that of C_2 for faster dc settling lower steady-state errors, charge injection errors and leakage errors.

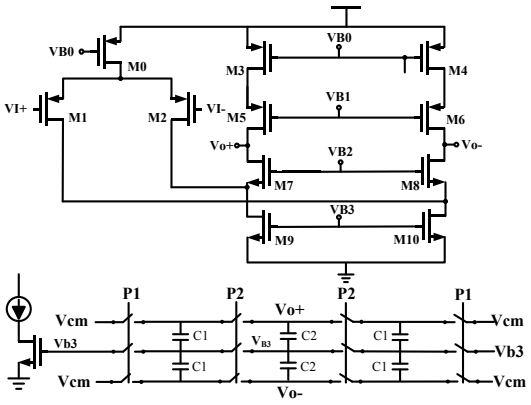


Figure 3-12.1(a): The folded cascode amp with SC_CMFB

3-12.2 SDM Op-amp

In TT corner, 1.8V, and 27℃, Figure 3-12.2(a) shows the DC gain up to 66.13db, phase margin 89.86 (deg), unit gain bandwidth (UGB) 7.055 Hz with 2pF loading.

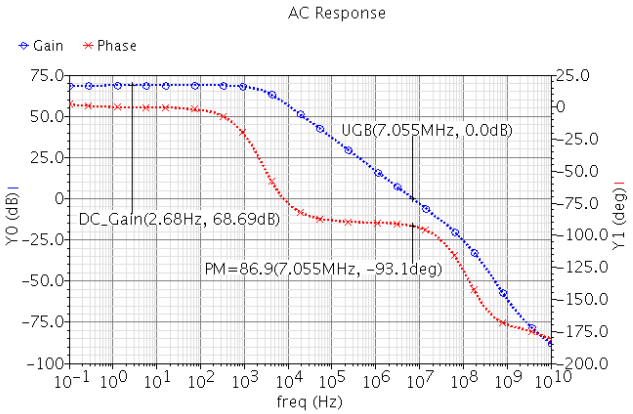


Figure 3-12.2(a): AC response of the discrete time folded cascade op

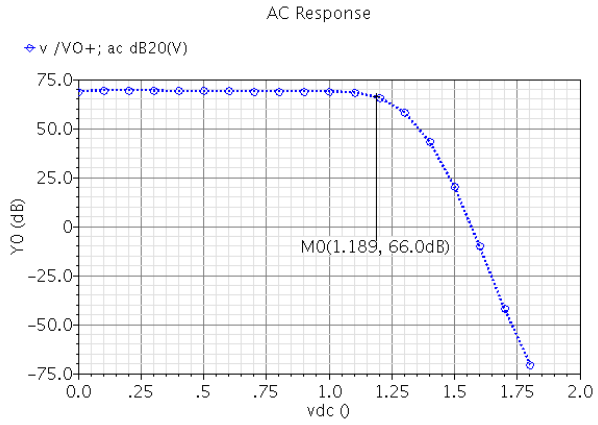


Figure 3-12.2(b): ICMR of the discrete time folded cascade op

Table 3-12.1: Other corners simulation of the continuous time folded cascade op

	Unit	**TT**	**SS**	**FF**
DC gain	dB	68.69	68.98	65.76
PM	Deg	86.9	86.57	90.14
UGB	MHz	7.055	6.26	8.22
ICMR(V)	Volt	0~1.189	0~1.153	0~1.22

From the above simulation results, the discrete time Op-amp fulfills the specifications requirement that was simulated in behavior simulation in this section.

3-13 Transistor Level Simulation of The 2nd SDM

3-13.1 2nd SDM

Figure 3-13.1(a) shows the schematic of the proposed 2nd SDM which is controlled by the non-overlap clocks ϕ_1 and ϕ_2. The auto-zeroing (AZ) technique is adopted to suppress the 1/f noise and DC offset of the first integrator that cannot be removed by noise shaping. The main ideal of the AZ technique is never to disconnect the top plate of the capacitor C_S from the negative input of the op-amp. The switched path between the negative input and output of the op-amp is needed to charge the input capacitance C_S during the sampling phase. The SR latch is configured with strong buffers by shunt 32 CMOS inverters in order to drive large loading.

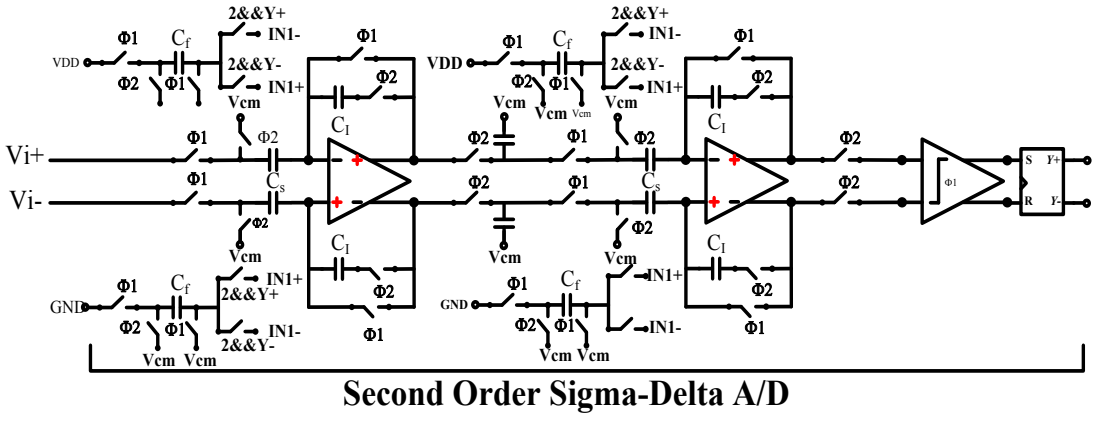


Figure 3-13.1(a): The schematic of the 2nd SDM

3-13.2 2nd SDM Simulation Results

Pre-layout Simulation

In TT corner, 1.8V, and 27℃, Figure 3-13.2(a) shows the transient simulation results, The waveforms are the outputs of the second integrator, the first integrator, and comparator from top to bottom respectively. And the Figure 3-13.2(b) ~ Figures 3-13.2(d) is the PSD in each corner. And the simulation environment is the same as behavior simulation in section 3-10.

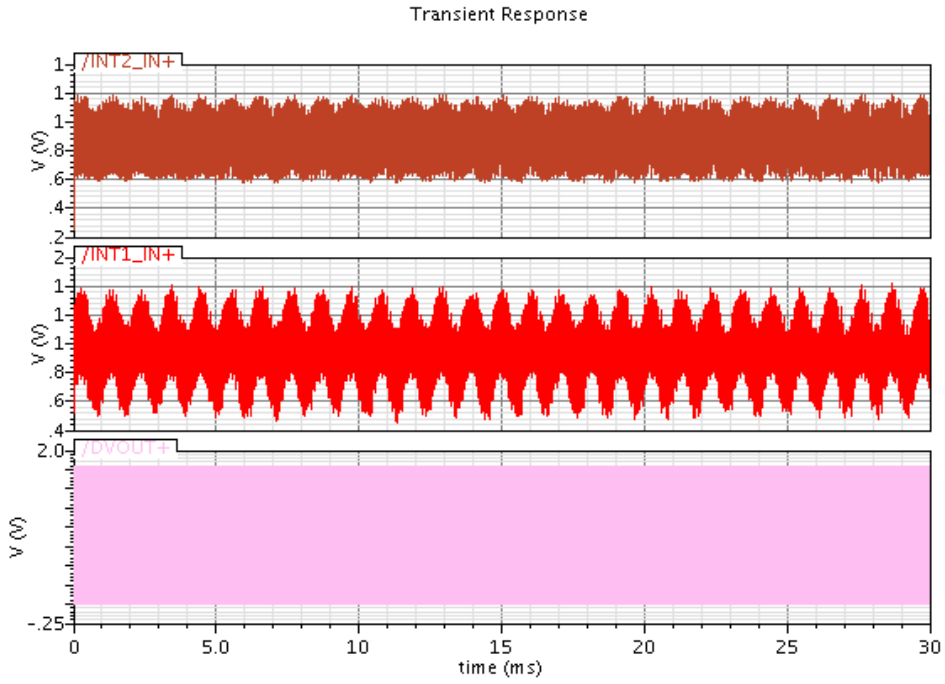


Figure 3-13.2(a): Transient response of the 2nd SDM (from top to bottom: the second integrator, the first integrator, comparator)

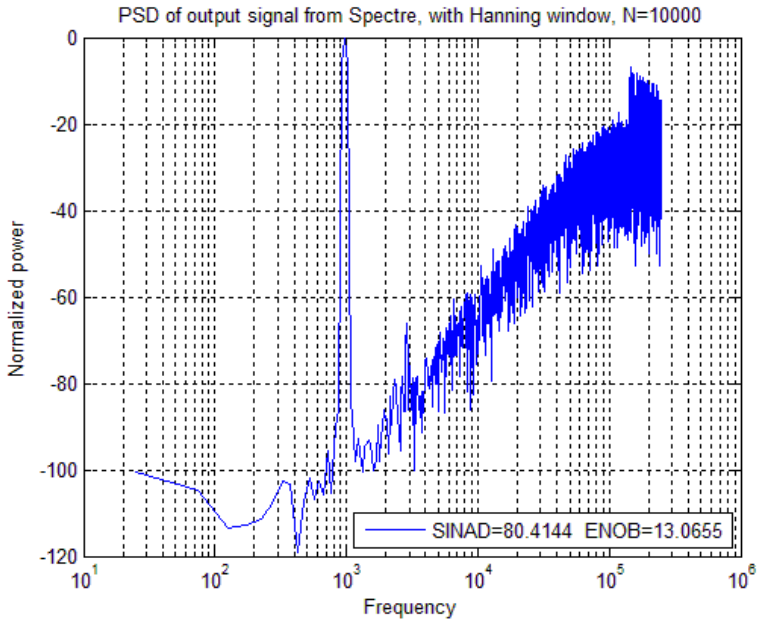


Figure 3-13.2(b): PSD in TT_corner

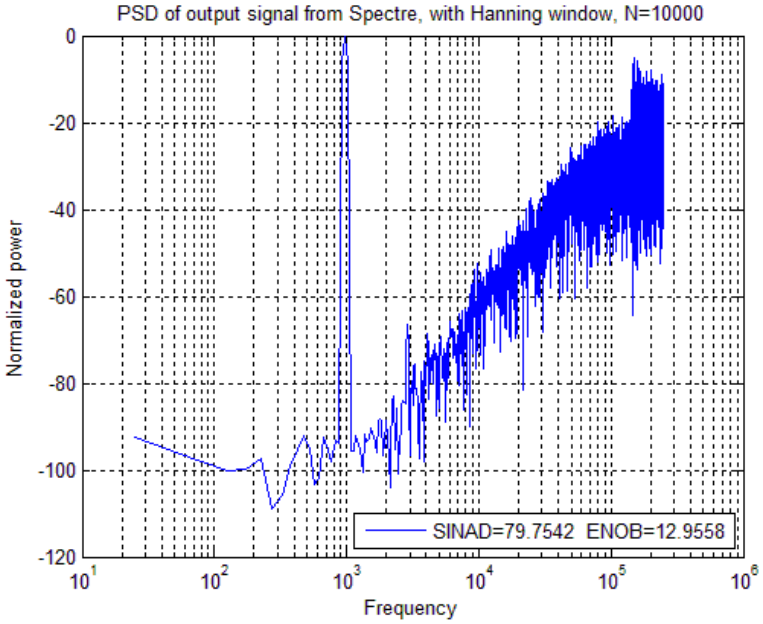


Figure 3-13.2(c): PSD in SS corner

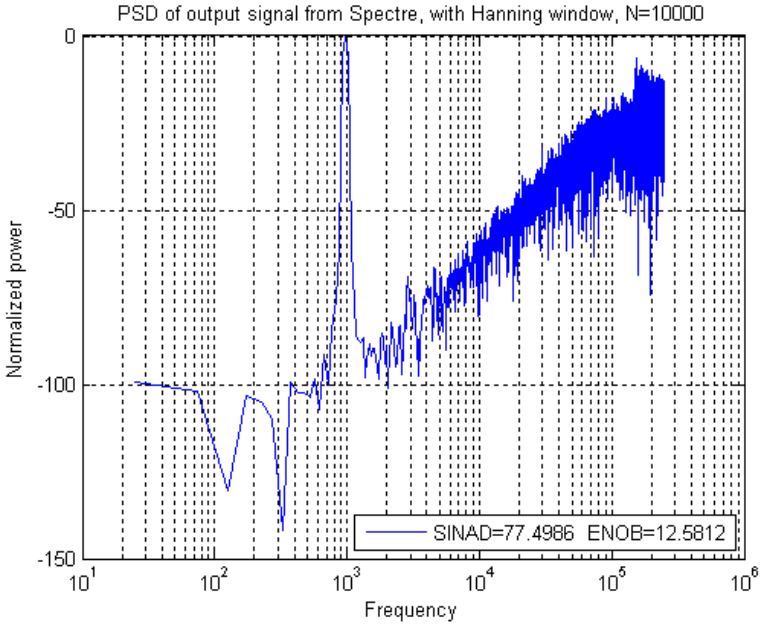


Figure 3-13.2(d): PSD in FF corner

Post-layout Simulation

.

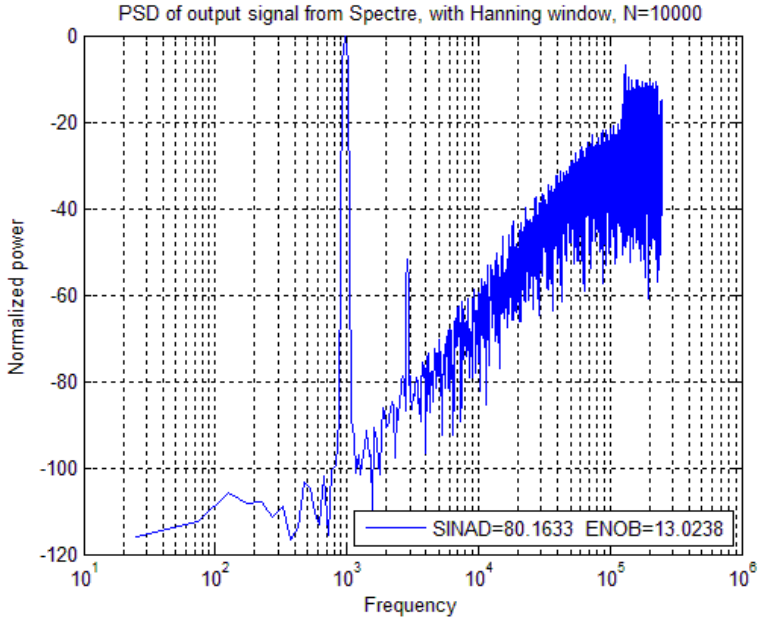


Figure 3-13.2(e): PSD in TT_corner

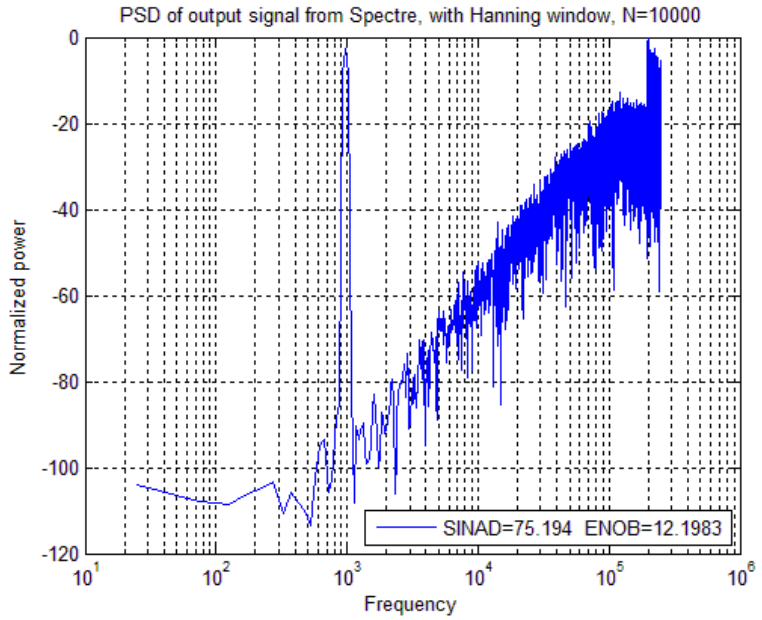


Figure 3-13.2(f): PSD in SS corner

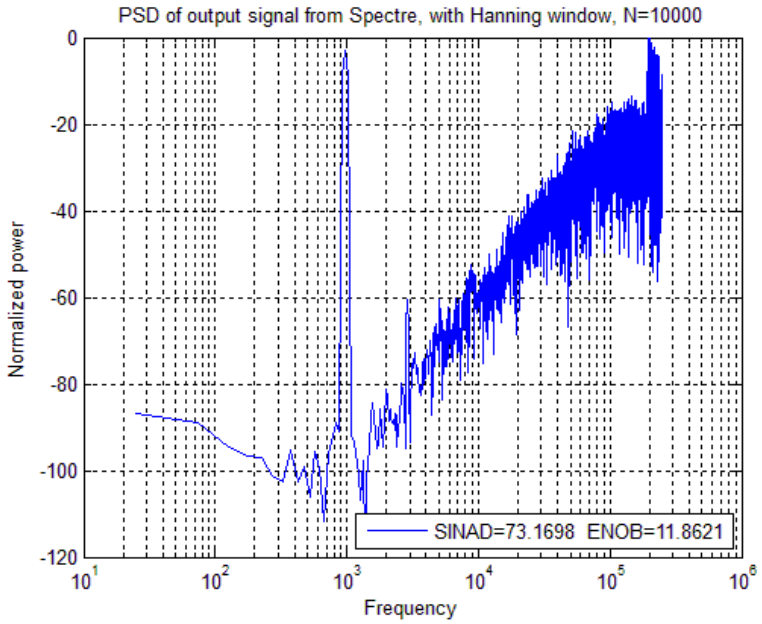


Figure 3-13.2(g): PSD in FF corner

Post-layout Worst Case Simulation

Take the speed worst case and power worst case into consideration. The speed

worst case is VDD_{min}, T_{max}, (1.62V,80℃), and SS corner:

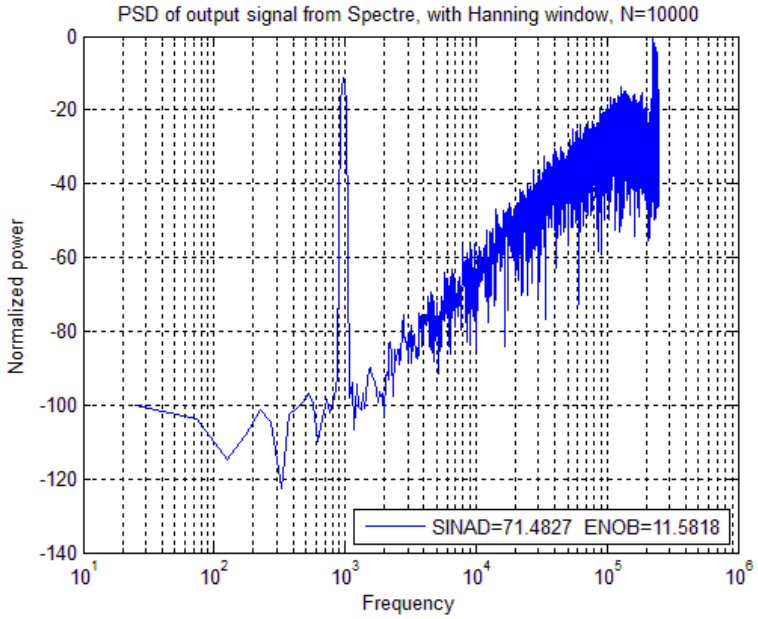


Figure 3-13.2(h): PSD of the speed worst case

The power worst case is VDD_{max}, T_{min}, (1.92V,-30℃), and FF corner:

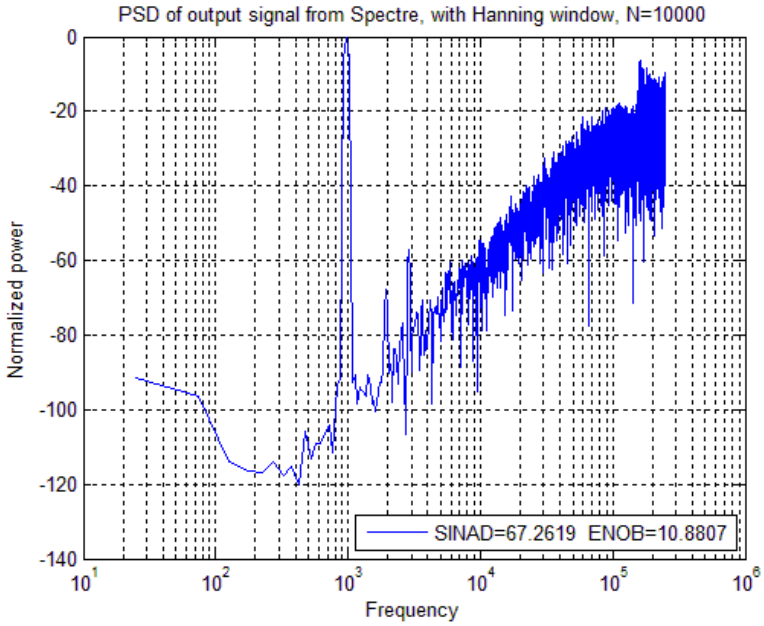


Figure 3-13.2(i): PSD of the power worst case

The performance of the pre-ampifier and the 2nd SDM in other corner case are

listed in Table 3-13.2. The FOM is calculated by the power consumption during each bit conversion cycle and it is given by:

$$\text{FOM} = \frac{\text{Power}}{2^{B} \times f_{nyquist}} \quad \text{(PJ/Conversion)} \quad (3\text{-}14.1)$$

Where $f_{nyquist}$ is the Nyquist frequency, here is 2 KHz.

Table 3-13.2: Specifications in each corner case

	SNDR(SINAD)(dB)	ENOB	Power (mW)	FOM
Normal case TT	80.16	13	1.436	87.28
Normal case SS	75.194	12	1.061	129.51
Normal case FF	73.16	11	1.91	466.3
Speed worst case FF	71.4	11	0.875	213.6
Power Worst case TT	67.26	10	2.047	999.5

3-14 Physical Layout and Summary

3-14.1 Physical Layout

We had go over two times of tapeout scheduled on February 13, 2012 and August 13, 2012.

The First Tapeout

The physical layout of the first tapeout is shown in Figure 3-14.1(a). This layout does not include the SDM A/D converter, and its total area is 1573.351um*1829um. The label names of the bond pads are shown in Figure 3-14.1(b). DVDD and DGNDD are the power and ground of the digital circuits. AVDD and AGND are the power and ground of the analog circuits. ACCTUNE+, ACCTUNE-, VCKTTUNE+, and VCKTTUNE- are the dc tuning voltages. Vc is the dc control voltage. GMC-, GMC+, VGA-, VGA+, Vo+, and Vo- are the analog outputs. VDD and VSS are the power and ground of the ESD protection circuits. CLOCK is the digital clock.

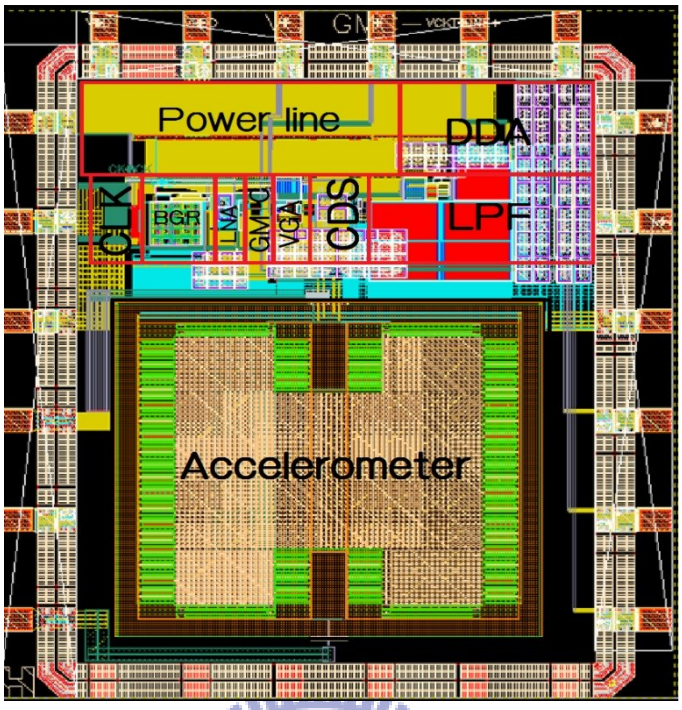


Figure 3-14.1(a): Physical layout of the first tapeout

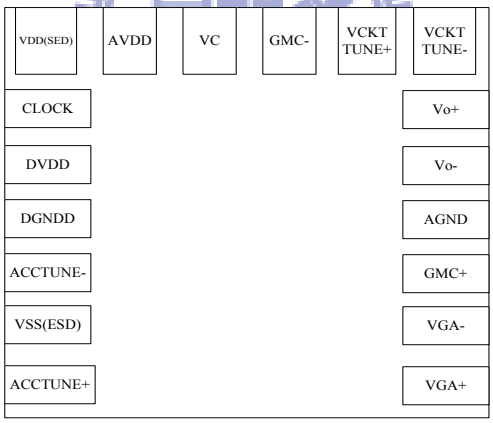


Figure 3-14.1(b): The bond PADs of the first tapeout

The Second Tapeout

The physical layout of the second tapeout is shown in Figure 3-14.1(c). This layout does not include the SDM A/D converter, and its total area is 2048um*1998um. The label names of the bond pads are shown in Figure 3-14.1(d).

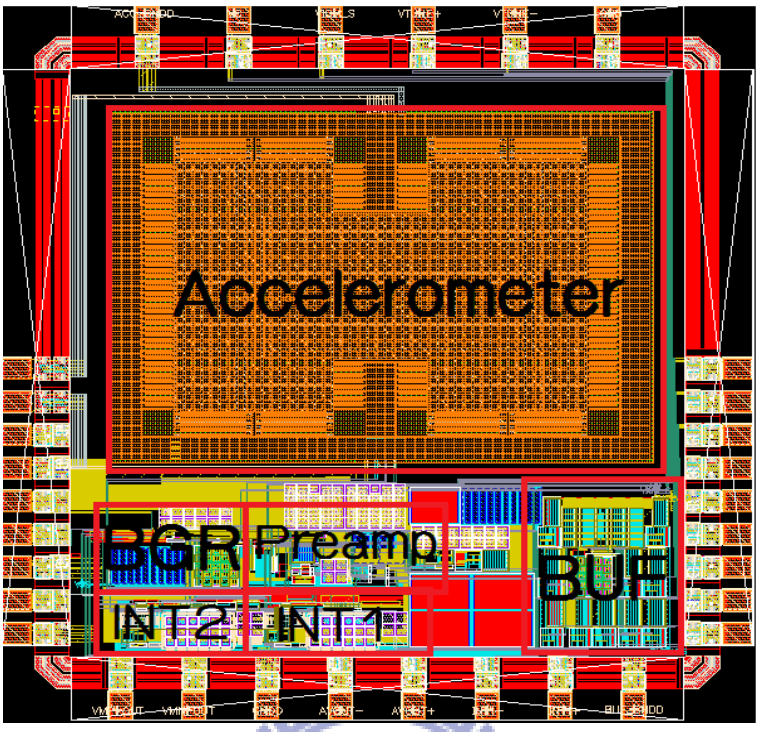


Figure 3-14.1(c): Physical layout of the second tapeout

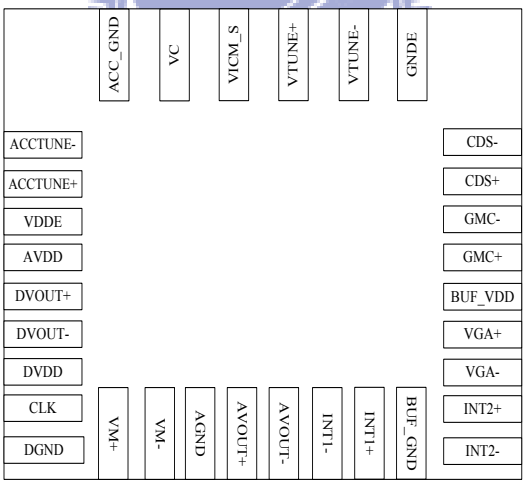


Figure 3-14.1(d): The bond PADs of the second tapeout

DVDD and DVSS are the power and ground of the digital circuits. BUF_VDD, BUF_GND, AVDD and AGND are the power and ground of the analog circuits. ACCTUNE+, ACCTUNE-, TUNE+, and TUNE- are the dc tuning voltages. Vc is the control voltage. ACC_GND is the ground of the accelerometer. VICM_S, GMC-,

GMC+, CDS+, CDS-, VGA-, VGA+, AVOUT-, AVOUT+, INT1+, INT1-, INT2+, and INT2- are the analog outputs. VDDE and GNDE are the power and ground of the ESD protection circuits. CLK is the digital clock. VM+, VM-, DVOUT+, and DVOUT- are the digital outputs.

3-14.2 Preamp Noise and Power

The new approach in the proposed pre-amplifier is the Dual-chopper combined with the CDS demodulation. Figure 3-14.2(a) shows the noise and power location with other architectures which are published in recently year. (The noise floor is converted to the resolution of the minimum detectable capacitance variation by multiplying the sensitivity of the designed accelerometer). The diamond denotes the measurement results and the triangle denotes the post-layout simulation results.

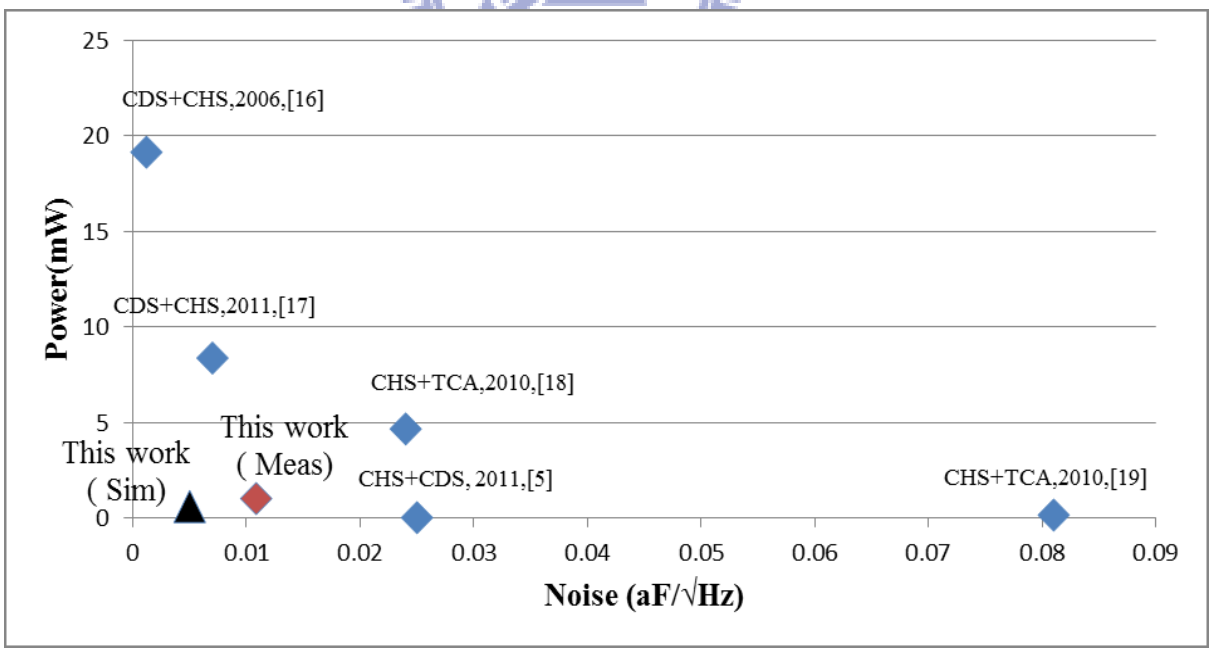


Figure 3-14.2(a): Noise and power distribution

3-14.3 Comparison with Previous Work

Pre-amplifier

The specifications of the low noise pre-amplifier are simulated in TT corner, 1.8V power supply, and temperature 27℃ as listed in Table 3-14.3(a).

Table 3-14.3(a): Pre-amp comparisons with prior works

	2010[19]	**2011[3]**	**2011[4]**	**2011[5]**	**This work**
Processes	0.13um	0.35um	0.8um	0.18um	0.18um
Architecture	TCA+CHS	DCA	CHS+CDS	CHS+CDS	DCA+CDS
Power	0.17mW	1mW	8.38mW	0.036mW	0.62mW
Supply Voltage	1.5	3.3	5	1.8	1.8
System Bandwidth	0.4K	N/A	N/A	0.1K	0.5K
Sensitivity	18mV/g	180mV/g	9980 mV/fF	Sensor: 2mVpp/g Ckt: 150mV/g	Sensor: 0.98mVpp/g (0.369f/g) Ckt: Max:17425.47 mV/fF Min:324.8 mV/fF
Linear Range	+-1mg~ +-25g	+-11.5	N/A	+-4g	+-1g~ +-10g
BNEA	N/A	N/A	N/A	20.65 ug/√Hz	4.2ug/√Hz
CNEA	N/A	N/A	N/A	9.82nV/√Hz	12.57nV/√Hz
TNEA	4.2ug/√Hz	40ug/√Hz	N/A	22.866 ug/√Hz	13.4966ug/√Hz
DR	87	N/A	N/A	84.8	90.41
Resolution	N/A	N/A	0.5aF/√Hz	0.025 aF/√Hz	0.005aF/√Hz

Pre-amplifier and 2nd SDM

The specifications of the low noise pre-amplifier with 2nd SDM are simulated in TT corner, 1.8V power supply, and temperature 27℃ as listed in Table 4.2. And the FOM is calculated by the power consumption during each bit conversion cycle and it is given by:

$$\text{FOM} = \frac{\text{Power}}{2^{B} \times f_{nyquist}} \quad \text{(PJ/Conversion)} \qquad (3\text{-}14.1)$$

Where $f_{nyquist}$ is the Nyquist frequency, here is 2 KHz. The functions and performances of the whole chip of the second tapeout are listed in Table 3-14.3(b).

Table 3-14.3(b): Pre-amp and 2nd SDM comparisons with prior works

	2010[26]	**2011[27]**	**2012[28]**	**This work**
Processes	O.35um CMOS technology	0.13um CMOS technology	0.35um CMOS technology	0.18um CMOS technology
Sensor On Chip	No	No	No	Yes
Sensitivity Tuning	No	No	No	17425.47mV/fF~ 324.8 mV/fF
Sampling Freq	5.12M	160K	1.25M	500K
Bit	1	1	1	1
Order	2	1	3	2
Power (mW)	17.8	0.53	15	1.436mW
Supply Voltage	3.3	1.8	3.3	1.8
SNR(db)	N/A	62.98	N/A	88
SNDR(db)	N/A	N/A	N/A	80.16
ENOB	N/A	10	17.2	13
System Bandwidth	N/A	0.5K	N/A	1K
Sensing Range	N/A	N/A	N/A	±1g~ ±10g
Noise Floor	20ug	N/A	65aF	13.4966ug/√Hz
FOM	N/A	1035.15	1.95	87.28

Chapter 4

Measurements

4-1 Measurement Environment

Figure 4-1(a) shows the measurement instruments. The measurement instruments include the power supply, function generator, oscilloscope, multimeter, source meter, and RT_Pro spectrum analyzer. The two power supplies provide the 1.8V to digital control clock circuits and analog circuits respectively. The function generator provides the 500K Hz clock to the DCA control circuits. The source meter is used to measure the static and dynamic power respectively. The DC testing is recorded in the oscilloscope. And the AC response is measured by RT spectrum analyzer such as noise, AC offset, bode plot and so on. Figure 4-1(b) shows the MEMS testing setup. The MEMS measurement instruments include the Mems Motion Analyzer (MMA) and the White Light Interferometer. Put the die chip on the MMA, the MMA is used to record the displacement of the accelerometer in different vibration frequency in order to obtain the nature frequency. The white light interferometer takes the photographs to measure the altitude difference to get the surface warping of the proposed MEMS structure.

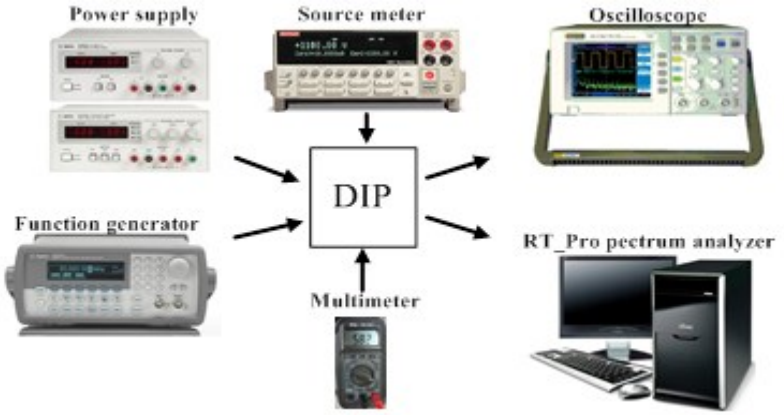


Figure 4-1(a): The CKT measurement instruments

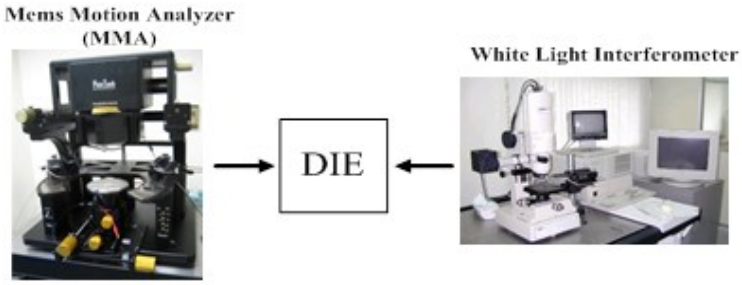


Figure 4-1(b): The MEMS measurement instruments

The tested chip is packaged (Die in package (DIP)) and mounted on the experimental circuit board for measurement as shown in Figure 4-1(c). And the instruments setup and overview is shown in the Figure 4-1(d).

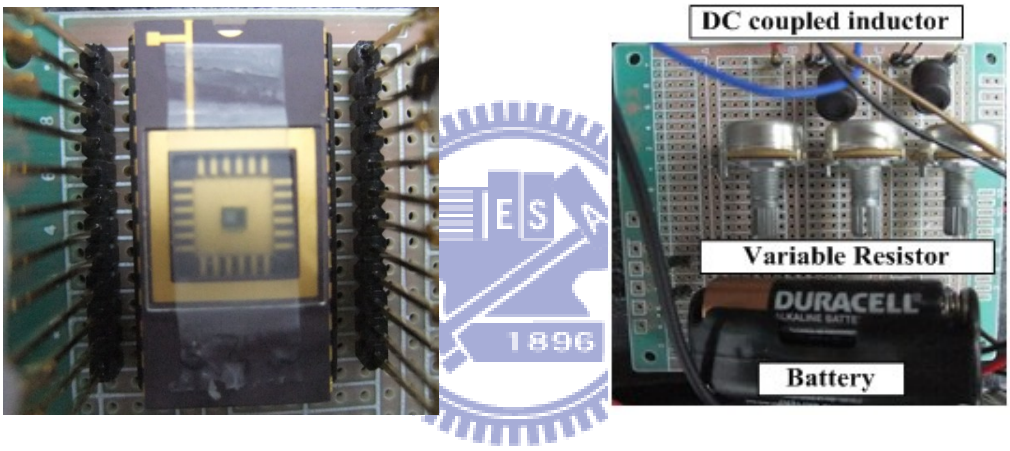


Figure 4-1(c): The tested chip

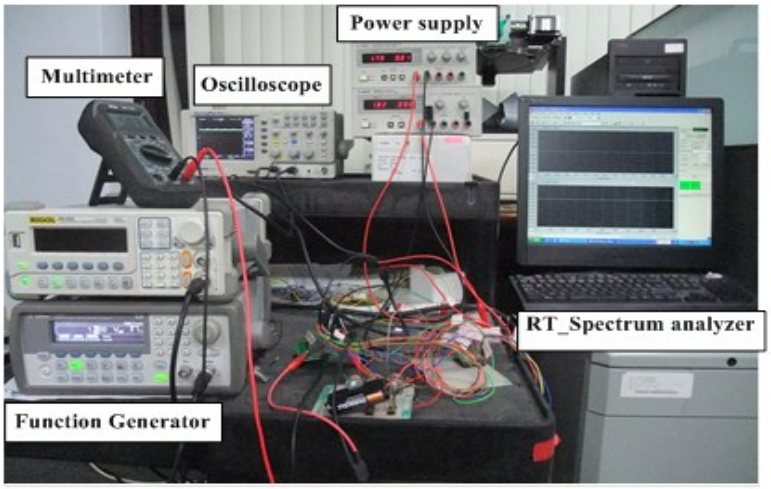


Figure 4-1(d): The instruments setup and overview

4-2 Performance of The Pre-amplifier

4-2.1 Measurement Steps

The measurement items are divided into DC and AC testing, and the measurement steps are explained by Figure 4-2.1(a). At first, we observed the DC offset of the signal paths such as GmC+, GmC-, VGA+, VGA-, and AAF outputs. We records the DC offset in each output nodes, if the DC offset appeared at the AAF outputs, it will be vanished by tuning voltage from V_{tune+} and V_{tune-}. At the second step, we shock the chip to detect the signal by a shaker or just by hand. If there are no voltage signals at AAF outputs (accelerometer does not work correctly), the sine wave will be applied in V_{tune+} in order to get the performances of the circuits such as bandwidth, noise, power, output swing, and slew rate.

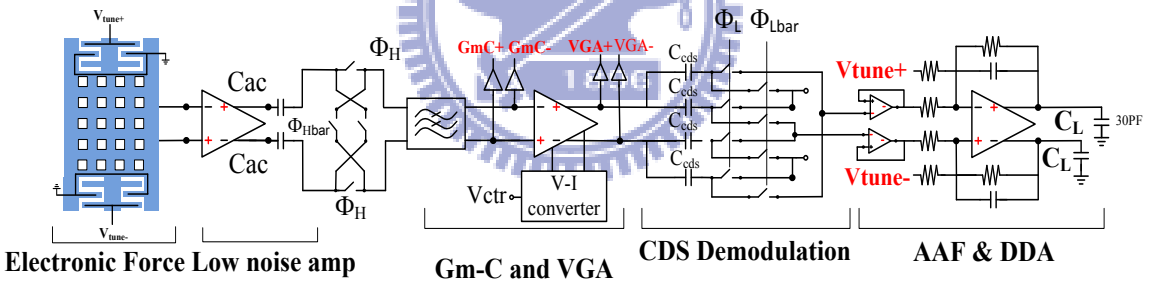
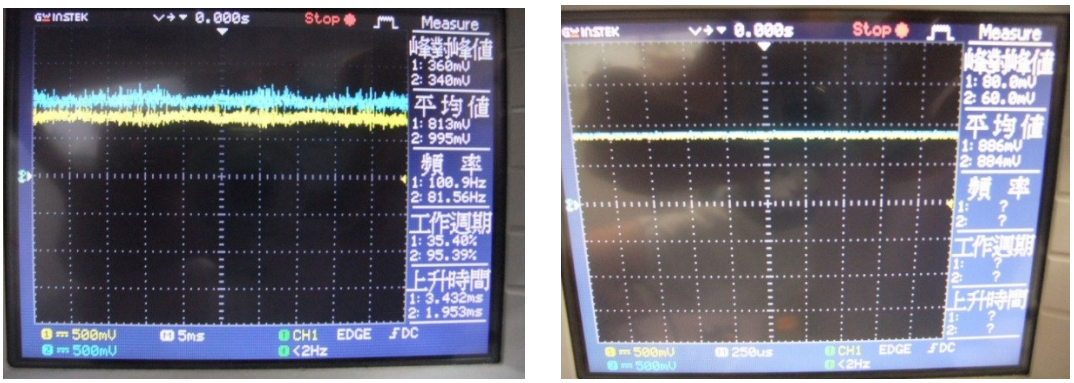


Figure 4-2.1(a): The schematic of the tested chip

4-2.2 DCA function and DC Offset Compensation

At the beginning, the AAF output is noisy and has DC offset 182 mV if there is no DCA, CDS function (the control clock is not applied) as shown in Figure 4-2.2(a). The DCA and CDS function is shown in Figure 4-2.2(b), besides, the DC offset is alleviated to 2mV when the DC offset compensation voltages are applied.



(a) (b)

Figure 4-2.2(a): Without and; (b): With the DCA and the offset compensation

4-2.3 Bandwidth

Apply the sine wave at the V_{TUNE+}, and alter the frequency to record the amplitude. Depend on the simulation, the AC response is about 12dB gain and the 3dB bandwidth is 500K Hz. The Figure 4-2.3(a) ~ Figure 4-2.3(r) show the measurement results.

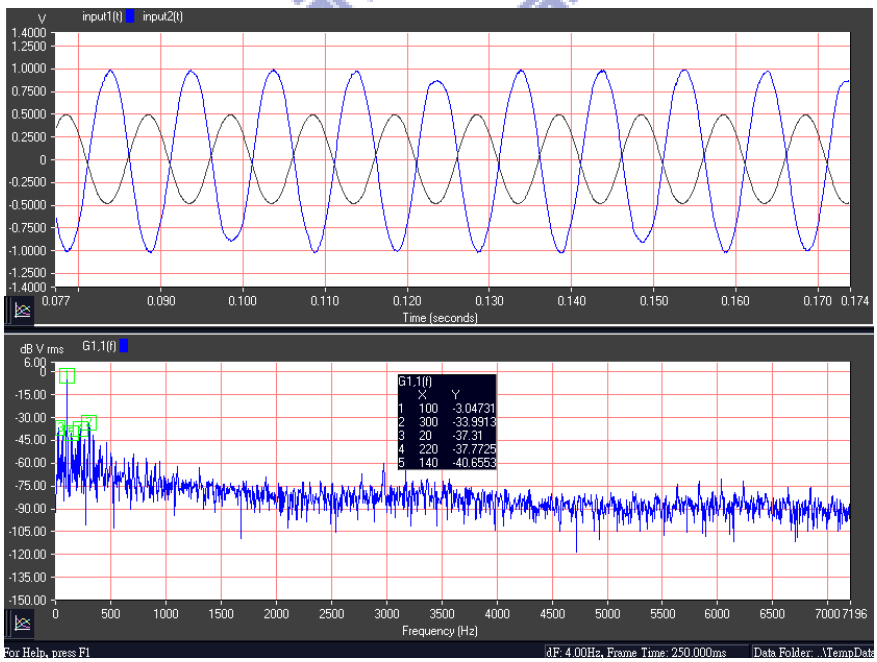


Figure 4-2.3(a): 1Vpp with 0.1k Hz input

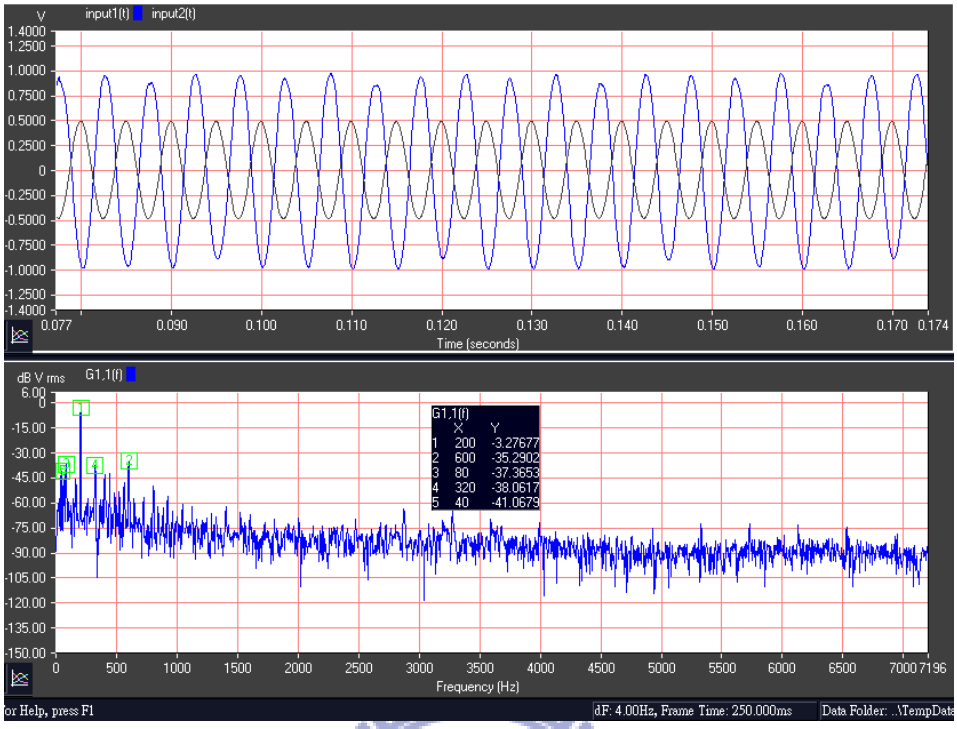


Figure 4-2.3(b): 1Vpp with 0.2k Hz input

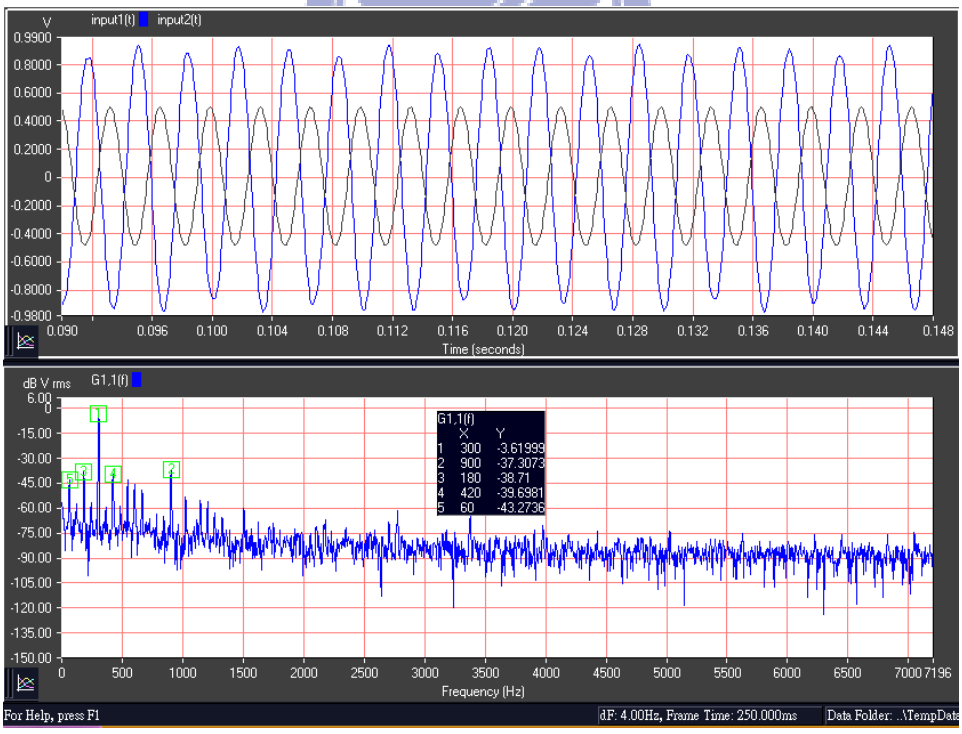


Figure 4-2.3(c): 1Vpp with 0.3k Hz input

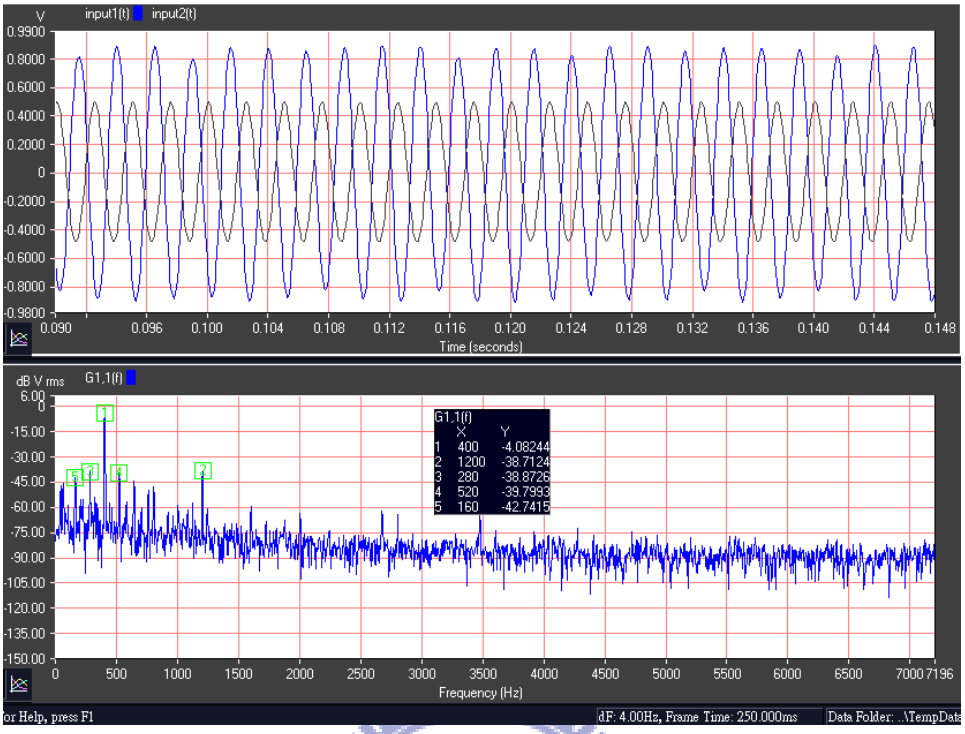


Figure 4-2.3(d): 1Vpp with 0.4k Hz input

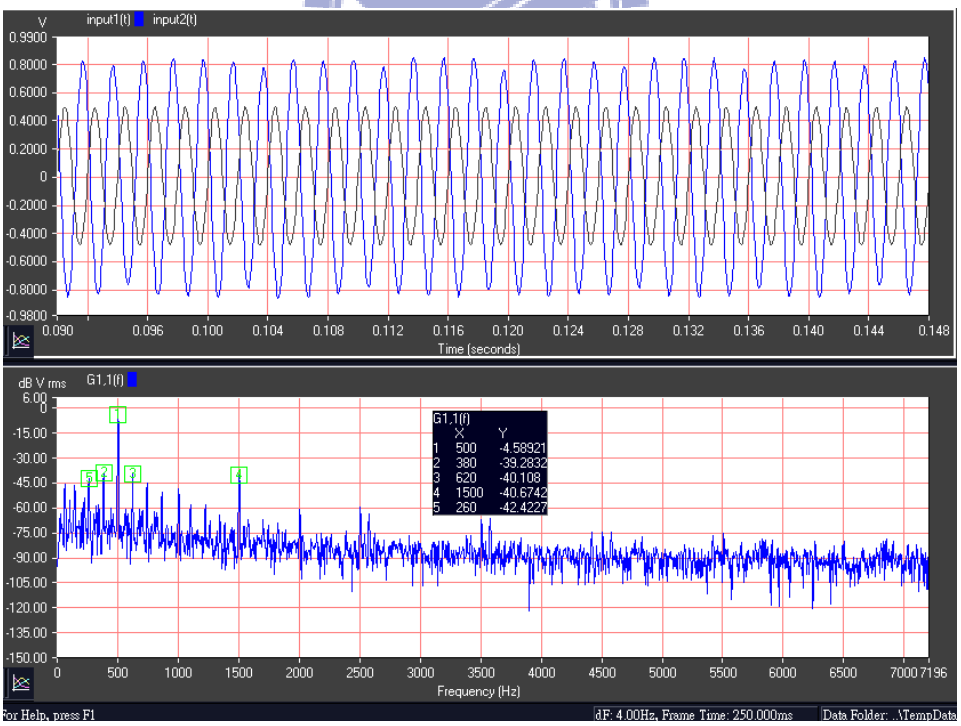


Figure 4-2.3(e): 1Vpp with 0.5k Hz input

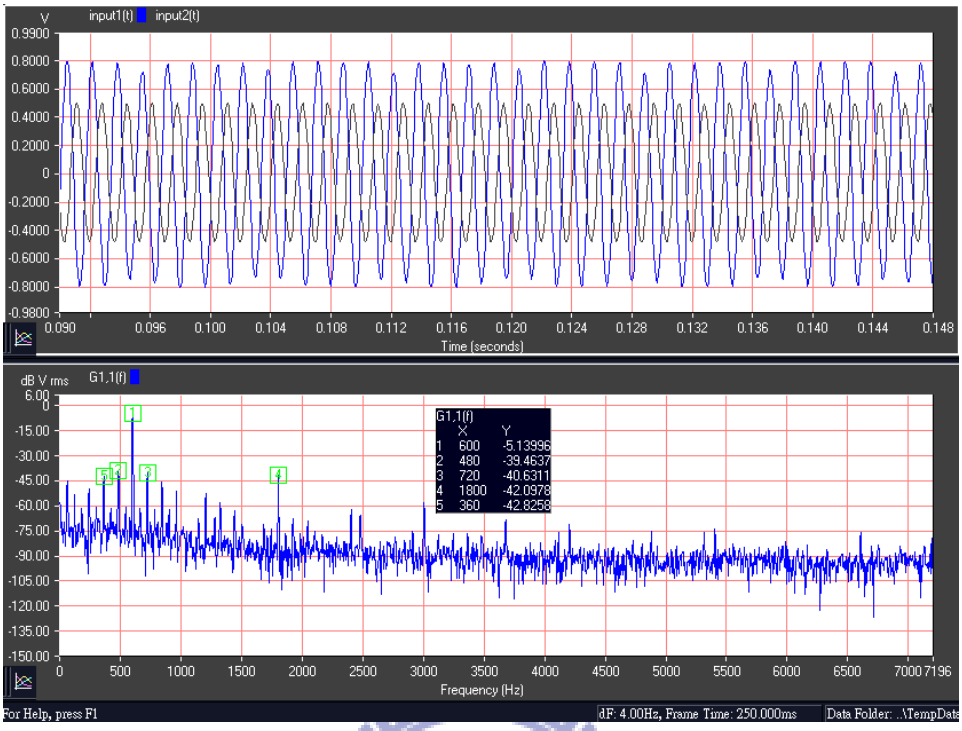


Figure 4-2.3(f): 1Vpp with 0.6k Hz input

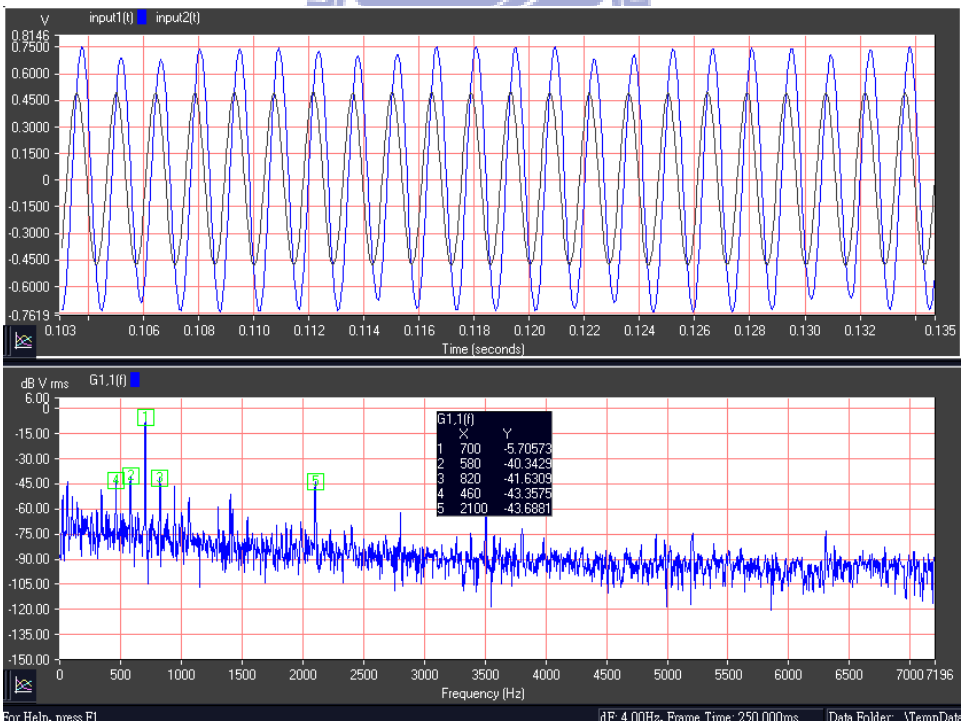


Figure 4-2.3(g): 1Vpp with 0.7k Hz input

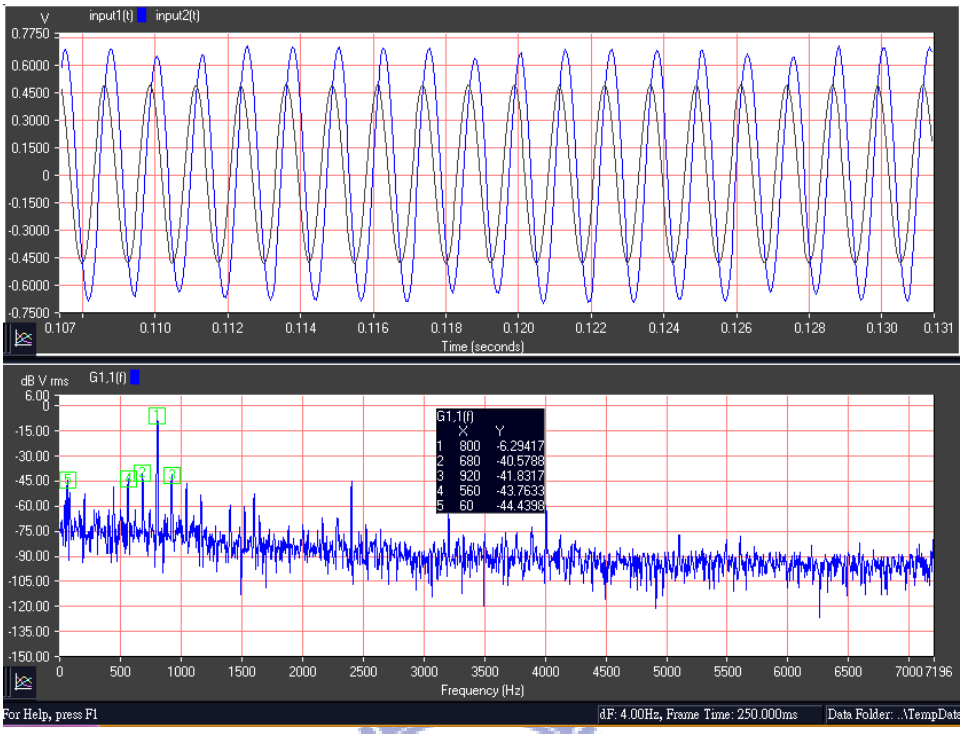


Figure 4-2.3(h): 1Vpp with 0.8k Hz input

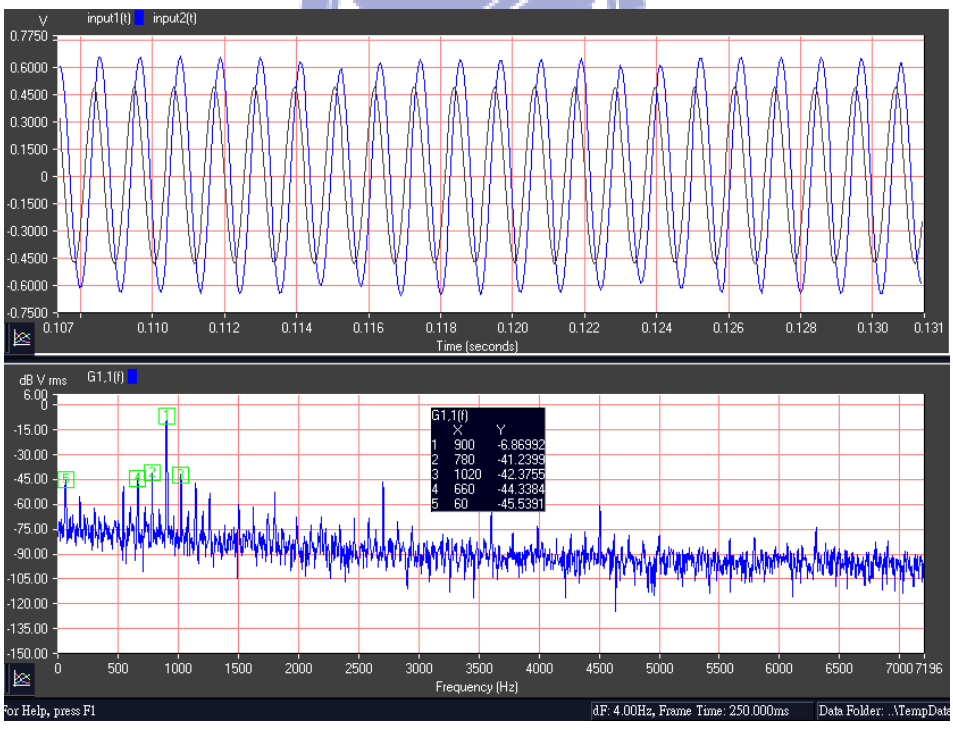


Figure 4-2.3(i): 1Vpp with 0.9k Hz input

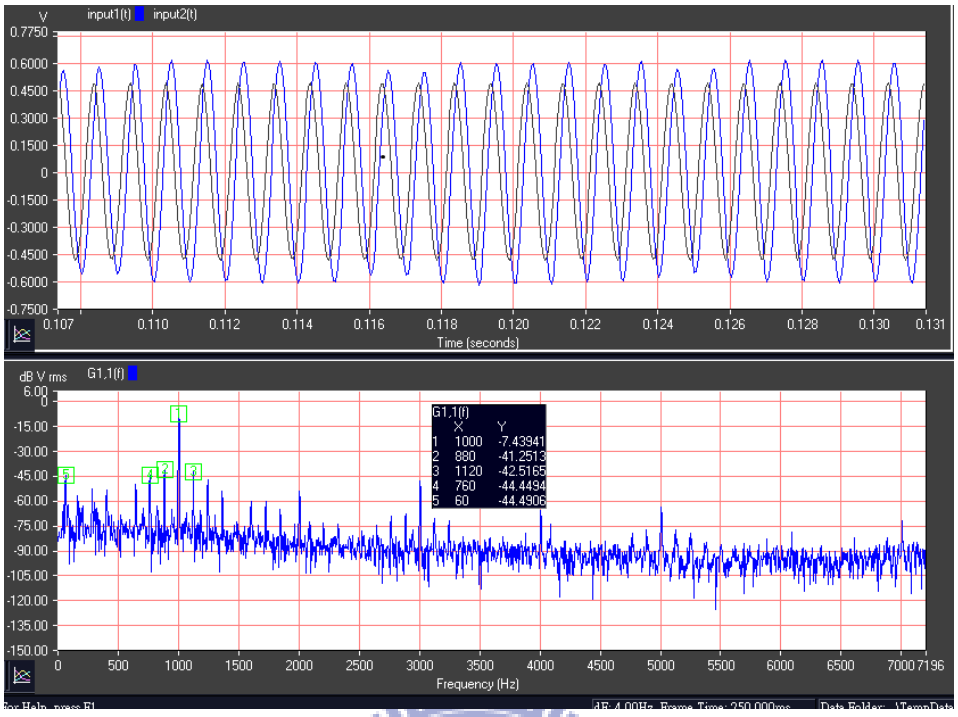


Figure 4-2.3(j): 1Vpp with 1k Hz input

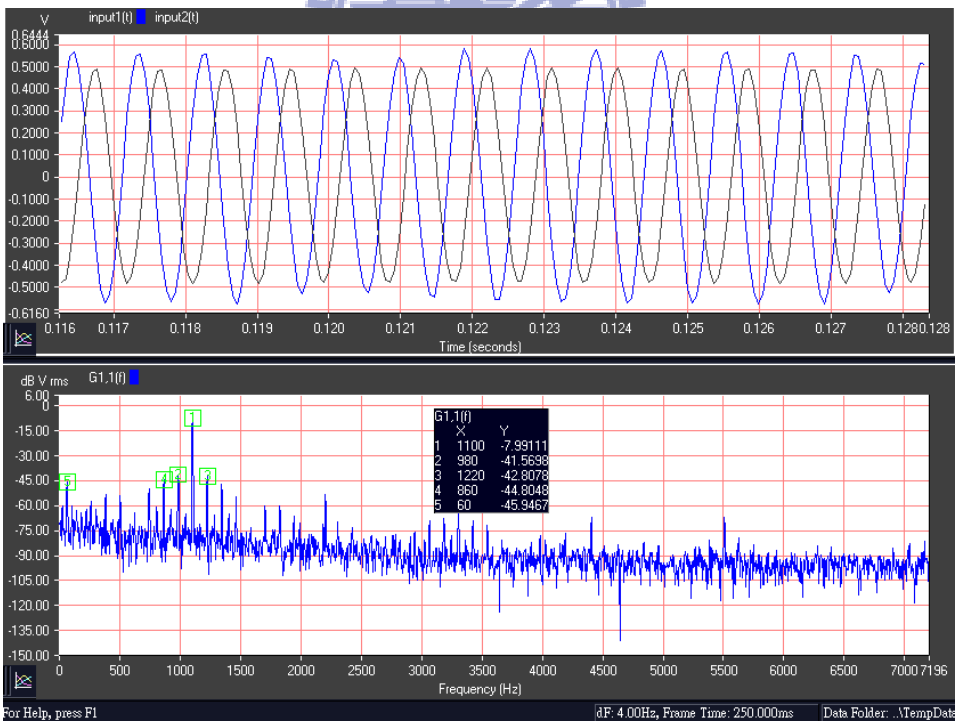


Figure 4-2.3(k): 1Vpp with 1.1k Hz input

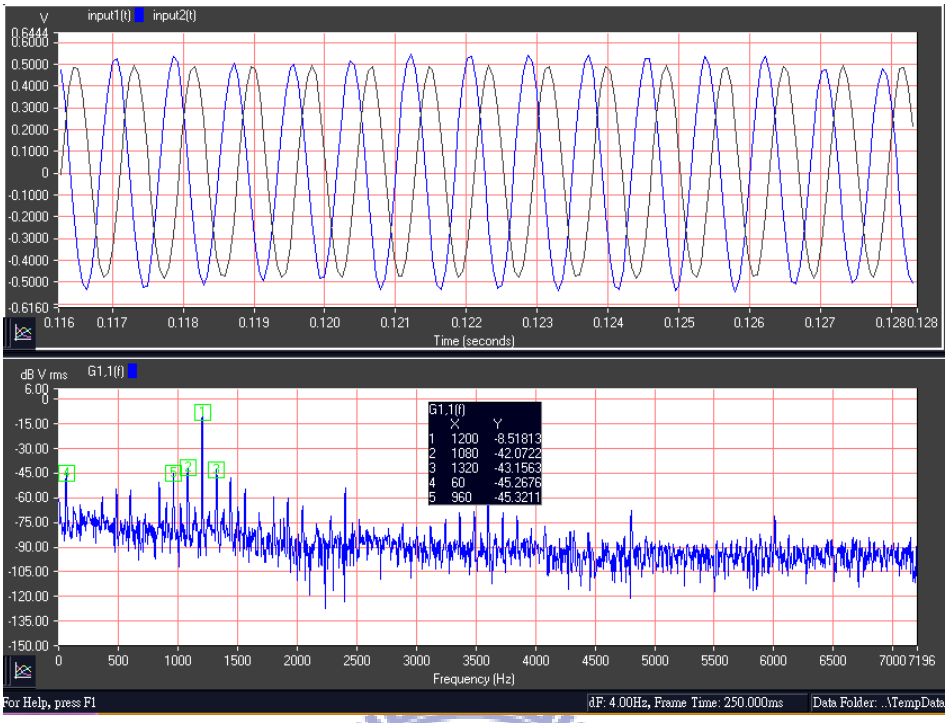


Figure 4-2.3(l): 1Vpp with 1.2k Hz input

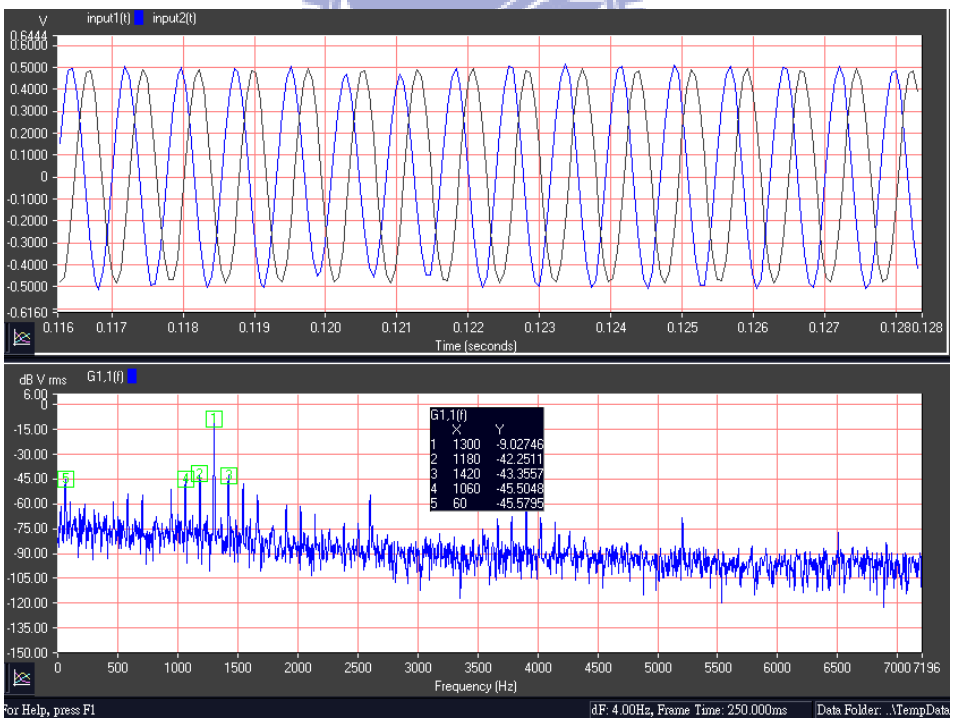


Figure 4-2.3(m): 1Vpp with 1.3k Hz input

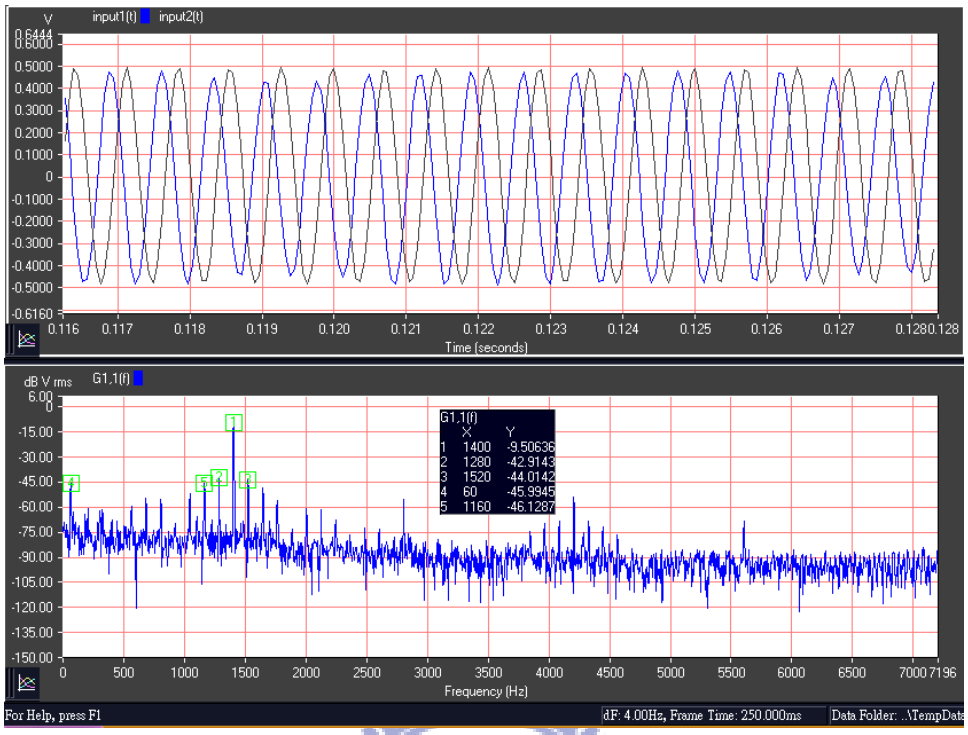


Figure 4-2.3(n): 1Vpp with 1.4k Hz input

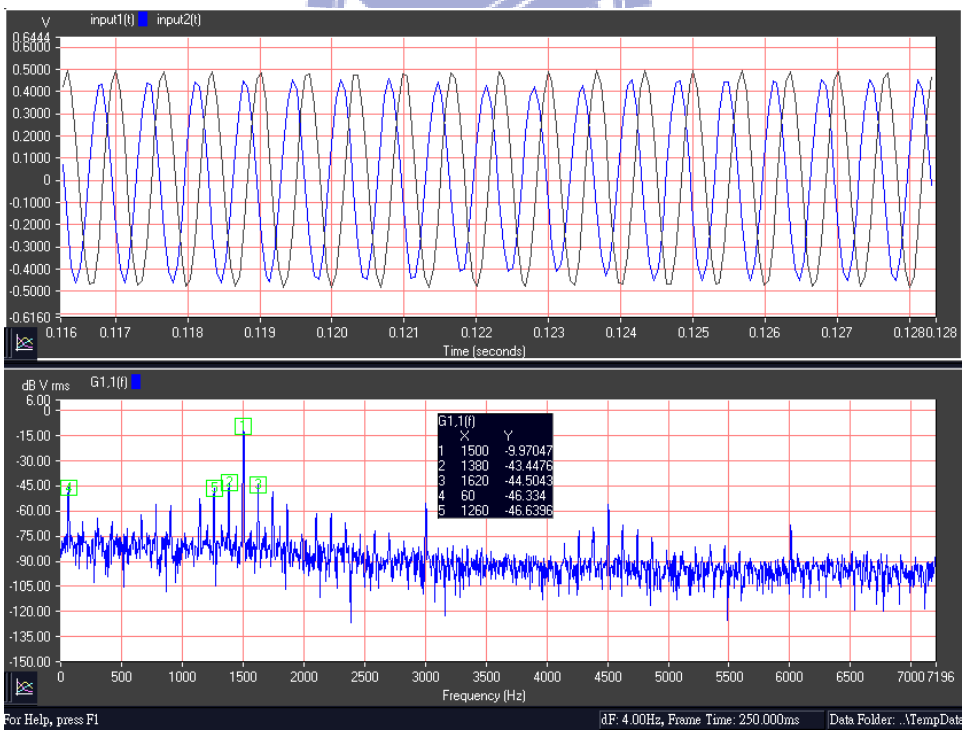


Figure 4-2.3(o): 1Vpp with 1.5k Hz input

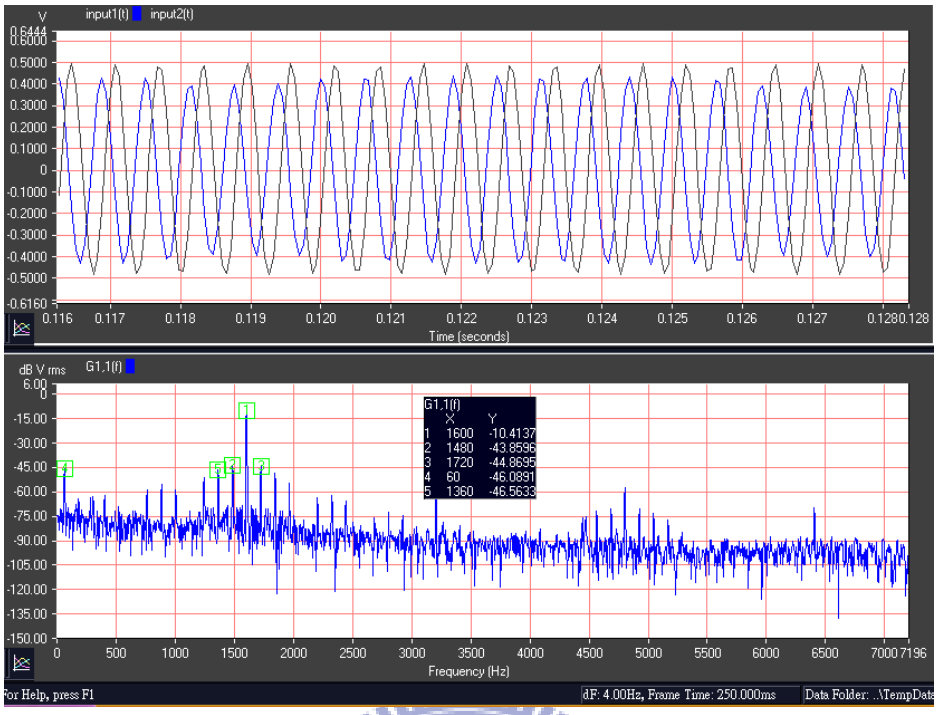


Figure 4-2.3(p): 1Vpp with 1.6k Hz input

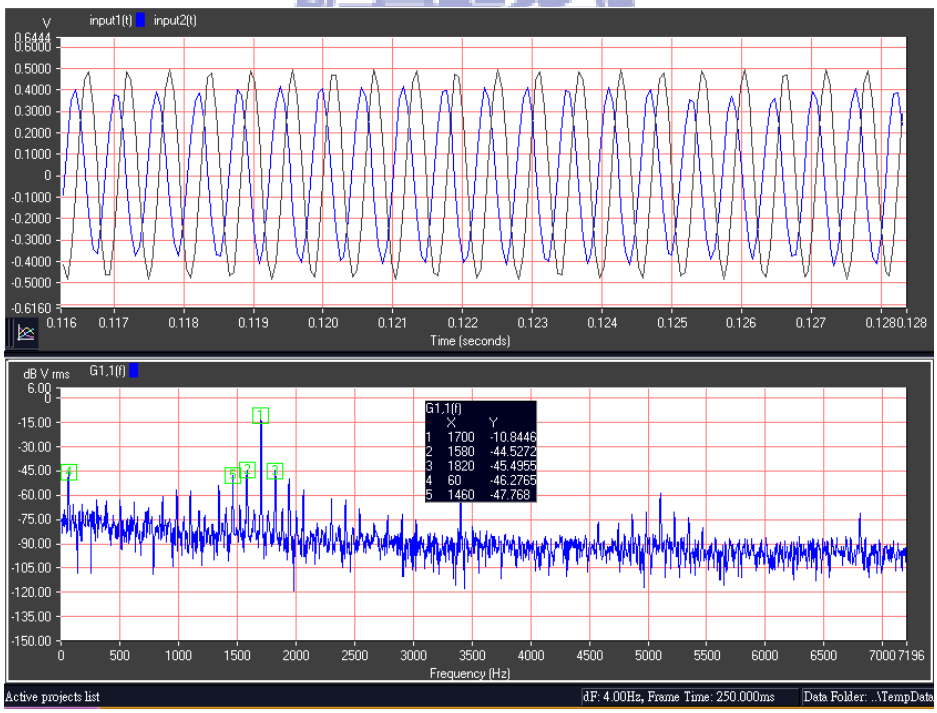


Figure 4-2.3(q): 1Vpp with 1.7k Hz input

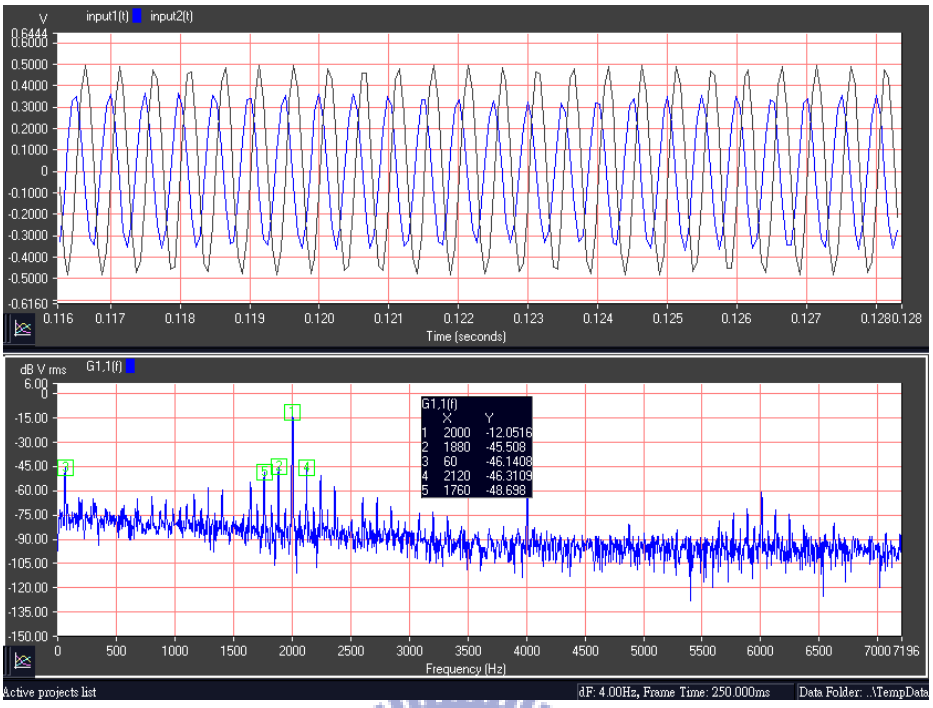


Figure 4-2.3(r): 1Vpp with 2k Hz input

The system AC response is plotted in the Figure 4-2.3(s). The 3db bandwidth can be calculated to be 734 by the interpolation.

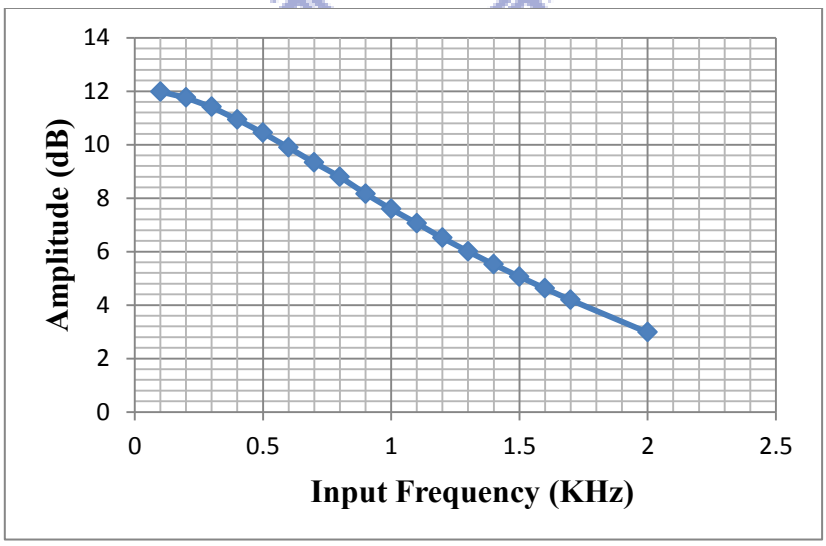


Figure 4-2.3(s): Measurement results of the pre-amplifier AC response

4-2.4 Noise and Residual Offset

The noise floor and residual offset of the DCA architecture are measured in the Figure 4-2.4(a). The noise floor is -90dB voltage (31.6×10^{-6}uV/$\sqrt{}$Hz) (RMS) and the input referred noise (IRN) is 25.829 nV/$\sqrt{}$Hz at 4 g mode. The residual offset is -39.23dBV (RMS) at the second chopper frequency about 31.3K Hz.

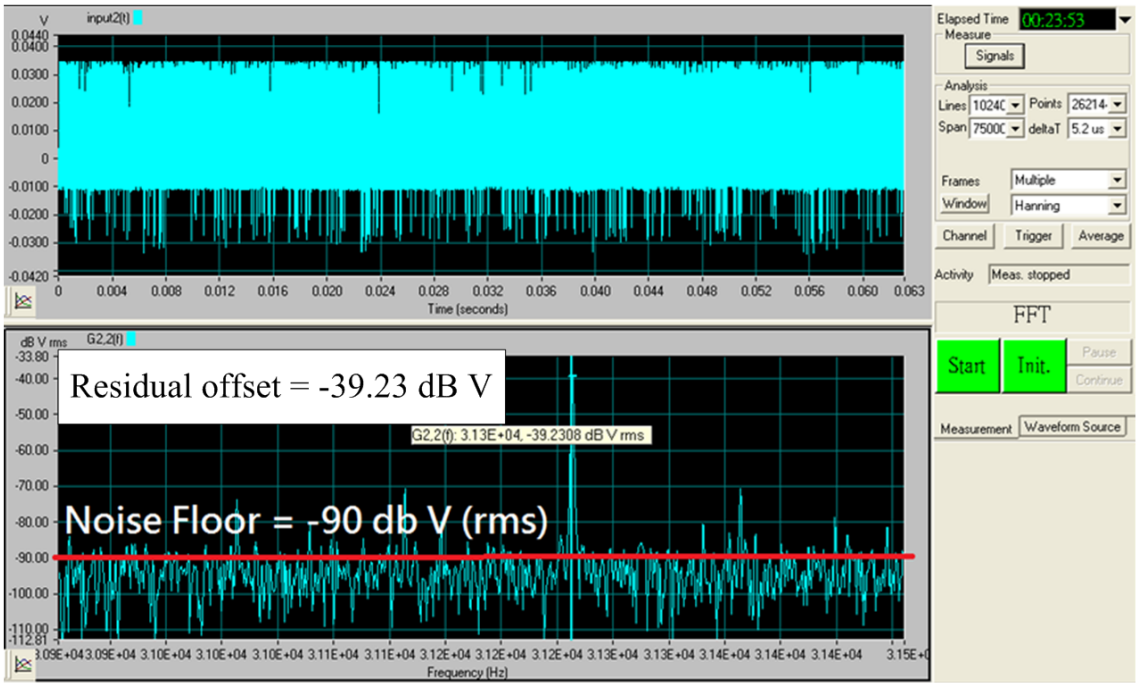


Figure 4-2.4(a): Measurement result of the Noise floor and residual offset

4-2.5 System Output Swing and Slew-Rate

The differential output swing of the AAF is 2.96 Vpp as shown in Figure 4-2.5(a). And the positive slew rate and negative slew rate are $6_{V/msec}$ and $8_{V/msec}$ for single signal respectively.

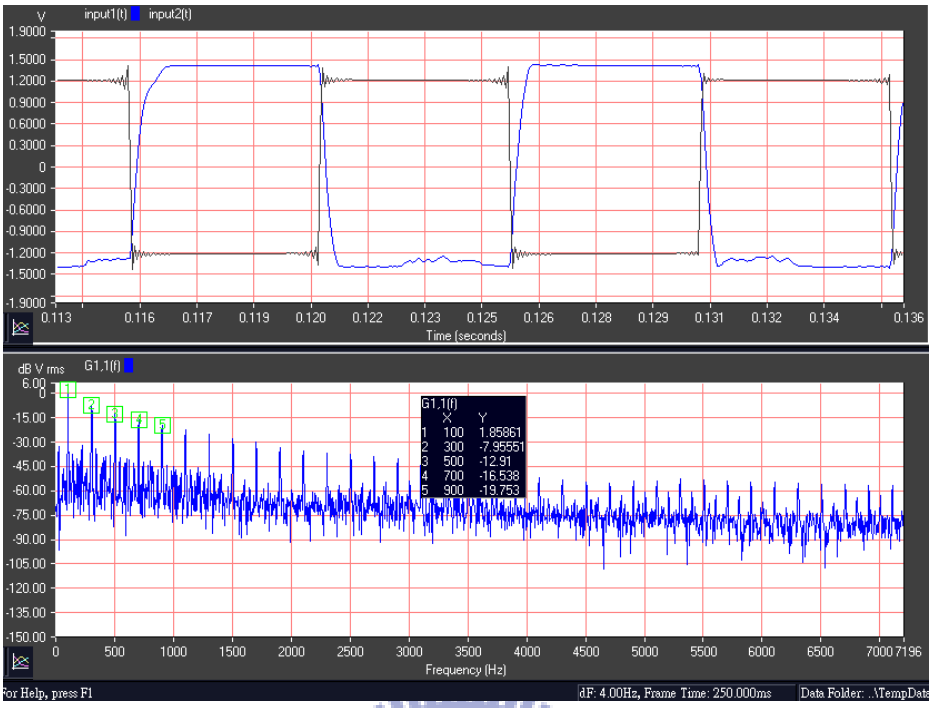


Figure 4-2.5(a): Differential output swing

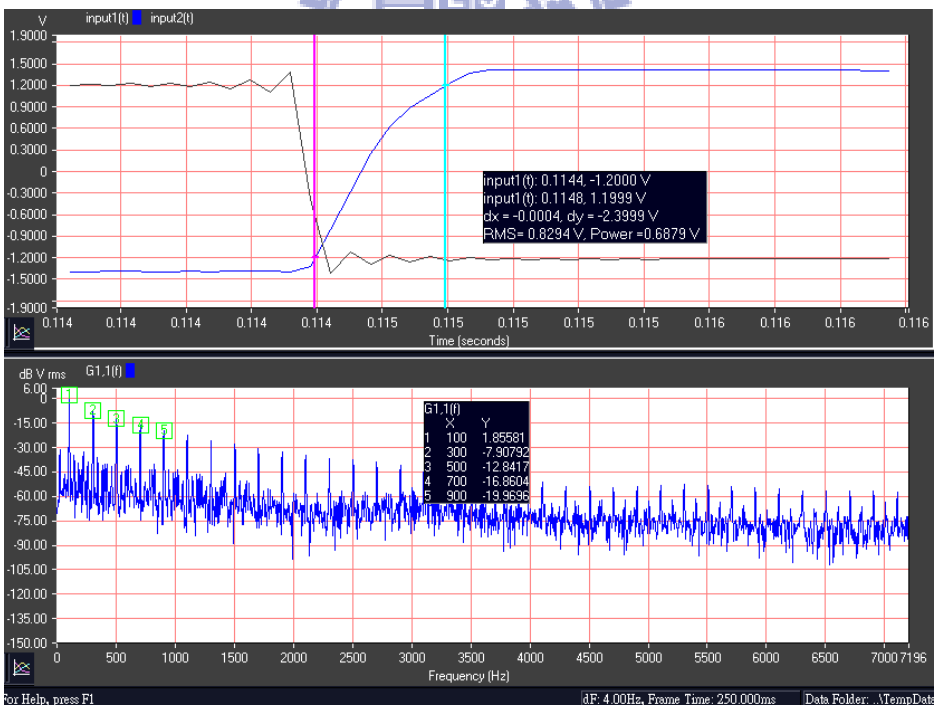


Figure 4-2.5(b): Positive slew rate

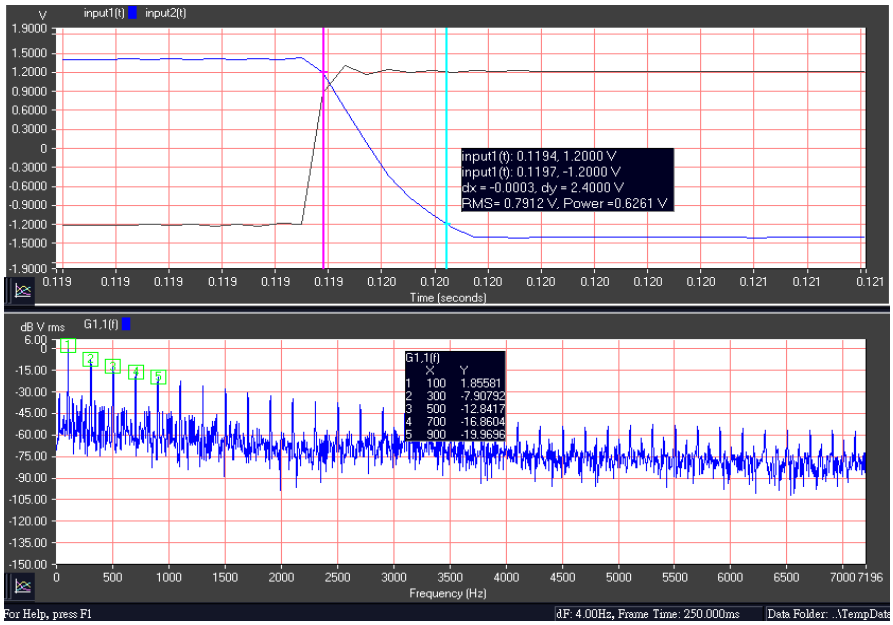
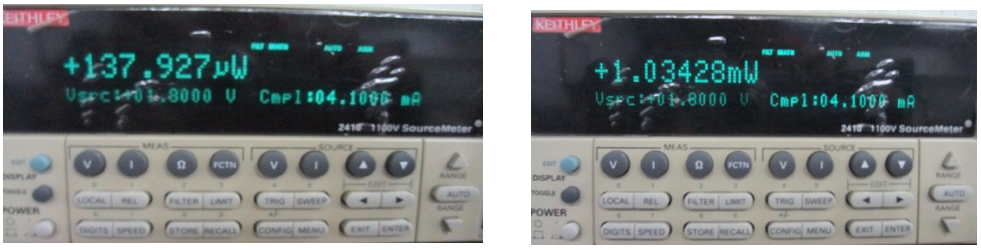


Figure 4-2.5(c): Negative slew rate

4-2.6 Power Consumption

The dynamic and static power consumption of the proposed pre-amplifier is 137.927uW and 1.03428mW respectively as shown in the Figure 4-2.6(a). The total equivalent RMS power consumption is calculated to be 1.043mW by following equation, and the P_d and P_s is the dynamic and static power consumption respectively.

$$P_{tot} = \sqrt{{P_d}^2 + {P_s}^2} \tag{4.2.1}$$



(a) (b)

Figure 4-2.6(a): Dynamic and; (b): Static power consumption

4-2.7 Pre-amplifier Measurement Summary

The Table 4-2.7 shows that the measurement results which are compared to the simulation results in each corner. The output range is the single ended.

Table 4-2.7: Pre-amplifier measurement summary

		Simulation			Measurement
	Unit	**TT**	**FF**	**SS**	
CNEA	ug/√Hz	12.82	12.2	13.75	29.41
Power	uW	619.08	1183	556.24	1043
DC gain	@10Hz(db)	11.89	11.98	11.87	11.98@100Hz
3db-BW	Hz	591	504	703	734
AAF SR+	(V/ms)	18.44	12.14	25.1	12
AAF SR-	(V/ms)	17.12	10.03	23.24	18
Output Range	Volt (Vpp)	1.4983	1.51	1.5022	1.48

4-3 Debug for The Accelerometer

Because of the unstable post process, the accelerometer cannot be released in DRIE step. Figure 4-3(a) shows the etching hole of the proof mass. After Focused Ion Beam (FIB), the residual silicon substrate still exists as shown in Figure 4-3(b).

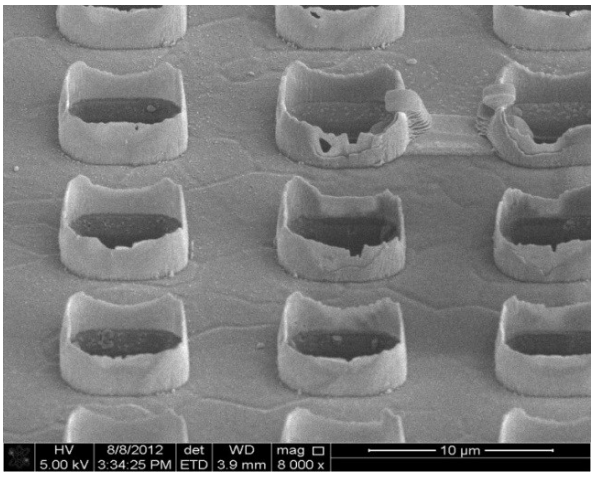


Figure 4-3(a): The proof-mass etching holes

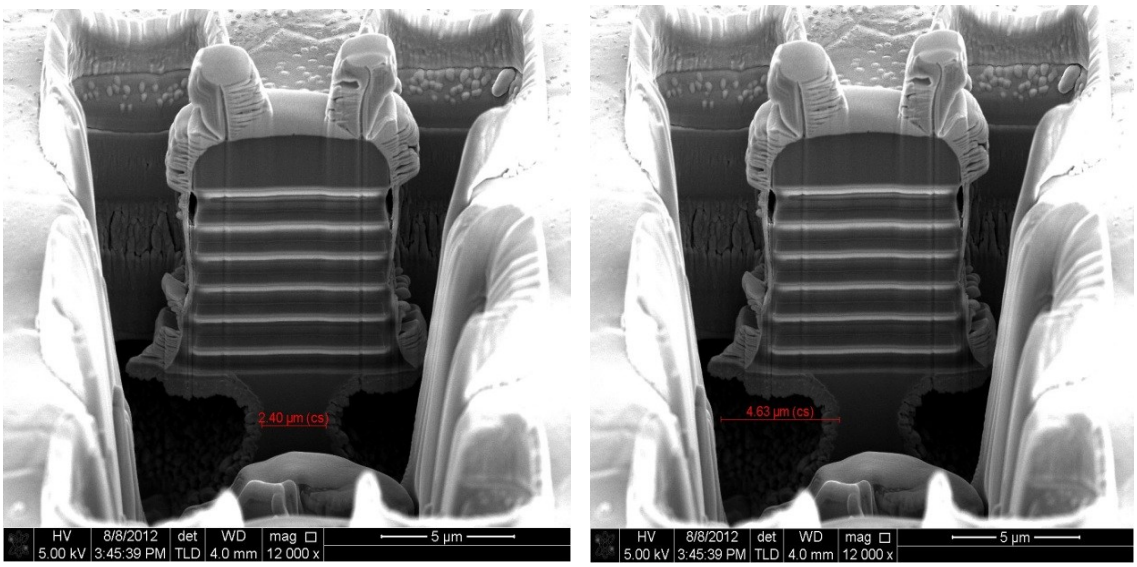
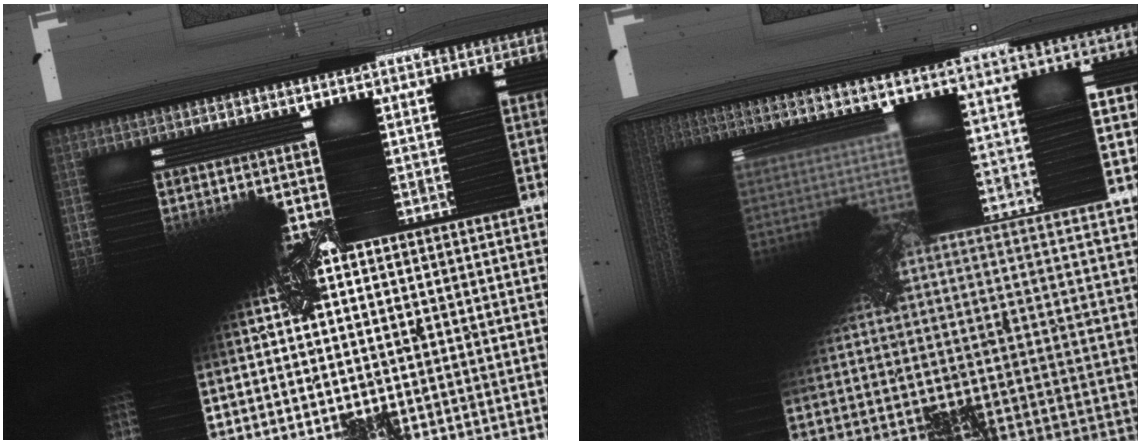


Figure 4-3(b): The residual silicon substrate

That makes the proof mass and residual silicon substrate cohere. Therefore, try to increase the etching time to release the structure is the only solution. By means of the probe, the proof mass can be pushed in z-axis as shown in Figure 4-3(c) (The right one is out of focus), the phenomenon implies that there are still four adhesion positions that are indicated by the box text as shown in Figure 4-3(d).



(c) (d)

Figure 4-3(c): Before; (d): After push the proof mass by the probe

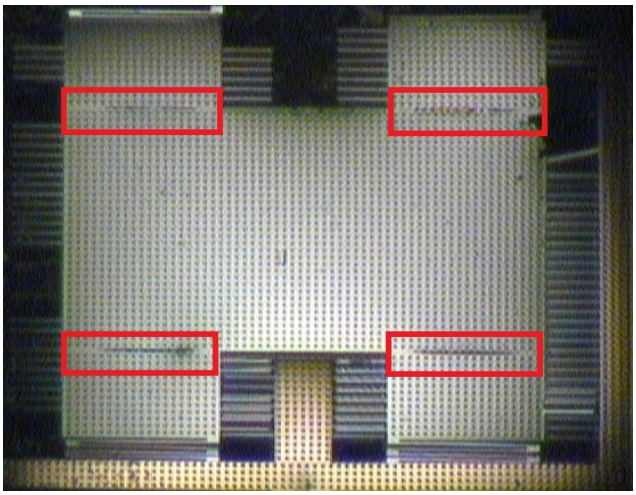


Figure 4-3(e): The adhesions positions

Further, by using the white light interferometer to make sure that the stress warping on the proof mass approaches zero as shown in the Figure 4-3(e) ~ Figure 4-3(f). That implies the structure is not released. The other stress warping data of the accelerometer is measured in Figure 4-3(g) ~ Figure 4-3(i)

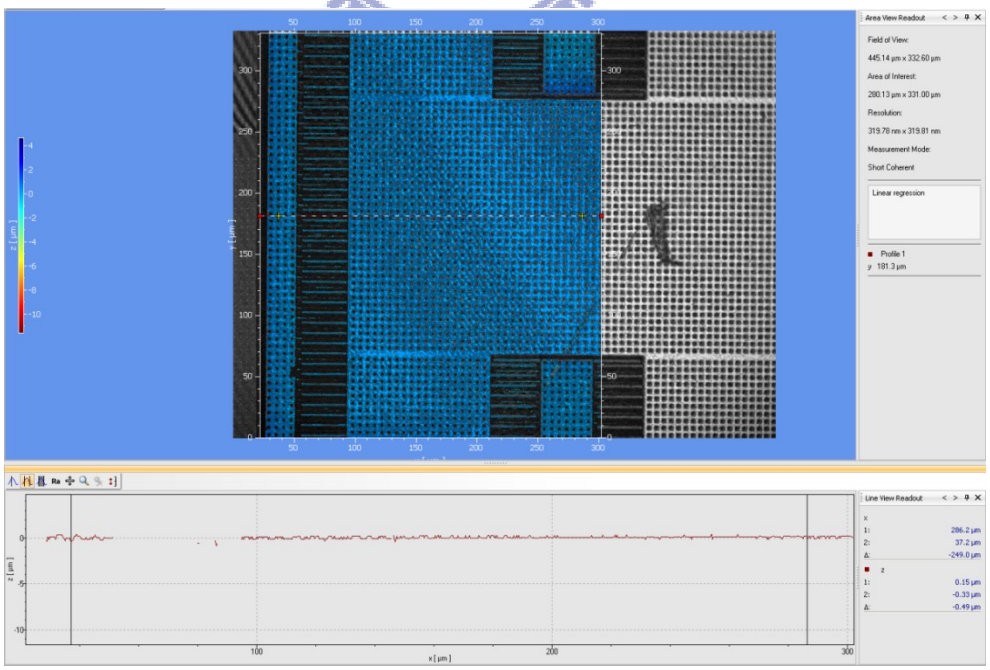


Figure 4-3(f): The stress warping of the proof-mass (1)

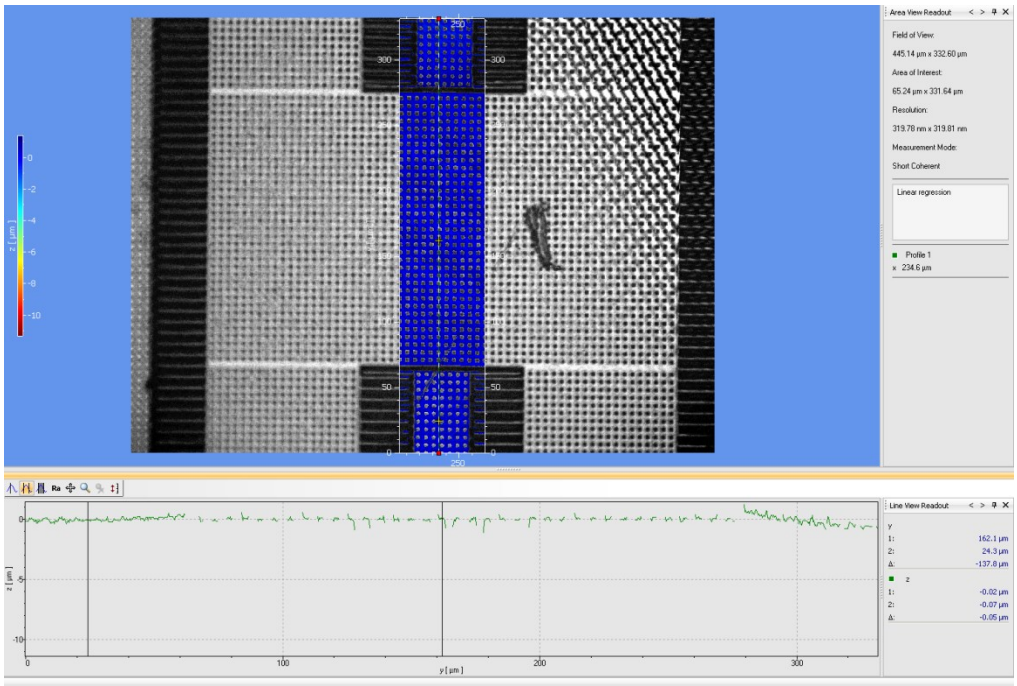


Figure 4-3(g): The stress warping of the proof-mass (2)

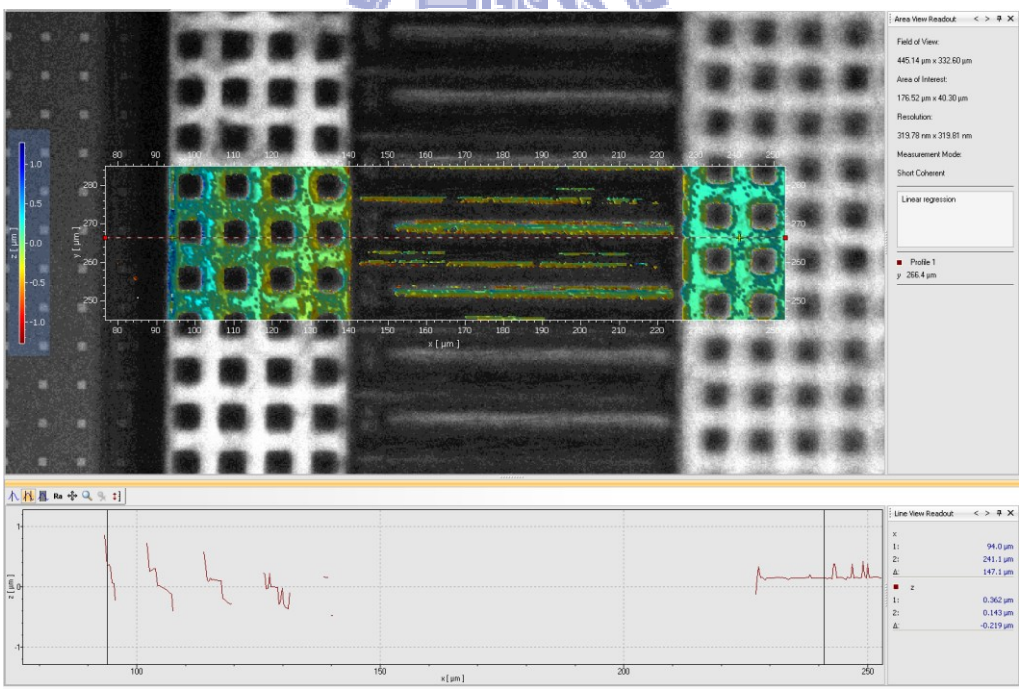


Figure 4-3(h): The stress warping of the comb finger

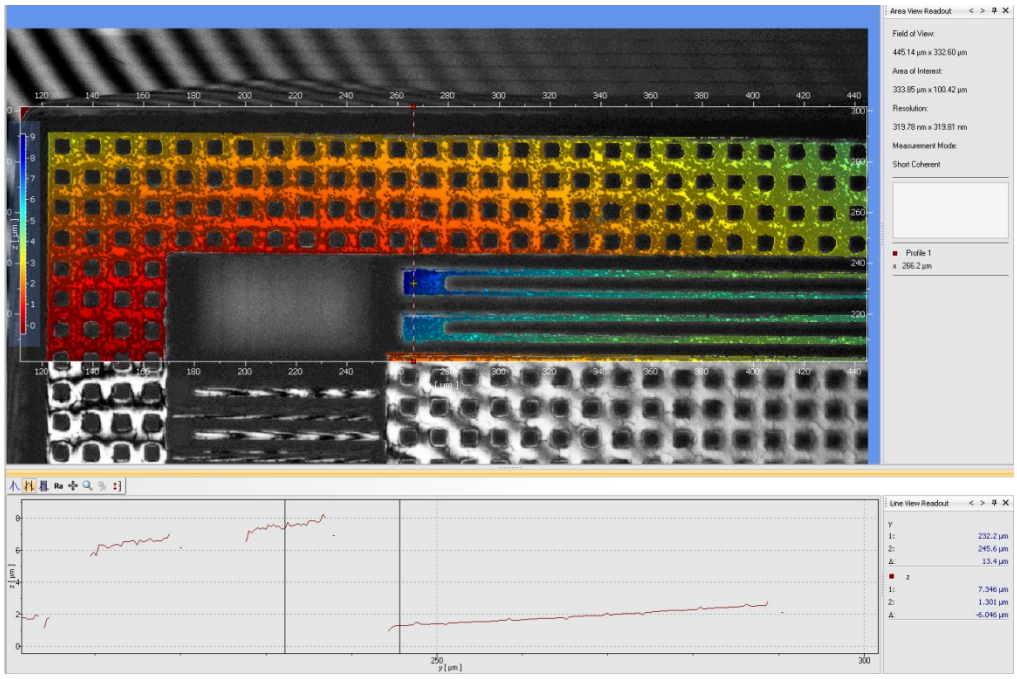


Figure 4-3(i): The stress warping of the spring (1)

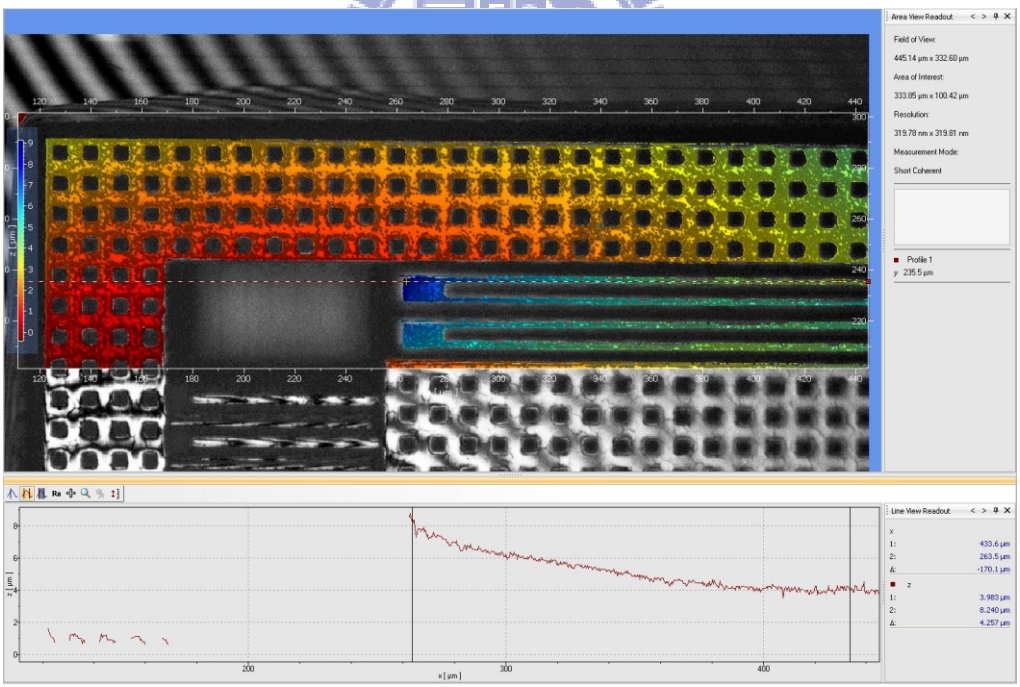


Figure 4-3(j): The stress warping of the spring (2)

Chapter 5 Conclusions and Future Work

5-1 Discussion and Conclusions

Discussion

About the noise power contributions of the DCA architecture, we ameliorate the DCA architecture into single-chopper architecture as shown in Figure 5-1(a), and compare the noise and power between the single-chopper and dual-chopper architecture in this section.

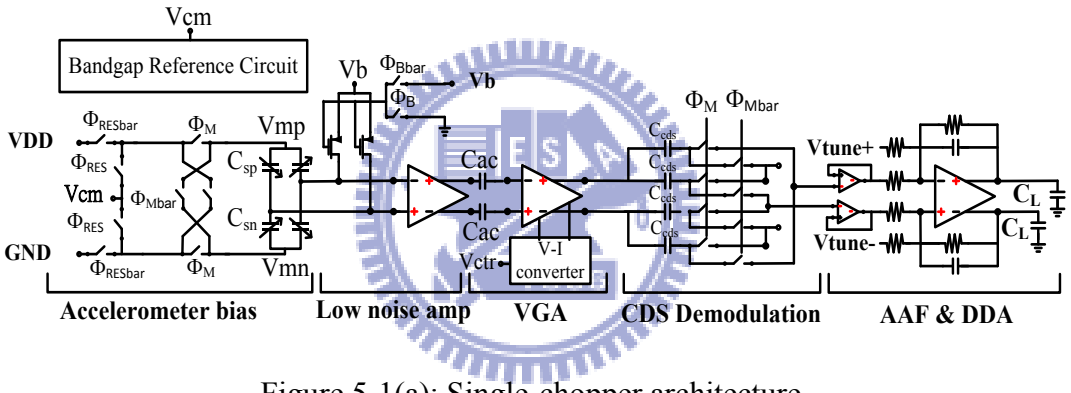


Figure 5-1(a): Single-chopper architecture

The noise performances of the three architecture dual-chopper, single-chopper architecture, and without chopper technique are simulated in Figure 5-1(b). The noise floors of the dual-chopper, single-chopper architecture, and without chopper technique are 12.57 nV/√Hz, 55.22 nV/√Hz, 384.7nV/√Hz respectively. As expected, the noise of the low noise amplifier are not filtered out by Gm-C filter and amplified by the following VGA that increases the noise.

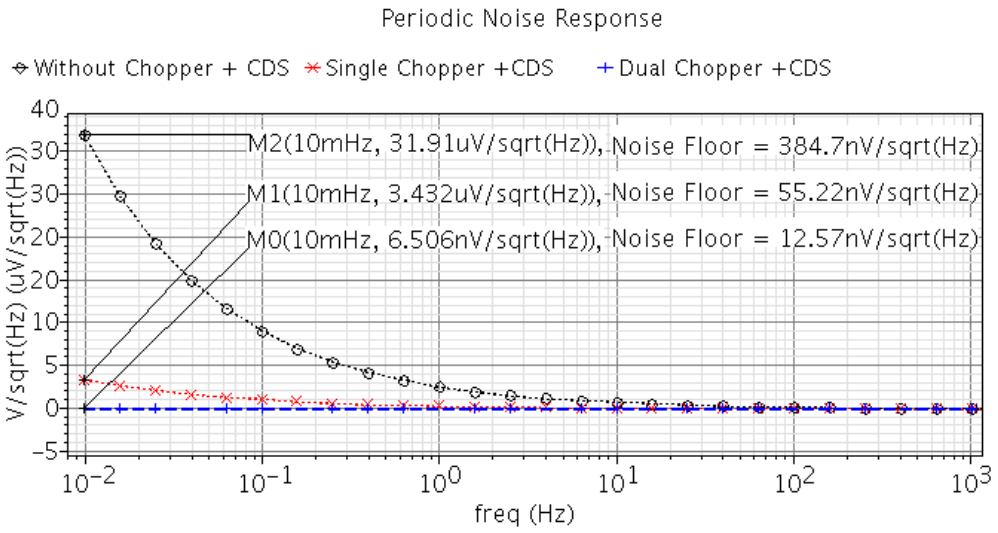


Figure 5-1(b): System input referred noise simulation results in different architectures

About the power consumptions, the single-chopper amplifier saves the Gm-C filter and extends the 3dB bandwidth of the VGA to 500K Hz. According to the bandwidth formula of the proposed VGA, we can estimate the power requirement of the single-chopper amplifier, and the 3dB bandwidth is given by:

$$\omega_{-3dB} = \frac{G_m}{C_L} \tag{5-1}$$

Where G_m is the load resistor, C_L is the load capacitance (1.57pF). According to the simulation results of the designed Gm-C filter, the current requirement is about 10.34uA. And the 3 dB bandwidth of the VGA must be extended from 32K to 500K Hz, and the drive current must be increased. The current is 66.76uA for 31 KHz 3dB bandwidth. According to (5-1), the supply current must be increased to about 256 times 66.76uA for the same loading..

Conclusions

Since the unstable CMOS MEMS post process, the accelerometer is not released completely. That results the sensitivity tuning function cannot be measured. From the comparison between the simulation and measurement results of the circuit part, the noise and DC offset cancelation function of the DCA and CDS work correctly. The measured input referred noise floor is 29.41ug/√Hz, the power consumption is 1.043mW. The bandwidth is 734 Hz.

5-2 Future Work

In the future, a single sensor cannot fulfill the demand of the trends of the System on Chip (SoC). A multi-sensor on a single chip must be developed for wider applications. But under the limitation of the finite chip area, a single readout circuits with auto-gain tuning is very suitable for multi-sensor sensing system that is low cost for commercial considerations. Moreover, the smarter methodologies for the auto-calibration become an important issue for CMOS MEMS sensor.

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