# 國 立 交 通 大 學

## 電子工程學系 電子研究所碩士班

## 碩 士 論 文

### 電容式加速度計暨電容轉數位介面電路設計

### Capacitive Accelerometer with Capacitance to Digital Interface Circuit Design

研究生：王竣傑 Chun-Chieh Wang

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中華民國一〇一年九月

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中華民國一〇一年九月

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## 摘　　要

本論文提出一建立在混合信號微機電製程下具電容轉數位讀出電路之單晶加速度計設計。加速度計操作範圍設計在-5g 到 5g 內，電容變化為 441.2fF 到 470fF，敏感度 2.88fF/g，利用電容轉脈寬電路讀取此範圍電容值，能達到靈敏度為 6.94us/pF，相當於 20ns/1bit，因此在不須任何類比轉數位電路情況下，能轉出為數位訊號，以便後續數位訊號處理。為了從整合的前端電路取得精準值，採用感測器電腦輔助設計軟體與電子設計自動化軟體模擬整合後的電路暨加速度計，具體分析模擬與實際量測差異處，並完成微機電製程與積體電路整合設計流程。

# Capacitive Accelerometer with Capacitance to Digital Interface Circuit Design

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## ABSTRACT

A monolithic accelerometer with integrated capacitance to digital readout circuit in 0.18um CMOS MEMS process is proposed to demonstrate sensor to bit integration. The sensing range of the accelerometer is designed from -5g to 5g and the variation of the capacitance is from 441.2fF to 470fF. The sensitivity of the accelerometer is 2.88fF/g. The capacitance value of the sensing range is readout by the capacitance to pulse-width circuit to readout. The capacitance to pulse-width circuit of the sensitivity is 6.94us/pF which is equivalent to 20ns/1bit. Therefore, without any analog to digital module, the output signal can be directly interface to digital signal process. In order to get the accurate value of monolithic front-end circuits, the computer aided design flow for MEMS and IC integration is used to co-simulate the monolithic circuits with

the accelerometer and to provide comprehensive analysis of the difference between the simulation and the measurement results.

# 誌謝

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# List of Figures and Tables

# Chapter 1 Introduction

Due to the impact of the economic benefits and heterogeneous integration, micro-mechanical structures [1] and circuits integrated on a single chip have been attracted the significant researches and developments for low cost and high volume applications. The integration also brings many applications like inertial sensor aided navigation system, gaming control interface, and etc.

There are different transduction mechanisms to catch the acceleration signal, such as the piezoresistive and capacitive accelerometer. Compared with the capacitive accelerometer, the piezoresistive accelerometer is pressed by the physical stress to change the variation of the resistance value. The working principle of the capacitive accelerometer is to convey to the capacitance value by the external forces. Then, by using the readout circuits, the capacitance or resistance values are converted to the analog or digital signals. In order to get the digital signal, ADC or C-to-D (capacitance to digital) circuits are frequently used. The advantage of C-to-D circuits compared with ADC circuits is the low-complexity structure.

## 1.1 Motivation

Over the past two decades, MEMS sensors such as accelerometers and gyroscopes [2] have been extensively applied to airbags and to smart phones to detect direction and locations, magnitude and vibration for smart phones. There always

involves signal conversion relation by converting a non-electrical quantity such as pressure, acceleration, and angular velocity into an electrical signal like resistance and capacitance values on MEMS sensors and actuators.

In [3], it have been summarized that the standard CMOS process and several CMOS post-processes for the applications of sensors with circuits. CMOS-based MEMS processes are normally classified as pre-CMOS, intra-CMOS, and post-CMOS approaches. In order to integrate into a foundry CMOS run, the micro-fabrication steps must be with a flat, no contaminants and clean silicon surface. Therefore, the few MEMS processes added into CMOS flow have the advantage of monolithic integration of integrated circuits (ICs) with microstructures.

In order to get accurate simulation results, a new design flow is needed to extract the sensor model under specified process flow. The offset of the sensor after MEMS post process is an important issue due to the residue stress gradient which induces the curling mismatch of the fingers as shown in Figure 1.1 (a). It reduces the sidewall capacitance values and thus the sensitivity of the capacitance. As illustrated in Figure 1.1 (b), the matching technique of the rigid frame is added to the accelerometer design to deal with the curling influence [1]. It is used to do a first-order curling matching, but the trade-off is that it consumes more area than Figure 1.1 (a). Another design issue of the sensor offset is the in-plane curling of beams such as springs and fingers,

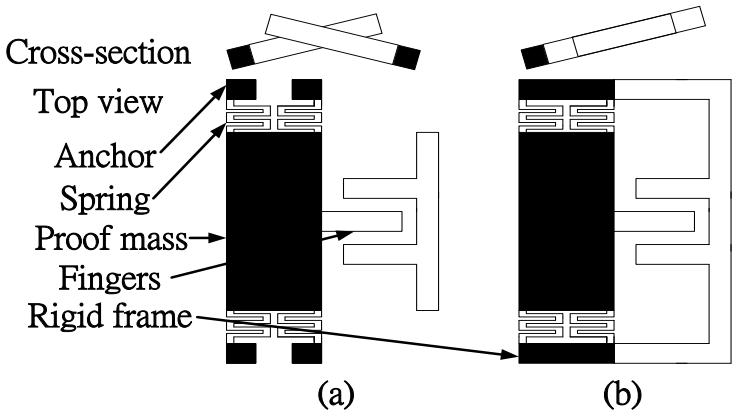



Figure 1.1: Curling matching technique: (a) Without curling matching and (b) With curling matching

which results in the offset of the lateral positions [4]. The design of multilayer beams which have the same metal width for 3D MEMS model is shown in Figure 1.2 (a). However, the actual asymmetric structure by the process variations, particularly from the photolithography misalignment, causes the lateral curling as shown in Figure 1.2 (b). In order to solve the problem, the design of multilayer tapered beams is illustrated in Figure 1.2 (c) and the rule is that lower level metal layers are designed to be wider. Compared with Figure 1.2 (b), the multilayer structures from the process are with lower position offset for reducing in plane curling mismatch as shown in Figure 1.2 (d). However, in the DRIE (Deep reactive ion etching) process, the oxide material fills the vacancy part next to the shifted metal when the top metal is used as the hard mask for DRIE etching. In other words, the oxide material controls the in plane curling and the top metal layer is used to define the structure sidewall. Note that the exposed top metal layer without the protection of the passivation layer is easily corrupt.

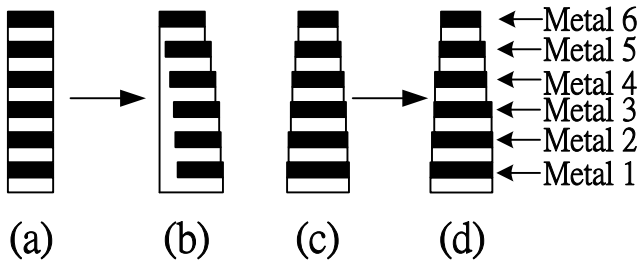



Figure 1.2: Cross-section part of the metal-oxide structure with the consideration of the misalignment: (a) The normal beam design without photolithography misalignment, (b) The normal beam design with photolithography misalignment, (c) The tapered beam design without photolithography misalignment, and (d) The tapered beam design with photolithography misalignment

There are various types of sensor readout circuits such as capacitance to voltage (C-to-V), frequency (C-to-F), or time (C-to-T), and C-to-V circuits are also called analog front-end (AFE) which will connect analog to digital converters (ADC) to generate digital signals for digital signal processing (DSP). C-to-F and C-to-T circuits are also called pulse-frequency modulation and pulse-width modulation, respectively. In fact, C-to-F and C-to-T circuits can be directly used to catch the quasi-digital signals. With a counter being combined with C-to-T circuits to count the pulse width, the fully digital signal can be generated for digital signal processing. Compared with C-to-T circuit, the combination of AFE plus ADC not only increases the complexity and power consumption but also introduces extra noise [5]-[9]. Rather than the analog voltage or current output in analog readout circuits, digitization of C-to-T circuit is achieved by encoding the information in the time or frequency domain. Moreover, there is a strong contrast between ADC and PWM on the issue of the dynamic range.

Quasi-digital readouts such as PWM and PFM are not limited by the supply voltage or current. Furthermore, the digital output provides robustness against environmental noise due to its digital nature.

Table 1.1: The comparison of pulse width modulation circuits

<table>
<tr><td></td><td>[6] 2007</td><td colspan="6">[5] 2011</td><td>[7] 2012</td></tr>
<tr><td>Type</td><td>Dual slope integration</td><td colspan="6">RC charging</td><td>Dual slope integration</td></tr>
<tr><td>Output</td><td>Quasi-digital</td><td colspan="6">Quasi-digital</td><td>Quasi-digital</td></tr>
<tr><td>On-chip sensor</td><td>No</td><td colspan="6">No</td><td>No</td></tr>
<tr><td>Circuit complexity</td><td>High</td><td colspan="6">Low</td><td>Medium</td></tr>
<tr><td>Power</td><td>16.5mW</td><td colspan="6">60uW</td><td>54uW</td></tr>
<tr><td rowspan="2">Cap. dynamic range</td><td rowspan="2">0.8pF~ 1.2pF</td><td>Range(F)</td><td>1p</td><td>9p</td><td>28p</td><td>211p</td><td>10.2n</td><td rowspan="2">2.5pF~ 2.82pF</td></tr>
<tr><td>Ref(Ω)</td><td>10M</td><td>2.7M</td><td>1M</td><td>100k</td><td>3k</td></tr>
</table>

As shown in Table 1.1, it summarizes some parameters of the three pulse-width modulation interface circuits. In [5], it focuses on a capacitance or resistance change in a wide dynamic range and provides a less complexity circuit architecture by the RC charging and discharging principle to get the time signal. In [6], it uses a double slope approach using transconductor-based Miller integrators to be a capacitance to

pulse-duration converter. In [7], it could readout seven segments from 2.5pF to 2.82pF in the capacitance range. The capacitance to time sensitivity is 3.88us/pF and the resolution is 46.5fF. The output is a quasi-digital signal.

In this thesis, it focuses on readouting the capacitance value range smaller than [7] and the slight capacitance variation for the monolithic of circuits with the one axial accelerometer. The resolution is 2.88fF and the output signal is the digital signal by adding a counter circuit for digital signal process. We use TSMC 0.18-um CMOS-MEMS technology to design the capacitive accelerometer with the capacitance to digital interface circuit. Figure 1.3 illustrates the system architecture. The working principle is to generate -5g to 5g by the LDS shaker to drive the accelerometer to change its top capacitance value. The C-to-Pulse-width circuit is operated by the clock signal and readouts the variation of the capacitance to transform into the pulse width. The pulse width is counted by the 9 bits counter. It means that the digital signal of the output node represents the pulse width which shows the capacitance variation of the accelerometer between -5g and 5g. In addition, the

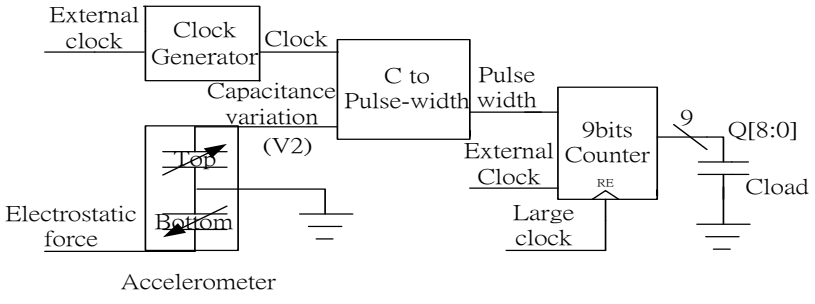



Figure 1.3: The system architecture of the thesis

counter is reset by the large clock signal and making sure it to count from 000000000. In order to prevent the accelerometer to be driven by the LDS shaker, we reserved the electrostatic force node to generate the electrostatic force to drive the accelerometer.

## 1.2 Organization

The thesis shows the C-to-D circuit with the one axial accelerometer and co-simulation for the integrated circuit with the sensor. In chapter 2, introduction and implementation of the one axial MEMS accelerometer will be presented. The proposed readout C-to-D circuit will be reported in chapter 3. In chapter 4, co-simulations and implementation of the circuit with the accelerometer will be presented. In chapter 5, the measurement results will be displayed. The conclusion and future work will be given in chapter 6.

# Chapter 2 CMOS MEMS Accelerometer

## 2.1 CMOS MEMS Fabrication

### 2.1.1 Process

The capacitance to digital circuit of one axial accelerometer proposed in this thesis is manufactured by the CMOS MEMS 0.18um process of CIC (National Chip Implementation Center). The diagram of MEMS post-process is illustrated in Figure 2.1 [1] and it takes two steps after the 1P6M CMOS process to complete the MEMS sensors. The first step is anisotropic oxide etching, and the second is isotropic substrate etching. The passivation layer above the microstructure is removed during the standard 1P6M CMOS process and it is above the electronic circuits protects the devices in Figure 2.1 (a). After the CMOS process, the microstructure which has no protection of the photoresist is etched by the anisotropic oxide etching (DRIE) in Figure 2.1 (b) and it results in the vertical sidewalls and comb fingers to sense the force, added on when the accelerometer. Then, the isotropic silicon substrate etching is used to etch the microstructure of the substrate and release the accelerometer in Figure 2.1 (c).

### 2.1.2 CMOS MEMS Layout Rules

The layout rules are defined by TSMC in the process, and they are applied to construct the microstructure of the devices. All of them should be completely obeyed

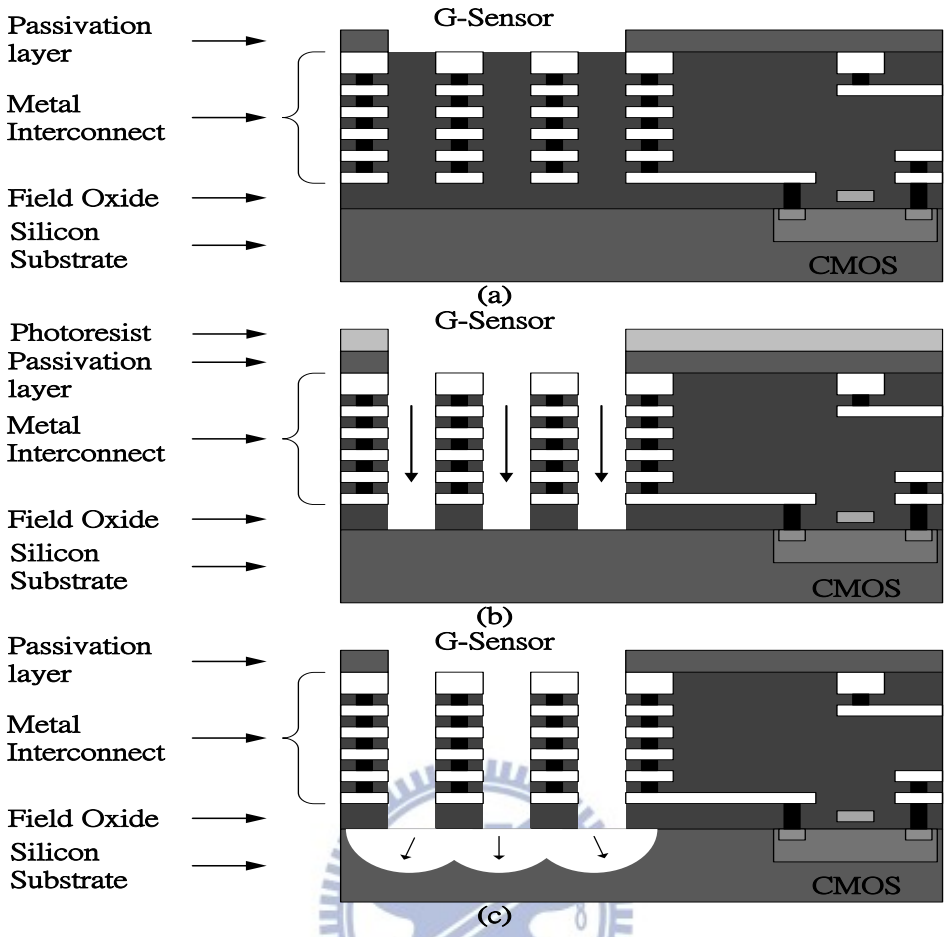



Figure 2.1: Cross-section view of MEMS process flow: (a) After completion of CMOS, (b) After anisotropic oxide etching, and (c) After isotropic substrate etching to release the G-sensor

to implement the design of the chip. The definitions of layout locations at the same layer or between two different layers are shown in Figure 2.2. The location definitions are applied to define the distance constraint. The passivation mask (PAD) is used to define open-windows for the signal pads and MEMS process. To satisfy the MEMS etching process, PAD mask is also used to overlap the RLS region as shown in Figure 2.2 and the RLS region are used to define MEMS etching region.

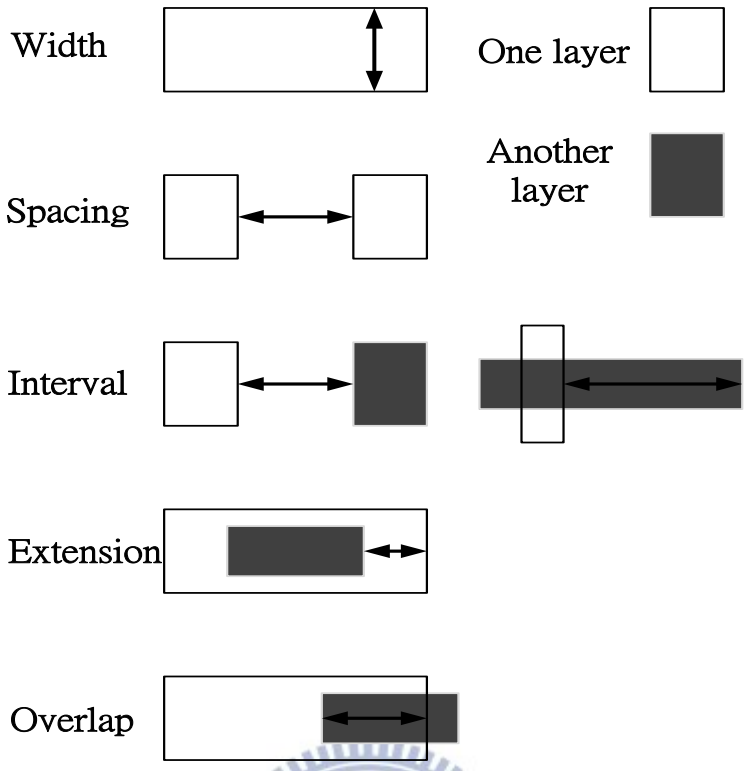



Figure 2.2: The definitions of layout locations

RLS mask defines the MEMS etching region in post-process, and the design is shown in Table 2.1 [10] and Figure 2.3. Note that if the expected structural line width or spacing is beyond the limit of lithography (< 4 um) in post process, metal layer can be used as the hard-mask for the purpose of high resolution, but it is not guaranteed to be implementable. Figure 2.4 is an example of RLS-mask layout in the etching window. Case A just uses RLS mask to define the window size when the RLS width is larger than 4um. In another case B, the top metal and RLS-mask are used to define the etching width which is smaller than 4um because the minimum width of RLS is 4um in rule A of Table 2.1. Although the microstructure could be designed less than 4um by the method, it still gets risk of losing the thickness of metal microstructures used as

hard mask and the sensors will be subjected to the unsuspended risk. To appropriately select the width of etching window, the vertical and lateral etching profiles versus the size of etching window are list in Figure 2.5.

Table 2.1: The definitions of RLS-mask in CMOS MEMS process [10]

| Rule # | Description | Rule (μm) |
|---|---|---|
| RLS.W.1 | Min. Width of RLS | A 4μm |
| RLS.METALx.1 | Max. overlap of RLS on Metal ( If using Metal as hard mask ) | B 1μm |
| RLS.Poly.1 | Max. overlap of RLS on POLY | B 1μm |
| RLS.S.1 | Min. Spacing between RLS regions | C 4μm |
| RLS.PASS.1 | Min./Max. extension of PAD mask over RLS mask | D 1um |
| RLS.PASS.2 | Min. Interval between wide RLS (width > 20um) and SIGNAL PAD | E 50μm |
| RLS.ACTIVE.1 | Min. Interval from RLS to unsuspended PMOS or NMOS | F 50μm |
| RLS.Cap.1 | Min. Interval between wide RLS (width > 20um) and un-suspended capacitors | F 50μm |
| RLS.Res.1 | Min. Interval between wide RLS (width > 20um) and un-suspended resistors | F 50μm |
| RLS.R.1 | Max Area ratio of RLS to wide PAD (width >100um) in Etching-Region | 60% |

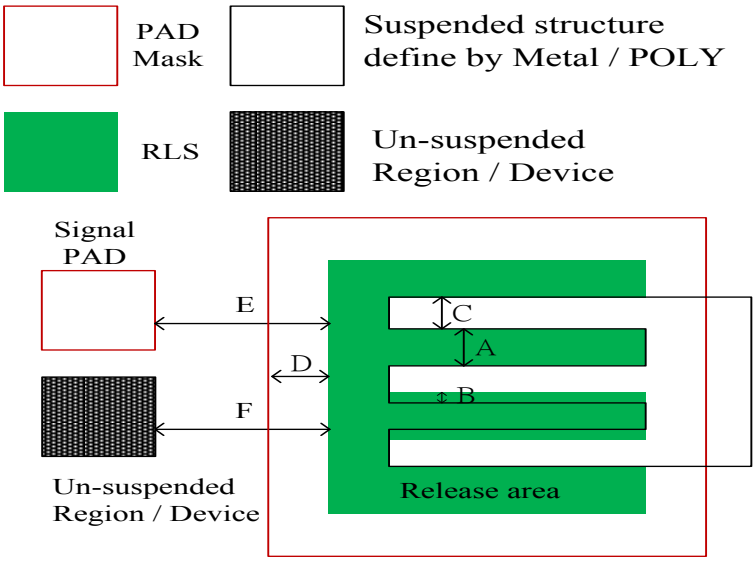



Figure 2.3: The definition of RLS-mask

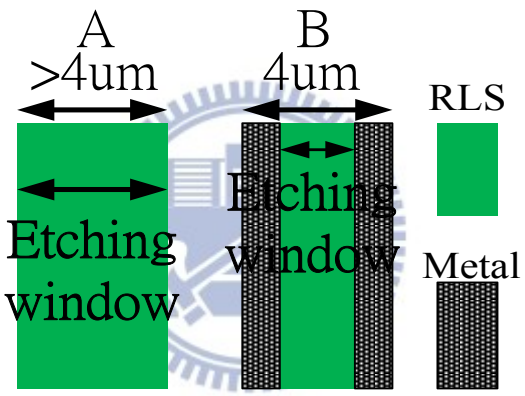



Figure 2.4: RLS-mask layout of etching window width larger and smaller than 4um

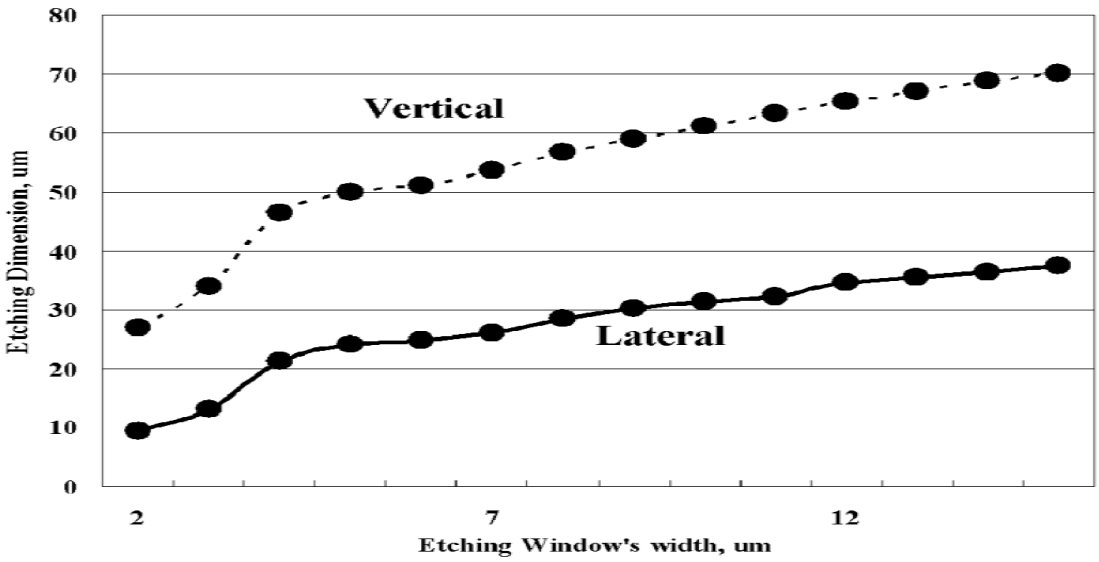



Figure 2.5: The etching dimension v.s. the width of etching window [10]

## 2.2 The One Axial Accelerometer Design

### 2.2.1 Working Principle of Accelerometer

Schematic of the one axial accelerometer is shown in Figure 2.6 [11]. It is the part of the microstructure during the MEMS post-process in Figure 2.1. As shown in Figure 2.6 (a), the accelerometer consists of the proof mass, comb fingers, springs, etching holes, and the ridge frame. The rigid frame is designed to the accelerometer for dealing with the curling influence as mentioned in previous section. The etching holes are used to make the proof mass to suspend by DRIE step. It forms a mass-spring-damper system due to force-driven in Figure 2.6 (b). The external acceleration $a_{in}$ generates an inertial force on the proof mass.

Then, the inertial force induces the displacement of the proof mass. When the accelerometer is driven, the motion differential equation is given as

$$m\ddot{x} + b\dot{x} + kx = ma_{in} \tag{2.1}$$

where m, b, k, $a_{in}$, and x are the mass of the accelerometer, damping coefficient, spring constant, the external acceleration, and the displacement of the proof mass, respectively. Therefore, the accelerometer in the form of mechanical model is equivalent to the four fully differential capacitances in the form of circuit in Figure 2.6 (c) where $C_s$ is the initial capacitance and $\Delta C$ is the variation of the initial capacitance. The displacement value transforms into the variation of the capacitance

value. The circuits are designed to readout the variation of the capacitance value. Consequently, the value of external acceleration can be readout due to the circuits in the sensing range. Taking Laplace transform of Eq. (2.1), we obtain the transfer function of acceleration to displacement in s-domain.

$$\frac{X(S)}{A_{in}(S)} = \frac{1}{s^2+s\frac{b}{m}+\frac{k}{m}} = \frac{1}{s^2+s\frac{\omega_n}{Q}+{\omega_n}^2} \tag{2.2}$$

The Q value is designed to affect the setting time for open-loop operation of the accelerometer. High Q could result in taking long settling time. Too small Q also leads to an over-damped system with long setting time. Q=0.5 is the value for fastest setting time. However, Q is design to be higher than 0.5 in one axial accelerometer due to process limitation, area, and mechanical noise.

With the first order approximation from Eq. (2.1), the equation of mechanical sensitivity could be simplified as

$$x = \frac{a_{in}}{{\omega_n}^2} \tag{2.3}$$

where $\omega_n$ is the natural frequency.

$$\omega_n = \sqrt{\frac{k}{m}} \tag{2.4}$$

Because the input frequency is much lower than the resonant frequency, the mechanical sensitivity of the accelerometer is given as

$$\frac{x}{a_{in}} = \frac{m}{k} = \frac{1}{{\omega_n}^2} \tag{2.5}$$

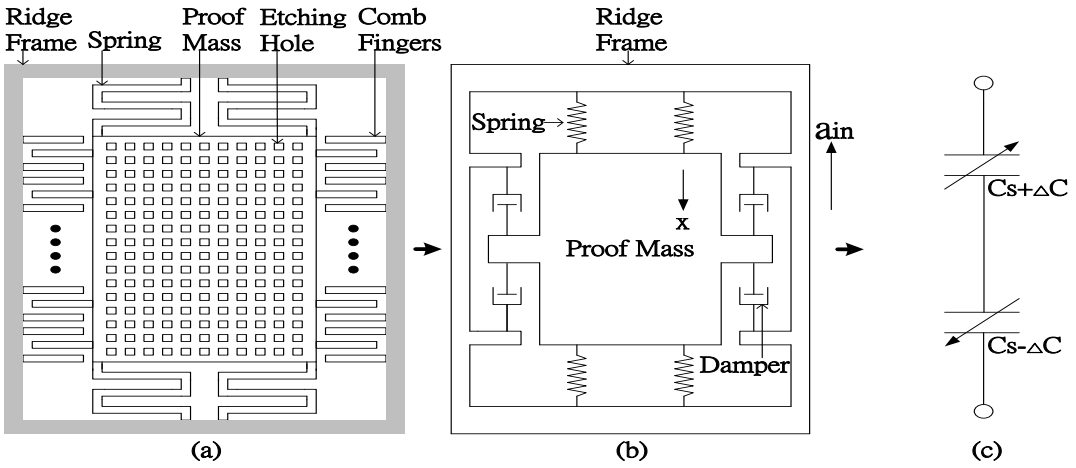



Figure 2.6: The accelerometer: (a) Notional layout view, (b) Mechanical parameter model, and (c) The schematic of the equivalent capacitors

## 2.2.2 Spring Constant

The folded-beam is used to measure the inertial force by the displacement value in the accelerometer as shown in Figure 2.7. Eq. (2.3) is the formula that the spring constant of the folded-beam in the sensing axis.

$$k = Et\left(\frac{w}{l}\right)^3 / N \tag{2.6}$$

where k, E, t, w, l, and N are spring constant, multilayer structure effective young's modulus of elasticity, thickness, the width and length of the beam, and the turns, respectively.

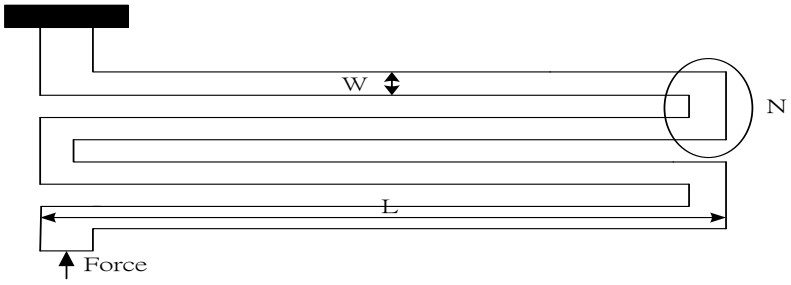



Figure 2.7: Folded-beam

### 2.2.3 Squeeze Film Damping

The squeeze film damping between the parallel-plate comb capacitor fingers in the out-of plane of the one axial accelerometer is the dominant damper [11], and its formula is given as

$$b = 7.2N_{gap}\mu l_{ov}\frac{t^3}{d^3} \tag{2.7}$$

where b, $N_{gap}$, μ, $l_{ov}$, t, d are damping coefficient, the number of air gaps, the viscosity of the air, the finger overlap, thickness, and the initial gap between a rotor and stator. The μ value is $1.85\text{x}10^{-6}$ $N \cdot s/m^2$ and the viscosity of the air under atmospheric pressure at the room temperature.

### 2.2.4 Brownian Noise

Mechanical noise which is also called Brownian noise is directly related to the damping coefficient b, and it is equivalent to an input-refer noise acceleration given as

$$\overline{a_n^2} = \frac{4k_BTb}{9.8^2m^2}\ {G^2}/{Hz} \tag{2.8}$$

where $k_B$ is the Boltzmann constant and equals to $1.381\text{x}10^{-23}$ $JK^{-1}$, T, m are the absolute temperature and mass, respectively.

## 2.3 Accelerometer Simulation

### 2.3.1 Microstructure Geometry Parameters

Based on the working principle, the accelerometer which consists of the proof mass, comb fingers, springs, and etching holes is designed as shown in Figure 2.8 by

MEMS+ [12]. MEMS+ is the sensor design tool and could create the physical behavior model (PBK) for co-simulation. The co-simulation part will be described in detail in Chapter 4. Process and material parameters of designed accelerometer are listed in Table 2.2. All of the parameters are at the condition of room temperature 293.15k. The parameter of permittivity is related to the value of sensing capacitance. The density of SiO2 and Al are related to oxide and metal layers, respectively. And they are also related to the weight of sensors. The designed geometry parameters of the accelerometer are listed in Table 2.3. The finger gaps of the accelerometer are design to be 4um in order to obey the minimum design rule. The size of etching hole is 6x6 $um^2$ and the ratio of metal width to hole with is 8: 6. According to Figure 2.5, the accelerometer is designed to suspend by the ratio in theory.

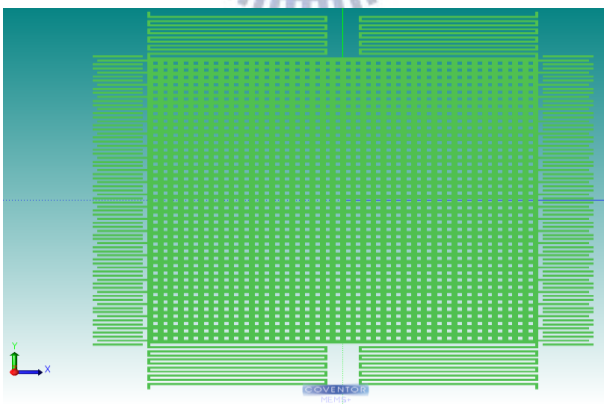


Figure 2.8: Physical behavior model of the one axial accelerometer

### 2.3.2 Accelerometer Simulation

The PBM is imported to Cadence environment using Spectre simulator and the performance results are simulated as shown in Figure 2.9 which shows the parts of the

Table 2.2: Process and material parameters of designed accelerometer

| Process and Material parameters | |
|---|---|
| Coefficients | TSMC |
| Temp(K) | 293.15 |
| Boltzmann(kb) | 1.381E-23 |
| Permittivity(Eox) | 8.854E-18 F/um |
| Young's modulus(SiO2) | 7.5E+10 |
| Young's modulus(Al) | 7.0E+10 |
| Structure thickness(t) | 10.49um |
| SiO2 density | 2.2E-15 kg/um$^3$ |
| Al density | 2.3E-15 kg/um$^3$ |
| Viscosity( $\mu$ ) | 1.85E-6 |

Table 2.3: Designed accelerometer geometry parameters

| | Value | Unit |
|---|---|---|
| Area | 793x815.2 | um$^2$ |
| Proof mass length | 564 | um |
| Proof mass width | 542 | um |
| Etching hole | 6x6 | um$^2$ |
| Metal width to hole width | 8:6 | |
| Finger width | 4 | um |
| Finger overlap length | 64 | um |
| Finger gap width | 4 | um |
| Spring length | 249 | um |
| Spring width parallel | 4 | um |
| Spring width perpendicular | 4 | um |
| Stator & Rotor finger length | 70 | um |
| Stator number | 24x2x2 | |
| Rotor number | 24x2 | |

performances. However, the damping coefficient from the squeeze film of the fingers is simulated by DampingMM analysis in CoventorWare [13]. Only a single overlapped region of the fingers is simulated for simplicity and the result is shown in Figure 2.10. The result of damping coefficient is multiplied by the total finger gap

numbers between rotors and stators to obtain the total damping coefficient. The sensor performances are summarized in Table 2.3.

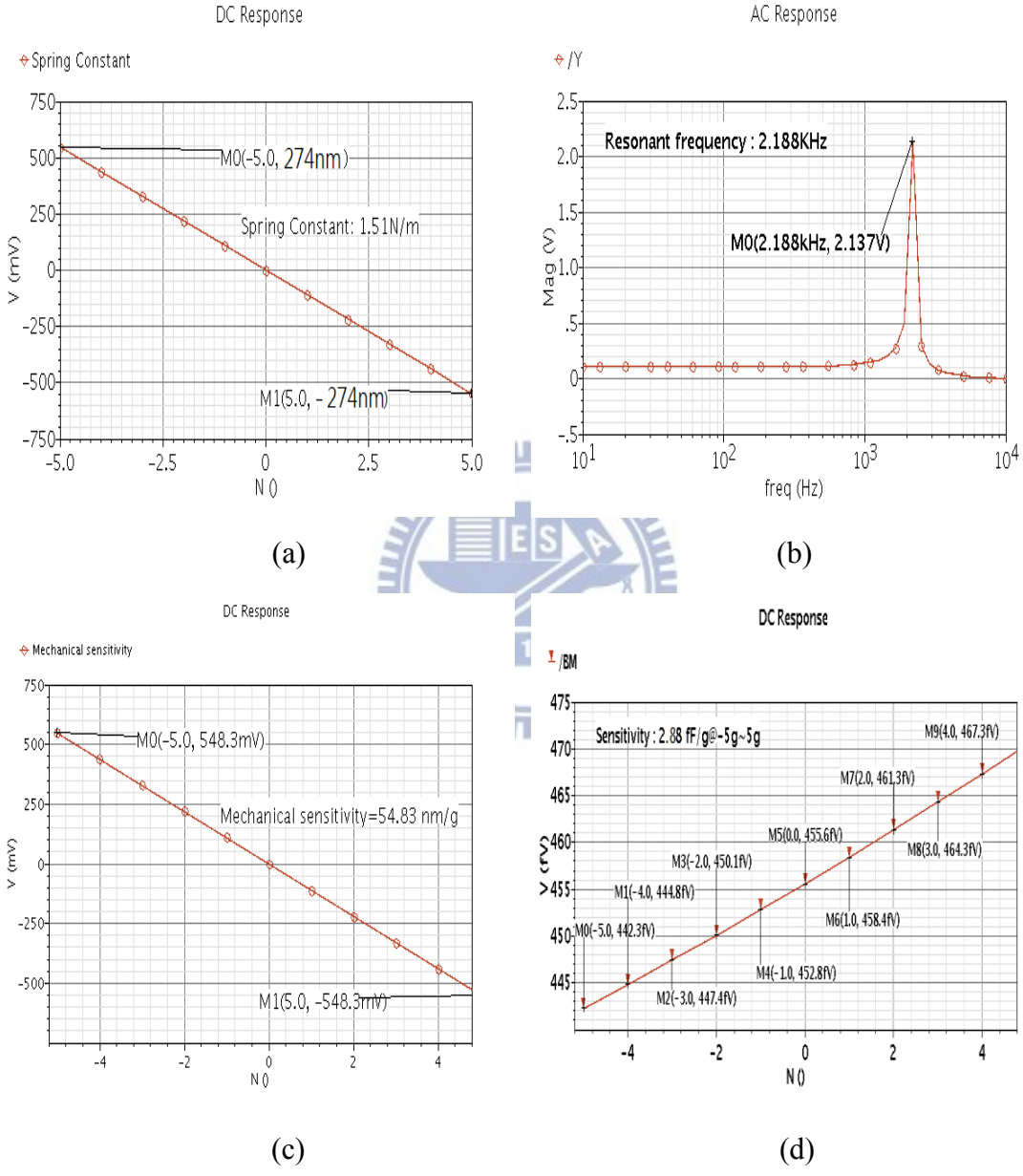



Figure 2.9: The simulation results of one axial accelerometer: (a) spring constant, (b) resonant frequency, (c) mechanical sensitivity, and (d) capacitance sensitivity

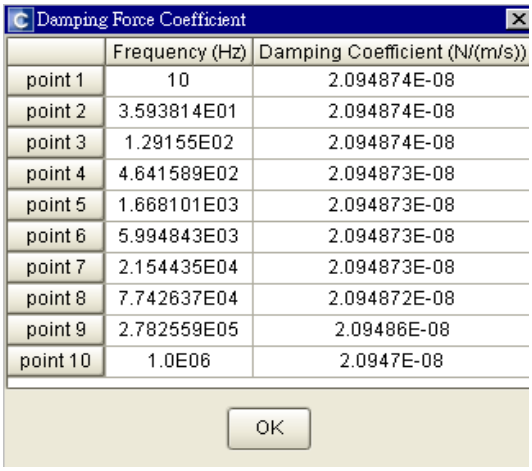



Figure 2.10: Damping coefficient by DampingMM analysis

Table 2.4: Designed accelerometer performances

| | Value | Unit |
|---|---|---|
| Mass | 8.44 | μg |
| Spring constant | 1.51 | N/m |
| Resonant frequency | 2.19 | KHz |
| Damping | 2.06E-6 | kg/s |
| Initial capacitance | 455.6 | fF |
| Mechanical sensitivity | 54.83 | nm/g |
| Capacitance sensitivity | 2.88 | fF/g |

## 2.4 Implementation of Accelerometer

The photos for the sensors implemented on CIC MEMS platform as shown in Figure 2.11 from T18-101B are obtained by focused ion beam (FIB) of the proof mass and etching hole. From Figure 2.11 (c), we can find that there is not excess sediment on the proof mass and the etching holes and it's clean. The phenomenon is related to the following statement. The photos as shown in Figure 2.12 from T18-101A

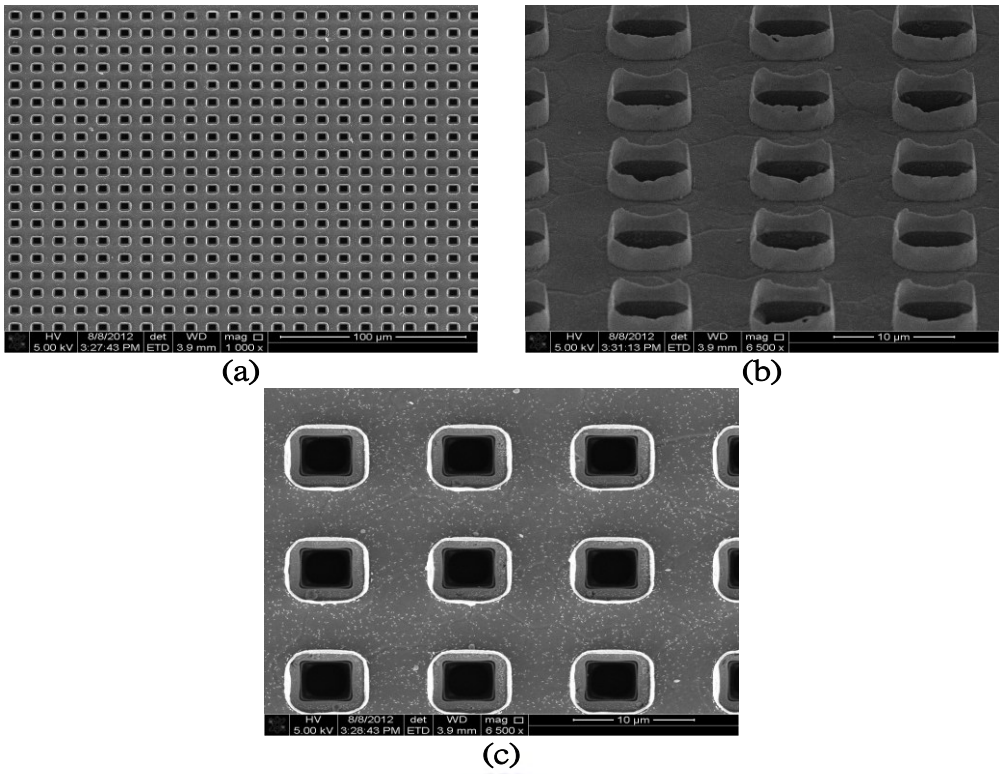



Figure 2.11: The FIB photos of proof mass: (a) the vertical view of a wide proof mass, (b) the oblique view of the etching holes, and (c) the vertical view of a small-scale proof mass

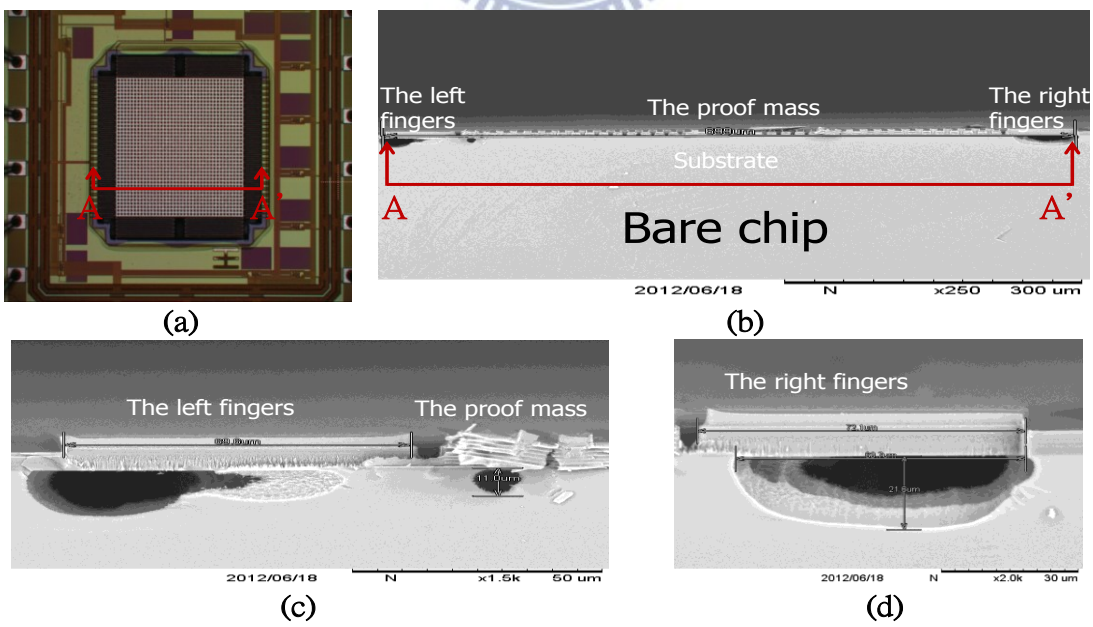



Figure 2.12: The SEM Photos of the chip from T18-101A: (a) the vertical view, (b) the horizontal view, (c) the left fingers, and (d) the right fingers

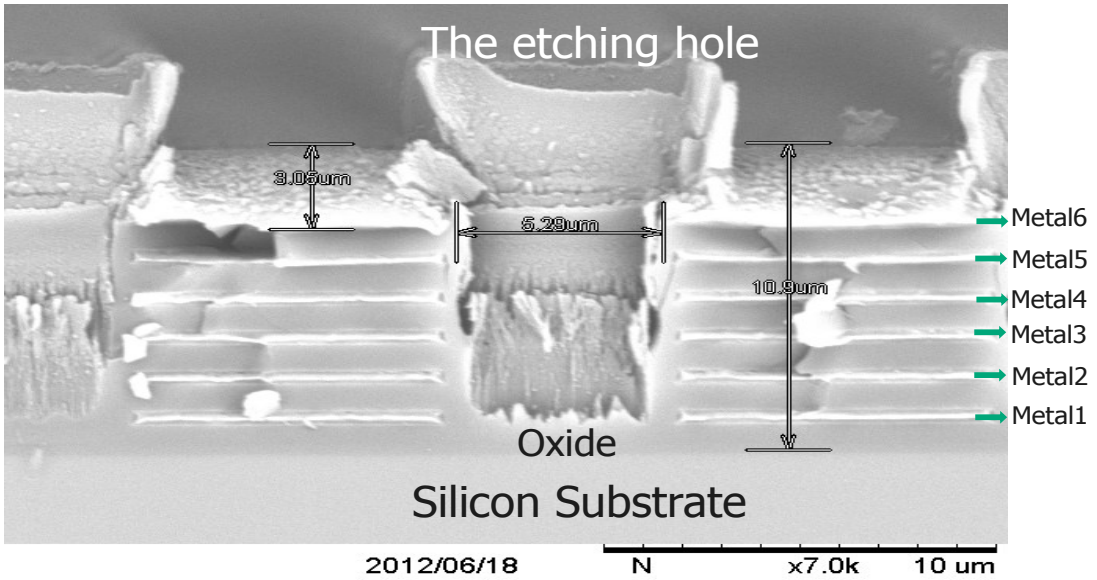



Figure 2.13: The first uncompleted step of DRIE in MEMS process from T18-101A

are obtained by scanning electron microscope (SEM) of the one axial accelerometer. The red-line AA' part of Figure 2.12 (a) from the vertical view is the same as Figure 2.12 (b) from the horizontal view. According to the photos, we could find that the parts of the left and right fingers are released by DRIE as shown in Figure 2.12 (c) and (d), respectively. But the substrate of the proof mass part is unreleased and it results in that the accelerometer is at the unsuspended situation. As shown in Figure 2.13, it shows that the first step of the MEMS process is not yet completed before the start of the second step and the residual oxide has not been etched. There are two possible reasons for the special phenomenon: One is that the size of RLS-mask is too small to make the unreleased structure and maybe there are other MEMS designed devices with different etching size longer than 6um on the same wafer and the etching concentration is adjusted for that design. However, based on Figure 2.5 and the row of

etching holes in Table 2.1, the width of RLS mask is 6um and the width could result in etching the structure 50um in the vertical direction. 50um is enough to etch the substrate part of the accelerometer, but the photos show that the accelerometer is still stuck. The other reason is that the mass structure which is equivalent to capacitances has been short to the ground plan of the circuits as shown in Figure 2.14 (a). The working principle of DRIE is to apply radio-frequency (RF) voltage to parallel capacitor plates to form a high voltage electric field in a chamber by a capacitive process [14]. An etching gas is fed into the electric field to ionize and ions react on the oxide layer to form the etching channel. But, based on CIC's comments, that ions are drained off to result in the first uncompleted anisotropic etching due to one of the two parallel capacitor plates connects with the ground of the circuits in the internal core only by Asia Pacific Microsystems (APM), the MEMS manufactory. The dies shown in Figure 2.15 and 2.16 are the evidences to support the comments. Figure 2.15 (a) and (b) on different dies of the same wafer fabricated by CIC are the photos by optical microscope (OM). The difference between them is the proof mass with more and less reflection. The reason is that if the proof mass is released by etching, the substrate is suspended and empty to let proof mass bending. Based on the bended proof mass, the focal distance on the proof mass is made with alterations to result in less reflection. Most of dies are like Figure 2.15 (a) on the wafer of T18-101B, and only a few of dies

are like Figure 2.15 (b) on the rim of T18-101B's

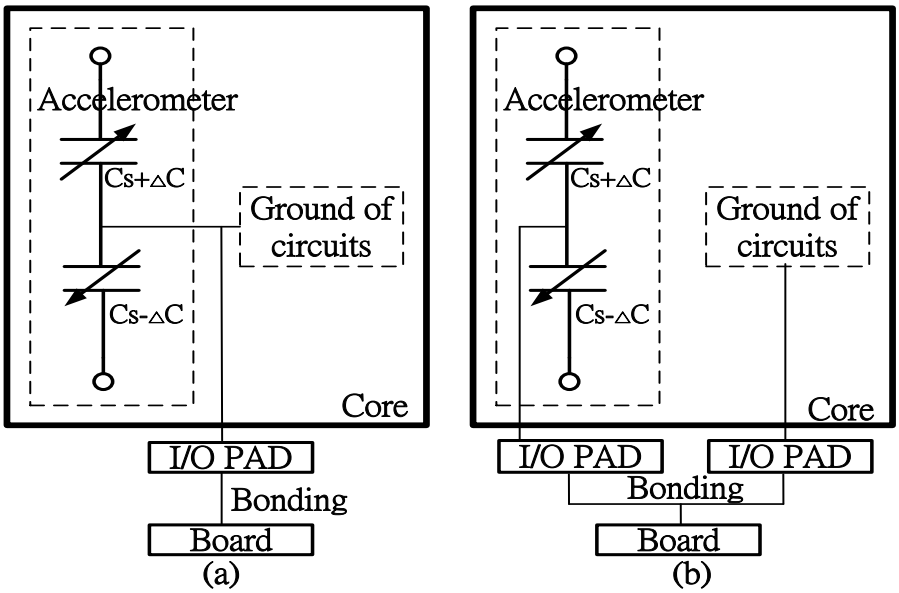
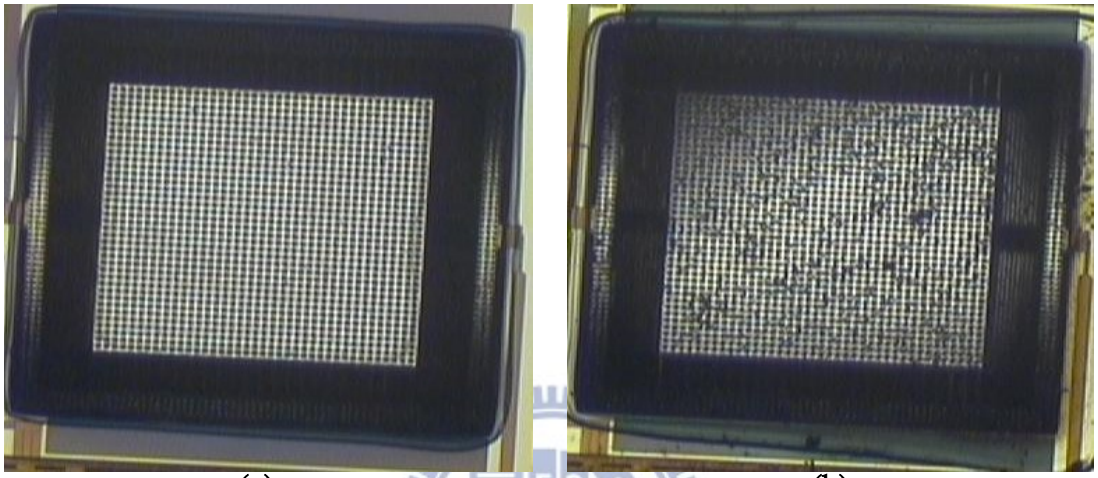



Figure 2.14: The accelerometer connects with the ground of the circuits: (a) internal connection by metal layers, and (b) external bonding

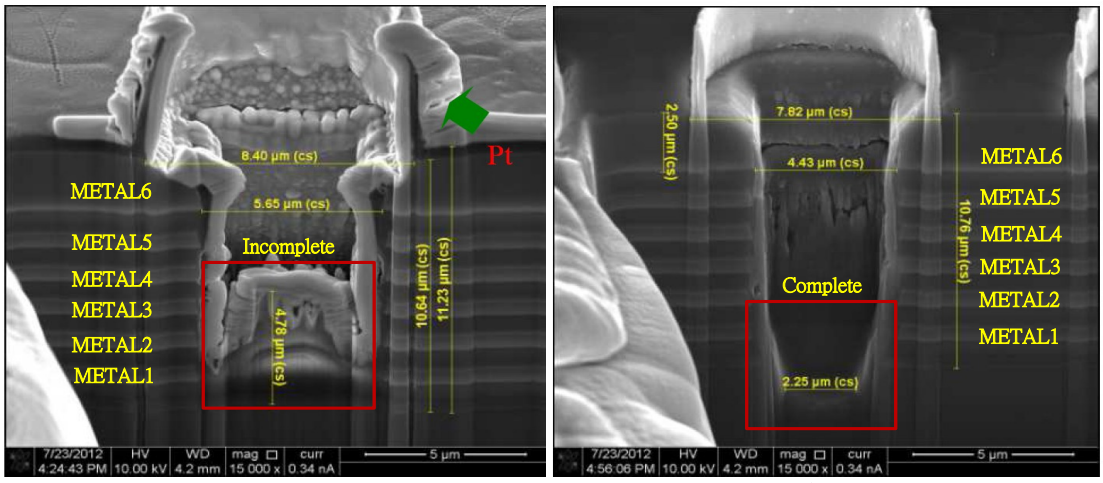
wafer. Figure 2.16 (a) and (b) are also on the same wafer from T18-101B and the etching hole of Figure 2.16 (a) is on the proof mass of Figure 2.15 (a). Figure 2.16 (b) is another accelerometer designed on the same wafer. The etching width of Figure 2.16 (a) and (b) are 6um and 5um of RLS-mask layout design, respectively. The etching width in Figure 2.16 (a) is bigger than Figure 2.16 (b) and they are both on the same wafer under the same recipe and etching time. The sedimentary phenomenon of Figure 2.11 (c) and Figure 2.16 (b) are cleaner compared with Figure 2.16 (a), and it infers that the anisotropic process has not been completed due to the ions catch charges to form the chemical sediments. The case of Figure 2.16 (a) should be finished on the first etching MEMS process, but it doesn't meet the specification of

this implementation. We have tested the special cases with and without connecting the ground of the circuits by MEMS process of APM. We think that the case is worthy to waiting for further investigation. The uncompleted etching phenomenon is also tested by CIC as shown in Figure 2.17 (a) and (b). They have tested that springs



(a) (b)

Figure 2.15: The OM Photos of the accelerometer from T18-101B: (a) the part of proof mass with more reflection, and (b) the part of proof mass with less reflection




(a) (b)

Figure 2.16: The FIB Photos of etching holes from T18-101B: (a) with 6um etching design width, and (b) with 5um etching design width

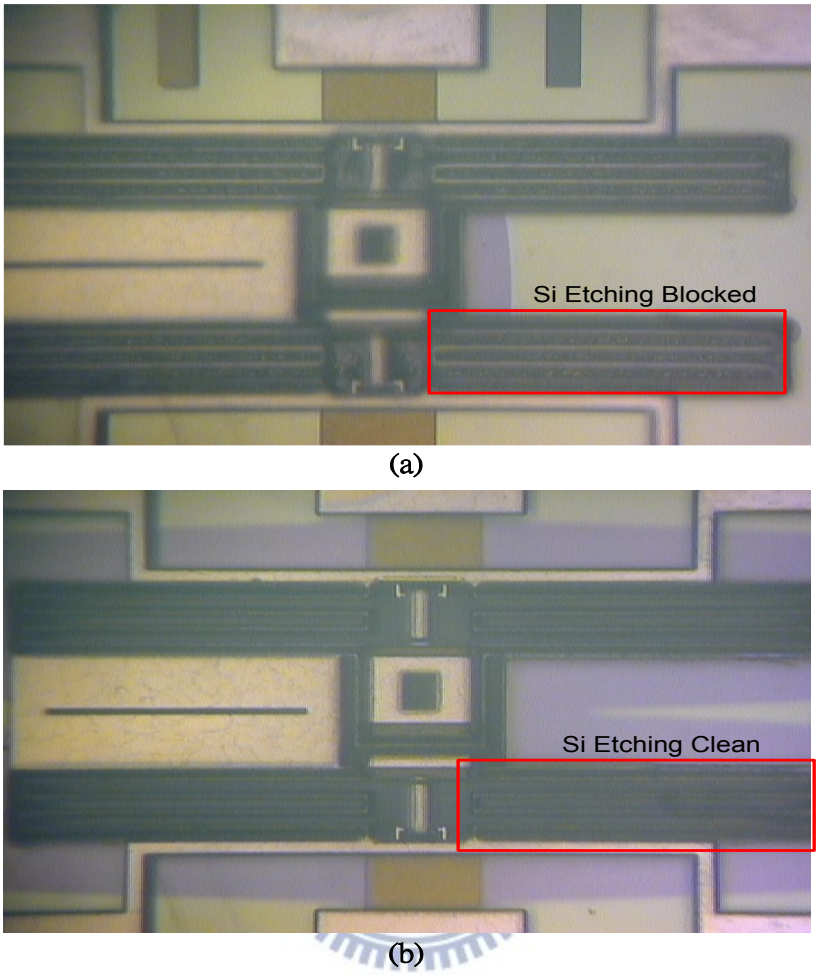
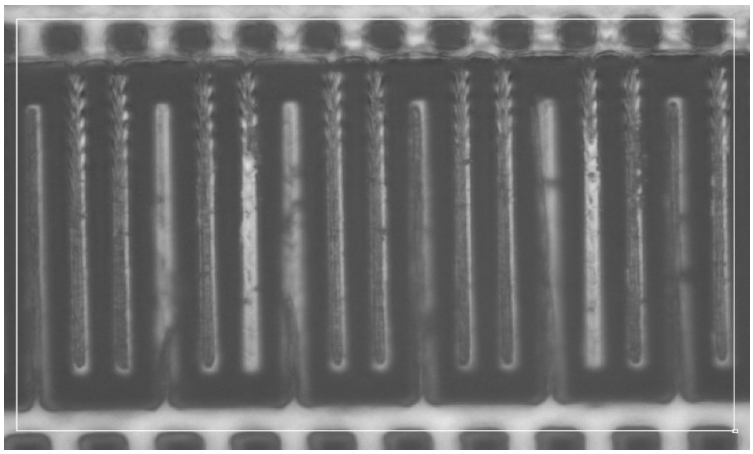



Figure 2.17: The spring test by CIC: (a) spring is short to P-substrate, and (b) spring is floating [10]

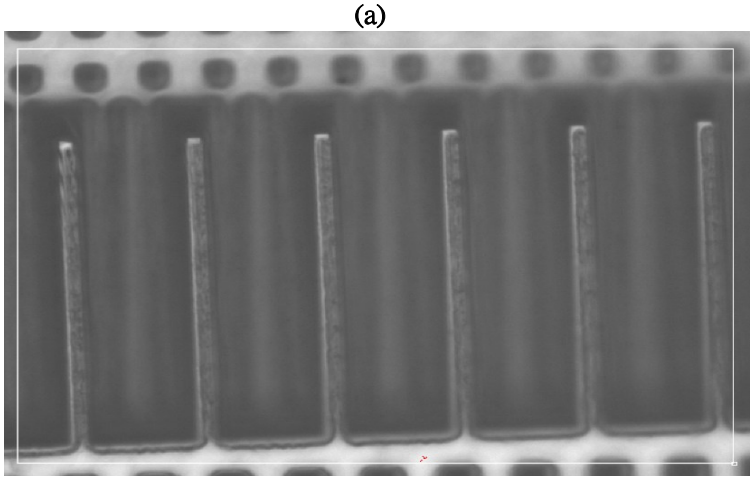
are short to the P-substrate of circuits and the floating status. Based on the conditions of the same wafer, the same MEMS process, the same circuits, and the size of the same structure, the results revealed that the reflection of Figure 2.17 (a) is more than Figure 2.17 (b). They both show that whether the silicon substrate is etched and clean or not under the rectangular boxes of figures.

## 2.5. Surface Topography Measurement

The sensor structure was implemented prior to the readout circuit, and surface topography measurement was carried out to manifest the sensor microstructure curling effect by using NewView 7300. The white light interferometer (WLI) is utilized to offer other evidence to proof whether the one axial accelerometer is released and suspended or not. The Figure 2.18 (a) and (b) are the unsuspended and suspended situations of the one axial accelerometer, respectively. Obviously, if the



(a)



(b)

Figure 2.18: The fingers of the one axial accelerometer: (a) the rotor and stator are at the same focal length, and (b) the rotor and stator are at different focal length

structure is unreleased and unsuspended, it must be at the flat situation and few curling phenomenon due to few residual stress. Therefore, the focal length between the rotor and stator fingers is almost the same such as Figure 2.18 (a) by WLI. On the other hand, if the sensor is released and suspended, it must be at the bending situation of proof mass. It results in that the fingers are in different benchmark due to more residual stress. Therefore, the focal length between the rotor and stator fingers is

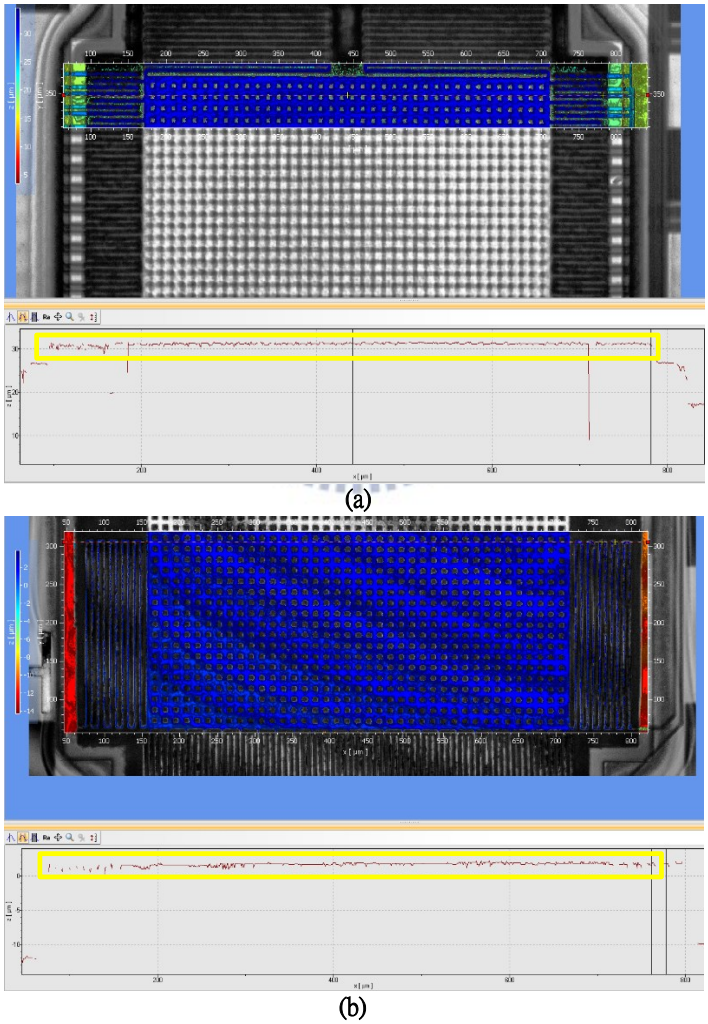



Figure 2.19: The curling measurement of the one axial accelerometer: (a) at proof mass and fingers, and (b) at proof mass and springs

different such as Figure 2.18 (b) by WLI. Another curling phenomenon of measurement about the accelerometer is shown in Figure 2.19 (a) and (b) by WLI of CIC. The instrument is focused on measuring the curling ratio between A and B under the same horizontal line. The measured chip is at the unreleased situation and we can find that the fingers, the springs, and proof mass are almost the same altitude from the line of the below window as shown in Figure 2.19 (a) and (b).

## 2.6 Proposed Troubleshooting Methods

There are two proposals for troubleshooting and one is that the RLS mask will be designed to a rectangle form as shown in Figure 2.20 (b) because the fingers has been etched from the observation of Figure 2.12 (c) and (d). The other is that the RLS mask will be designed to a large square in order to enlarge the released area as shown in Figure 2.20 (c) due to the etching selectivity, but it still gets risk of losing the thickness of metal microstructures used as hard mask.

The other problem is that the accelerometer of MEMS structure connects with the ground of the circuits. The proposed method is shown in Figure 2.14 (b) from the designer's view. We could make the ground of the accelerometer and circuits to connect to different I/O pads, and then the pads are bonded to the same pin on the measured board.

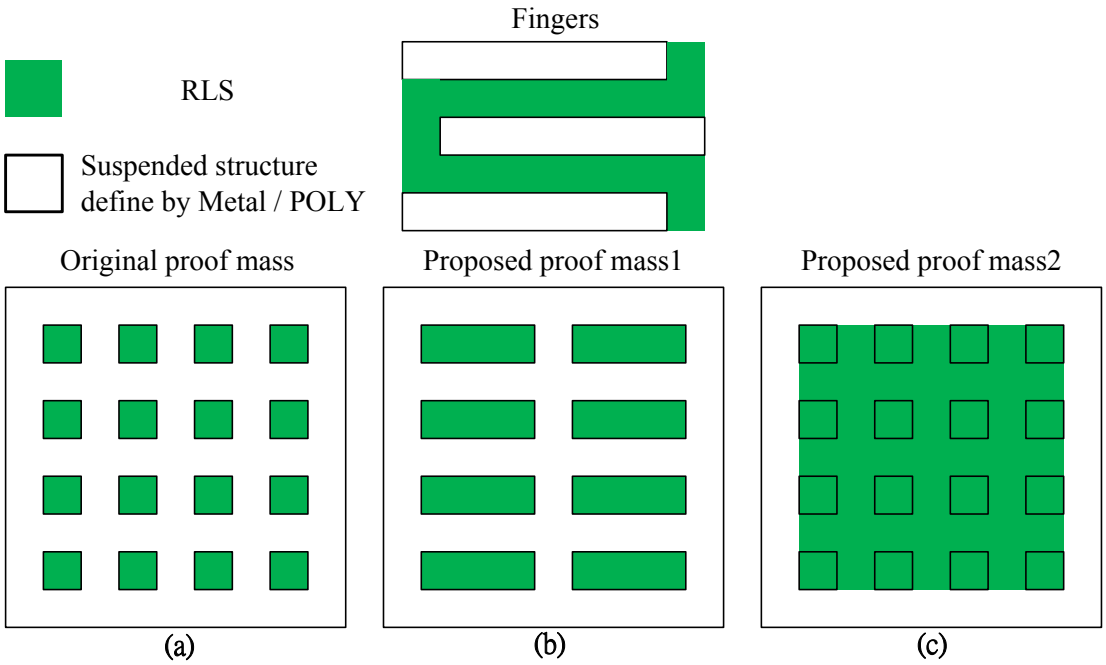



Figure 2.20: The proposed methods: (a) original design, (b) rectangle form of RLS mask, and (c) large area of RLS mask

# Chapter 3 Capacitance to Digital Circuit Design

In this chapter, the proposed capacitance to digital circuit design for the capacitance variation of the accelerometer will be described.

## 3.1 System Architecture

As shown in Figure 3.1 (a), the system architecture of this thesis is proposed. An external force drives the accelerometer to generate capacitance variation at the sensing range. The capacitance variation is fed into (capacitance to pulse-width) circuit for the pulse width as shown in Figure 3.1 (b). The counter counts pulse width up to bits number. It means that bits number such D0 to D8 is equivalent to the capacitance variation. Because it requires external and internal clocks, the clock generator are designed accordingly. The internal charging and reset clock is 1024 times bigger than the external sampling clock. The system specification is shown in Table 3.1. Input sensing range is designed for that one axial accelerometer could be operated in the range by a shaker.

Table 3.1: System specification

| | |
|---|---|
| Input sensing range | ±5g (10g) |
| Circuit voltage | 0V to 1.8V |
| Sampling rate | 50MHz |
| Sensitivity | 20 ns/bit |
| Chip size | 2 $mm^2$ |

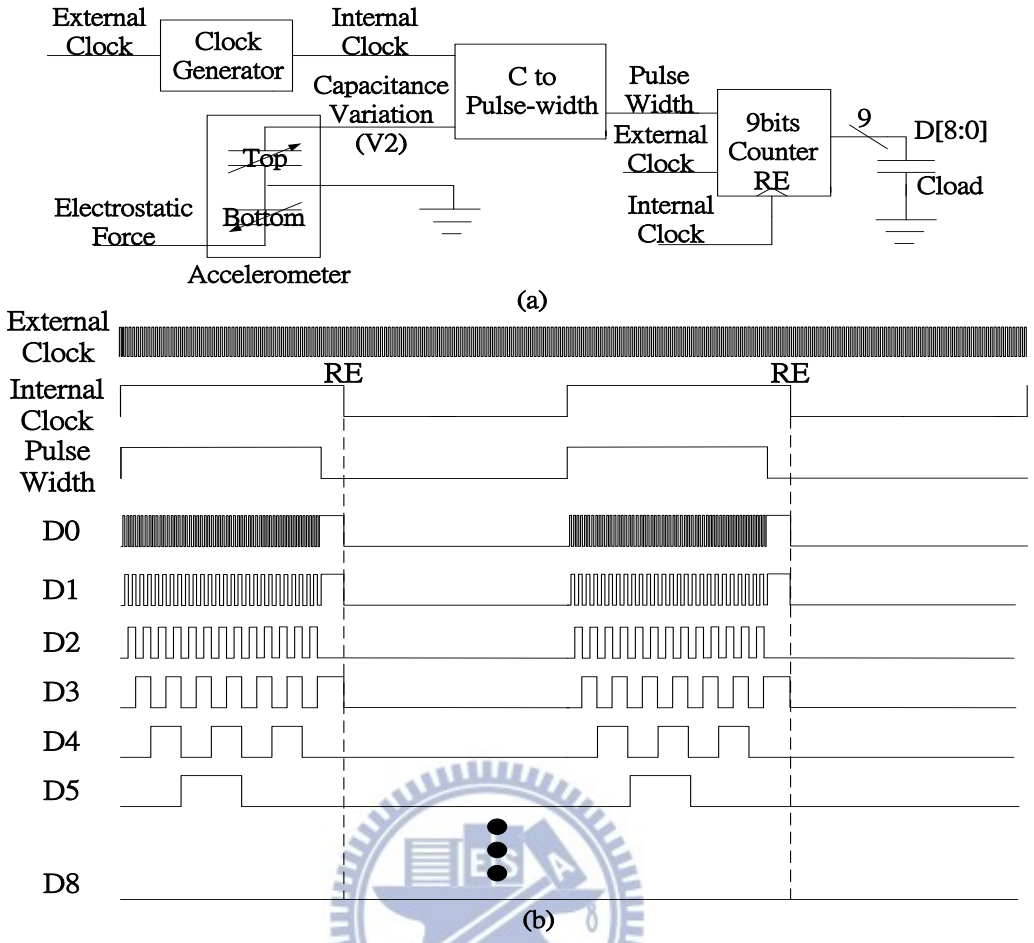



Figure 3.1: (a) The system architecture, and (b) The timing diagram

## 3.2 Capacitance to Pulse-Width Circuit Design

### 3.2.1 Capacitance to Pulse-Width

The C-to-PW circuit is shown in Figure 3.2 (a) and its timing diagram is shown in Figure 3.2 (b). The internal clock signal from the clock generator drives the circuit. The delay of the comparators [15] which does not impact the circuit response is neglected and considering both comparators have the same delay. When internal clock signal is high, Node $V_1$ and $V_2$ are used to be charged and discharged with RC time constant. The threshold of the comparator is set to 0.5 $V_{DD}$ in the design. When $V_2$

node is charged from 0V to $V_{charge}$, it triggers the digital comparator to generate the square-wave cycle signal at $O_2$ node. The XOR gate which operates as a phase detector to obtain of the pulse-width and catches the outputs of the digital comparators. To understand the sensing range of the readout design, we illustrate the exponential charging and discharging behavior of the capacitor. Defining $V_i$ the initial voltage, $V_f$ the final voltage and $\tau = RC$, the formulas at any time t are

$$V_{charge} = V_f \cdot (1 - e^{-t/\tau}) \tag{3.1}$$

$$V_{discharge} = V_i \cdot e^{-t/\tau} \tag{3.2}$$

Substituting $V_{charge} = \alpha V_{DD}$ and $V_f = V_{DD}$ where $\alpha$ is a constant smaller than 1 into (3.1) to solve for t, we get the pulse-width:

$$PulseWidth = t = RC \cdot \ln(\frac{1}{1-\alpha}) \tag{3.3}$$

Equation (3.3) shows that the output pulse-width is linearly proportional to the sensing capacitance. The capacitance is replaced by the one axial accelerometer. The range of the initial capacitance value is from 441.2fF to 470fF and the resistance is set to 10MΩ. The sensitivity of the C to T circuit is 6.94us/pF. When the clock signal is low, the inverter generates the reverse signal to trigger the discharging path and reset C-to-PW circuit. Therefore, $V_2$ node is discharged to 0V and it forms the period cycle. The simulation results of C-to-PW circuit are shown in Figure 3.3 from -5g to 5g with physical behavior model and every division at the sensing range is about

20ns.

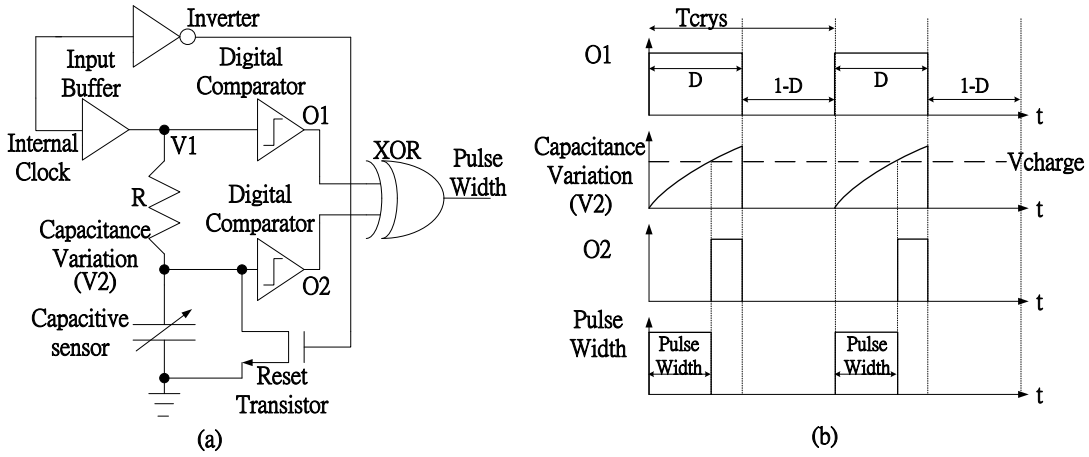



Figure 3.2: (a) C to Pulse-Width circuit, and (b) The timing diagram

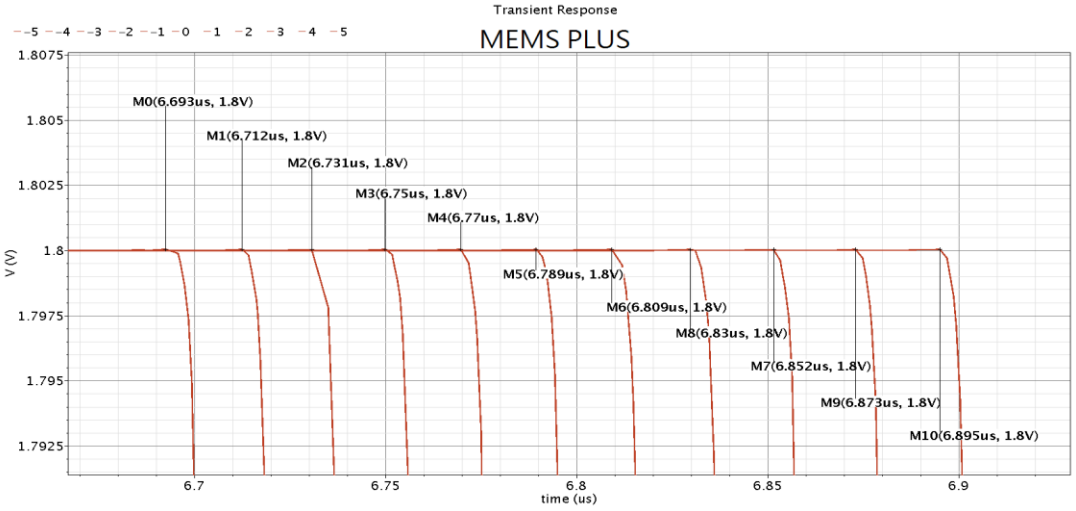



Figure 3.3: The Pulse-Width signal from -5g to 5g

## 3.2.2 Sub Circuit Design

The simple digital inverters are used to be comparators which present slew rate, but it's not limited by the supply current and consumes low power. However, due to temperature variations and the process, traditional inverter-based comparators suffer from comparator threshold voltage deviations. To overcome the issue, a self-tuning inverter-comparator based is designed. The schematic of the comparator is shown in

Figure 3.4. The digital comparator is designed to be single input single output. The master part of the comparator is used to define the threshold voltage, and the slave part is used to implement the comparator operation. Resistors R9 and R10 form a resistive divider that set the master threshold voltage Vmstr is designed to generate the comparison value. According to the comparison, it generates a digital output Vout.

As shown in Figure 3.5, they are the inverter, the XOR gate, and the buffer, respectively. Consideration for the mobility between an electron and a hole, the three sub circuits are designed that the width ratio of PMOS and NMOS is 3:1.

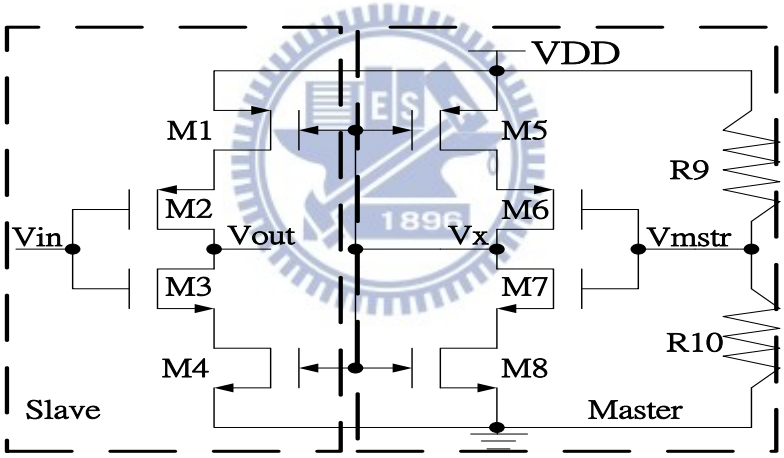



Figure 3.4: Self-tuning inverter-comparator

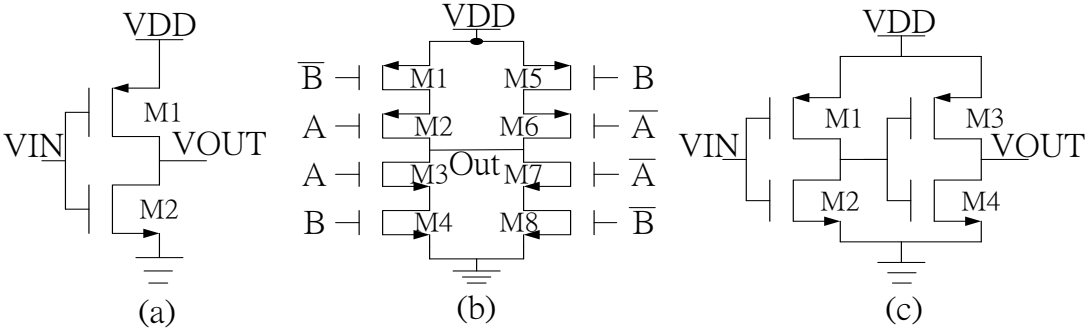



Figure 3.5: (a) Inverter, (b) XOR gate, and (c) Buffer

### 3.2.3 The Maximum Value of Capacitance

Introduction to the maximum value of capacitance, it is related to C-to-PW circuit of duty cycle. The optimum duty cycle value is calculated by the intersection of two relations. When C-to-PW circuit is at the situation of RC charging, the first relation is given as from (3.3)

$$C_{max} = \frac{D \cdot T_{crys}}{R \cdot \ln 2} \tag{3.5}$$

where $C_{max}$, D, and $T_{crys}$ are the maximum of capacitance value, duty cycle, and one period of clock, respectively. When C-to-PW circuit is at the situation of RC discharging, the $r_{on}$ is designed to satisfy the relation (3.6).

$$5(r_{on} \parallel R) \cdot C < (1 - D) \cdot T_{crys} \tag{3.6}$$

where $r_{on}$ is the discharging resistance. Multiplication by 5 to ensure the circuit to be discharged up to steady state. Therefore, here is the second relation given as

$$C_{max} = \frac{(1-D) \cdot T_{crys}}{5 \cdot (r_{on} \parallel R)} \tag{3.7}$$

The intersection of two relations, (3.5) and (3.7) is shown in Figure 3.6 where $D_{opt}$, f1(D), and f2(D) are the optimum of duty cycle, (3.5), and (3.7), respectively.

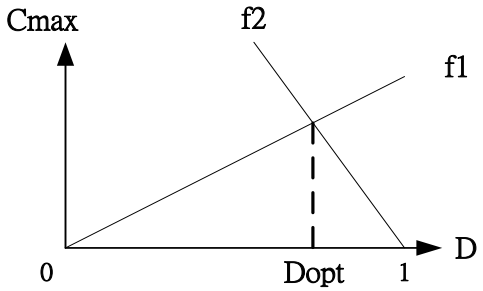



Figure 3.6: The optimum design of duty cycle

## 3.3 Counter Circuit Design

In order to readout the capacitance variation from C-to-PW circuit, the counter is designed to be reset to zero in the beginning of every period. The input node of D-flip-flop is designed to add one AND gate to control the reset path in order that every period is independent of others [16]. To ensure that the counter will be reset, the period signal which controls the reset node is also designed to be the same as the charging and discharging time signal of C-to-PW circuit. As shown in Figure 3.7, the counter consists of D-flip-flop, AND gate, and XOR gate. As shown in Figure 3.8 (a), the input node of d flip flop is designed to add one AND gate to control D-flip-flop by RE node due to the counter needs the reset function. Therefore, the counter is ensured to be reset. As shown in Figure 3.8 (b), the d flip flop has the reset function and its waveform is illustrated. When RE node is at high situation, the positive clock signal triggers D-flip-flop to catch D value and then generate Q value. When RE node is at low situation, Q value is zero regardless of D-flip-flop is triggered by the positive clock signal.

To minimize power consumption, all of the logic gates are designed by using fully complementary logic. Its mutually exclusive pull-up, pull-down networks and rail-to-rail voltage swing provide many advantages such as low-power, high slew-rate, and robustness against environment noise.

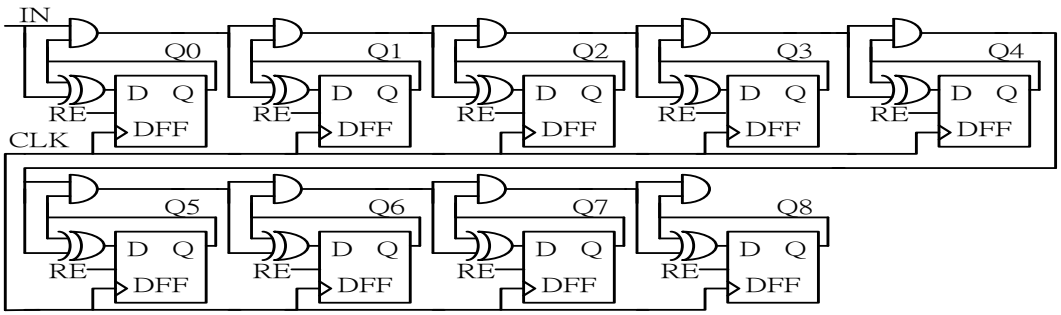



Figure 3.7: The 9 bits counter

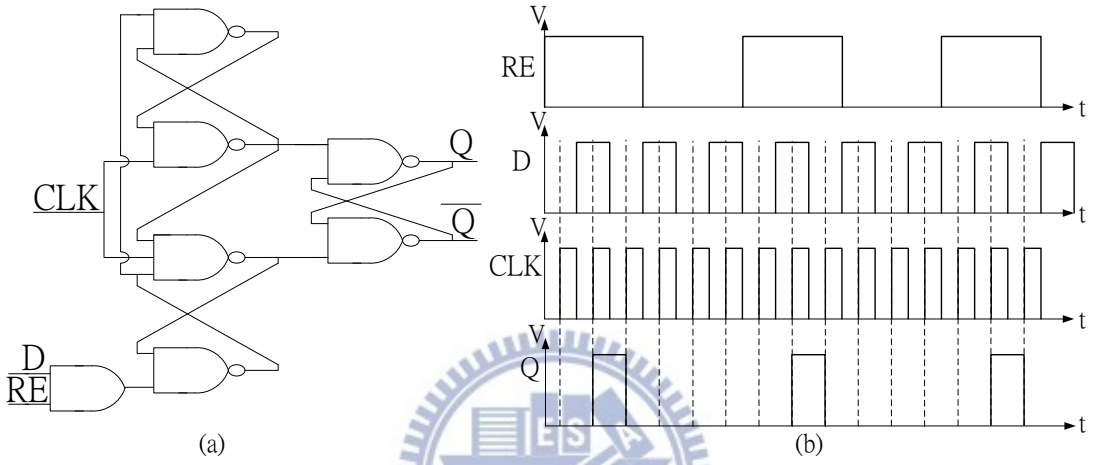



Figure 3.8: (a) D-flip-flop with reset, and (b) The timing diagram of d-flip-flop

## 3.4 Clock Generator Circuit Design

The C-to-PW circuit and the counter both need the clock signal, but they need different clock frequency signals. In order to input just one clock signal and make the relation between the two circuits of the trigger signals. The external sampling signal is 20ns and duty cycle 50%. By the clock generator, the internal period signal is enlarged to 20.48us and duty cycle 50%. The enlarged internal signal could provide the time for RC charging and discharging. The clock generator circuit is composed of ten D-flip-flops as shown in Figure 3.9 (b). The D-flip-flop is triggered by the positive edge external signal and its waveform of simulation result is shown in Figure 3.10.

The result shows that it is 20.48us one period, 50% duty cycle and delays 100ns in the beginning of every period because the input simulaiton clock signal is set 100ns delay.

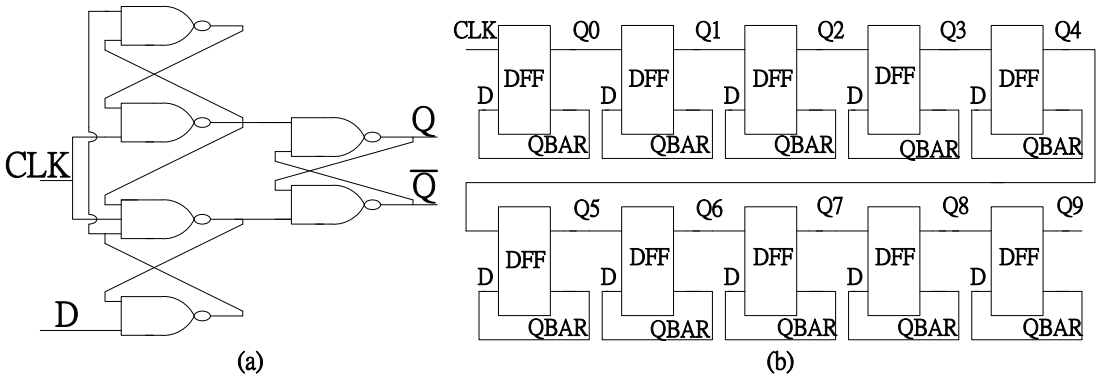



Figure 3.9: (a) D-flip-flop, and (b) The clock generator

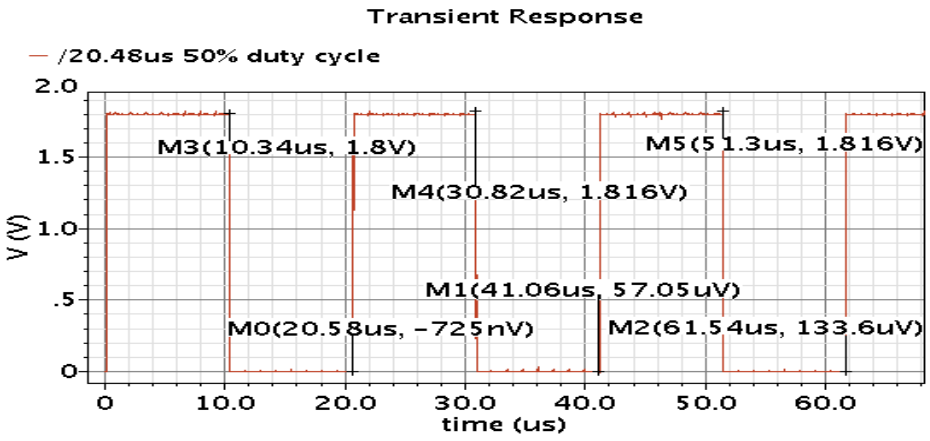



Figure 3.10: The generated clock signal of simulation result

## 3.5 ESD Protection

To reduce the opportunity of IC failure by electrostatic discharge (ESD), the ESD protection circuit provided by STC I/O PAD is utilized to guarantee the low impedance ESD path between any I/O pads of the chip. As shown in Figure 3.11, I/O ports are protected by NMOS and PMOS with gates connected to ground and power supply respectively [17]. In normal operation, there is no leakage current since the

transistors are turned off by power rail. However, when the circuits are under ESD, forward biased parasitic diodes with RC triggered power rail ESD clamp circuit provide low impedance ESD current paths.

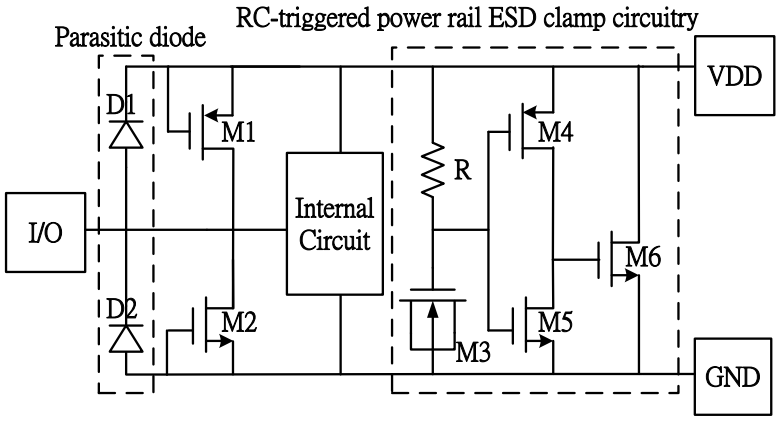



Figure 3.11: The circuit design of ESD protection

# Chapter 4 MEMS and ASIC Co-Simulation

In this section, we explore the model for co-simulation and monolithic circuits with one axial accelerometer of simulation results. It's so important that the computer aided design flow for MEMS and IC integration is used to co-simulate. The difficulty is that the multi-layer structure of CMOS MEMS sensors are either modeled with highly simplified lumped-mass models, or simulated by accurate, but very time-consuming, finite element analysis (FEA). Therefore, a newly proposed approach provides the accuracy of FEA and connection with circuits for co-simulation by MEMS+ with parametric computation to save computational time.

## 4.1 The Introduction of MEMS+

### 4.1.1 The Flow of MEMS and ASIC Co-Simulation

In order to reach high integration of integrated circuits with sensors, the relations between simulation and measurement results must be highly accurate. As shown in Figure 4.1, the design flow for MEMS design and co-simulation is illustrated and the tool is divided into four parts, material data base, process editor, innovator, and MEMS+ scene 3D. Material data base and process editor are the same as the parts on CoventorWare. We set material parameters and process on material data base and process editor, respectively. Like the library of circuit design, the component library of MEMS+ such as rigid plate and suspensions is used to construct the sensors in

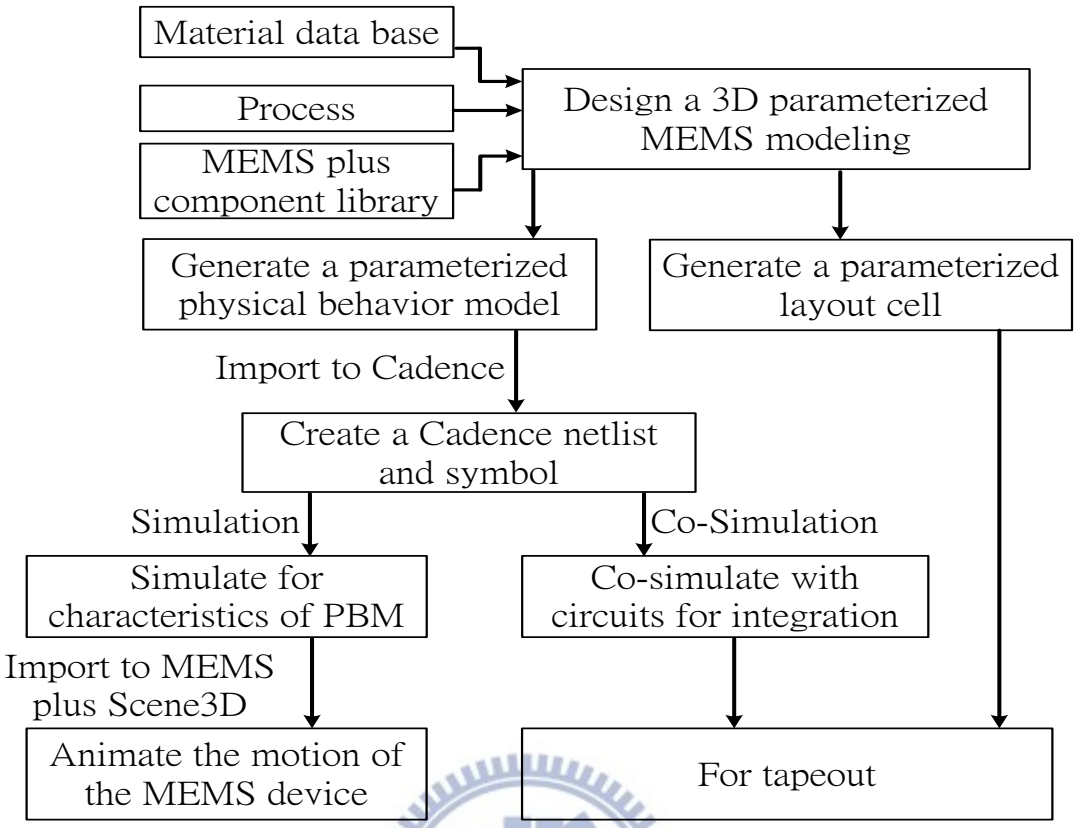



Figure 4.1: The flow of co-simulation

innovator. Contrast with finite element analysis by CoventorWare, MEMS+ generates the physical behavior model (PBM) more quickly and easily and it is absolutely designed for co-simulation with IC design. The PBM generated from MEMS+ is imported to Cadence and then it generates a Cadence netlist and symbol for sensor performances such as resonant frequency and mechanical sensitivity. After simulating for characteristics of PBM at DC and AC analyses, the results could be imported back to MEMS+ for animating the sensors. The PBM symbol is used to connect with circuits for co-simulation. The parameters of the symbol could be set as variables and its values could be changed before co-simulation. The voltage values in Cadence are

used to on behalf of the mechanical force. According to the final co-simulation results, the final integration system is determined to be worthy to implement it.

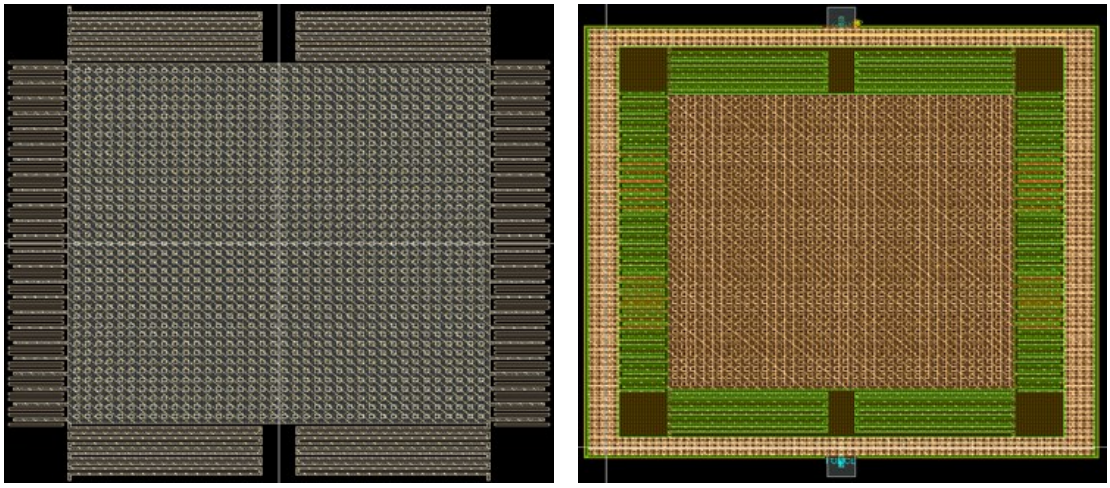
### 4.1.2 Auto-Generated Layout of One Axial Accelerometer

Comparing with the artificial layout of the accelerometer by layout tool such as Virtuoso and Laker, the auto-generated layout is error-free as long as ensuring each component connecting others on MEMS+. In order to produce the auto-generated layout, the gds numbers of layers need to be set in the process editor window on MEMS+ as shown in Figure 4.2. The auto-generated layout from Metal1 to Metal6 layers is shown in Figure 4.3 (a) compared with Figure 2.8. Assisted by other layout tool, the auto-generated layout is added to other layers for MEMS process as shown in Figure 4.3 (b).

ProcessEditor | Innovator

| Name | Layer Name | Material Name | Material Color | Thickness | Mask Name | Photoresist | Mask Offset | Sidewall Angle | Wafer Side | Gds Number |
|---|---|---|---|---|---|---|---|---|---|---|
| Substrate | Substrate | Silicon | | 400 | L3D0 | | | | | |
| Planar Fill1 | FieldOxide | Oxide | | 0.35 | | | | | Front | |
| *Planar Fill2* | *Poly1* | *Polysilicon* | | *0.2* | | | | | *Front* | |
| *Straight Cut1* | | | | | *PO1* | *Positive* | *0* | *0* | *Front* | *41* |
| *Planar Fill3* | *ILD2* | *Oxide* | | *0.55* | | | | | *Front* | |
| Planar Fill4 | METAL1 | Aluminum | | 0.53 | | | | | Front | |
| Straight Cut2 | | | | | METAL1 | Positive | 0 | 0 | Front | 16 |
| Planar Fill5 | IMD1 | Oxide | | 0.85 | | | | | Front | |
| Planar Fill6 | METAL2 | Aluminum | | 0.53 | | | | | Front | |
| Straight Cut3 | | | | | METAL2 | Positive | 0 | 0 | Front | 18 |
| Planar Fill7 | IMD2 | Oxide | | 0.85 | | | | | Front | |
| Planar Fill8 | METAL3 | Aluminum | | 0.53 | | | | | Front | |
| Straight Cut4 | | | | | METAL3 | Positive | 0 | 0 | Front | 28 |
| Planar Fill9 | IMD3 | Oxide | | 0.85 | | | | | Front | |
| Planar Fill10 | METAL4 | Aluminum | | 0.53 | | | | | Front | |
| Straight Cut5 | | | | | METAL4 | Positive | 0 | 0 | Front | 31 |
| Planar Fill11 | IMD4 | Oxide | | 0.85 | | | | | Front | |
| Planar Fill12 | METAL5 | Aluminum | | 0.53 | | | | | Front | |
| Straight Cut6 | | | | | METAL5 | Positive | 0 | 0 | Front | 33 |
| Planar Fill13 | IMD5 | Oxide | | 1 | | | | | Front | |
| Planar Fill14 | METAL6 | Aluminum | | 2.34 | | | | | Front | |
| Straight Cut7 | | | | | METAL6 | Positive | 0 | 0 | Front | 38 |
| Straight Cut8 | | | | | HM | Positive | 0 | 0 | Front | 24 |
| Straight Cut9 | | | | | RLS | Negative | 0 | 0 | Front | 114 |

Figure 4.2: The process editor window



(a) (b)

Figure 4.3: (a) The auto-generated layout of the accelerometer, and (b) Adding RLS and PAD layers to the auto-generated layout

## 4.2 Co-Simulation Model

Three co-simulation models of MEMS sensors will be described in this section. Two of them are generated from VerilogA in Cadence. The other is generated from MEMS+ and imported to Cadence.

### 4.2.1 Co-Simulation with Lumped-Parameter Macro Model

According to the second order motion equation of (2.1), the principle of co-simulation models is the equivalent relationship between mechanical structures and circuits. The equation (2.1) is equivalent to

$$L\frac{d^2q}{d^2t} + R\frac{dq}{dt} + \frac{1}{C}q = V \tag{4.1}$$

where L, R, C, q, and V are inductance, resistance, capacitance, coulomb and voltage, respectively. The following simplifications listed in Table 4.1 are used to get the lumped-parameter macro-model of the accelerometer through the second-order

motion equation. As shown in Figure 4.4 (a), the proof mass m is equal to L, the damping coefficient b is equal to R, and the spring constant k is equal to 1/C. Others such as g1, g2, and g3 are used for co-simulation. Cs and d are the initial capacitance value and the distance of gap between a stator and a rotor, respectively. The equivalent capacitors of equations are given as

$$\mathrm{Cupe} = \frac{\mathrm{Cs}*\mathrm{d}}{\mathrm{d}-\Delta\mathrm{d}} = \frac{\mathrm{Cs}}{1-g_3*\mathrm{Vs}} \tag{4.2}$$

$$\mathrm{Cdne} = \frac{\mathrm{Cs}*\mathrm{d}}{\mathrm{d}+\Delta\mathrm{d}} = \frac{\mathrm{Cs}}{1+g_3*\mathrm{Vs}} \tag{4.3}$$

where Cupe and Cdne are the macro model symbol of the top and bottom capacitance plates, respectively. Vs is the force in the voltage form of Cadence. The equivalent capacitors in the circuit form shown in Figure 4.4 (b) are connect to the C to T circuit for RC charging and discharging. The principle of the equivalent capacitor is simplified to first order only by the displacement of the variation ($\Delta$d) from Hooke's law. Therefore, the simplified accelerometer model of the simulation time is faster than the PBM, but the available data are fewer than the PBM.

Table 4.1: Mechanical parameters transfer to electronic parameters

| Mechanical | Electrical | Value |
|---|---|---|
| m | L | 8.44e-9 |
| b | R | 2.06e-6 |
| 1/k | C | 0.68 |
| g1 | 9.8*m | 8.271e-8 |
| g2 | Cs/2d | 5.695e-8 |
| g3 | C/d | 1.7e+5 |

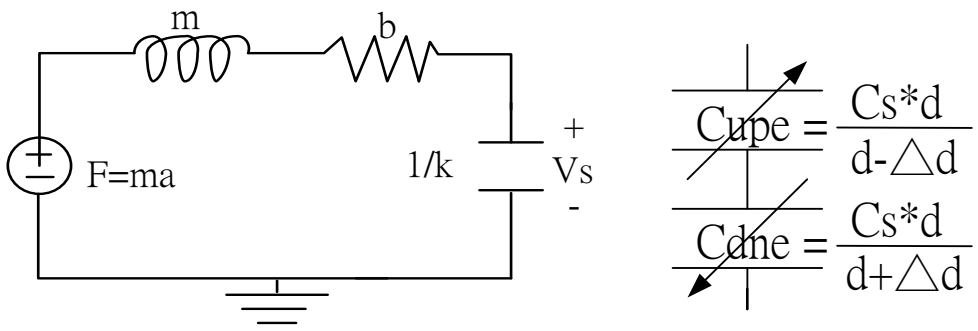



Figure 4.4: (a) Equivalent lumped-parameter macro-model circuit of the accelerometer, and (b) The equivalent capacitors of the macro model

### 4.2.2 Co-Simulation with Linear Model

Another co-simulation model with the linear characteristic is designed in VerilogA form. In order to know what the PBM is, the linear model is generated to make sure that if it is similar to PBM or lumped-parameter macro-model in the part of the sensing capacitance. The capacitance value of the equivalent Cupl and Cdnl are proportional to the sensitivity of the accelerometer as shown in Figure 4.5. The Cupl and Cdnl of the equations are given as

$$\mathrm{Cupl} = \mathrm{Cs} + \mathrm{sen} * \mathrm{V} \tag{4.4}$$

$$\mathrm{Cdnl} = \mathrm{Cs} - \mathrm{sen} * \mathrm{V} \tag{4.5}$$

The sen and V are the capacitance sensitivity of the accelerometer and the force in the voltage form of circuit, respectively. One volt is used to simulate one gravity in the two VerilogA models, lumped-parameter macro model and linear model. These are the same parameters in Table 5.1 for the linear model except the equivalent capacitors, the variation of the displacement and the linearity.

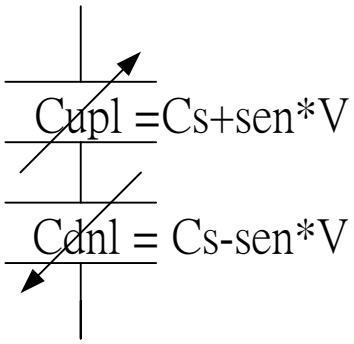



Figure 4.5: The equivalent capacitors of the linear model

### 4.2.3 Co-Simulation with Physical Behavior Model

The MEMS+ generates the PBM symbol for co-simulation in Cadence as shown in Figure 4.6. The sensors are designed from MEMS+ component library such as rigid plates and suspensions by MEMS+ and the feature is that the width and length of components could be parameterized. The parameterized sensors are imported to Cadence which creates physical behavior model (PBM) for mechanical characteristics and co-simulation. The mechanical characteristics of the accelerometer about Table 2.3 are simulated in Cadence design environment using Spectre simulator. The model is divided into two parts, input and output nodes. Acceleration and angular velocity of stimulating sources in circuits form as shown in Table 4.2 could drive sensor models in the circuit simulation platform. Variables at the input node signify that the length and width of sensors could be changed before running the simulation. The function of electrical connectors is used to connect to circuits such as C to V or pre-amplifier to simulate the action of capacitances for co-simulation. The mechanical features of

sensors as shown in Table 4.3 are simulated from mechanical connectors. Initial capacitance and capacitance sensitivity between any two capacitor plates are simulated from the output node of capacitance.

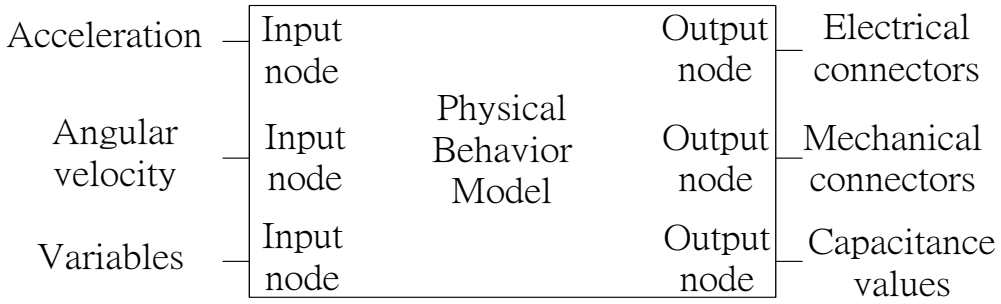



Figure 4.6: The symbol of physical behavior model

Table 4.2: Input node of PBM

| Input | Unit Scale Factor |
|---|---|
| Acceleration | 1 m/s^2=1e-6 V |
| Angular velocity | 1 rad=1e-4 m<br>1 m/s=1e-2 V<br>1 rad/s=1e-6 V |
| Variables | Constant |

Table 4.3: Output node of PBM

| Output | Feature |
|---|---|
| Electrical Connectors | For connecting to circuits |
| Mechanical Connectors | Displacement、Resonant frequency、Rotation |
| Capacitance Values | Initial capacitance、Sensitivity |

### 4.2.4 Comparison

In this section, the above-mentioned co-simulation models will be compared at the situation which C to D circuits are connected. The sensor structure is simulated by

finite element analysis (FEA) to obtain the sensor characteristics and fed parameters into simplified macro model and linear model on MEMS designs. Based on connecting with capacitance to pulse-width circuit in the simulation time part, the macro model and linear model are the second order due to equation (4.1), and simulation time of PBM is longer than the other two. Then 9bits counter is added to pulse-width circuit to form C-to-D circuit and the simulation time of PBM is still longer than the other two. The simulation time between lumped-parameter macro model and linear model is almost the same due to the only dissimilarity in equivalent sensing capacitance model. According to the two row results of the simulation time, the situation of PBM with more circuits will take more simulation time than the two others. And the difference of the relative time with adding more circuits will be longer. In the available data part, macro model and linear model are only used to show the results of equivalent sensing capacitance on Cadence, but PBM is used to both present the results of equivalent sensing capacitance and mechanical features like Table 4.3. PBM is like a block box that we don't know its principle. Therefore, based on the co-simulation with capacitance to pulse-width circuit at -5g to 5g and transient analysis in the simulation result part, Figure 4.7 is showed that PBM is similar to the linear model in the part of equivalent sensing capacitance with circuit. The pulse-width steps of macro model in simulation result are bigger than the linear model

and PBM, and it will result in that the sampling rate and power consumption are smaller than the others. Due to the aided design and co-simulation of MEMS+, we use PBM to finish the design. However, the three models are still compared with the measurement results.

Table 4.4: The comparisons of three co-simulation models

| | Lumped-Parameter Macro Model | Linear model | PBM |
|---|---|---|---|
| Simulation time (Connecting with pulse-width circuit) | 1.015 (Unit: second/period) | 0.961 | 12.9 |
| Simulation time (Connecting with C-to-D circuit) | 773 (Unit: second/period) | 769 | 3600 |
| Available data | Sensing capacitance | sensing capacitance | Showed in Table 4.3 |
| Simulation result | Green triangle in Figure 4.7 | Red square in Figure 4.7 | Blue diamond in Figure 4.7 |

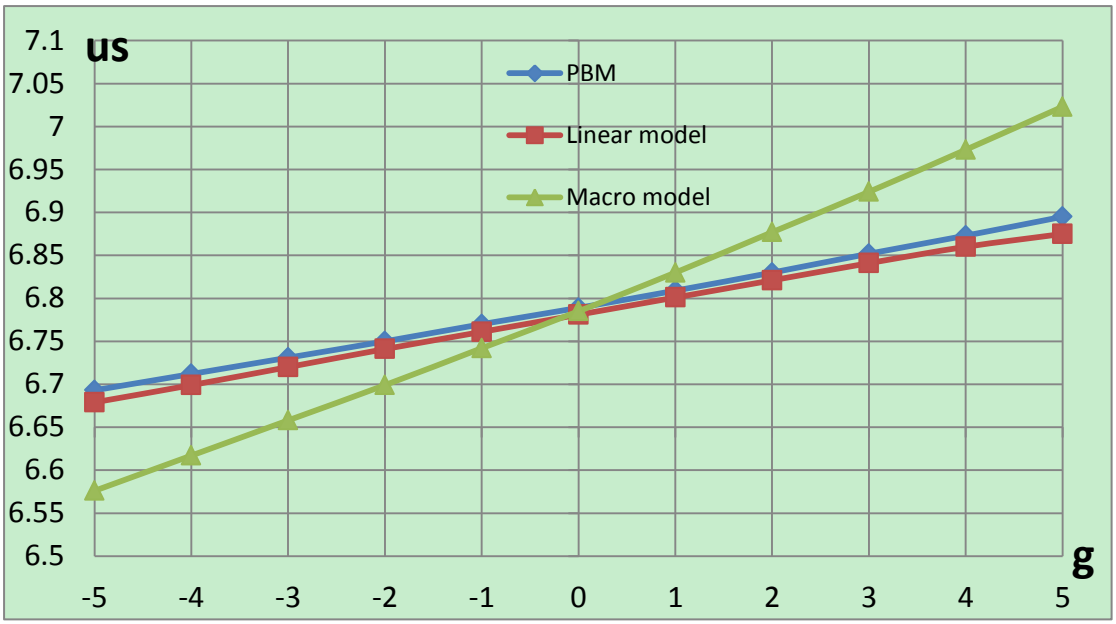



Figure 4.7: The pre-simulation of the three models with capacitance to pulse-width

## 4.3 System Simulation

The proposed circuit with one axial accelerometer is simulated in Cadence design environment using Spectre simulator and operated with supply voltage 1.8V. The PBM is used to the co-simulation with circuits in Cadence. As shown in Figure 4.8, there are seven simulation results on typical-typical, slow-slow, fast-fast, 0 and 50 degrees Celsius, VDD of 90% and 110% conditions. Each result just changes one condition and fixes the six others. One set of code is equivalent to one set of time value in -5g to 5g. At the sensing range, the resolution reaches to 20ns/1bit by C-to-D circuit. The system simulation results of C-to-D circuit with one axial accelerometer are shown in Table 4.5.

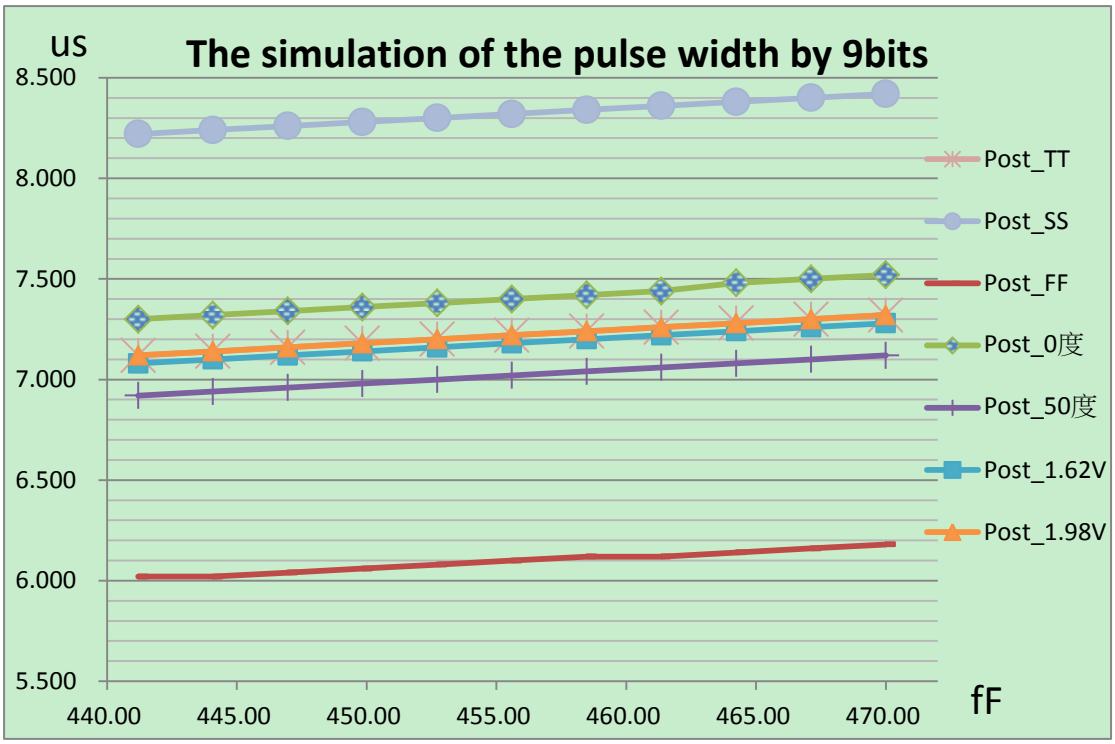



Figure 4.8: The post-layout simulation of the pulse-width in C to D circuit with accelerometer

Table 4.5: Specifications of C-to-D circuit with the accelerometer

| | Unit | Value |
|---|---|---|
| Sensitivity | us/pF | 6.94 |
| Dynamic range | fF | 441.2~470 |
| Resolution | ns/1bit | 20 |
| Sampling Rate | MHz | 50 |
| Power Consumption | mW | 5.47 |

# Chapter 5 Measurement

## 5.1 Measurement Results of T18-101A

The monolithic accelerometer with C-to-Pulse-Width circuit has been implemented in T18-101A. The designed core of T18-101A is focused on the sensitivity of C-to-PW circuits with the fixed capacitance value, 100fF to 1100fF, and the initial capacitance value of the accelerometer compared with the value of the co-simulation. The results of measurement and co-simulation are shown in Figure 5.1, and the measurement results of chip1~8 are averaged to form the square symbol curve in Figure 5.2. We can find that there is one unusual thing in the measurement from Figure 5.2. The initial capacitance value of the accelerometer which is with star mark

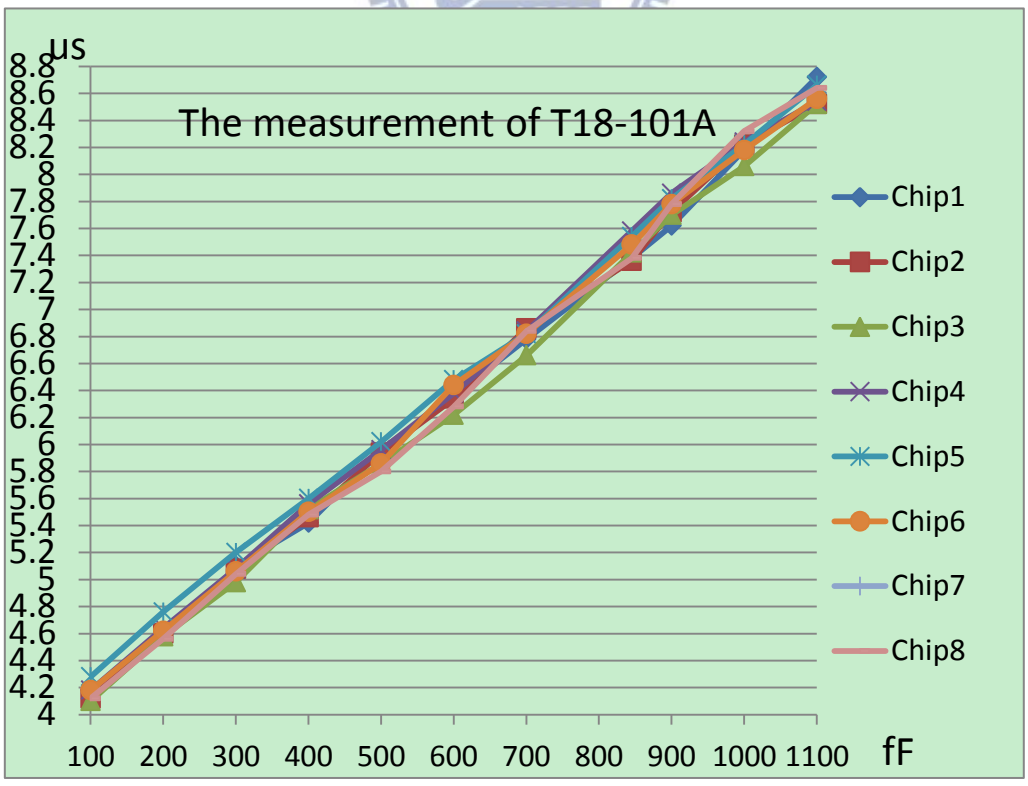



Figure 5.1: The measurement of chip1~8 of T18-101A

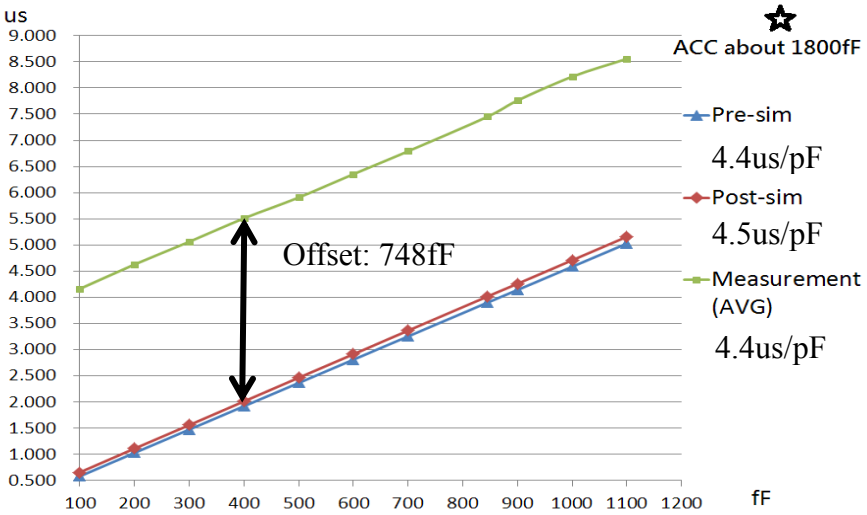



Figure 5.2: The comparison of T18-101A between simulation and measurement

the value is about 1800fF compared with 455.6fF of the simulation. There are two possible reasons for the difference, and one is that effect of parasitic capacitance results in the enlarged pulse width. The effective sensing capacitance, $C_{eff}$, is dependent on the parasitic capacitance seen by the sensing node $V_2$ of Figure 3.2. We can express $C_{eff}$ as follows:

$$C_{eff} \approx C_{PCB} + C_{MOS} + C_x \tag{5.1}$$

where $C_{MOS}$ is the capacitance from MOS devices, $C_x$ is the sensing capacitance, and $C_{PCB}$ is the off-chip PCB parasitic capacitance seen by the sensing node $V_2$. The linearity between the pulse-width and sensing capacitance is not affected by the parasitic capacitance. It only introduces a fixed offset proportional to $C_{PCB}$ and $C_{MOS}$ in the pulse-width. The other possible reason is that the accelerometer is unreleased and unsuspended to result in parasitic capacitance of silicon substrate to enlarge the

pulse-width compared with the simulation. The reason is also that why we took SEM and FIB pictures in the cross-section of the sensor and find a series of issue of the sensor.

## 5.2 Measurement Results of T18-101B

The monolithic accelerometer with C-to-D circuit has been implemented by TSMC 0.18um 1P6M CMOS mixed-signal process and APM MEMS process in T18-101B. The layout of the accelerometer with C-to-D circuit on a single chip is shown in Figure 5.3 and its size is 1343um*1419um. The accelerometer takes an area of 793um*812.5um. The die photo of the integrated chip by optical microscope is shown in Figure 5.4. The chip connects to the circuit board through bonding wires as shown in Figure 5.5.

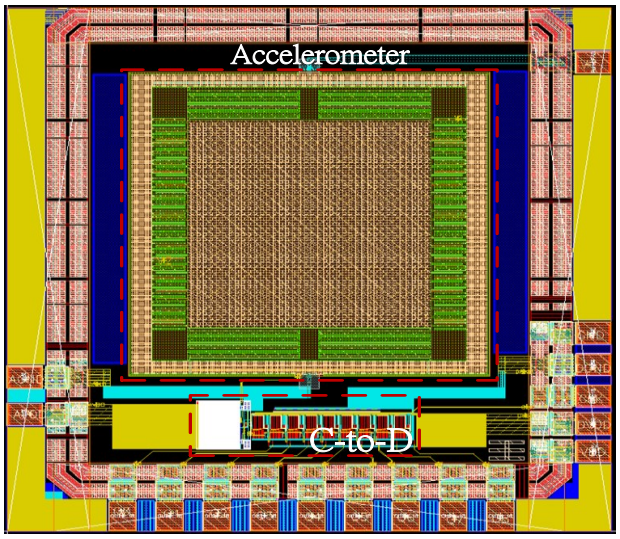



Figure 5.3: The layout of the integrated chip

MEMS motion analyzer (MMA) of CIC is used to test the movement and resonant frequency of sensors as shown in Figure 5.6, and the setting of the measurement is set to sweep from 1kHz to 4kHz. The measurement results of the Chip1, 2, and 6 are 2.5kHz as shown in Figure 5.7 compared with 2.19kHz of the simulation.

Measuring instruments used in the measurement include a shaker with vibration control system, a reference accelerometer, power supplies, a function generator, a

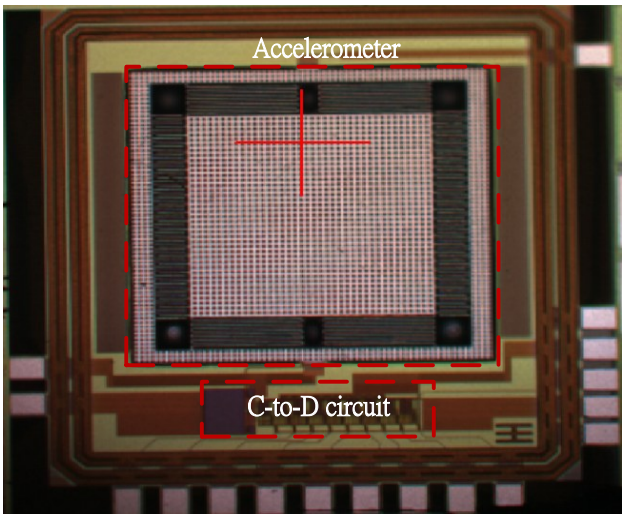



Figure 5.4: The die photo of the chip

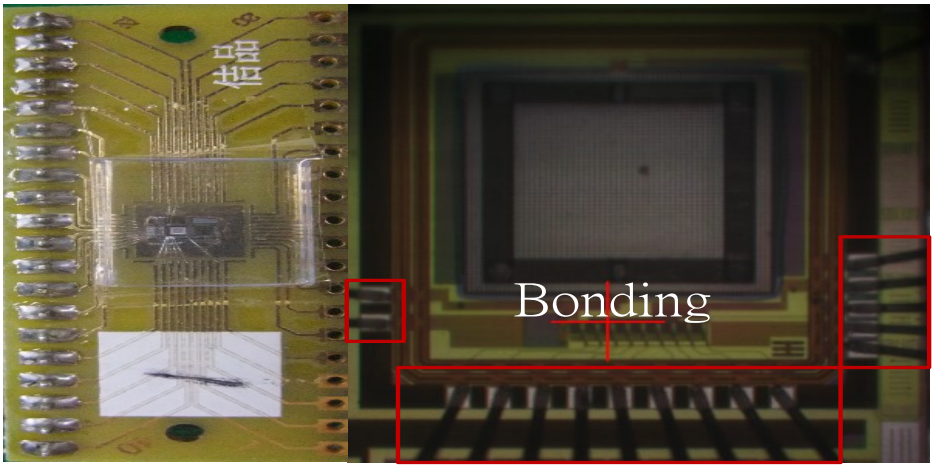



Figure 5.5: Photos of bonding board and bonding wire

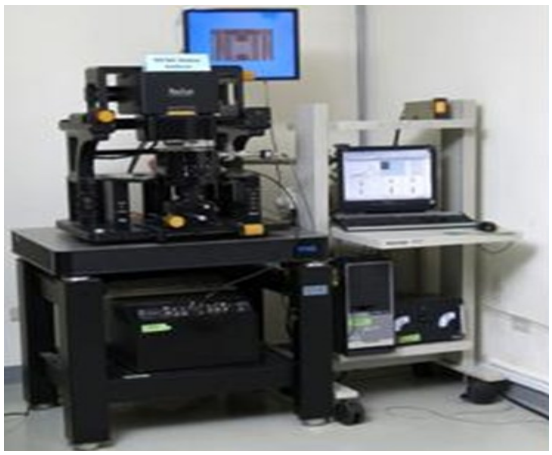


Figure 5.6: MEMS Motion Analyzer

logic analyzer, and other supporting instruments. The function of the reference accelerometer is used to detect the current force value. The reference accelerometer PCB 352C44 is fixed on the shaker with a sensitivity of 100mV/g. The sinusoidal reference acceleration input, with 100Hz and 1-gravity to 5-gravity, are shown in Figure 5.8 to 5.12. The logic analyzer is used to catch the data of 9bits counter in the range of 0 to 25m second about four periods, and the bits number is related to the gravity of the moment when the reference sinusoidal acceleration is at the peak value. Then the bits number of the peak value is averaged in the peak of four periods.

The chip under test is wire bonded on the package and mounted on the experimental circuit board for measurement. LDS shaker generates the input acceleration to test the initial capacitance and the capacitance sensitivity. The major instruments used in the measurement are summarized in Table 5.1. The setup of the

measurement environment is shown in Figure 5.13 for testing the chip. There are two single-axis accelerometers on LDS shaker. One is the reference accelerometer with orange clay for fix the reference one, and the other is the designed accelerometer on the test board. With supply voltage $V_{DD}$=1.8V, it dissipates a 428.9uA of current and results in a 772uW of static power consumption.

Table 5.1: Instruments used in the measurement

| Instrument | Model | Key Features |
|---|---|---|
| Shaker | LDS 406-PA100E | Input acceleration range: ±10g<br>Frequency range: 5Hz-9kHz |
| Vibration control system | LDS Laser USB | Signal analysis<br>Spectrum analysis |
| Reference accelerometer | PCB 352C44 | Acceleration:±5g<br>Sensitivity: 100mV/g |
| Power supply | Agilent E3632A | Output: 15V/7A |
| Function generator | Tabor Electronics WW2572A | Square wave:50MHz |
| Logic analyzer | Agilent 16902A | 4 pods, 16channels/pod |
| Fixture | Local customization | Length x Width x Height: 11x6.5x9.5 |

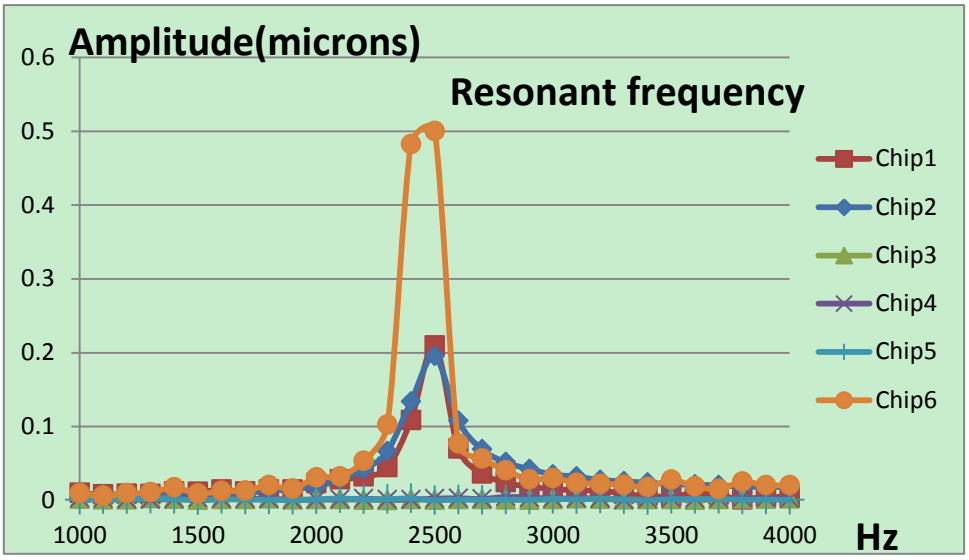



Figure 5.7: The measurement results of resonant frequency of the accelerometer

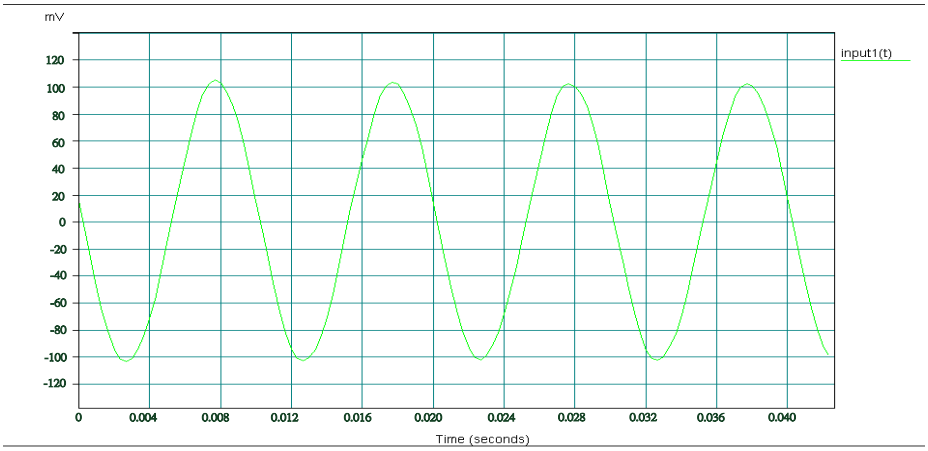



Figure 5.8: 1G, 100Hz sinusoidal reference acceleration input

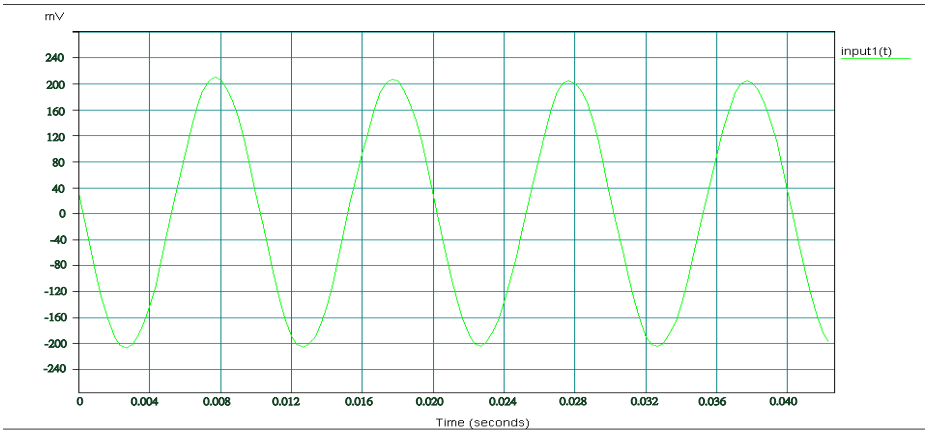



Figure 5.9: 2G, 100Hz sinusoidal reference acceleration input

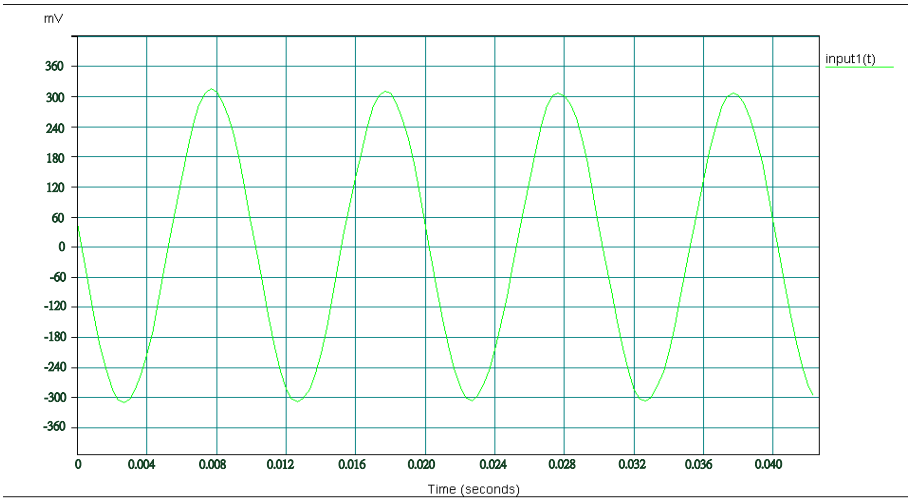



Figure 5.10: 3G, 100Hz sinusoidal reference acceleration input

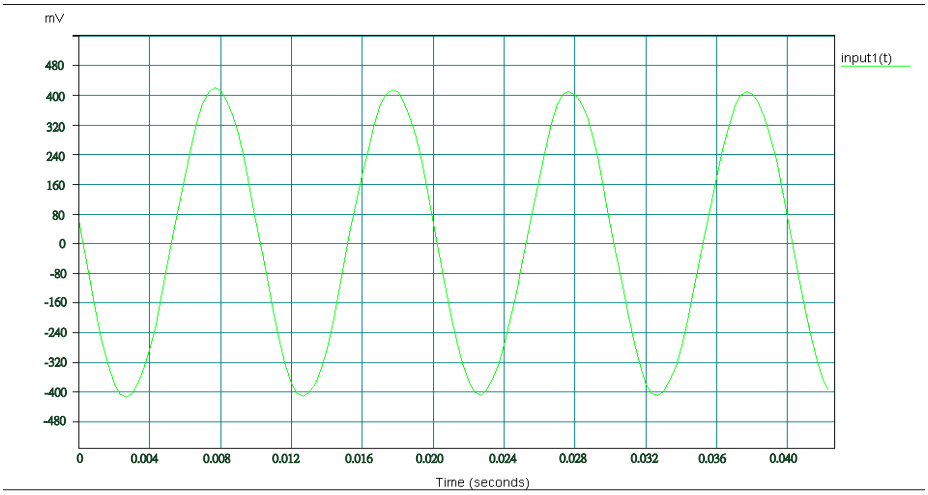



Figure 5.11: 4G, 100Hz sinusoidal reference acceleration input

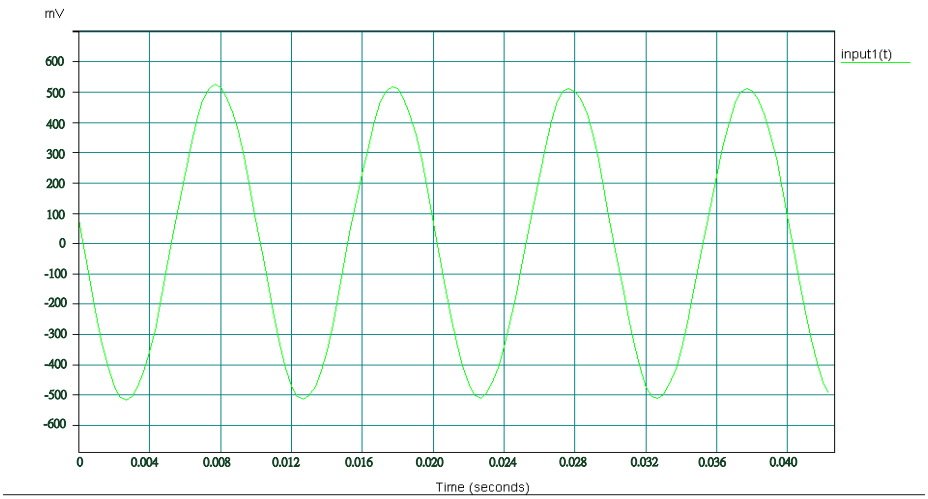



Figure 5.12: 5G, 100Hz sinusoidal reference acceleration input

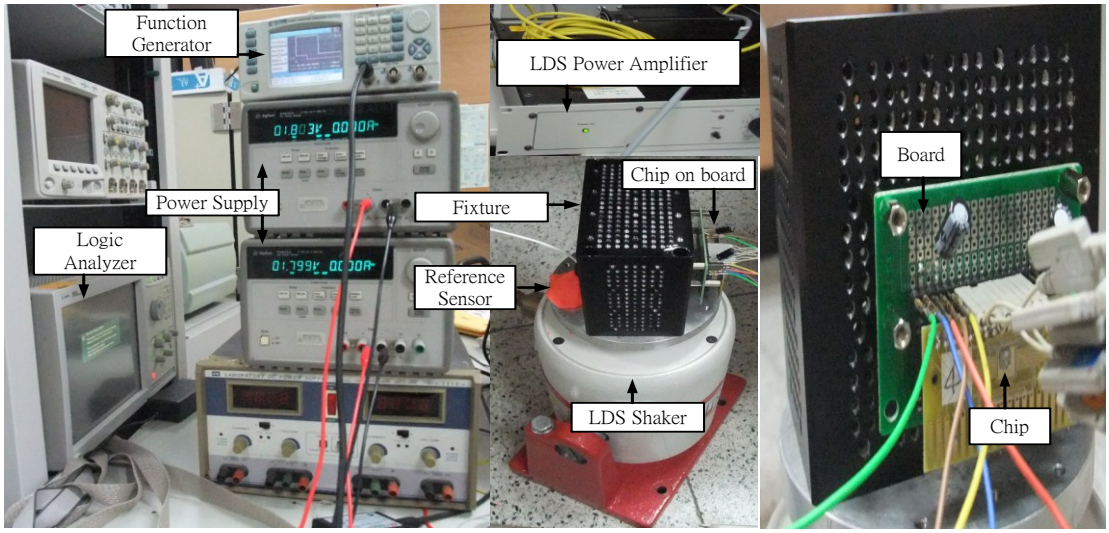



Figure 5.13: Photos of instruments

The chip5 is destroyed due to the bonding. With -5 to 5 acceleration of gravity of input from LDS shaker, the measurement results of gravity to Time (g to T) of other chips are shown in Figure 5.14, and it shows that chip1, 2, and 6 are close to increase linearly and more linear than chip3 and 4. Chip1, 2, and 6 are averaged to form the AVG curve as shown in Figure 5.14. The measurement results compared with the simulation are shown in Figure 5.15. The results are divided into two parts, gravity to capacitance (g to C) and g to T. The part of g to T is measured from the testing environment, and the other part of g to C is derivate from both g to T of measurement and capacitance to time (C to T) of the simulation. It shows higher capacitance sensitivity and lower linear characteristic compared with the simulation. The measurement results show that the capacitance range is 640fF to 890fF with -5 to 5 gravity and the capacitance sensitivity of the black linear trend line is 23.02fF/g. All chips of the measurement results are shown in Table 5.2 compared with the simulation.

Because the curves of measurement results show the non-linear feature, the sensitivity of capacitance and g to T are simplified from linear trend line of each chip. Obviously, the sensitivity and dynamic range of the measurement results are bigger than the simulation. The possible reasons are that the parasitic capacitance and offset of circuits are made to enlarge the pulse-width and digital bits. The overall conversion relation is given as

$$g \rightarrow C \rightarrow PW \rightarrow D \tag{5.2}$$

where g is gravity, C is the measured capacitance, PW is pulse-width, and D is the digital bit. There is some capacitance offset in C-to-PW circuit, but the sensitivity is accurate from the measurement results of T18-101A. The measured D values are directly transferred to PW values. Therefore, there are two possible reasons. One is the accuracy of the co-simulation model from MEMS+, and the other is the added D values due to the noise. The resolution of PW could be introduced the noise, but the design is based on one bit for one gravity from MEMS+ because the capacitance range between simulation and measurement is still verified.

Comparing with [7], the sensing capacitance range of this design is smaller 10 times as shown in Table 5.3. The sensor with circuits on single chip and fully digital output signal of the features are over than others. The circuit is designed to use the 9bits counter and 50MHz sampling rate to readout the fully digital, so the power

consumption is over than others.

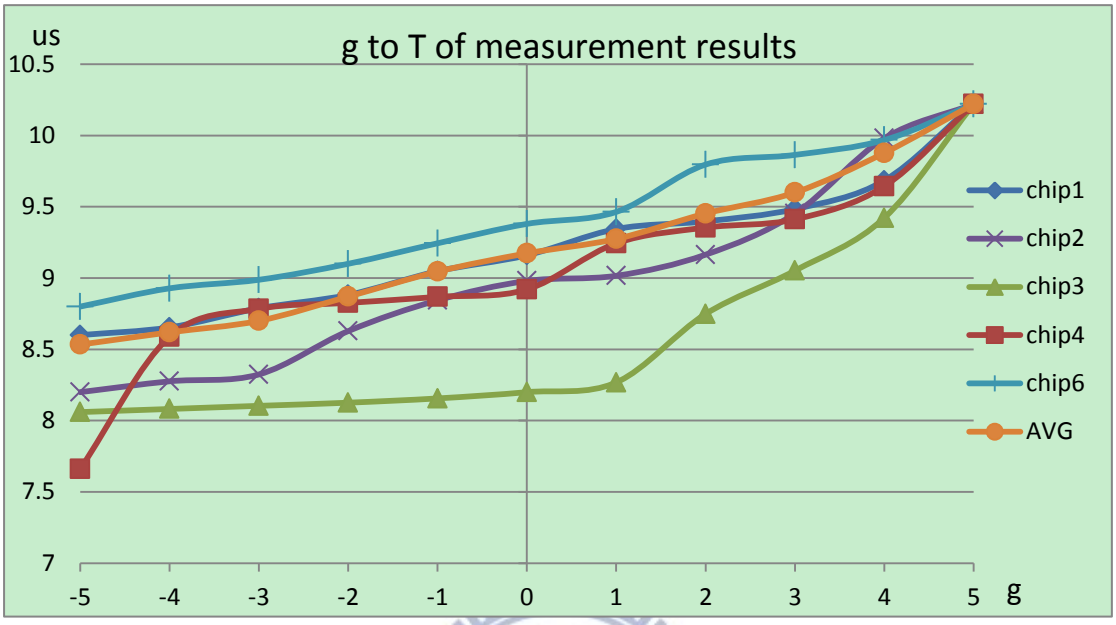



Figure 5.14: The measurement results of g to T of chips

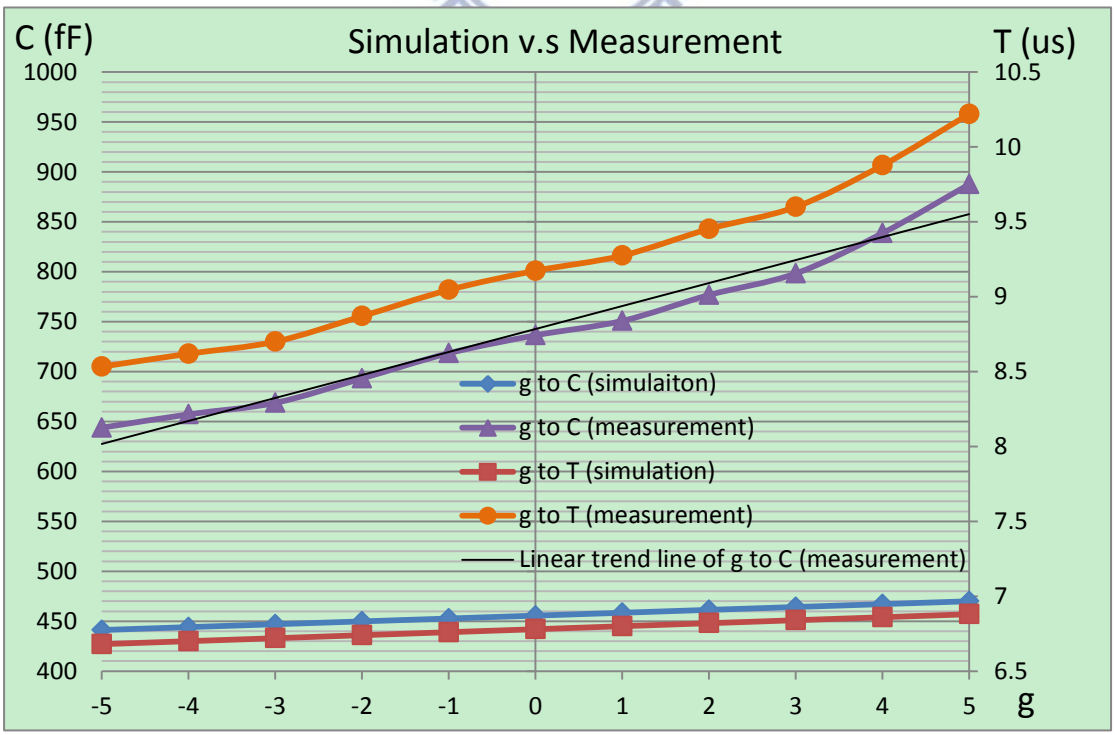



Figure 5.15: The comparison between simulation and measurement

Table 5.2: The summary of simulation and measurement results

| | Simulation | Chip1 | Chip2 | Chip3 | Chip4 | Chip5 | Chip6 |
|---|---|---|---|---|---|---|---|
| Resonant frequency (KHz) | 2.19 | 2.5 | 2.5 | X | X | X | 2.5 |
| Sensitivity of g to T (ns/g) | 20 | 142.1 | 195.9 | 185.1 | 184.9 | X | 140.9 |
| Capacitance sensitivity (fF/g) | 2.88 | 20.45 | 28.19 | 26.65 | 26.58 | X | 20.28 |
| Dynamic range (fF) | 441.2~470 | 654.3~ 887.6 | 596.7~ 887.6 | 576.6~ 887.6 | 519~ 887.6 | X | 683.1~ 887.6 |
| Dynamic power consumption (mW) | 5.47 | 5.284 | 5.034 | 5.259 | 5.159 | X | 5.209 |

Table 5.3: Comparisons

<table>
<tr><td>Year</td><td>2007[6]</td><td colspan="2">2011[5]</td><td>2012[7]</td><td>This simulation</td><td>This measurement</td></tr>
<tr><td>Technology</td><td>0.35um CMOS</td><td colspan="2">0.13um CMOS</td><td>0.35um CMOS</td><td colspan="2">0.18um CMOS</td></tr>
<tr><td>Sensor integrated</td><td>No</td><td colspan="2">No</td><td>No</td><td colspan="2">YES</td></tr>
<tr><td>Topology</td><td>Quasi-digital</td><td colspan="2">Quasi-digital</td><td>Quasi-digital</td><td colspan="2">Digital</td></tr>
<tr><td>Power & VDD</td><td>16.5mW,3.3 V</td><td colspan="2">60uW,1V</td><td>54uW,3V</td><td>5470uW, 1.8V</td><td>5189uW, 1.8V</td></tr>
<tr><td>Sensitivity</td><td>47us/pF</td><td colspan="2">7us/pF<br>Rref:10MΩ<br>0.5ns/Ω<br>Cref:800pF</td><td>3.88us/pF<br>Cref:3pF</td><td>6.94us/pF<br>Rref:10MΩ</td><td>6.93us/pF<br>Rref:10MΩ</td></tr>
<tr><td>Segment</td><td>NA</td><td colspan="2">NA</td><td>46.5fF/seg at 7segment<br>180ns/seg</td><td>2.88fF/seg at 10 segment.<br>20ns/seg</td><td>23.02fF/seg at 10 segment.<br>159.6ns/seg</td></tr>
<tr><td>C dynamic range</td><td>0.8pF~1.2pF</td><td colspan="2">Range / Ref Ω<br>1pF / 10M<br>9pF / 2.7M<br>28pF / 1M<br>211pF / 100k<br>10.2nF / 3k</td><td>2.5pF~2.82pF</td><td>441.2fF~ 470fF</td><td>643.8~ 887.6fF</td></tr>
<tr><td>Sampling rate(Hz)</td><td>20K</td><td colspan="2">32.768K</td><td>25K</td><td colspan="2">50M</td></tr>
<tr><td>Area($mm^2$)</td><td>0.2</td><td colspan="2">0.011</td><td>0.09</td><td colspan="2">0.061 with circuits<br>0.8 with sensor & circuits</td></tr>
</table>

# Chapter 6 Conclusions and Future Work

## 6.1 Conclusions

In the measurement, the capacitance sensitivity under the situation of linear trend line is 23fF/g compared with 2.88fF/g of the simulation in -5 to 5 gravity. The initial capacitance of measurement result is about 730fF compared with 455.6fF of the simulation.

In the future, the improvement will be focused on both reading capacitance and resistance on a single chip. We will add offset cancellation to readout practical capacitance, and temperature compensation of circuits for compensating the sensors.

## 6.2 Future Work

Sensor fusion is the combining of sensory data or data derived from sensory data from disparate sources such that the resulting information is in some sense better than would be possible when these sources were used individually. The term better in this case can mean more accurate, more complete, or more dependable, or refer to the result of an emerging view, such as stereoscopic vision (calculation of depth information by combining two-dimensional images from two cameras at slightly different viewpoints).The data sources for a fusion process are not specified to originate from identical sensors. One can distinguish direct fusion, indirect fusion and fusion of the outputs of the former two. Direct fusion is the fusion of sensor data from

a set of heterogeneous or homogeneous sensors, soft sensors, and history values of sensor data, while indirect fusion uses information sources like a priori knowledge about the environment and human input. Sensor fusion is also known as (multi-sensor) Data fusion and is a subset of information fusion.

Beyond figuring out the basics for how a Windows 8 system might use sensors, we also needed to think about how apps might use sensors. We looked at a variety of examples of sensor-enabled apps including games, commercial applications, tools, and utilities, to help us determine which scenarios to support as shown in Figure 6.1. First on the list was the ability for apps to understand motion and screen rotation. This requires an accelerometer, a device that can be used to measure the force due to gravity, and the motion of the device itself. But most scenarios require more than just an understanding of motion and gravity. Orientation is also an important requirement for many applications. To enable a PC to understand orientation, we needed to integrate the functionality of a compass. A 3D accelerometer and a 3D magnetometer are required. This combination of sensors is called a 6-axis motion and orientation sensing system, and can support a basic tilt-compensated compass, screen rotation, and certain casual game apps like a labyrinth style game. Recently, a new type of sensor has started to emerge on phone platforms, the gyro sensor. Gyro sensors measure angular speed, typically along 3 axes. We can also use the data from gyro

sensors to increase the responsiveness and accuracy of 3D motion-sensing systems. A gyro sensor is very sensitive. Now let's take a look at sensor fusion in action from the above sensors.

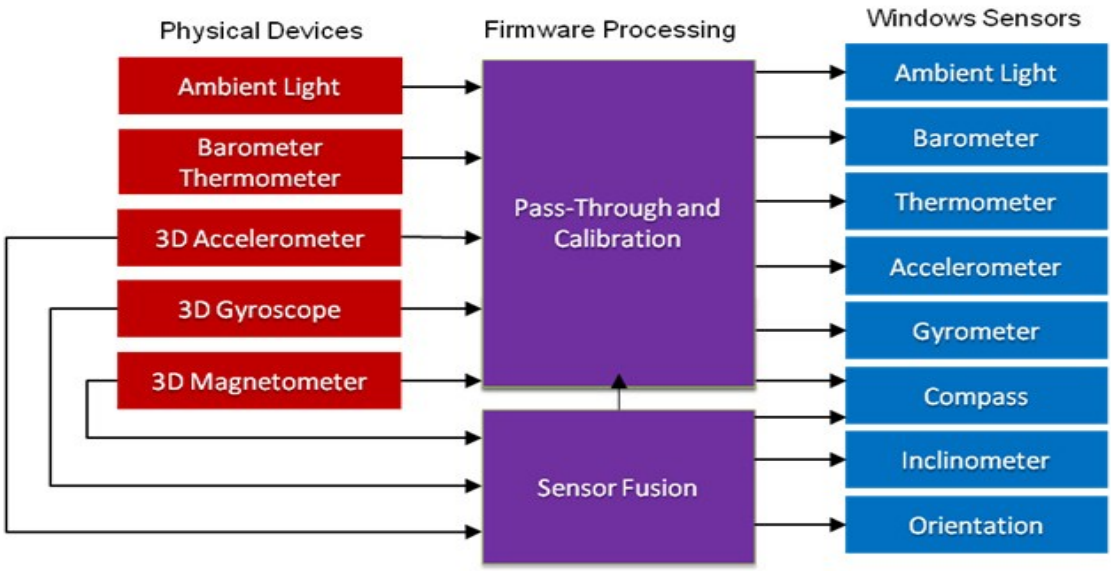



Figure 6.1: Freescale Microsoft® Windows® 8 Sensor Fusion Data Flow

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