國 立 交 通 大 學

電機與控制工程學系

碩 士 論 文

應用於初次側調整控制器之高效率及低成本膝點電壓追蹤調整技術

Primary-Side Regulator with Self-Calibration Knee Voltage Detection (KVD) Technique for High Efficiency and Low Cost

研 究 生：葉之樸

指導教授：胡竹生　博士

陳科宏　博士

中 華 民 國 一百零一 年 十一 月

用於初次側調整控制器之高效率及低成本膝點電壓追蹤調整技術

Primary-Side Regulator with Self-Calibration Knee Voltage Detection (KVD) Technique for High Efficiency and Low Cost

研 究 生：葉之樸　　Student：Chih-Pu Yeh

指導教授：胡竹生　　Advisor：Jwu-Sheng Hu

陳科宏　　Advisor：Ke-Horng Chen

國 立 交 通 大 學

電 機 與 控 制 工 程 學 系

碩 士 論 文

A Thesis

Submitted to Department of Electrical Control Engineering

College of Electrical Engineering

National Chiao Tung University

in partial Fulfillment of the Requirements

for the Degree of

Master

in

Electrical Control Engineering

November 2012

Hsinchu, Taiwan, Republic of China

中華民國一百零一年十一月

用於初次側調整控制器之高效率及低成本膝點電壓追蹤調整技術

研究生：葉之樸　　指導教授：胡竹生博士　陳科宏博士

國立交通大學電機與控制工程研究所碩士班

摘 要

在現今社會，可攜式產品已經成為人人不可或缺的必備工具。隨著電子產品的蓬勃發展，可充電電池也成為目前最適合可攜式產品使用的行動電源。因此，如何以最理想且安全的方式將能量傳遞到電池，對電池進行最快速也最有效率的充電是一個重要的課題。基於通用串行總線充電變成一種趨勢，從交流市電直接對電子產品充電是現在大部分可攜式產品的充電方式。初次側調整控制器是一種高效率而且低成本的充電器，同時也是一種能容忍市電的高輸入電壓隔離式充電器。為了確保充電器在定電流充電模式與定電壓充電模式皆能保持穩定且平穩切換，本切換式充電器將定電流充電迴路與定電壓充電迴路並聯，且同時達到兩者的穩定性。但是初次側調整控制器與一般控制器最大的分別就是它並沒有直接的迴授路徑來獲取輸出資訊，因此如何準確從輔助繞組中去取得膝點電壓進而去控制整個系統變成一個重要問題。

本篇論文完成一具有膝點電壓偵測電路，同時針對偵測的時間做自我的調整來避免發生偵測錯誤。不同於以往的方式，這次提出的偵測電路不僅能準確的偵測膝點電壓，並不需要外部原件來做修正，同時也使所有的控制路徑在定電流充電模式與定電壓充電模式皆能保持穩定且平穩切換。為了使效率更進一步提升，波谷切換以及動態頻率切換被應用在定電壓充電模式。

Primary-Side Regulator with Self-Calibration Knee Voltage Detection (KVD) Technique for High Efficiency and Low Cost

Student: Chih-Pu Yeh Advisor: Dr. Jwu-Sheng Hu & Dr. Ke-Horng Chen

Department of Electrical Control Engineering

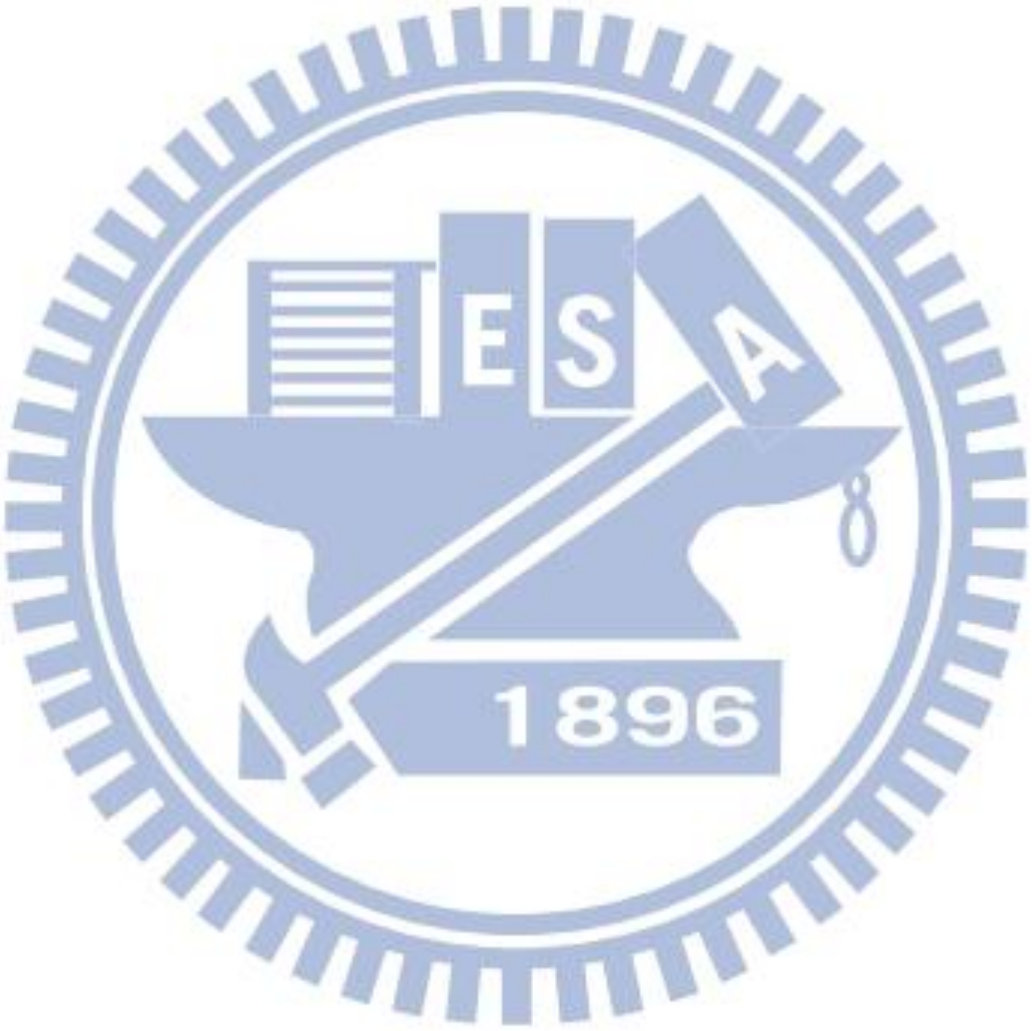
National Chiao-Tung University

Abstract

Nowadays portable devices have been considered a necessity by a lot of people and have become an essential part of everyday life. With the rapid growth in the consumer electronics, rechargeable mobile battery bank has proved to be the most compatible and satisfactory solution for portable devices. Therefore, it will be an important task for us to create a fast and efficient battery charging method with safe delivery of energy to the battery. Since universal serial bus (USB) charging method is a common trend now, most of the portable devices are charged via alternating current (AC) supply combine with USB. Primary-side regulator (PSR) is a high efficiency and low cost solution for power applications. It is a high-input voltage isolated charger compatible with the AC supply. To stabilize and to smoothly transit between the constant voltage and the constant current modes, the constant voltage and constant current loops are connected in parallel in the proposed PSR charger. However, the prominent difference between the PSR and conventional regulators is that the PSR does not have direct feedback loop to obtain the output information. Hence, it is a major challenge to precisely detect knee voltage from the auxiliary winding and thus to accurately control the entire system.

This thesis introduces the PSR with self-calibration knee voltage detection (KVD)

technique, which it can perform self-calibration based on the detection period for error checking and correction. Moreover, the new detection method not only can precisely get the knee voltage without any external components, but also can have all control paths stabilized. The transition smoothly changes between the constant voltage and the constant current modes. Valley switching with a dynamic frequency switching is applied in the constant voltage mode in order to enhance its efficiency and performance.



誌　　謝

兩年多來的碩士班生涯，要感謝許多的人在這一路上對我的幫助。首先要感謝我的家人一直不斷的支持及照顧我。包括我的爸爸媽媽，還有露露，感謝你們長久的陪伴和督促，才能讓生性偷懶的我一直支撐下去。

首先要感謝我的指導教授陳科宏博士，您幽默風趣的談吐、不厭其煩的教導、與我們亦師亦友、共同進退的形象，會是最棒的回憶。更感謝您對此篇論文不厭其煩的修改與修正，真的是辛苦您了。除此之外，提供豐富的研究資源、充分給予挑戰嘗試的機會，並提供生活關心照顧，更是我學習成長的一大動力。

感謝實驗室學長們在研究生活中的照顧。感謝昱輝學長、期哥學長、斤哥學長、小契學長、小蔡學長、昭彰學長、暐中學長、蘇蘇學姊、雅萍學姐、怡婷學姐。感謝有你們在學業上與生活上的照顧與指導。

感謝同儕阿倪、垮克、GM、大龍。能夠與你們成為夥伴一起討論切磋、互相勉勵、共度實驗室生活，真的很開心。謝謝阿倪與 GM，你們是所有人之中我最能夠在修課中依賴的人，感謝你們不時地提醒我上課的資訊，以及督促我上課的內容，你們的努力絕對會在往後的日子給你的回報，希望你們日後都能飛黃騰達。感謝垮克與大龍，你們是我在實驗室中能夠陪我聊天講垃圾話的夥伴，有你們在的日子中，實驗室變得開心許多，希望你們都可以找到你們的目標，做你們真正想做的事，也希望大家以後可以多聚聚。

感謝各位學弟，澎澎、亞當、祖為、pony、紹祥、浩子，實驗室有你們變的更活潑有朝氣。感謝澎澎、祖為、亞當以及紹祥，謝謝你們的陪伴與討論，也謝謝你們在娛樂方面的切磋以及指教，也感謝助理巧潔平時的幫忙。同時也感謝五年碩的學弟們，感謝你們為實驗室帶來了許多了歡樂。

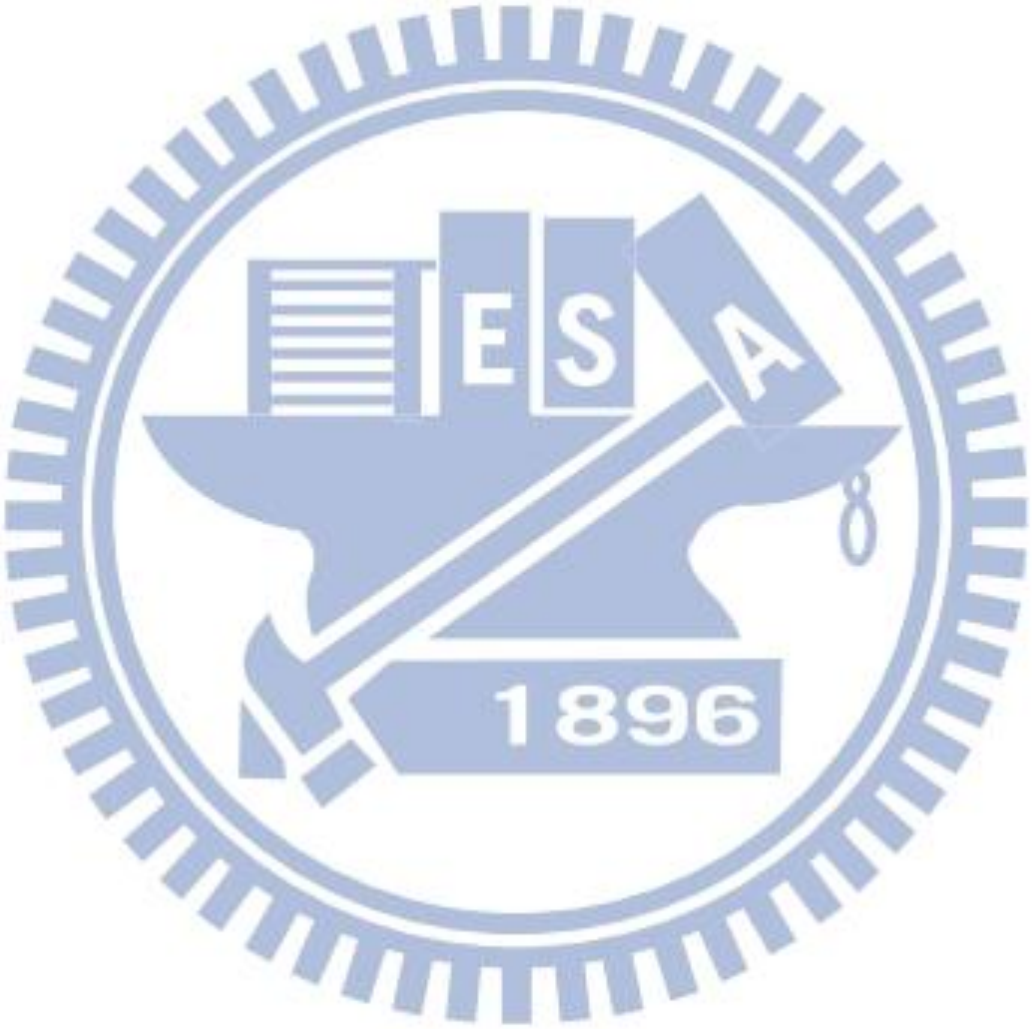
最後我要特別感謝我的最愛露露，感謝你一路陪伴我，陪我來到了新竹。感謝你雖然辛苦，但都盡力滿足我的一切。跟你一起在新竹的這 2 年給了我很多成長，也讓我在課業之餘，能過得非常充實，也謝謝你的不離不棄，以及你們家人的包容與幫助。

僅以此論文獻給我愛的人及愛我的人，家人們、同學們、朋友們和所有關心我的人。因為有你們，使本論文豐富不少，謝謝你們。

之樸 于 小雪

國立交通大學

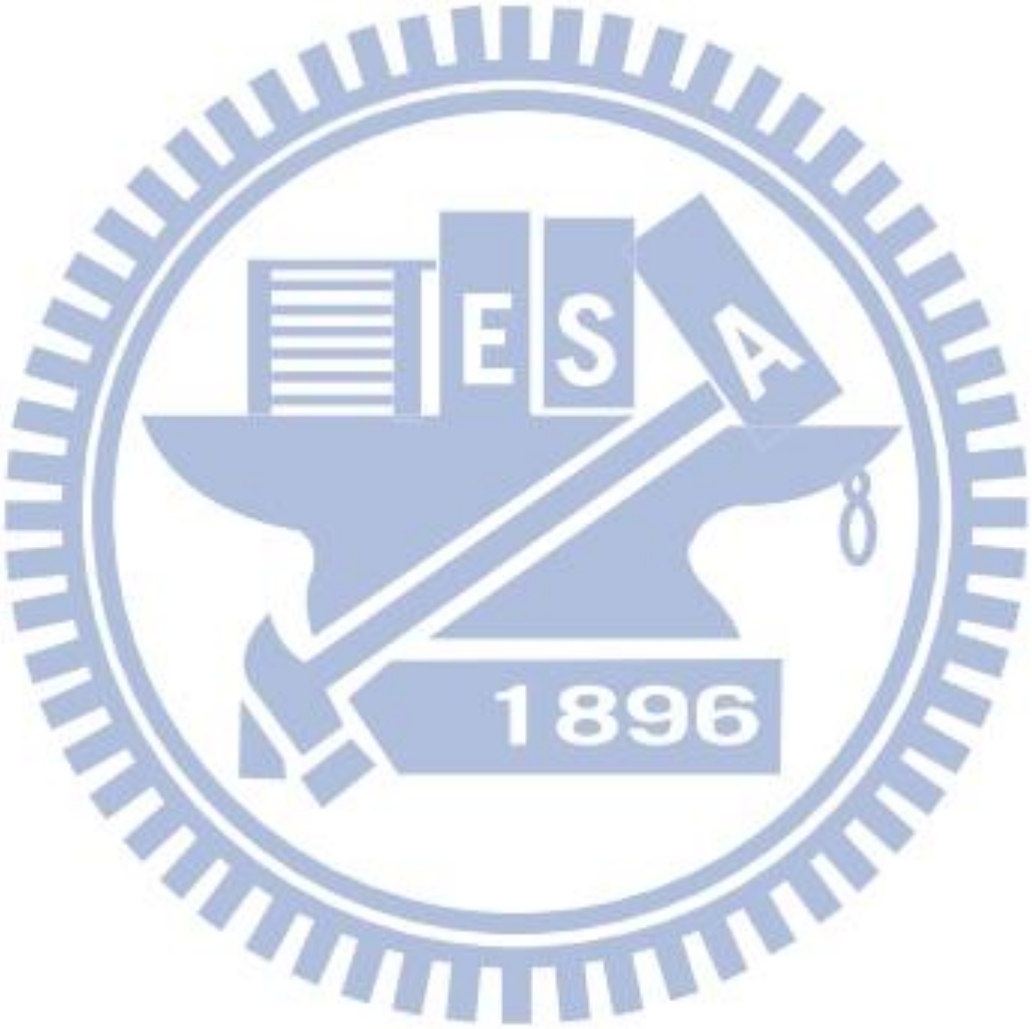
中華民國一百零一年十一月



Contents

FIGURE CAPTIONS

Table Captions



Chapter 1

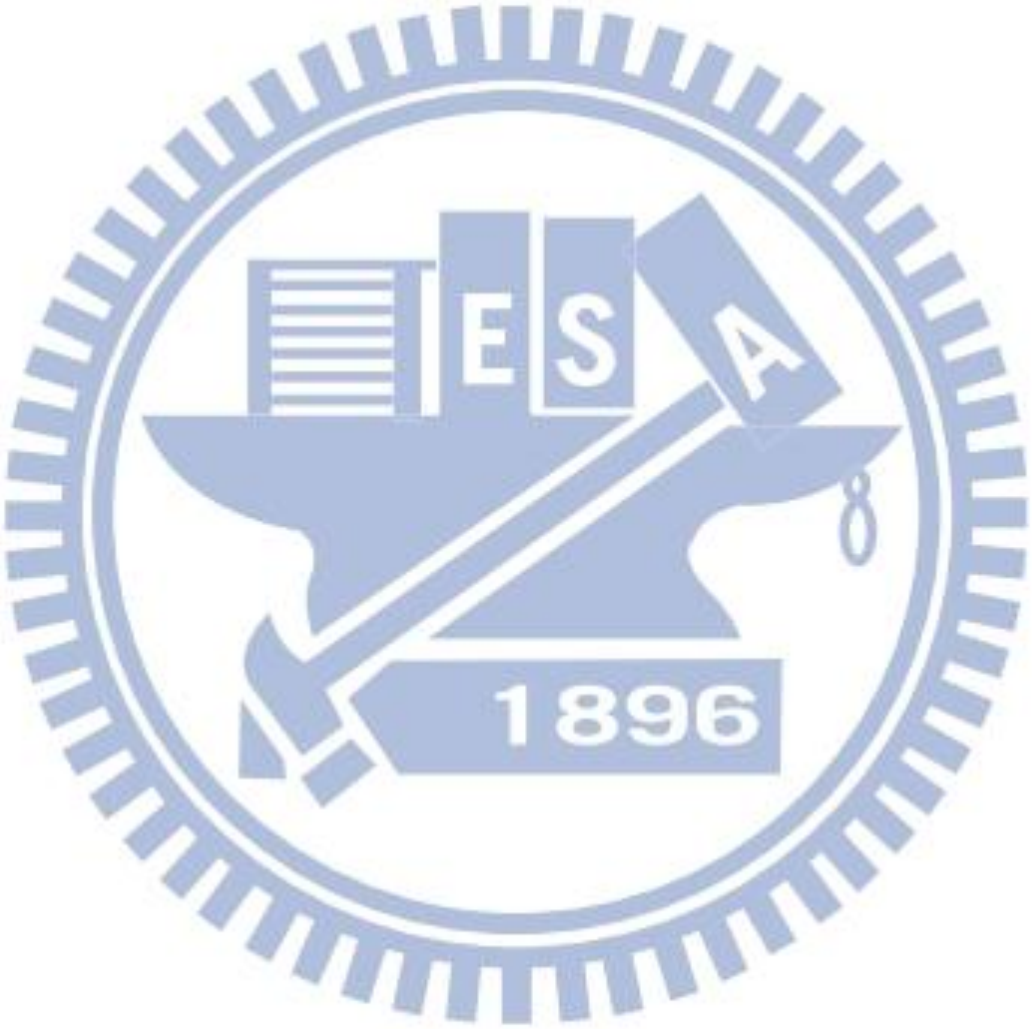
Introduction

The isolated architecture is widely used in nowadays power system because of it has many advantages. Such as it is quite safety and convince to design in wide range voltage difference situation between output and input voltage. Flyback [1] converter is one of isolated converter [2]. Unlike the conventional power system, isolated converter uses a pair of coils to transmit electric power via magnetic coupling. It protects the back-end device from high input voltage through the isolation from transformer. In view of the portable device become a trend, one of control methods of flyback called primary-side regulator (PSR) becomes more important.

Recently, the portable devices like personal digital assistants, smart phones, laptops and digital cameras etc., have become the most popular applications [3]. Rechargeable batteries combine universal serial bus (USB) charging method are used in these applications for green energy and linking devices to personal computer. Also most of the portable devices are charged via alternating current (AC) supply. PSR is a high efficiency and low cost solution for these power applications. It is also a high input voltage isolated charger compatible with AC supply.

The proposed PSR is using the topology of flyback converter and used for battery charger. Also the self-calibration with knee voltage detection (KVD) technique is proposed to enhance the accuracy of sensing battery voltage. The improving of the sensing accuracy can make the charging sequence changing precisely between constant current (CC) and constant

voltage (CV). It can prevent overcharging for battery [4] [5] and improve the efficiency of the system.



1.1 The Basic Concept of the Isolated Converter

The switching mode charger can be classified according to system topology. The most important distinction is isolated converters and non-isolated ones. Most of the electrical equipment needs the isolation for high-voltage safety consideration. The advantages about isolation such as the separation of direct contact from input to output, and the improved common-mode voltage rejection from input source. Moreover, there are some standards defined by different institutions in different countries such as the U.S. specifications (UL, CSA) and the European specifications (IEC, EN). Every product on the market must be approved by these institutions.

The isolated power converters have many different topologies according to the application of output watts of electrical device. Fig. 1. shows some common isolated topologies that apply in different output power. Each topology has different designed complexity and conversion efficiency. TABLE I shows some different types of isolated converters and some of its characteristic.

According to the operation of the isolated converter, there are two types of isolated topologies like asymmetrical and symmetrical. The asymmetrical type uses only one switch to transfer the energy from primary side to output side through the transformer such as flyback and forward. And the symmetrical type always uses an even number of switches. Compare to asymmetrical converters, it is better exploits the transformer's magnetic circuit than in asymmetrical converters. So, smaller size and weight can be achieved. In other words, if it uses the same size of transformer, the symmetrical type could supply more output power. The three most common symmetrical structures are push-pull, half bridge and full bridge.

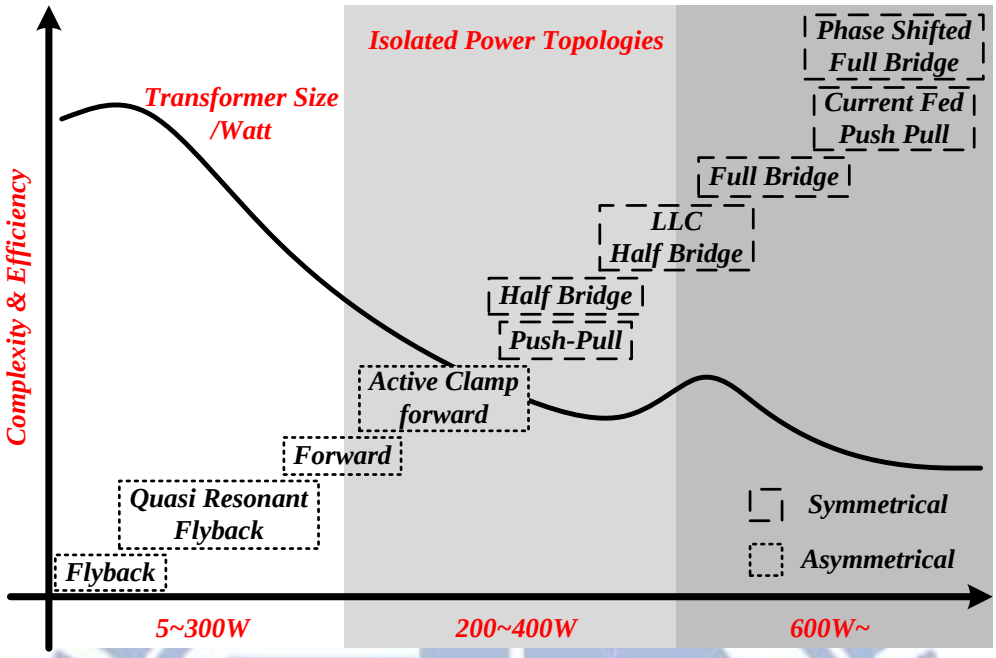


Fig. 1. Isolated power topologies with complexity and efficiency

TABLE I

Different types of isolated converters.

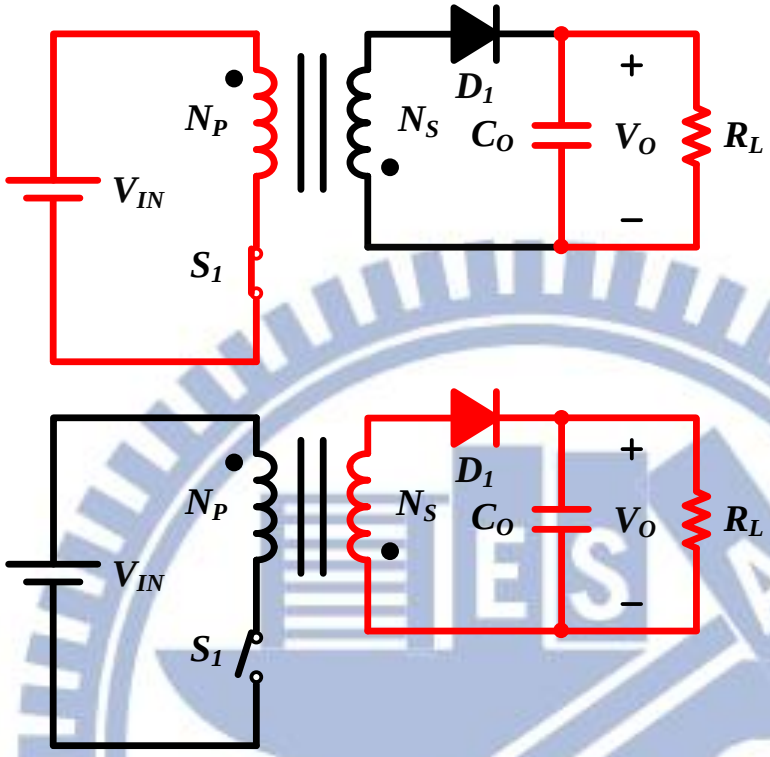
Converter Type	Power (W)	Relative Cost	Input Range (V)
Flyback	0-250	1.0	5-600
Half-Forward	0-250	1.2	5-500
Forward	100-200		60-200
Push-Pull	100-1000	1.75	50-1000
Half-Bridge	0-2000	>2.0	50-1000
Full-Bridge	400-5000	>2.0	50-1000

1.1.1 Architecture of Asymmetrical Isolated Converters

One of the most common asymmetrical isolated converters is flyback converter. The flyback converter is used in both AC/DC and DC/DC conversion with galvanic isolation between the input and any outputs. More precisely, the flyback converter is a buck-boost converter with the inductor split to form a transformer, so that the voltage ratios are multiplied with an additional advantage of isolation. When driving for example a plasma lamp or a voltage multiplier the rectifying diode of the buck-boost converter is left out and the device is called a flyback transformer.

Fig. 2 shows the structure of flyback converter [6]. When the switch is closed, the primary of the transformer is directly connected to the input voltage source. The primary current and magnetic flux in the transformer is increasing, and storing energy in the transformer. The voltage induced in the secondary winding is negative, so the diode is reverse-biased (i.e., blocked). When the switch is opened, the primary current and magnetic flux drops. The secondary voltage is positive, forward-biasing the diode, allowing current to flow from the transformer. The energy from the transformer core recharges the capacitor and supplies the load. The output capacitor supplies energy to the output load. The operation of storing energy in the transformer before transferring to the output of the converter allows the topology to easily generate multiple outputs with little additional circuitry, although the output voltages have to be able to match each other through the turns ratio. Also there is a need for a controlling rail which has to be loaded before load is applied to the uncontrolled rails, this is to allow the PWM to open up and supply enough energy to the transformer. If the turns ratio of the transformer $n=N_P/N_S$ and D means the duty cycle of on-time, the conversion ratio of V_{IN} and V_O is shown below. Flyback regulators are mainly used for an output power ranging

from 5W up to 250W. Flyback topology is dedicated to multiple low cost output switch mode power supply as there is no filter inductor on the output.



$$\frac{V_O}{V_{IN}} = \frac{1}{n} \cdot \frac{D}{1-D}$$

Fig. 2. Flyback converter.

The forward converter as shown in Fig. 3 is a DC/DC converter that uses a transformer to increase or decrease the output voltage (depending on the transformer ratio) and provide galvanic isolation for the load [7]. With multiple output windings, it is possible to provide both higher and lower voltage outputs. It operates in a manner similar to the flyback converter, but is generally more energy efficient. A flyback converter stores energy as a magnetic field in an inductor air gap during the time the converter switching element (transistor) is conducting. When the switch turns off, the stored magnetic field collapses and the energy is transferred to the output of the flyback converter as electric current. The flyback converter can be viewed as two inductors sharing a common core. In contrast the forward converter (which is based on a transformer) does not store energy during the conduction time of the switching element - transformers cannot store a significant amount of energy unlike inductors. Instead, energy is passed directly to the output of the forward converter by transformer action during the switch

conduction phase. The demagnetization and primary windings have to be tightly coupled to reduce the voltage spike more than the theoretical *2Vin* occurring at turn-off across the power switch. Besides, forward regulators are commonly used for output power up to 300W.

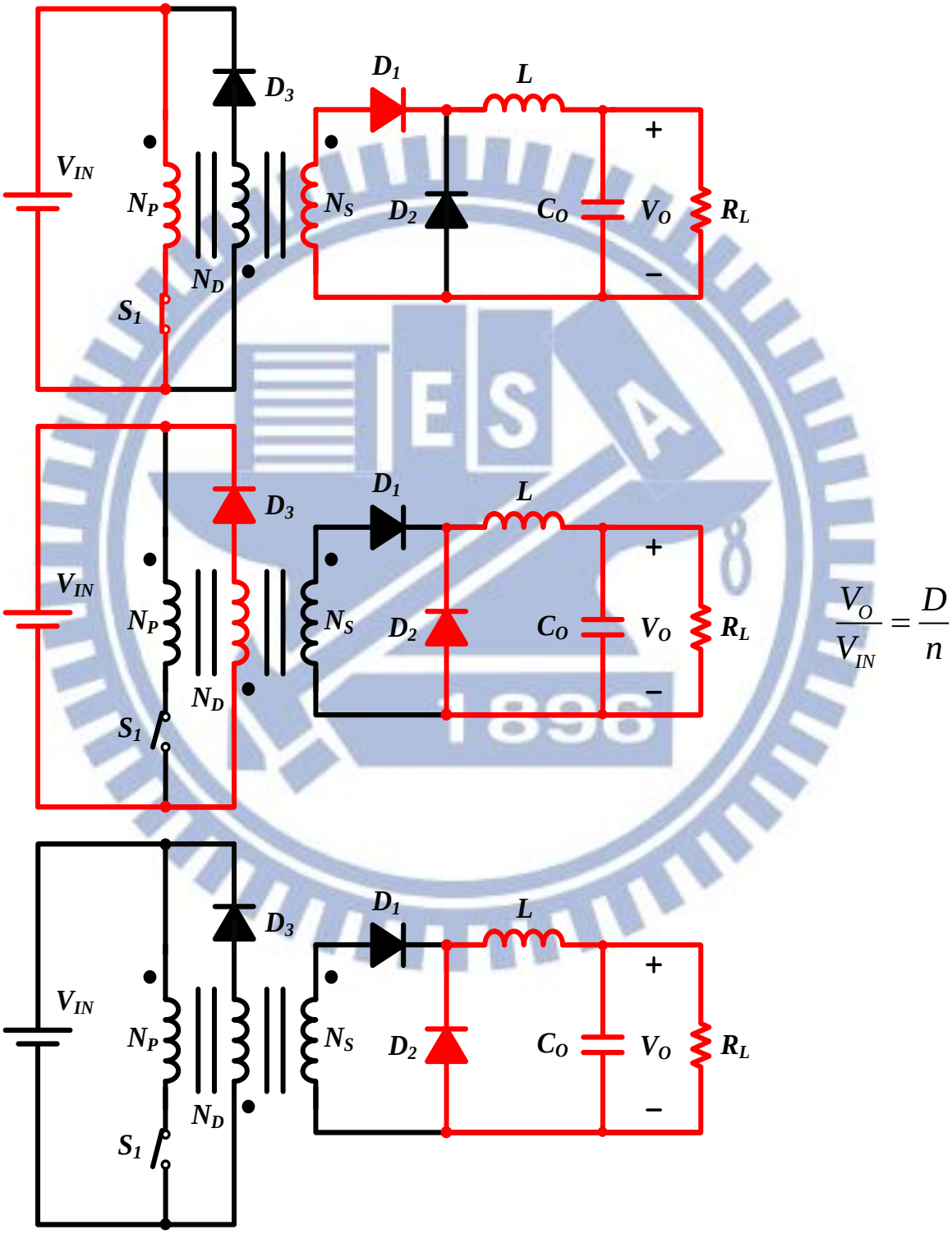
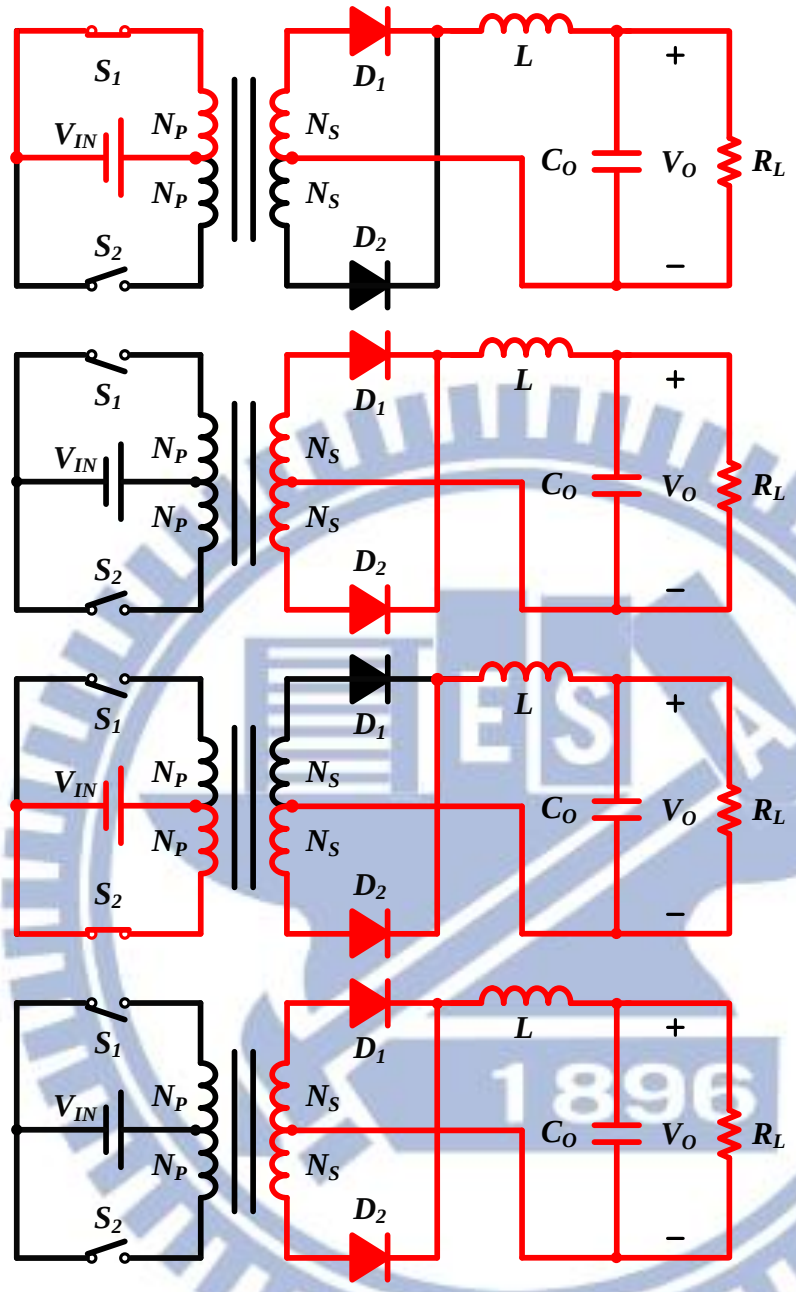


Fig. 3. Forward converter.

1.1.2 Architecture of Symmetrical Isolated Converters

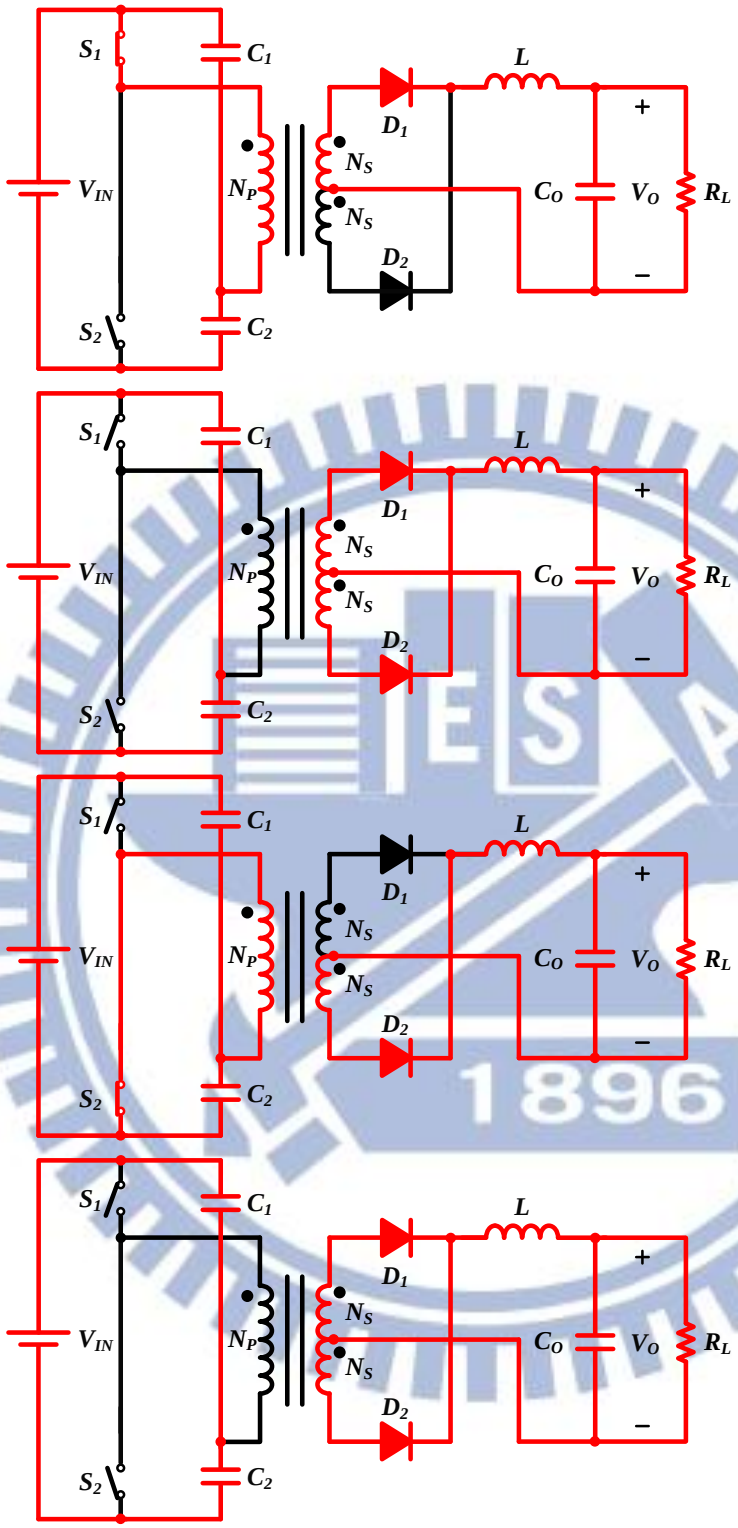
There are three types of symmetrical isolated converters will be introduced below. Firstly, push-pull has two switches and two diodes as shown in Fig. 4. S_1 and S_2 switches are alternately turned on. The push–pull converter is also a type of DC-to-DC converter, a switching converter that uses a transformer to change the voltage of a DC power supply. The distinguishing feature of a push-pull converter is that the transformer primary is supplied with current from the input line by pairs of transistors in a symmetrical circuit. The transistors are alternately switched on and off, periodically reversing the current in the transformer. Therefore current is drawn from the line during both halves of the switching cycle. This contrasts with buck-boost converters, in which the input current is supplied by a single transistor which is switched on and off, so current is only drawn from the line during half the switching cycle. During the other half the output power is supplied by energy stored in inductors or capacitors in the power supply. Push-pull converters have steadier input current, create less noise on the input line, and are more efficient in higher power applications.



$$\frac{V_O}{V_{IN}} = \frac{2D}{n}$$

Fig. 4. Push-pull converter.

Fig. 5 shows the PWM half bridge DC-DC converter, which contains two transistors, a transformer and a rectifier. It main advantage is that the voltage stresses of the transistors are low and equal to the maximum dc input voltage of converter. Another advantage is that the core saturation problems are minimized because the dc component of the current through the primary is zero due to the coupling or blocking capacitors in series with the primary. This topology can be used for an output power capability up to 500W.



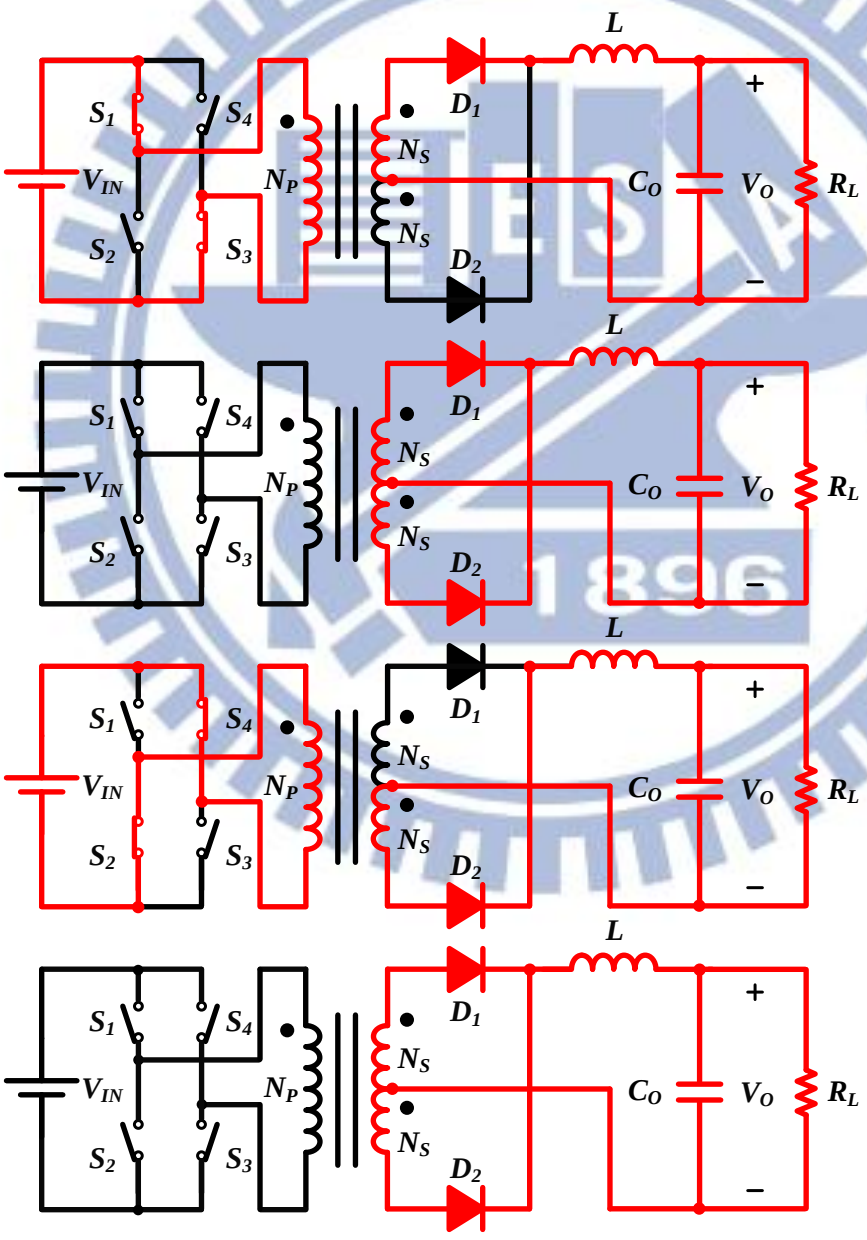
$$\frac{V_O}{V_{IN}} = \frac{D}{n}$$

Fig. 5. Half-bridge converter.

Fig. 6 shows the structure of full bridge converter. Because of the number of components, the full bridge is for high power applications, ranging from 500 up to 2000W. Sometimes, power transformers are paralleled to provide higher output power. Switch pairs S_1 and S_3, S_2

and S_4 are alternately driven. The full bridge provides twice the output power of the half bridge circuit with the same switch ratings. Nevertheless, this topology requires four switches and clamping diodes.

Many types of isolated converter are designed for different application according to the output voltage and load current. And the power supply designs are often tailored to specific applications. For the lower power application such as LED tube and notebook, the flyback converter is used in this thesis.



$$\frac{V_O}{V_{IN}} = \frac{2D}{n}$$

Fig. 6. Full-bridge converter.

1.2 Motivation

Almost all high-performance portable products use rechargeable batteries, because it is reusable for green energy. Also the personal computer now is used to synchronous with portable device through USB. So charging the battery from AC input through USB becomes the important issue in nowadays. The most common charging method in present days is the CC-CV (Constant Current-Constant Voltage) method. First, the charger charges the battery in constant current to the specified voltage. Once the battery reaches the rated voltage, the charger enters the constant voltage mode and keeps the battery in stable voltage.

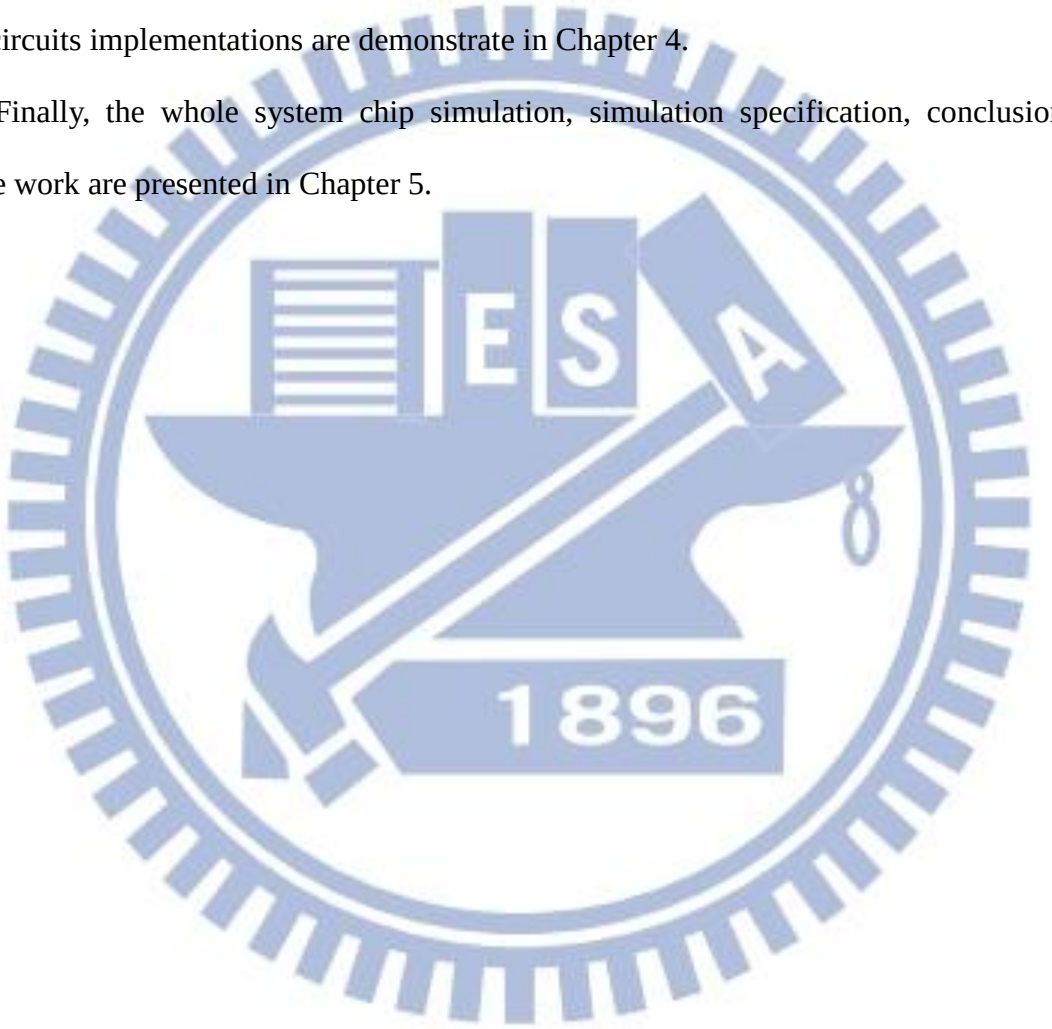
To protect the battery from being overcharged, the charging process needs to switch from CC phase to CV phase to gradually reduced the charge current until the process is finished [8] [9]. So the transition time of two phases is also needed to be carefully designed. How to sense the correct output voltage and current is the key point to changing precisely from CC to CV.

This thesis proposed a robust isolated switch-mode charger instead of a conventional charger to guarantee the protection for application of portable product. For the entire isolated converter, flyback converter appears commonly in the electrical devices around modern people because of the lower output power application. The combination of flyback converter for charger application is called primary side regulator (PSR). This proposed PSR is using self-calibration knee voltage detection (KVD) technique to achieve the correct sensing voltage. By changing the CC and CV phase precisely to prevent overcharge, it can also enhance the efficiency of whole system.

1.3 Thesis Organization

The thesis introduces the isolated charger PSR based on flyback converter and charging sequence. The basic concept and operation of flyback converter organized in Chapter 2. The proposed CC and CV regulation method compare to conventional is described in Chapter 3. The circuits implementations are demonstrate in Chapter 4.

Finally, the whole system chip simulation, simulation specification, conclusions and future work are presented in Chapter 5.



Chapter 2

Basic Definition Principles of Flyback Converters

From the previous discussion, the isolated converter plays an important role in the use of high input voltage application. Also the flyback converter has many advantages in low power application. In order to understand the concept of the flyback converter, this chapter first described the operation of flyback converter in different modes. In addition, the consideration between modes is described in this chapter. The efficiency also considered into the operation. One of the control methods named Quasi-Resonant (QR) is used in the CV regulation to save the efficiency. Besides, the non-ideal effect is demonstrated after the modes description. These non-ideal factors affect the design of this topology. Then the efficiency and losses of the power system will also demonstrate in this chapter.

2.1 The Basic Operation of Flyback Converter

All of the DC-DC converters' operation can be classified into discontinuous conduction mode (DCM) and continuous conduction mode (CCM) according to its switching timing. Continuous conduction mode means that the current in the energy transfer inductor never goes to zero between switching cycles. In discontinuous conduction mode (DCM) the current goes to zero during part of the switching cycle. Flyback converter can be operated in both modes depending on whether the primary inductance of the transformer is completely demagnetized or not. Fig. 7 shows the ideal waveform of flyback converter operating in DCM and CCM. The flow current of I_P and I_S represent the transformer's primary winding current and secondary winding current. I_O is the average current of output. And the V_S mean the voltage across power switch.

In DCM operation, the primary side current rises with the slope V_{IN}/L_m during the on time of power switch. L_m is the magnetizing inductance of transformer. And the secondary current falls with the slope V_{IN}/L_m, when the switch turns off. Therefore, it makes the current form a triangular wave. During the on time, the voltage across switch is the sum of input voltage and reflected voltage from output. Once the secondary current decreases to zero, the drain voltage drops to V_{IN}. On the other hand, the CCM operation makes the transformer's current never reach to zero. And the V_S is always at $V_{IN}+(N_P/N_S)V_O$ during the switch is off.

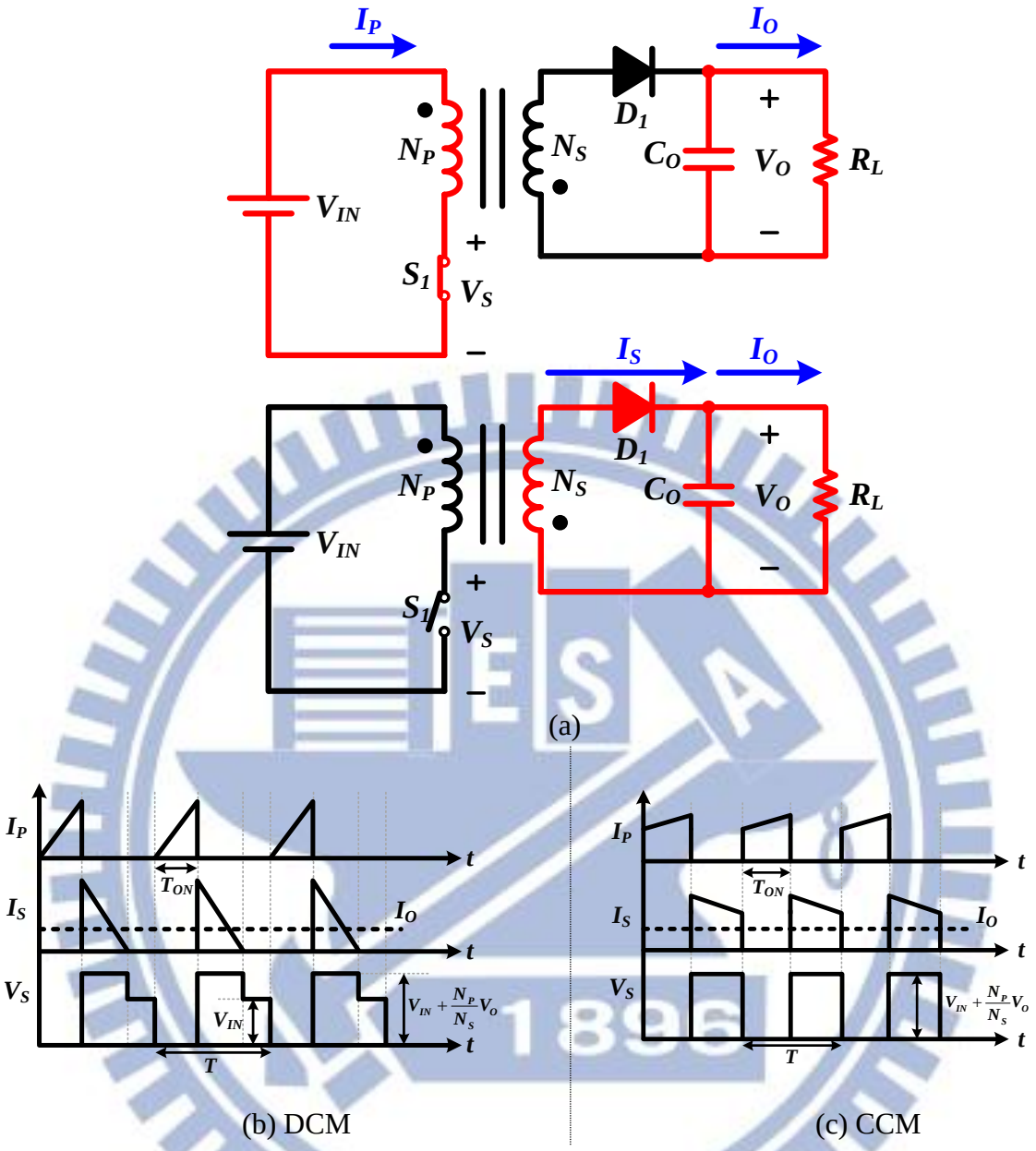


Fig. 7. Flyback converter operates in DCM and CCM.

To analyze the DCM and CCM in detail, each mode has its own advantages and drawbacks. The DCM operation has many merits such as the zero turn on losses for the power switch, good line and load transient response, the feedback loop has only single pole is easy to stabilize, the smaller transformer size because of the sharper current slope, and the recovery time of rectifier is not critical that means current is zero well before reverse voltage is applied. But DCM operation still have some disadvantage such as the larger output ripple and high peak currents in rectifiers and power switches.

The CCM operation is only good at small output ripple and the peak current of rectifier and switch is half the value of discontinuous mode. And its drawbacks are the rectifier losses of recovery time and the loop is difficult to stabilize owing to the two poles and right half plane zero.

TABLE II shows the comparison table of the flyback converter's operation between DCM and CCM. The blue color means the better performance than the other, and the red is opposite. Consequently, according to the table, the DCM operation in flyback converter has more advantages, so the DCM operation is common in flyback converter's control IC.

In general, flyback converter appears commonly in the electrical devices around modern people because of the lower output power application. Flyback converter has been employed operating both in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) as well as critical conduction mode (CRM), boundary between CCM and DCM. Compared with CCM, BCM enjoys benefits such as soft switching, fast transient response, smaller transformer, and easier compensation for system's stability [10] - [12].

TABLE II
Comparison of flyback converter operating at CCM and DCM

	DCM	***CCM***
Transformer size	***Small***	***Large***
Peak current of switch	***Large***	***Small***
Output ripple	***Large***	***Small***
Recovery time rectifier	***Small***	***Large***
Loop compensation	***Easy***	***Hard***
Line/Load transient response	***Fast***	***Slow***
Soft switching	***Yes***	***No***

2.2 Non-Ideal Phenomenon of Flyback Converter in DCM

The concept of flyback converter introduced in section 2.1 is the ideal. But flyback converter has non-ideal phenomenon. This section is describing the non-ideal when realize the flyback converter. First of all, the transformer has magnetizing inductance L_m. However, transformer also has leakage inductance L_K as shown in Fig. 8 (a). Leakage inductance is the property of an electrical transformer that causes a winding to appear to have some inductance in series with the mutually-coupled transformer windings. This is due to imperfect coupling of the windings and creation of leakage flux which does not link with all the turns of the winding. The leakage flux alternately stores and discharges magnetic energy with each electrical cycle and thus effectively acts as an inductor in series in each of the primary and secondary circuits. Leakage inductance is primarily caused by the design of the core and the windings.

To reduce the effect of L_K to the system, a simple circuit called snubber is applied, which composed by C_S, R_S and D_S in Fig. 8 (a). It can be used in electrical systems with an inductive load to suppress instantaneous voltage spike across the power switches in case of sudden current flow. Transient voltage variation will be a source of electromagnetic interference (EMI) in other circuits. Additionally, if the instantaneous voltage spike across the device is beyond what the devices can tolerate, it may damage or destroy the devices. Thus, the snubber provides a short-term alternative current path around the current switching device so that the inductive element may be discharged more safely and quietly.

Inductive elements are often unintentional, but arise from the current loops implied by physical circuitry. While current switching is everywhere, snubbers will generally only be required where a major current path is switched, such as in power supplies. Snubbers are also often used to prevent arcing across the contacts of relays and switches and the electrical

interference and welding/sticking of the contacts that can occur. In flyback converter, snubber is used to give a path to leakage inductance's resonant.

Second, the switch S_1 has the parasitic capacitor C_{DS}. It is an unavoidable and usually unwanted capacitance that exists between the parts of an electronic component. All actual circuit elements such as inductors, diodes, and transistors have internal capacitance, which can cause their behavior to depart from that of 'ideal' circuit elements. In addition, there is always non-zero capacitance between any two conductors. Also the forward diode D_1 has the forward drop V_D.

When switch turn off, the primary side current I_P is down to zero as shown in Fig. 8 (b). The magnetizing inductance L_m start to transfer energy to secondary side and make the current I_S starts to discharge. But there is only the magnetizing inductance can transfer energy, the leakage inductance has no path to secondary can discharge energy. Leakage inductance can only discharge to parasitic capacitor C_{DS}, and V_S start the first resonant in T_{LK} cause by L_K and C_{DS}. Also V_S reflect the output voltage V_O and forward voltage V_D. The forward voltage V_D is decreasing with I_S decreasing. When secondary current is discharging to zero, the forward voltage V_D is also zero. The reflected voltage only remain V_O. V_S is $V_{IN}+(N_P/N_S)V_O$ at the end of discharge time. Also the charges in C_{DS} start to discharge to L_m and resonant to each other until next cycle. The resonant of C_{DS} and L_m makes the V_S have many valleys in T_{RE}. It can make the valley voltage down to nearly zero. By using these valleys properly, the flyback converter can turn to the next cycle in soft switching and improve the efficiency. This soft switching technique by turning on the switch when resonant to valley is also called Quasi-Resonant (QR) control in flyback converter.

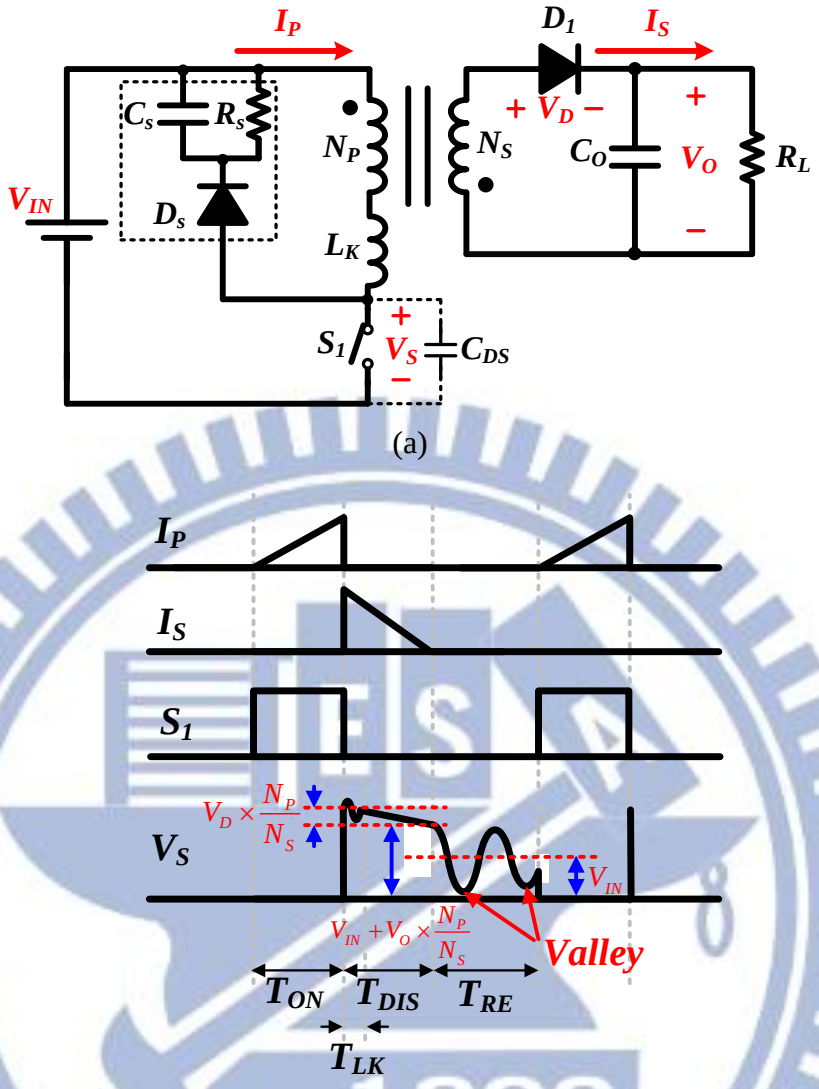


Fig. 8. (a) Non-ideal flyback converter. (b) Waveform of flyback converter.

2.3 Losses and Efficiency Analysis

Power loss of switching regulators is the combination of the switching loss and the MOSFET's conduction loss as shown in equation (1). The power loss is important factor to determine efficiency and it is briefly introduced as following.

$$P_{MOSFET} = P_{SW} + P_{COND} \tag{1}$$

2.3.1 Conduction Loss

The conduction loss is mainly related to high-side transistor loss and low-side transistor loss. High-side conduction loss is calculated straightforward that is just the I^2R loss timing the MOSFET's duty cycle as below:

$$P_{COND} = I_{OUT}^2 \cdot R_{DS(ON)} \cdot \frac{V_{OUT}}{V_{IN}} \tag{2}$$

Where $R_{DS(ON)}$ is at the maximum equivalent resistor on operation MOSFET.

In the same way, low-side conduction loss is determined as (3).

$$P_{COND} = I_{OUT}^2 \cdot R_{DS(ON)} \cdot (1 - \frac{V_{OUT}}{V_{IN}}) \tag{3}$$

2.3.2 Switching Loss

The switching interval begins when the high-side MOSFET driver turns on and begins to supply current power MOSFET's gate to charge its input capacitance. The switching loss is involved of the charge on the parasitic capacitor of switching node. Therefore, there is no switching loss until V_{GS} reaches the low-side MOSFET's V_{TH}.

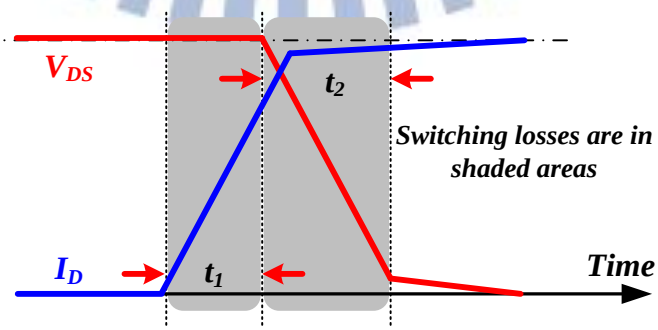


Fig. 9. Transient waveform of V_{DS} and I_D curve in switching losses on power MOSFET.

When V_{GS} reaches V_{TH}, the input capacitance of gate is being charged and the MOSFET's drain current I_D is rising up linearly until it reaches the current I_L which is presumed to be I_{LOAD}. During this period (t_1) the MOSFET is sustaining the entire input voltage V_{IN} across it, the energy in MOSFET during t_1 is:

$$P_{t_1} = t_1 \cdot (\frac{V_{IN} \cdot I_{LOAD}}{2}) \quad (4)$$

Sequentially, as the beginning time of second period t_2, the current flowing through high-side MOSFET is I_{LOAD}, and the V_{DS} begins to fall. All of the gate current will be going to recharge C_{GD}. C_{GD} is similar to the "Miller" capacitance of transistor, so t_2 could be thought of as "Miller time". During this time the current is constant as I_{LOAD} and the voltage is falling fairly linearly from V_{IN} to 0, therefore:

$$P_{t_2} = t_2 \cdot (\frac{V_{IN} \cdot I_{OUT}}{2}) \quad (5)$$

The total switching loss for any given edge is just the power that occurs in each switching interval, multiplied by the duty cycle of the switching interval:

$$P_{SW} = (\frac{V_{IN} \cdot I_{OUT}}{2}) \cdot (t_1 + t_2) \cdot F_S \quad (6)$$

2.3.3 Quiescent Loss

The quiescent loss also called as static loss that was consumed by other controllers of switching regulators. The smaller quiescent loss also causes higher efficiency.

$$P_Q = V_{IN} \cdot I_Q \quad (7)$$

The other power losses that don't be mentioned above obeyed the rules of I^2R.

2.3.4 Efficiency

The efficiency of switching regulator is defined as the ratio of the output power consumption and input power supplies, which is formed as below equation (8):

$$E_{ff} = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_O + P_{SW} + P_{COND} + P_Q + P_{Else}} \times 100\% \quad (8)$$

The total power consumption of input power supplies is involved of the output consumption (P_O), switching loss (P_{SW}), conduction loss (P_{COND}), quiescent loss (P_Q), and other losses (P_{Else}) in parasitic elements. A high efficiency results in a high performance extending the battery life.

Chapter 3

The Proposed Primary-Side Regulator with Self-Calibration Knee Voltage Detection (KVD) Technique

In this chapter, the primary-side regulator (PSR) is adopted to the design of flyback converter to show some significant advantages compared to conventional flyback converter. Furthermore, the self-calibration knee voltage detection (KVD) technique is presented to get rid of the disadvantage of inaccuracy caused by the remove of the feedback path from the opto-coupler. That is to say, the charger implemented by the PSR flyback converter must have the precise sensing technique, self-calibration knee voltage detection (KVD) technique, to ensure accurate charging process.

3.1 Significant Advantages of PSR Flyback Converter Compared to Conventional Design

Figs. 10 (a) and (b) illustrate the architecture of conventional flyback converter and the PSR flyback converter, respectively. In Fig. 10(a), conventional flyback converter uses one feedback from the secondary side through the use of the opto-coupler. Unlike the power stage discussed in chapter 2, the transformer also includes the auxiliary winding N_A to reflect the input and output voltage information to the controller and to provide energy to the V_{DDH} after

the start-up procedure is ended. The *opto-coupler* and the *TL431* work as the error amplifier to get the output voltage information, V_{FB}.

The PSR as shown in Fig. 10 (b) is similar to flyback converter mostly. The difference between flyback converter and PSR is the external components of *opto-coupler* and *TL431*. Instead sensing output voltage by external component, PSR is using auxiliary winding N_A to replace it. Compared with the conventional secondary-side regulation approach, the PSR can reduce the total cost, component count, size and weight.

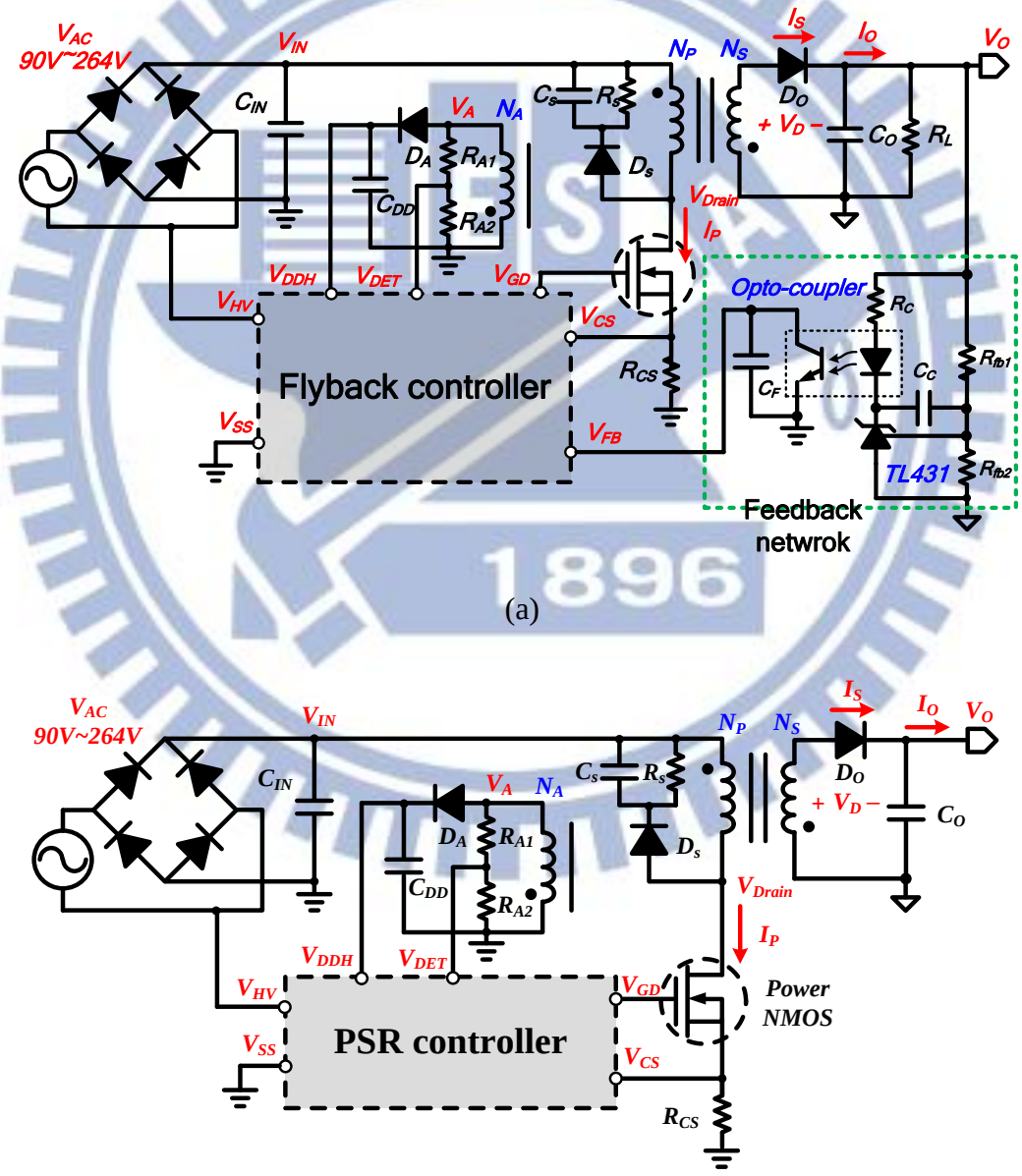
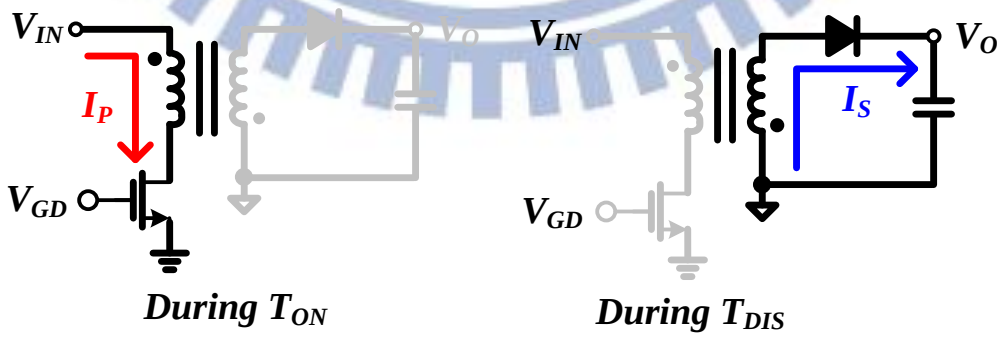


Fig. 10. (a) Conventional flyback converter. (b) Flyback converter with the PSR controller.

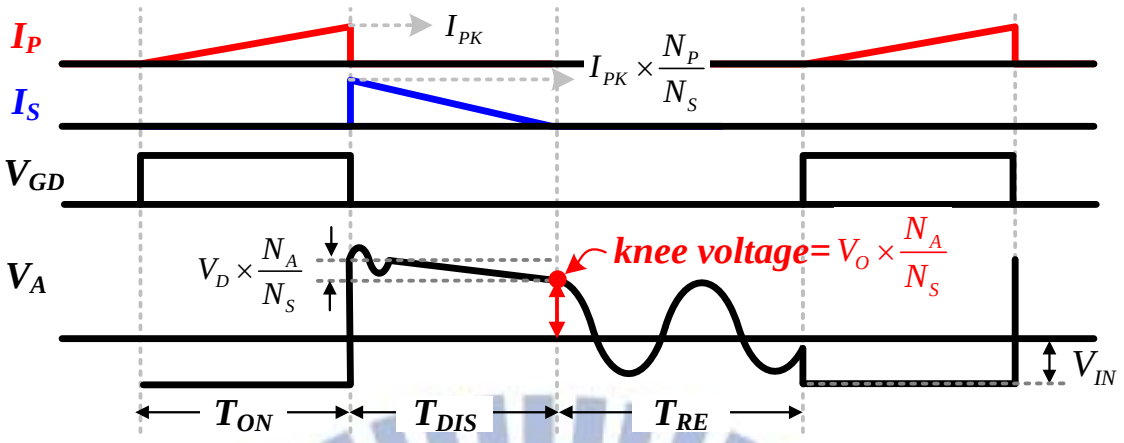
3.2 The Conventional Control of PSR

Conventional PSR system structure is depicted in Fig. 10 (b). The input bulk capacitor C_{IN} is used after full-bridge rectifier to reduce the AC line voltage ripple, which has the switching frequency of 120 Hz. Thus, the V_{IN} has a near DC voltage. Besides, the current sensing resistor R_{CS} is used to sense input line current. The auxiliary winding N_A can not only sense the output voltage V_O through the voltage divider (R_{A1} and R_{A2}) to get the voltage V_{DET} for the controller but also provide the power to the V_{DDH} if the controller works correctly.

Fig. 11(a) shows the basic operation of PSR. Instead of using secondary feedback components, the PSR can use the auxiliary winding to get the information of the output voltage V_O. During the inductor current discharge time T_{DIS}, the summation of the output voltage V_O and the diode forward voltage drop V_D is reflected to the auxiliary winding as the signal V_A. It is hard to get only the V_O information without being affected by the V_D from the V_A. Fortunately, at the end of the diode conduction time as depicted in Fig. 11(b), the auxiliary winding voltage simply reflects the V_O because the diode forward voltage drop decreases to zero as the diode forward current decreases to zero. By sampling the winding voltage at the end of the diode conduction time, the V_O information can be obtained as the knee voltage, $(N_A/N_S)*V_O$.



(a)



(b)

Fig. 11. (a) Operation of the PSR power stage. (b) Knee voltage reveals the V_O information.

Several literatures have been proposed to accurately get the information of knee voltage [13] - [15]. Sampling pulse generator as depicted in Fig. 12 (a) is used to emulate the charging and discharging of the inductor current [13]. The current source I_1 combine with n-transistor M_1 and capacitor C_1 are used to be a delay circuit. The I_4, M_4 and C_3 also do the same work. When the gate signal V_{GD} is on, the p-transistor M_2 is also turned-on. The current source I_2 then charges the capacitor C_2 to produce a charge time. When V_{GD} is off, the n-transistor M_3 is turned-on. The capacitor C_2 is discharged by current source I_3 to produce discharge time that is proportional to the charge time. When the voltage across C_2 is discharged to zero, it also means the discharge time is over. Then sampling pulse V_{SP} is triggered to sample V_A as knee voltage.

However, the discharging slope of inductor current is proportional to the output voltage V_O. When output voltage is not equal to expected voltage, some error operation will occurred as depicted in Fig. 12 (b). If the expected voltage higher then output voltage, the too early operation will occur and the sampling voltage will higher than knee voltage. On the other hand, if the expected voltage lower then output voltage, the too late operation will occur and the sampling voltage will lower than knee voltage. In worst case, it may sample the zero voltage.

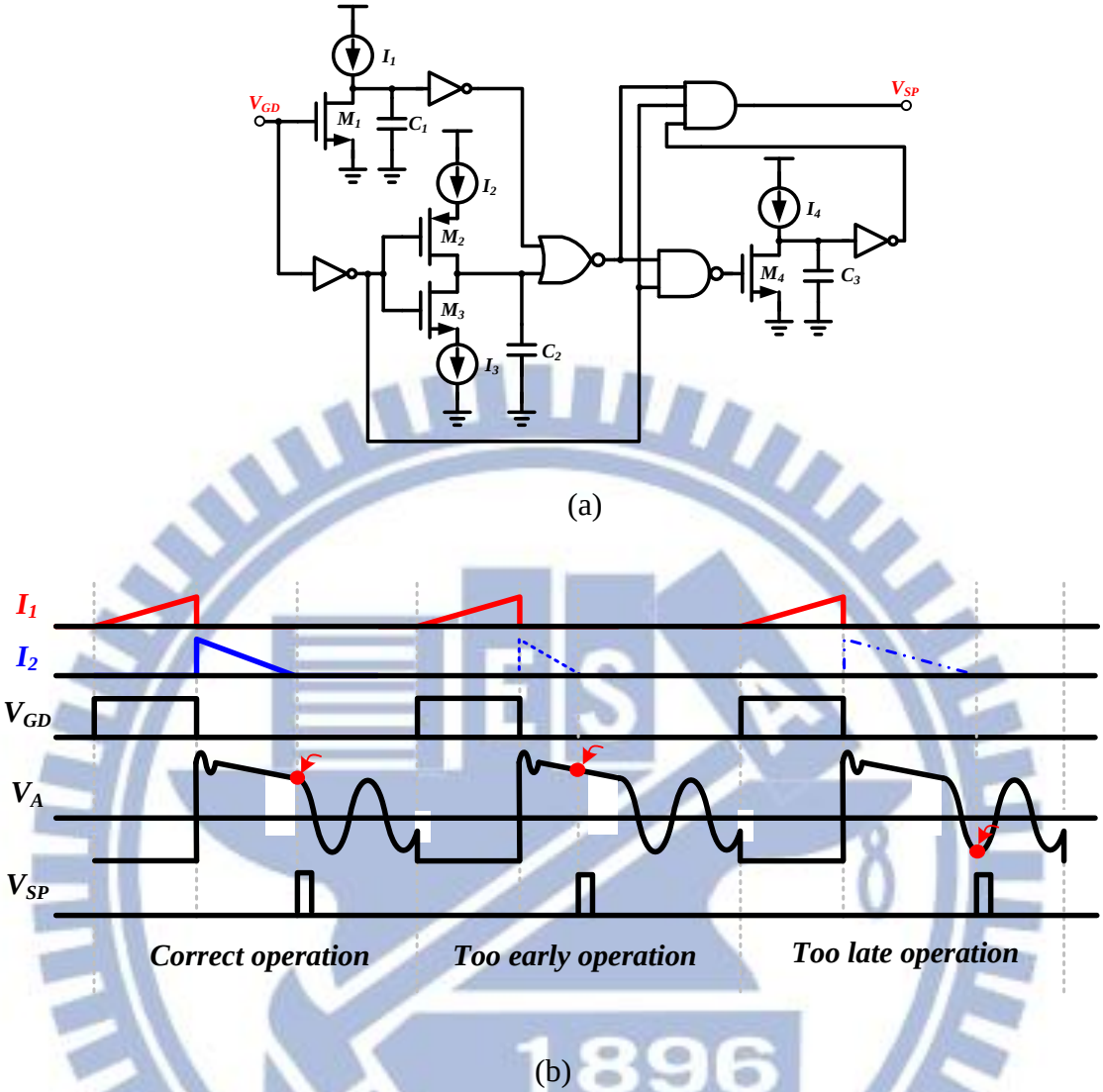


Fig. 12. (a) Sampling pulse generator. (b) Sampling pulse with different expected voltage's operation.

On the other hand, the regulation of V_O can be changed to regulate the summation of the V_O and the V_D. In [14], the summation of the V_O and the V_D can be derived by the proposed circuit in Fig. 13 (a). The V_O is expected to be regulated to V_{REF}. The V_D information can be got by the primary side current signal V_I. Therefore, the new reference V_{REF1} is equal to $V_{REF} + \frac{V_I}{R_1} \cdot \frac{R_3}{R_2} \cdot R_{ext}$. That is to say, if the sampling voltage **in the beginning of the discharging period after a blanking time** should be regulated to V_{REF1}, the V_O can be approximately regulated to the V_{REF} as shown in Fig. 13 (b).

However, the disadvantage is that it needs the external resistor R_{ext}. Because of the different forward diode has different forward voltage V_D. Using the same resistor cannot emulate different V_D correctly. An external resistor increase the cost and component count.

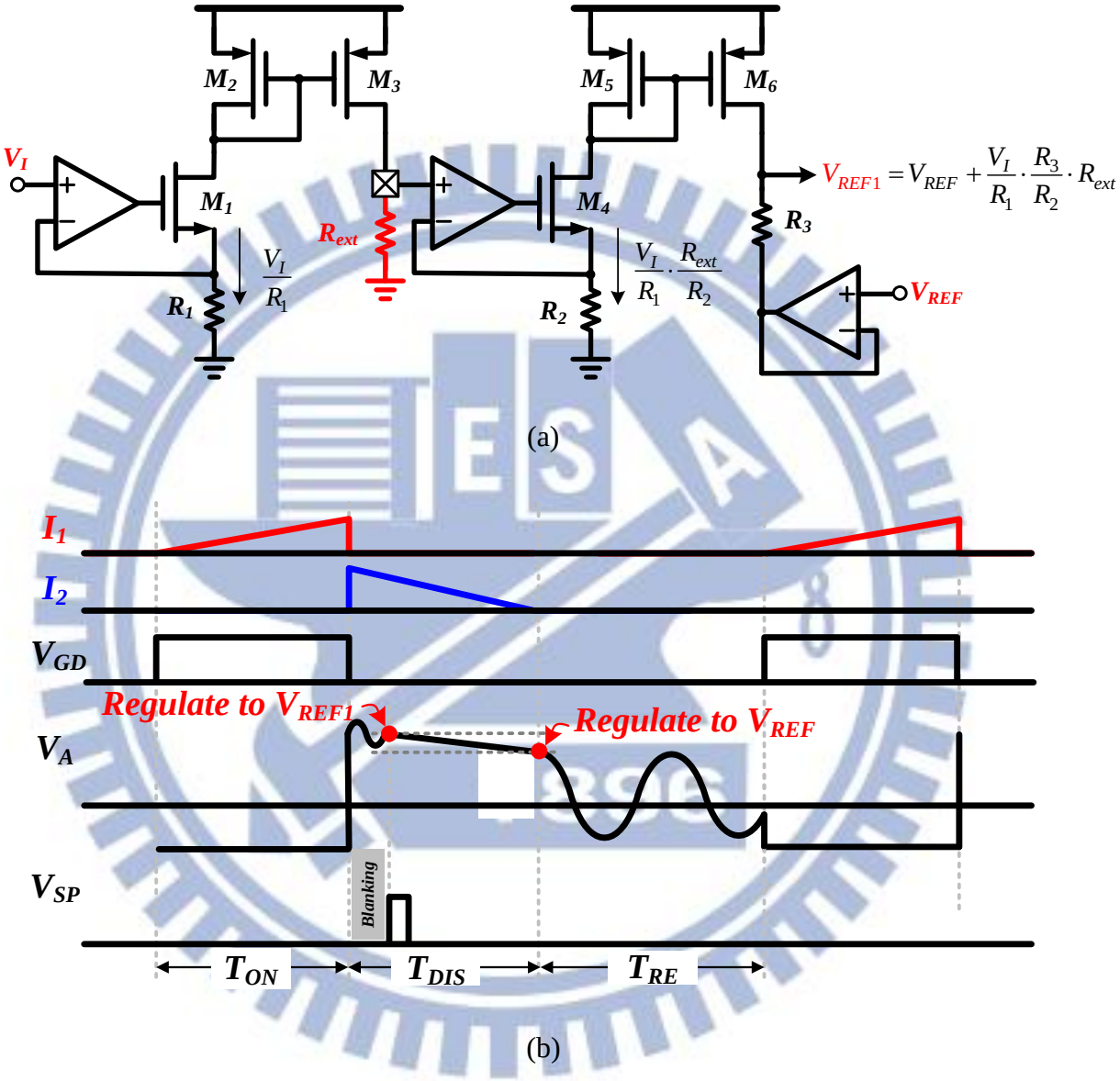


Fig. 13. (a) Adjust circuit. (b) Different regulation reference.

In [15], one RC circuit is utilized to generate a delayed waveform V_{DELAY} of the signal V_{DET} from the auxiliary winding. The original signal V_{DET} is used to determine the sampling time of the knee voltage from the V_{DELAY}. That is to say, in the beginning of the resonant period T_{RE} when the inductor current decreases to zero, the slope of the V_{DET} becomes extremely sharp. By comparing the slope of V_{DET} to a threshold value, it can determine if the

V_{DET} is in resonant period or not. Then sample the V_{DELAY} for knee voltage as depicted in Fig. 14.

However the slope of V_{DET} in resonant period depends on the LC values, which are transformer's magnetizing inductance L_m and power MOSFET parasitic capacitor C_{DS}. By using constant value compare to the slope of V_{DET} to determine the sampling time also needs to adjust the RC values for V_{DELAY} according to different LC values that can sample the correct knee voltage. In order to adjust the RC value, it needs external components. That also increase the cost and component count.

Fig. 14. The S/H of knee point according to V_{DET} and V_{DELAY}.

3.3 The Proposed Charger by the PSR Controller with the KVD Technique

The proposed PSR controller with the KVD technique is shown in Fig. 15. Similarly, the DCM is utilized in the PSR controller. Here, the PSR controller is used to control the charging process of the Li-Ion battery. That is to say, the PSR controller needs to have two control loops to provide the charging procedure of the constant current (CC) and the constant voltage (CV) stages.

The current information V_{CS} in (9) is derived from the primary side current I_P flowing through the sensing resistor R_{CS}, which is connected between the source of the power MOSFET and ground.

$$V_{CS} = I_P \times R_{CS} \text{ and } V_{CS,PK} = I_{PK} \times R_{CS} \text{ where } I_{PK} \text{ is the peak current.} \quad (9)$$

The V_I is proportional to the integration of the peak current information I_{PK} within one discharging time T_{DIS} in the current calculator circuit. Here, the T_{DIS} can be used to decide the integrating time. In the current loop, the modulation of the on-time of the CC stage is decided by the comparison result of the V_{RAMP} and the V_{ERR_I}, an error signal derived at the output of the error amplifier 1 (EA 1). As a result, the V_I can be regulated to the reference voltage V_{REF_I} to ensure constant current. Here, the CC stage is controlled by a constant switching frequency, which is determined by the oscillator OSC with a pulse signal V_{PULSE} as depicted in Fig. 16.

Here, the secondary side peak current $I_{S,PK}$ can be expressed by the I_{PK} and shown in (10) according the turn ratio of N_P/N_S where the primary winding and the secondary winding have N_P turns and N_S turns, respectively.

$$I_{S,PK} = I_{PK} \times \frac{N_P}{N_S} = \frac{V_{CS,PK}}{R_{CS}} \times \frac{N_P}{N_S} \quad (10)$$

Thus, the average output current can be expressed as (11).

$$I_{O,avg} = \frac{1}{2 \times T_S} \times I_{S,PK} \times T_{DIS} \quad (11)$$

Substituting for $I_{S,PK}$ from (10) gives (12).

$$I_{O,avg} = \frac{1}{2 \times T_S} \times \frac{V_{CS,PK}}{R_{CS}} \times \frac{N_P}{N_S} \times T_{DIS} \quad (12)$$

Interestingly, in the design of the PSR control, only two variables $V_{CS,PK}$ and T_{DIS} are needed to be determined. That can easily achieve CC regulation with constant switching frequency.

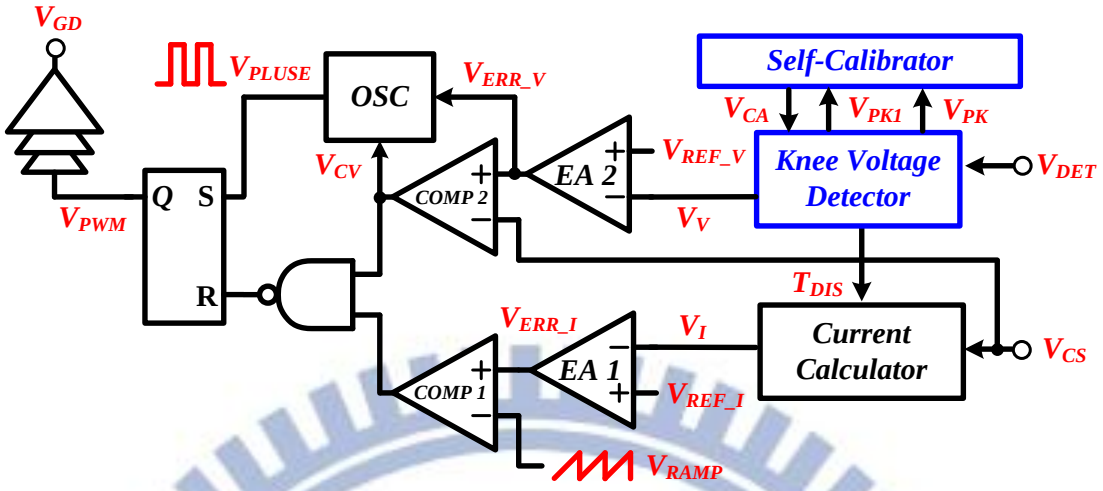


Fig. 15. Proposed PSR controller.

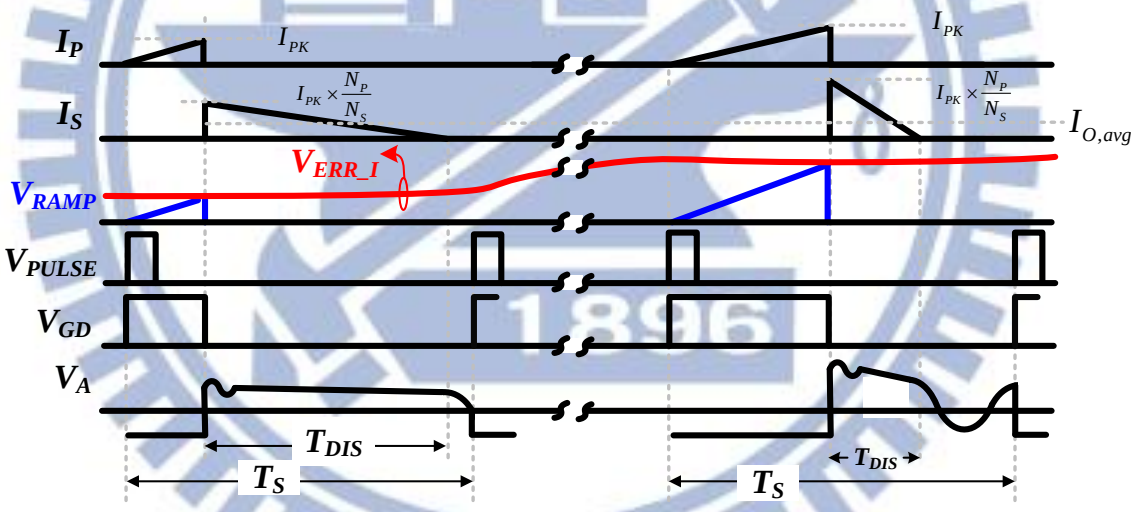


Fig. 16. Constant Current Operation in the PSR controller.

On the other hand, the other voltage loop is used for constant voltage (CV) stage. From the auxiliary winding N_A in Fig. 10(b), the voltage information V_{DET} is a scaled down value of the V_A by the voltage divider, composed of the resistors R_{A1} and R_{A2}. The knee voltage detector (KVD) and the self-calibrator circuit are designed to get accurate output voltage information. Thus, the knee voltage V_V can be got without being affected by the diode forward voltage V_D. The V_V can be regulated to be close to the reference V_{REF_V} by the voltage loop. In

the CV stage, the error signal V_{ERR_V} and the current sense signal V_{CS} are used to determine the on-time value as shown in Fig. 17. Besides, the switching frequency varies with the value of V_{ERR_V}. If the V_{ERR_V} becomes smaller, **the switching frequency will be extended by the *OSC* circuit to reduce the switching power loss** because the Quasi-Resonant (QR) technique is also used for zero voltage switching (ZVS) to improve the efficiency if there is a small input current.

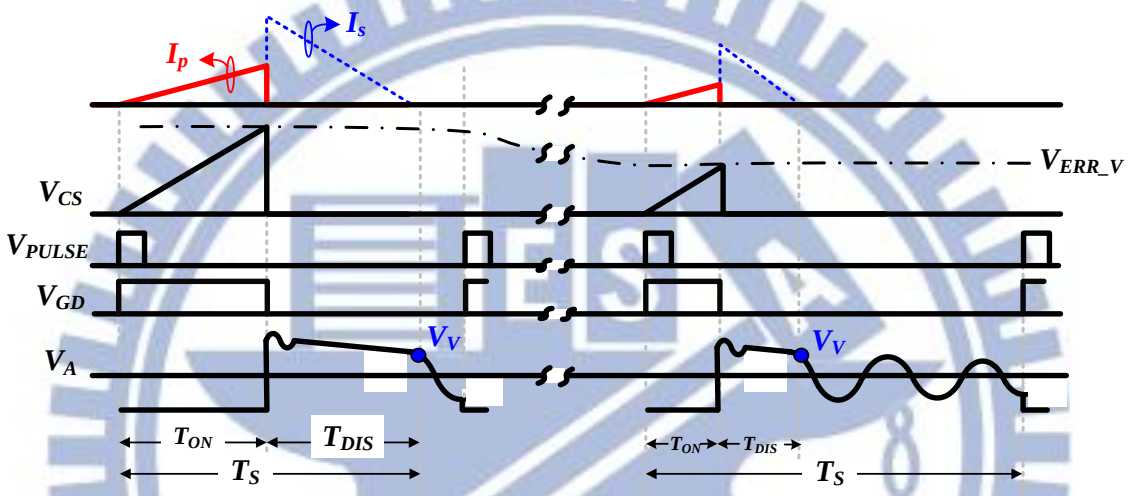


Fig. 17. Constant voltage operation in the PSR controller.

Fig. 18 shows the charging procedure of the battery charger. It includes the CC and the CV stages. In the CC stage, the output voltage V_O is charged from the minimum voltage $V_{O,min}$ to the nominal full-charged voltage $V_{O,max}$ with a constant switching frequency, which is equal to $1/T_S$. The value of the $V_{O,max}$ doesn't exceed the tolerance of the maximum allowable voltage of the battery while the $V_{O,min}$ can ensure the PSR operates in the DCM.

The discharging current rate is proportional to the V_O as shown in (13). ,where L_m is the magnetizing inductance of the transformer.

$$\frac{dI_S}{dt} = -\left(\frac{N_P}{N_S}\right) \times \frac{V_O}{L_m} \tag{13}$$

In Fig. 17, the I_{PK} and the T_{DIS} can be derived as shown in (14) and (15), respectively.

$$I_{PK} = \frac{V_{IN}}{L_m} \times T_{ON} \text{ where } T_{ON} = DT_S \tag{14}$$

$$T_{DIS} = \frac{I_{S,PK}}{\left(\frac{N_P}{N_S}\right)^2 \times \frac{V_O}{L_m}} = \frac{I_{PK}}{\left(\frac{N_P}{N_S}\right) \times \frac{V_O}{L_m}} = \frac{N_P}{N_S} \times \frac{V_{IN}}{V_O} \times T_{ON} \tag{15}$$

In case of minimum output voltage $V_{O,min}$, the T_{DIS} in (15) has a maximum value of $T_{DIS,max}$. To ensure the discharging phase can be finished within one constant switching period T_S, the inequality in (16) should be made. That is, the operation is always kept in the DCM due to the inductor current can be decreased to zero within one switching period.

$$T_{ON} + T_{DIS,\max} = T_{ON} + \frac{N_S}{N_P} \times \frac{V_{IN}}{V_{O,\min}} \times T_{ON} \le T_S \tag{16}$$

Therefore, the initial point of the output $V_{O,min}$ for the CC operation can be derived as shown in (17).

$$V_{O,\min} \ge \frac{D}{1-D} \times V_{IN} \times \frac{N_S}{N_P} \tag{17}$$

In other words, the startup circuit should ensure the output voltage is charged to $V_{O,min}$ first. Then, the charger is switched to the CC operation with a constant current defined by the reference voltage V_{REF_I}. Once the output is charged to the $V_{O,max}$ with a constant switching freuqency, the charger will be changed to the CV operation. In CV operation, the switching frequency varies with the value of the V_{ERR_V}. Besides, the QR technique is effectively used to decrease the switching frequency for high efficiency. Consequently, the V_O is finally regulated to the $V_{O,max}$ with a decreased charging current to end the whole charging function.

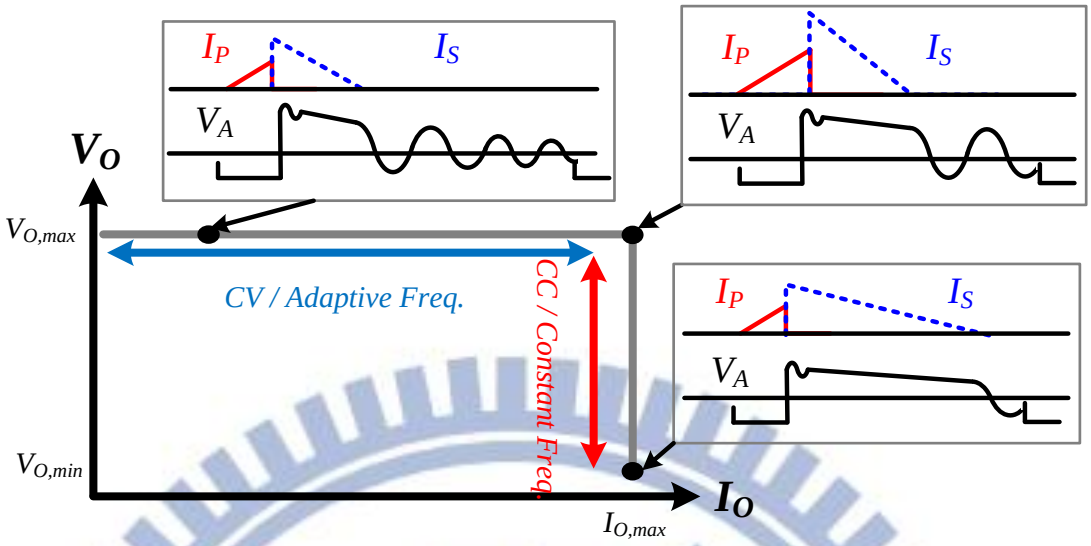


Fig. 18. The definition of CC/CV operation with output current/voltage.

The transition from the CC to the CV is depicted in Fig.19. The on-time value is determined by the V_{RAMP} and the V_{ERR_I} in the CC operation. On the other hand, the on-time value is determined by the V_{ERR_V} and the V_{CS}. In the beginning of the charging procedure, the duty cycle is determined by the CC operation because the duty cycle decided by the CV operation is too large under a high V_{ERR_V}. Once the V_O is gradually charged to the nominal value, the V_{ERR_V} will be pulled lower than the V_{ERR_I}. The transition from the CC operation to the CV operation happens. In other words, the duty cycle decided by the CV operation will be smaller than that of the CC operation. Thus, a smooth transition can be made. Here, a flag signal V_{CV} is used to indicate the CV operation is enabled and to decrease the switching frequency. The CV operation uses the adaptive valley selection method to decrease the switching frequency. The adaptive valley selection method depends on the decreasing output current to accordingly decrease the switching frequency for reducing switching power loss in the CV operation. Once the charging current is lower than a predefined value, the green mode is utilized to further reduce the switching power loss. Here, the green mode uses an ultra-low switching frequency for high efficiency.

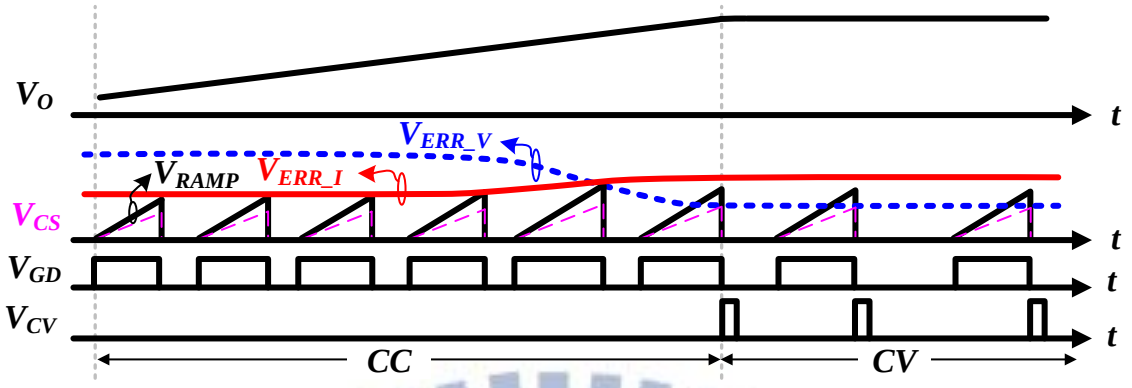


Fig. 19. The transition from the CC operation to the CV operation.

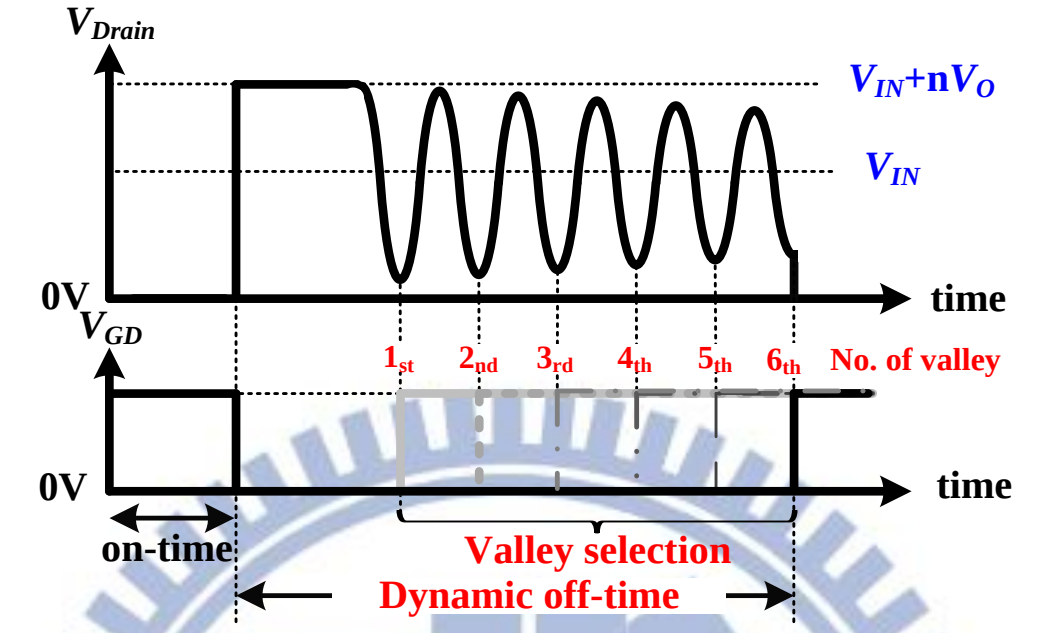
The stored energy in the primary winding (N_P) starts to transfer to the output once the V_{GD} changes from high too low to turn off the power MOSFET as depicted in Fig. 20(a). Due to Lenz's Law, the V_{Drain} at the drain of power MOSFET jumps from zero to V_{IN}+nV_O. At this moment, the secondary current decreases toward zero, the parasitic capacitance C_{DS} at the V_{Drain} starts to discharge the stored charges to the L_m and induce voltage resonance at the V_{Drain}. Resonant effect with resonant frequency determined by C_{DS} and L_m is reflected to the auxiliary side simultaneously. To reduce switching loss, the optimum turn-on time happens at the valley of the V_{Drain} due to near zero voltage switching. Thus, the valley voltage detection of the resonant effect can determine the next turn-on of the power MOSFET.

In case of large output load current, the first valley is an optimum selection to rapidly deliver energy to the output owing to minimum off-time. Theoretically, the switching loss dominates the total power loss in case of small output load current. That is to say the first valley is not the optimum selection at light loads. The dynamic frequency technique selects one of the valleys according to the output load current for reducing switching frequency and switching power loss. In other words, in this technique, dynamic off-time control can be

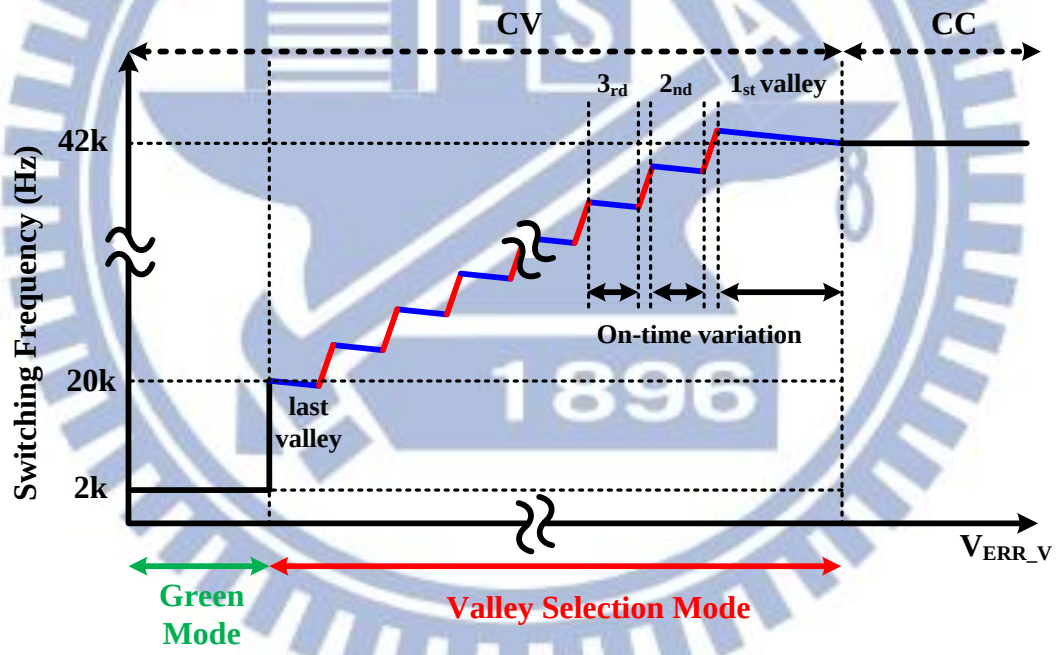
derived by the valley selection at different loads when the output load current decreases from large to small as illustrated in Fig. 20 (b).

At the CV stage, the error signal V_{ERR_V} is used to control the primary side current I_P so as to gradually decrease the output charging current I_O. If the output current continues to decrease, the switching frequency will locally increase in Fig. 20 (b) due to the decrease of the on-time if assuming that one of the valleys is selected; for example, the 2nd valley in Fig. 20 (c)) is selected. In other words, the selection of the valley can't continuously change from one valley to the other valley owing the quantization error at the valley selection. Once the valley selection is changed to the sequent next one, the switching frequency will have an instant decrease to further reduce the switching power loss. The local increase of the switching frequency won't result in large switching power loss. Contrarily, the instant decrease of the switching frequency caused by the change of the valley can greatly improve the efficiency.

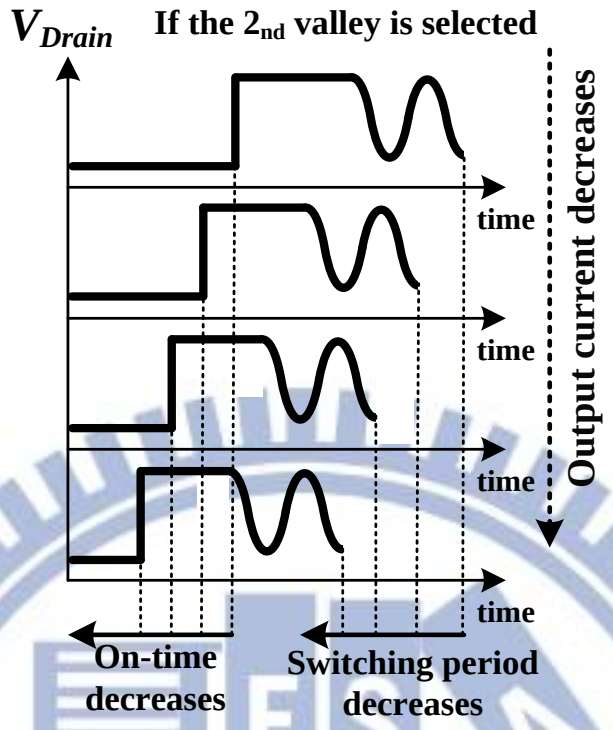
In summary, the trend of the switching frequency is decreasing when output charging current decreases. Simultaneously, the resonant amplitude becomes smaller because of the parasitic resistance at the resonant path. Gradually decreased resonant voltage may result in the failure of the valley voltage detection. That is to say, for safety the next on-time needs to be triggered by another mechanism. Thus, the green mode is proposed to set the off-time a constant value for ensuring the correct operation of the converter and further improving efficiency at ultra-low current. Besides, the charging current won't have over-current since the maximum current is limited by the CC regulation for system.


V_{Drain}
V_{IN}+nV_O
V_{IN}
0V
time
V_{GD}
1st 2nd 3rd 4th 5th 6th No. of valley
0V
time
on-time
Valley selection
Dynamic off-time

(a)


CV
CC
3rd 2nd 1st valley
42k
Switching Frequency (Hz)
On-time variation
20k
last valley
2k
V_{ERR_V}
Green Mode
Valley Selection Mode

(b)



(c)

Fig. 20. (a) The operation of the dynamic frequency technique. (b) The switching frequency versus the output current. (c) The slight variation of the switching frequency if one of the valley voltages is selected.

Chapter 4

The Proposed KVD Technique

The proposed KVD technique includes the current calculator, the KVD circuit, and the self-calibrator. Section 4.1 introduces the current calculator circuit. Section 4.2 introduces the KVD circuit. To improve the accuracy of the KVD circuit, the self-calibrator is implemented in Section 4.3 with a complete operation of the CV stage. Finally, the system stability is described in Section 4.4.

4.1 The Current Calculator

The current calculator circuit as illustrated in Fig. 21(a) is used to calculate the average output current according to the derivation of (12). To ensure the constant current of the CC stage is defined by the V_{REF_I}, the V_I is derived as (18) and regulated to the V_{REF_I} in the CC loop where the ratio of k_3 to k_2 is the ratio of the current mirror M_3 to M_2.

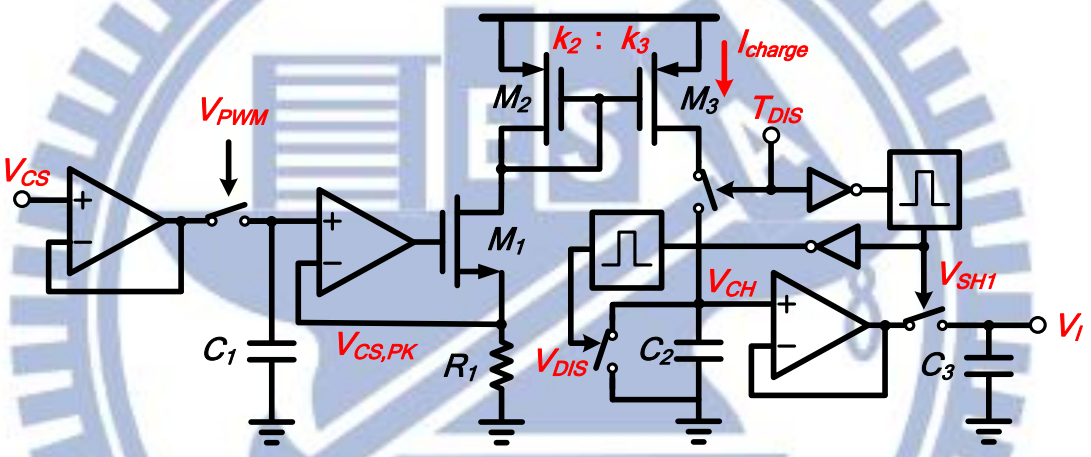
$$V_I = I_{charge} \times \frac{T_{DIS}}{C_2} \text{ where } I_{charge} = \frac{V_{CS,PK}}{R_1} \times \frac{k_3}{k_2} \tag{18}$$

Here, the peak current is indicated by the $V_{CS,PK}$, which can be determined and hold by the capacitor C_1 if the V_{PWM} changes from high to low. The discharging time T_{DIS} is used to determine how long the capacitor C_2 is charged by the I_{charge}, which is converted from the $V_{CS,PK}$. Thus, the value of the V_{CH} on the C_2 is proportional to the product of the $V_{CS,PK}$ and the T_{DIS}. At the end of discharging time, the sample-and-hold signal pulse V_{SH1} is triggered by the T_{DIS} to capture the V_{CH} as the V_I. After that, the V_{CH} is reset to zero by another one-shot signal

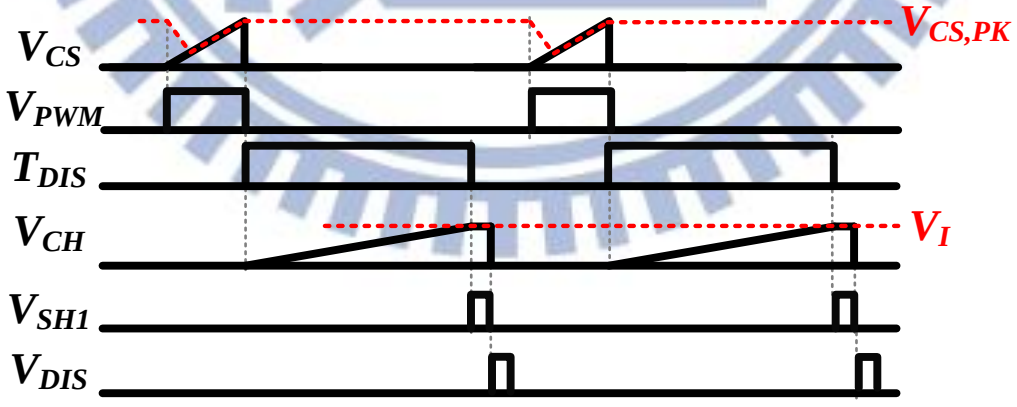
V_{DIS} and ready for next switching cycle. To use the V_I to indicate the output average current $I_{O,avg}$, it is necessary to force (18) to be equal to (12). Then, (19) can be derived.

$$\frac{1}{R_1}\times\frac{k_3}{k_2}\times\frac{1}{C_2}=\frac{1}{2\times T_S}\times\frac{1}{R_{CS}}\times\frac{N_P}{N_S} \tag{19}$$

Therefore, the selection of the values of R_1, C_2, k_2 and k_3 should follow the equation of (19). As a result, in the CC loop, the V_I can be regulated to the reference voltage V_{REF_I}, which indicates the desired output constant current. Fig. 21 (b) shows the timing diagrams of the current calculation circuit.



(a)

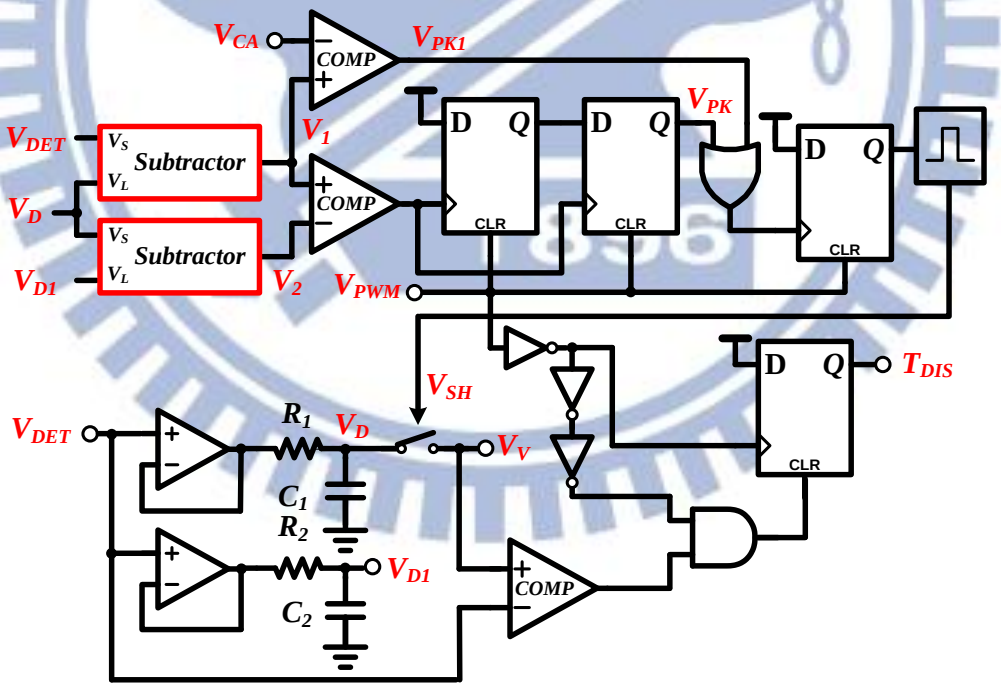


(b)

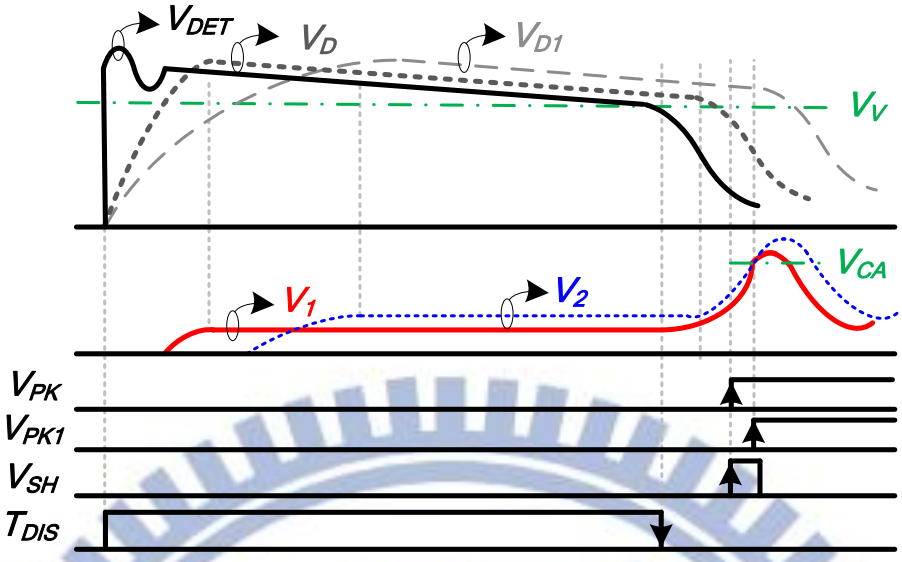
Fig. 21. (a) The current calculator circuit. (b) The timing diagrams.

4.2 The Implementation of Knee Voltage Detector

The KVD circuit as illustrated in Fig. 22 is used to accurately track the knee point of auxiliary winding voltage for getting the output voltage without being affected by the diode forward voltage in the CV regulation. The V_{DET} is the scaled-down value of the V_A by the voltage divider and its minimum value is clamped to zero. Two delayed signals V_D and V_{D1} are derived by passing the V_{DET} through different RC circuit. Thus, the time constant of R_2C_2 for the V_{D1} is two times that of R_1C_1 for the V_D. The delay time of the V_{D1} is larger than that of the V_D as shown in Fig. 22 (b). Two subtractors in Fig. 22 (a) are used to calculate the difference between the V_D and the V_{DET} and the difference between the V_D and the V_{D1} during the off-time period. **Owing to the usage of RC delay, the function of the subtractor can be seen as a slope calculator to detect the knee voltage.**



(a)



(b)

Fig. 22. (a) The KVD circuit. (b) Timing diagrams of the KVD technique.

The schematic of the subtractor is depicted in Fig. 23. Two voltage-to-current (V-to-I) converters are applied to convert two input signals V_L and V_S into two current signals. After the operation of three current mirrors, M_3~M_8, the difference between the V_S and the V_L is converted to the difference current I_{diff}. Then, converting the I_{diff} to the V_{diff} in (20) by the resistor R_3 can amplify the difference signal.

$$V_{Diff} = \begin{cases} \left(\frac{V_L}{R_2} - \frac{V_S}{R_1}\right) \times R_3 & \text{if } V_L > V_S, \\ 0 & \text{if } V_L \le V_S \end{cases} \tag{20}$$

Two outputs, V_1 and V_2, from the two subtractors indicate the difference between the V_D and the V_{DET} and the difference between the V_D and the V_{D1}. By subtracting V_{DET} from V_D and V_D from V_{D1}, we can obtain V_1 and V_2.

The V_2 is larger than the V_1 in the beginning time when the I_S starts to discharge to the output. At the end of discharging time, the V_{DET} will start to have the resonant effect. The difference between the V_D and the V_{DET} starts to rise. After more delay time, the V_2 start to rise, too. When the V_1 is equal to the V_2, the sample-and-hold signal V_{SH} will capture the V_D as the

V_V. The V_2 can be seen as an adaptive reference to compared to the V_1. Because the relationship between the V_1 and the V_2 is a relative value, whatever the slope value of V_{DET} is, V_{SH} still can sample an accurate knee voltage.

On the other hand, the V_1 and the V_2 may have no crossing point under two conditions. One of the conditions when system is in startup, the output voltage is still very low. It causes the amplitude of V_{DET} in resonant period T_{RE} is quite small. That also makes the amplitude of V_1 and V_2 too small to determine V_{SH}. Another condition occurs when V_O is very close to regulation voltage. It causes the on time and discharge time becomes very short. That makes the V_D and V_{D1} are still on the rise when discharge time is over. It also causes V_1 and V_2 cannot determine V_{SH} correctly. The calibrated voltage V_{CA} is used to calibrate these errors and substitute the role of the reference voltage to decide one suitable signal V_{SH}.

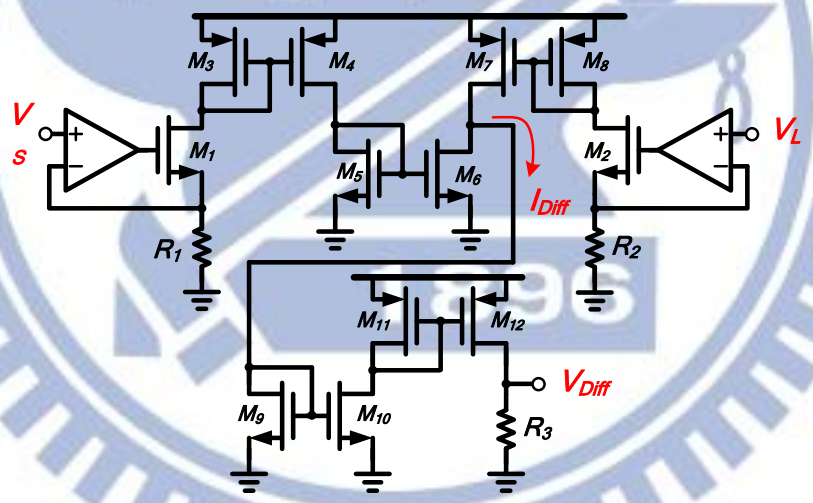


Fig. 23. The circuit of subtractor.

4.3 The Implementation of Self-Calibrator

The self-calibrator is used to detect the knee voltage if the KVD circuit fails to get an accurate knee voltage. The sequence of the V_{PK} and the V_{PK1} will affect the value of the V_V.

To avoid some conditions that the V_{PK1} triggers the V_{SH} prior to the V_{PK}, the state machine is depicted as a flow chart in Fig. 24. Here, the n^{th} cycle value of the V_{CA} is remarked as the $V_{CA,n}$. During the on-time period, the V_{CA} will keep the previous value and the values of the V_{PK} and the V_{PK1} are reset. The estimation period of the knee voltage is started in the beginning of the off-time and ended by the V_{END}, which is triggered by first valley of the V_{DET}. Changing the value of the V_{CA} based on different mode, precise CV regulation can be obtained. In this work, four modes are defined. When the V_{PK} and the V_{PK1} are all zero during the estimation period, it indicates the V_{SH} cannot change from low to high since the cross point between the V_1 and the V_2 doesn't happen and the V_{CA} is too high. This is the Mode-1 and the V_{CA} will be discharged in next sequent cycle to minimize the error. Another error may happen when the V_{PK1} is triggered prior to the V_{PK} because the V_{CA} is too low. When the V_{PK1} is triggered first, it leads the state machine into Mode-3. If the V_{PK} is still not triggered after the state is switched into Mode-3, it means that error is correctly fixed by the V_{CA}. The V_{CA} will not be changed in next sequent cycle. Contrarily, if the V_{PK} is triggered in Mode-3, the state will be switched into Mode-4. It means that the V_{CA} is too low and the V_{PK1} is triggered prior to the V_{PK}. In the next sequent cycle, the V_{CA} be charged to avoid the error.

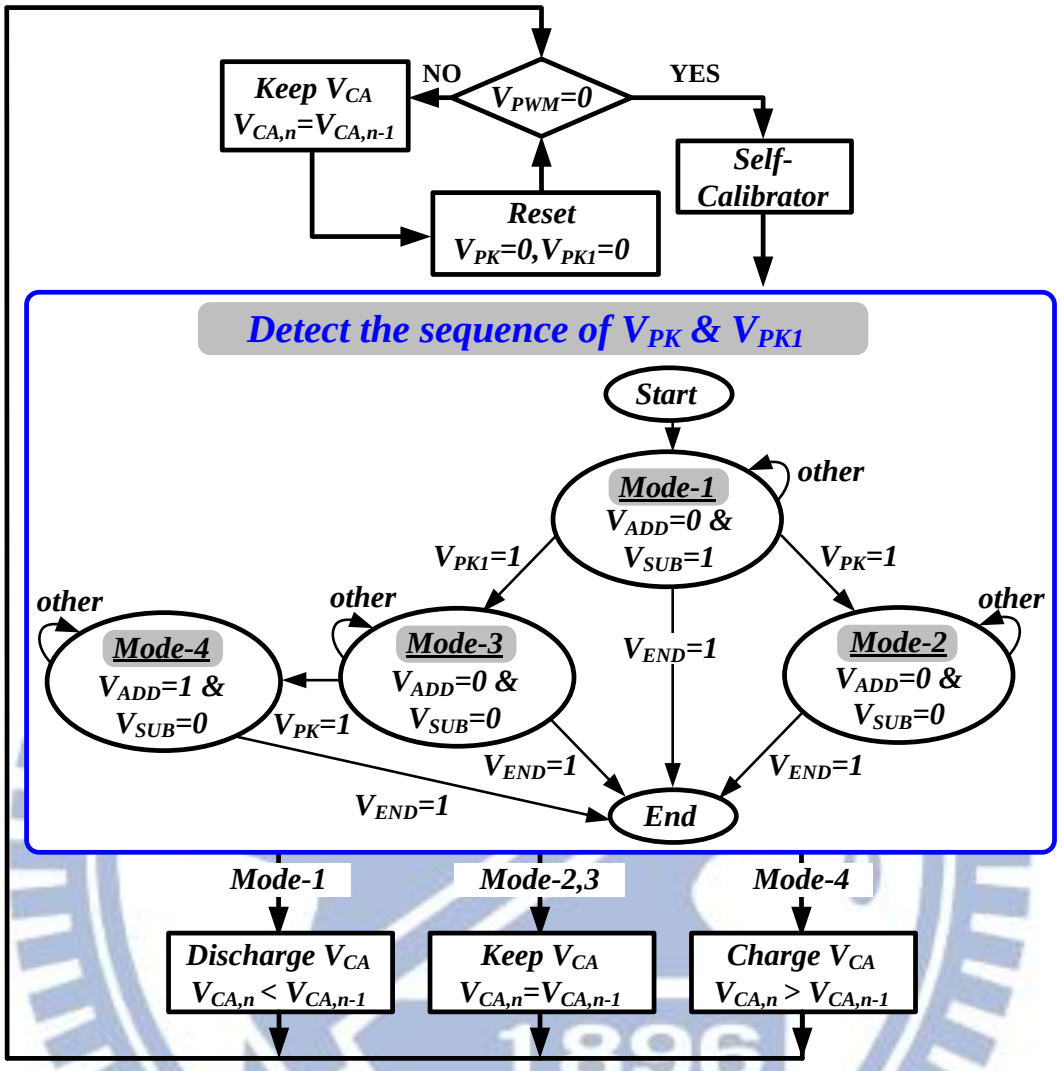


Fig. 24. Flow chart with state machine of Self-Calibrator.

The self-calibrator circuit is shown in Fig. 25 (a) and corresponding waveforms in different mode is also shown in Fig. 25 (b). Then state machine determines the modes and sends the addition result, V_{ADD}, or the subtraction result, V_{SUB}. The up/down counter receives the result and sends out a 3-bits control signal. The 3-bits signal is used to control the switch of current sources to adjust the V_{CA}. Fig. 26 shows the up/down counter, which is composed of a 3-bits binary adder. It can add or subtract the result of (S1 , S2 , S3) one bit a time. Besides, there is another overflow limiting circuit to ensure the range of (S1 , S2 , S3) is from (0, 0 , 0) to (1 , 1 , 1).

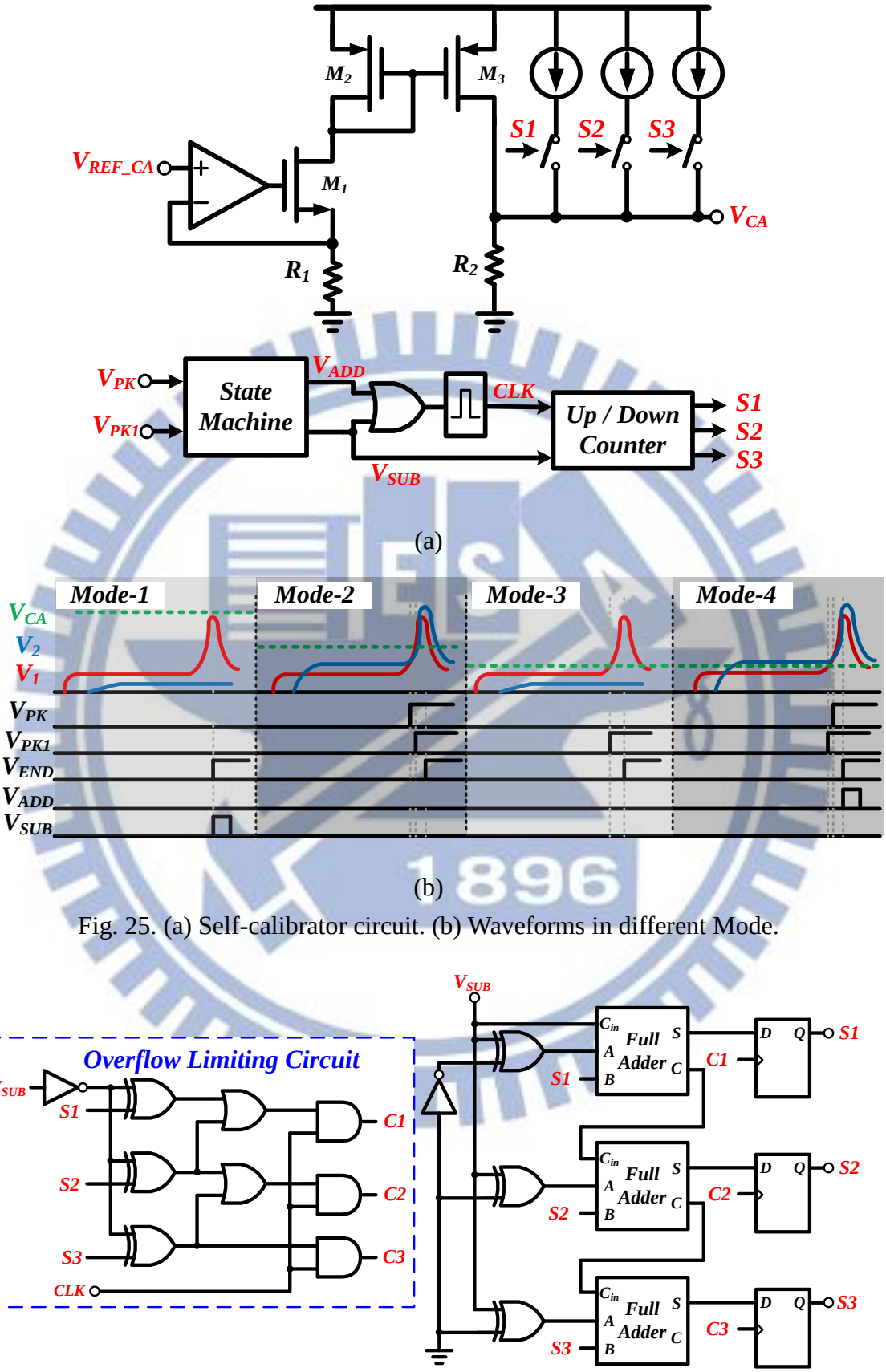


Fig. 25. (a) Self-calibrator circuit. (b) Waveforms in different Mode.

Fig. 26. Up/down counter.

4.4 The Stability of the System

Fig. 27 (a) shows an equivalent small signal model based on the architecture in Fig. 10 (b) and Fig. 15. The close loop can be divided into two parts, control-to-output transfer function, G_{CO}, and output-to-control transfer function, G_{OC}, [16]-[20]. As depicted in Fig. 27 (b), the $I_{S,avg}$ is the average value of the secondary-side current I_S within one switching cycle as shown in (21). The switching period can be written as the function of error signal V_{ERR_V} as shown in (22), where K and C are constant values. The value of discharging time T_{DIS} depends on the current peak value $I_{S,PK}$ and the discharging slope $L_m / V_O \cdot N_1^2$ as shown in (23). Also secondary current peak value $I_{S,PK}$ can be substituted for the relationship with input voltage V_{IN} and error signal V_{ERR_V} as shown in (24) (25). The $I_{S,avg}$ can be expressed as the function of the output voltage V_O, error signal V_{ERR_V}, the inductor L_m and the sensing resistor R_{CS} in (26).

$$I_{S,avg} = \frac{\frac{1}{2} \times \left(T_{DIS} \times I_{S,PK} \right)}{1 / f(V_{ERR\_V})} \tag{21}$$

$$f(V_{ERR\_V}) = K \cdot V_{ERR\_V} + C \tag{22}$$

$$T_{DIS} = I_{S,PK} \times \frac{L_m}{V_o \cdot N_1^{\,2}} \tag{23}$$

$$I_{S,PK} = \frac{V_{IN}}{L_m} \cdot T_{ON} \cdot N_1 \tag{24}$$

$$T_{ON} = V_{ERR\_V} \times \frac{L_m}{V_{IN}} \times \frac{1}{R_{CS}} \tag{25}$$

$$I_{S,avg} = \frac{\left(K \times V_{ERR\_V}^{\,3} + C \times V_{ERR\_V}^{\,2} \right) \times L_m}{2 \times V_O \times R_{CS}^{\,2}} \tag{26}$$

The averaged secondary-side current is, in general, a nonlinear function of the converter voltages and currents. Linearization at the quiescent operating point can derive the small ac current variation of the secondary-side as expressed in (27).

$$\hat{I}_{S,avg} = a_1 \cdot \hat{V}_{ERR\_V} + a_2 \cdot \hat{V}_O \text{ where } \begin{pmatrix} a_1 = \dfrac{\partial I_{S,avg}}{\partial V_{ERR\_V}} = \dfrac{3K \cdot {V_{ERR\_V}}^2 \cdot L_m}{2 \cdot V_O \cdot {R_{CS}}^2} \\ a_2 = \dfrac{\partial I_{S,avg}}{\partial V_O} = \dfrac{-K \cdot {V_{ERR\_V}}^3 \cdot L_m}{2 \cdot {V_O}^2 \cdot {R_{CS}}^2} \end{pmatrix} \quad (27)$$

The output voltage V_O is the product of the averaged secondary-side current $I_{S,avg}$ and the output impedance Z_O which includes the output capacitor and equivalent output loading. The small ac current variation at the secondary-side flowing through the impedance Z_O determines the perturbation of V_O as expressed in (28). Therefore, the control-to-output transfer function G_{CO}(s) is depicted in (29), which simply contains one zero and one pole. The C_O and its equivalent series resistor (ESR) R_{esr} contribute one ESR zero at high frequencies. And the pole can be seen as the combination of C_O and the equivalent loading resistance R_L.

$$\hat{V}_O = \hat{I}_{S,avg} \cdot Z_O = \left(a_1 \cdot \hat{V}_{ERR\_V} + a_2 \cdot \hat{V}_O\right) \cdot Z_O \quad (28)$$

$$G_{CO} = \frac{\hat{V}_O}{\hat{V}_{ERR\_V}} = \frac{Z_O \cdot a_1}{1 - Z_O \cdot a_2} = \frac{a_1}{1/R_L - a_2} \cdot \frac{1 + s \cdot C_O \cdot R_{esr}}{1 + \dfrac{s \cdot C_O \left(1 + R_{esr}\left(1/R_L - a_2\right)\right)}{1/R_L - a_2}} \quad (29)$$

As illustrated in Fig. 29(a), the transconductance of error amplifier *EA* is g_m. Thus, the output-to-control transfer-function G_{CO}(s) can be derived in (30).

$$G_{OC}(s) = \frac{\hat{V}_{ERR\_V}}{\hat{V}_o} = N_2 \times \frac{R_{A2}}{R_{A1} + R_{A2}} \times g_m \times \frac{R_C}{1 + sR_C C_C} \quad (30)$$

Hence, the transfer function G_{OC}(s) that contains one pole is used to compensate the zero in G_{CO}(s) should as pole-zero cancellation by choosing appropriate passive components. Thus, the pole in G_{CO}(s) is the dominant pole of the whole system. After the compensation, the system becomes the one-pole system and bandwidth is designed far away from the switching frequency.

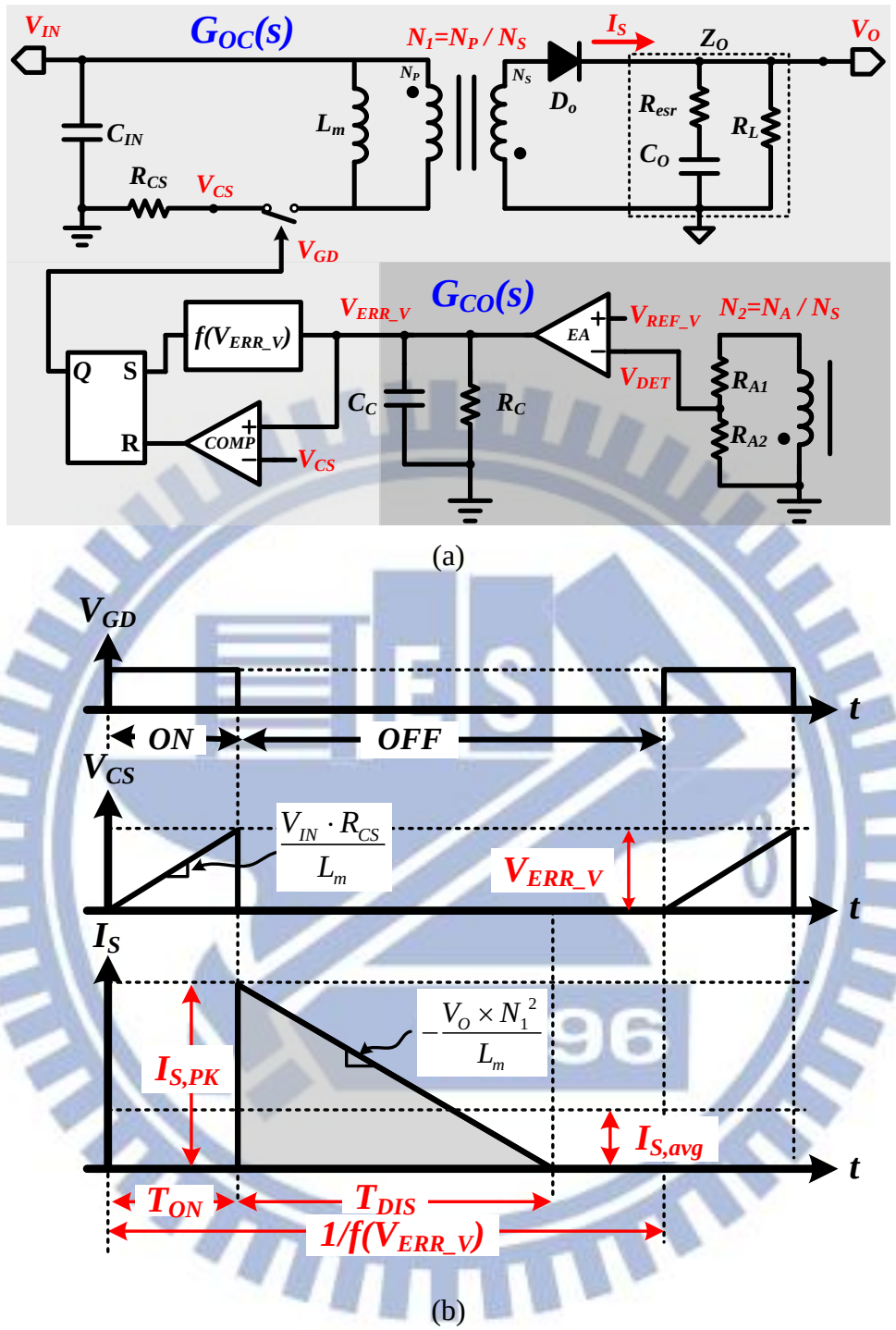


Fig. 27. (a) Equivalent small signal model of the proposed PSR in CV regulation. (b) Waveforms of the dynamic frequency technique.

Chapter 5

Simulation Results,

The proposed PSR charger with the KVD technique was implemented in 0.5μm 500V UHV process. The chip micrograph with an active area of **4 mm^2** is shown in Fig. 28. TABLE III is the design specification of PSR. The switching frequencies are 42 kHz and 1 kHz for CC stage and green mode, respectively. Besides, the switching frequency gradually decreases in CV stage if the output voltage is slowly regulated to 5V.

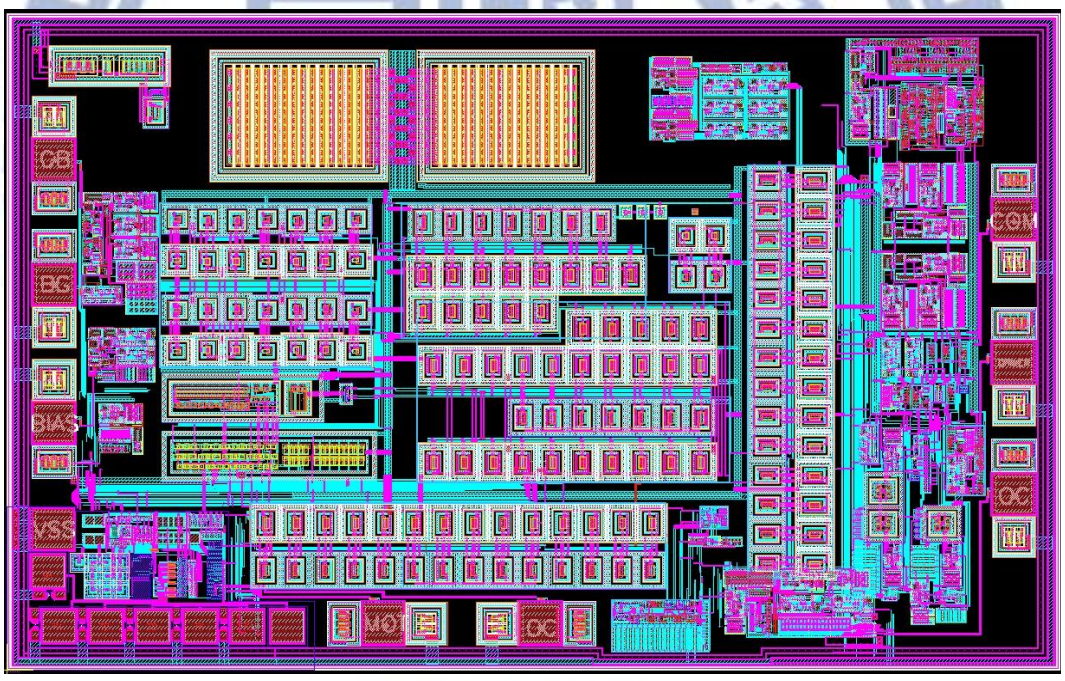


Fig. 28. Chip micrograph.

TABLE III: Design Specifications

Technology	***0.5μm 500V UHV***
Input line voltage range (V_{AC})	***90 V~264V(rms)***
Output voltage (V_O)	***1.5V~5V***

Output current (I_O)	***0A~1A***
Primary side inductance (L_P)	***2.3mH***
Primary winding turns (N_P)	***132T***
Secondary winding turns (N_S)	***11T***
Auxiliary winding turns (N_A)	***28T***
Switching frequency (f_{SW})	***1KHz~42kHz***

In this chapter, the simulation results are shown in Section 5.1. The comparison with the prior arts is shown in Section 5.2.

5.1 Simulation Results

Fig. 29 shows the simulation results when the PSR operation is in the DCM. The primary-side and the secondary-side currents of the transformer I_P and I_S are with the triangular sharp. The V_{DET} has the resonant effect when the discharging time is over. In CC regulation, the calculated current value V_I must be a constant as shown in Fig. 30. The V_{CS} is sampled as the $V_{CS,PK}$ when the V_{PWM} changes from high to low. Thus, the V_I can be derived by the charging result signal V_{CH} in the end of the discharging time T_{DIS}.

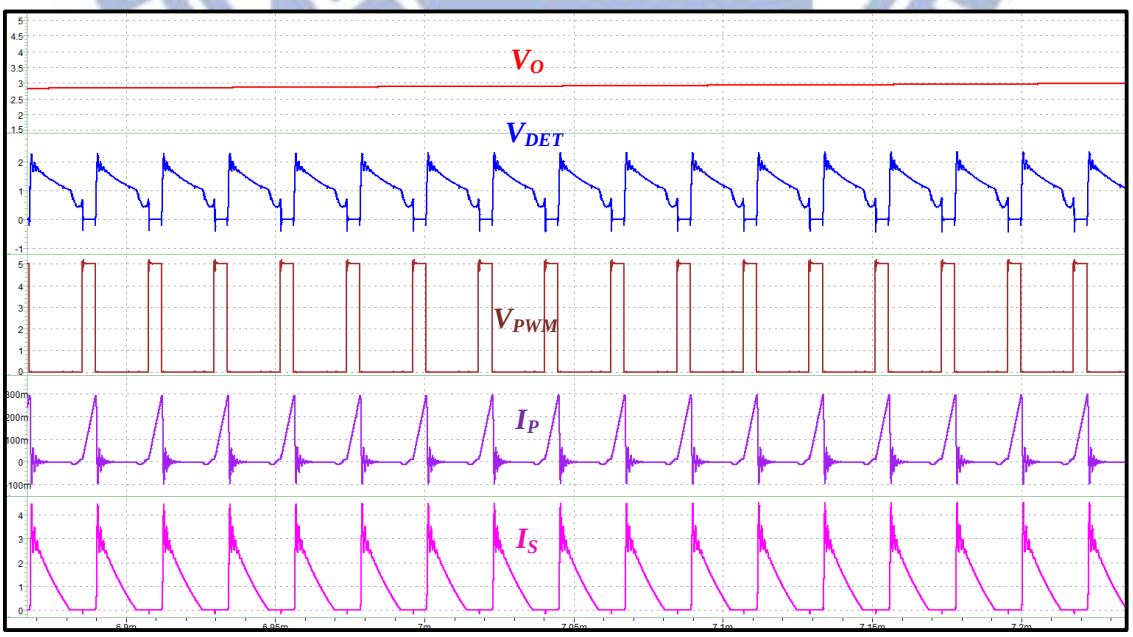


Fig. 29. Simulation results of the PSR operation in the DCM.

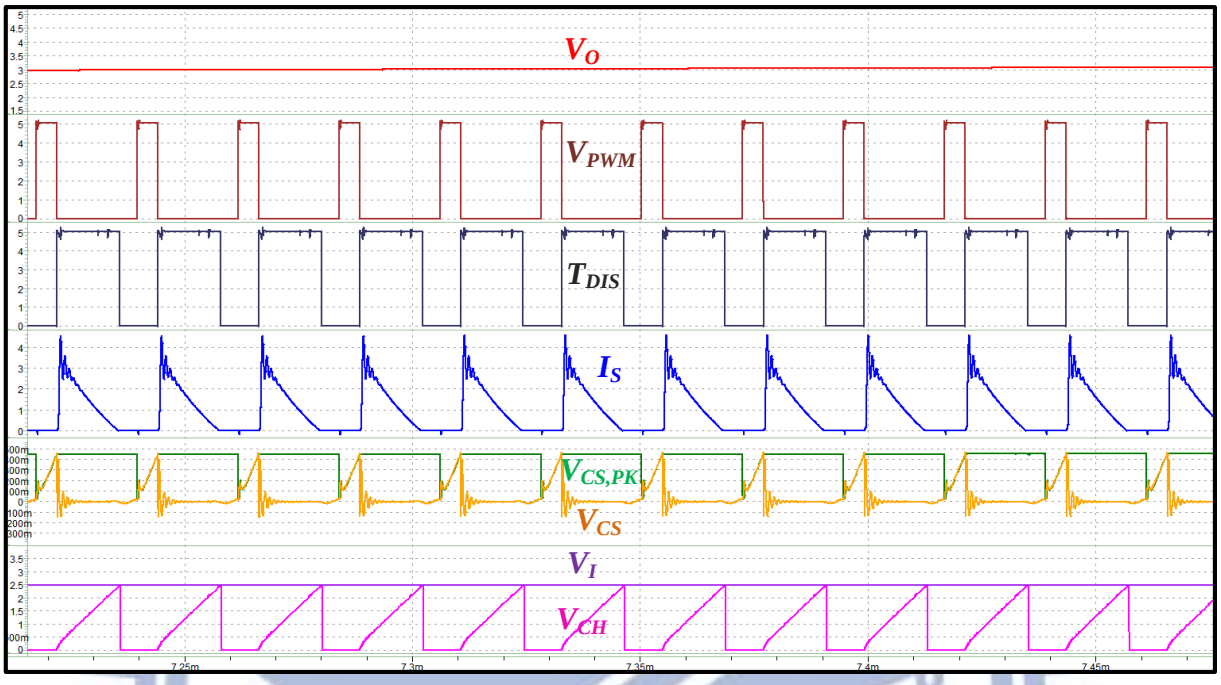


Fig. 30. Simulation results of the current calculator.

The KVD operation is also shown in Fig. 31.

Discharging time can be determined by comparing the V_V and the V_{DET}. The V_{DET} and two delayed signals V_D and V_{D1} are sent to two distinct subtractors to calculate the difference between the $V_1$and the V_2.

Using the V_1 and the V_2 can determine the timing of sample-and-hold signal V_{SH} by comparing V_1 to V_2 and V_1 to V_{CA}. The comparison result is V_{PK} and V_{PK1} are sent into the self-calibrator circuit to decide the sequent operation mode.

Fig. 32 shows different conditions in the self-calibrator. When the V_{PK1} is prior to the V_{PK} as shown in Fig. 32 (a), the state machine will send out V_{ADD} to charge the value of the V_{CA}. It can let the sample-and-hold signal V_{SH} controlled by the V_{PK}. Another situation is the operation changes from Mode 2 to Mode 4 when the output voltage is close to the regulation voltage as depicted in Fig. 32 (b). Because the non-ideal RC circuit is not only affected by the

delay effect but also has the signal distortion. Furthermore, discharging time becomes small when the V_O is close to regulation voltage. The distortion will let the V_D and the V_{D1} need enough time to be sampled as two delayed signals. If the discharging time is not enough for sampling the V_D and the V_{D1}, the V_1 and the V_2 cannot have an obvious cross point. In other words, another decision signal V_{CA} is utilized to improve the accuracy when the previous decision method fails. At this time, the state machine will be switched into Mode 3, but the KVD circuit can continuously sample the knee voltage.

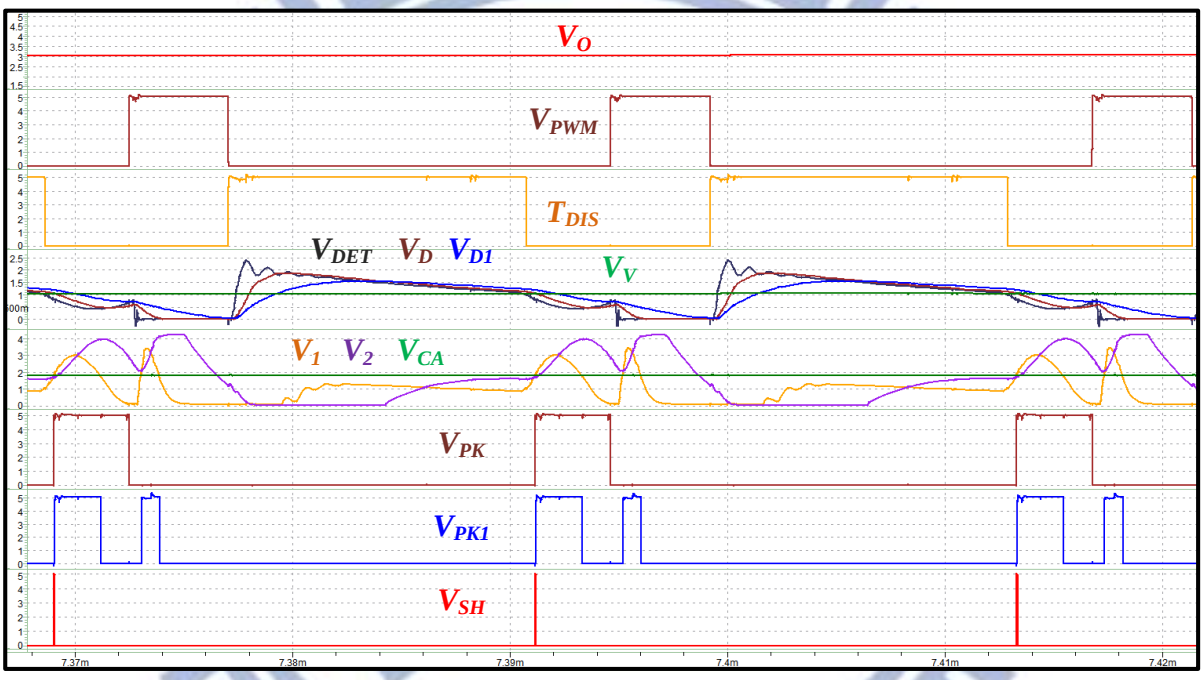
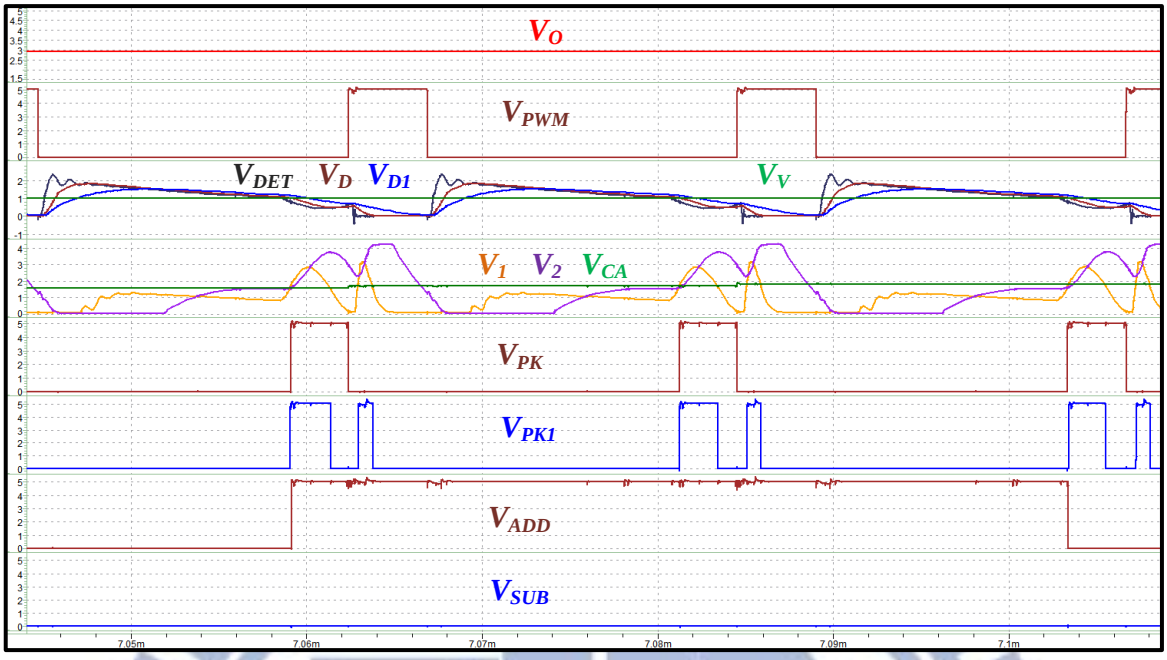
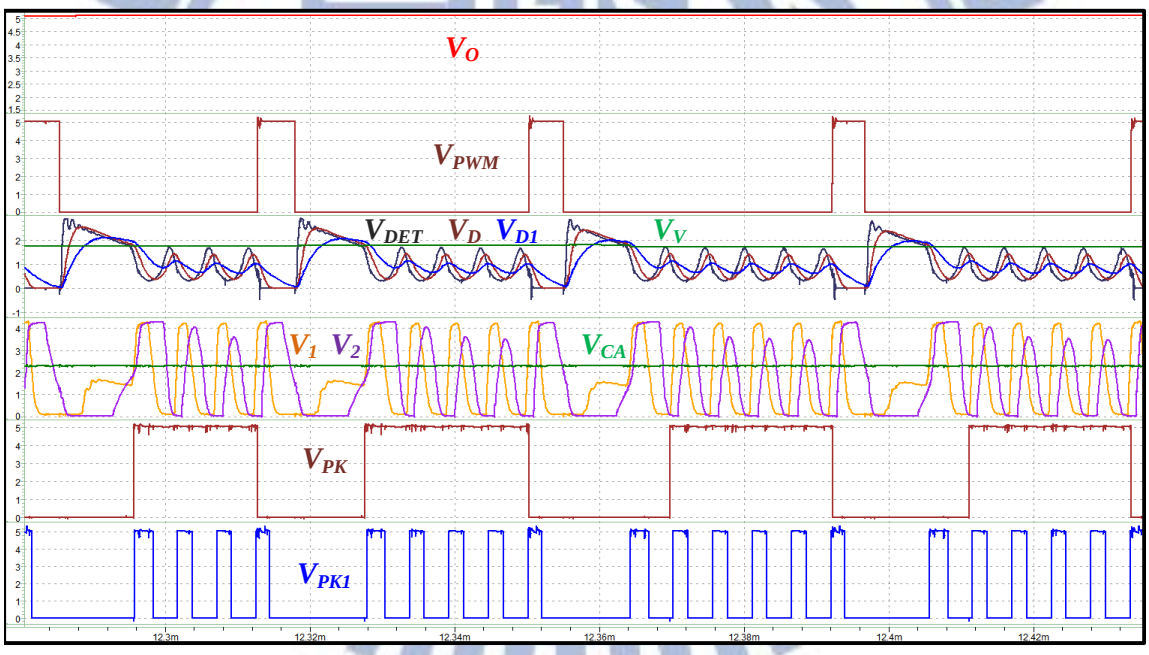


Fig. 31. Simulation results of the KVD technique.



(a)

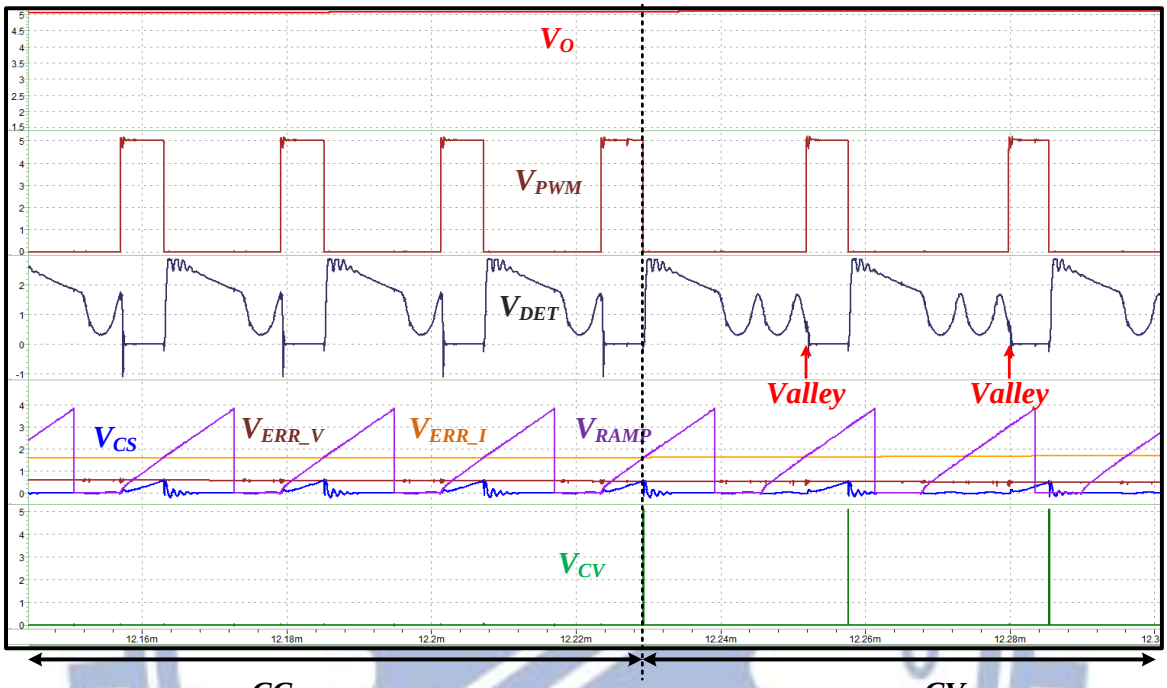


(b)

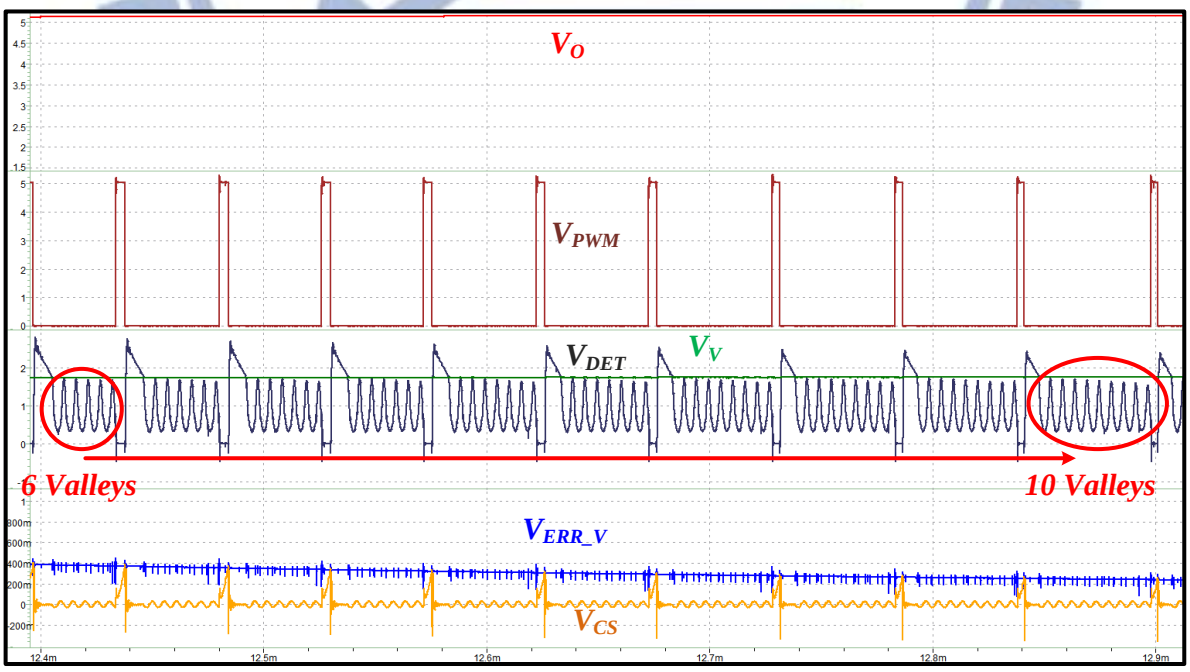
Fig. 32. (a) Self-Calibrator in Mode 2 to Mode 4 (b) Self-Calibrator form Mode 2 to Mode 3.

The proposed PSR's output voltage is designed from 1.5V to 5V. When the V_O is close to 5V, the voltage loop's error signal V_{ERR_V} is low enough for the V_{CS} to trigger the V_{CV} to decide the on-time value. Fig. 33 (a) shows the transition from the CC to the CV. In CV regulation, the valley selection mode is used. Every switching cycle in the CV stage select one of the

resonant valleys according to the loading condition. Simultaneously, the V_{ERR_V} is used to determine which one is the better solution from all resonant valleys. Lower the V_{ERR_V} is, lower switching frequency is since more valleys are selected. As a result, the CV regulation operates with a dynamic frequency as shown in Fig. 33 (b).



(a)



(b)

Fig. 33. (a) PSR Operation Changing from CC to CV. (b) Dynamic Frequency in CV

Regulation.

Whole the charging sequence is shown in Fig. 34. The V_O is charged from 1.5V to 5V. The V_I is a constant value in the CC regulation and the V_V is also constant in CV regulation. Two error signals illustrate the situation of voltage and current information. The CV stage is divided into two modes. One is valley selection mode and different valley is selected to decide different switching frequency due to the varied V_{ERR_V}. When the V_{ERR_V} is low enough, the CV regulation will be switched into the green mode for further reducing switching frequency.

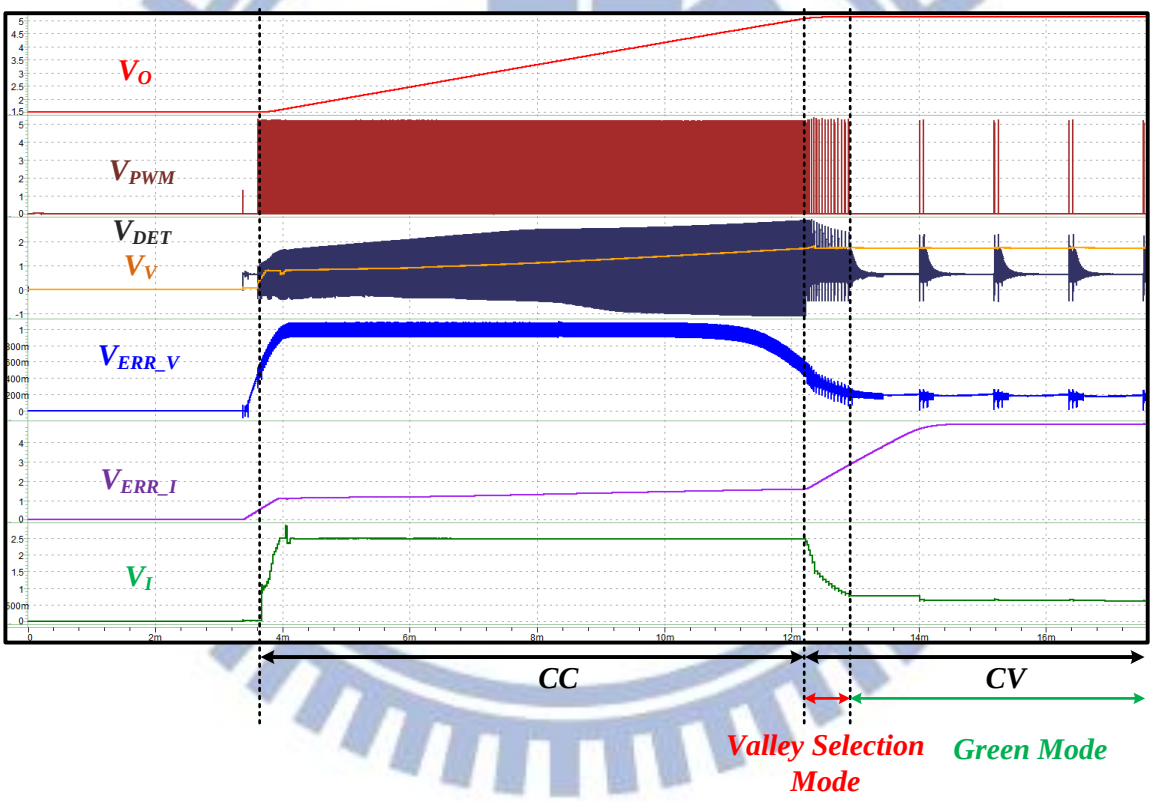


Fig. 34. Charging Sequence of PSR.

5.2 Comparison with the Prior Arts

Fig. 35 is the statistical chart of the knee voltage corresponded to the output voltage. The KVD has an initial value of 0.6V when the system starts up. When the output voltage reaches to about 2V, the ideal knee voltage is 0.69V and the KVD technique starts to work. Through

the self-calibration, the knee voltage can be close to an ideal value when the output voltage is 5V. The difference between ideal and simulation values when the output voltage around 5V is 0.01V. As a result the control of the transition from the CC to the CV will be perfect.

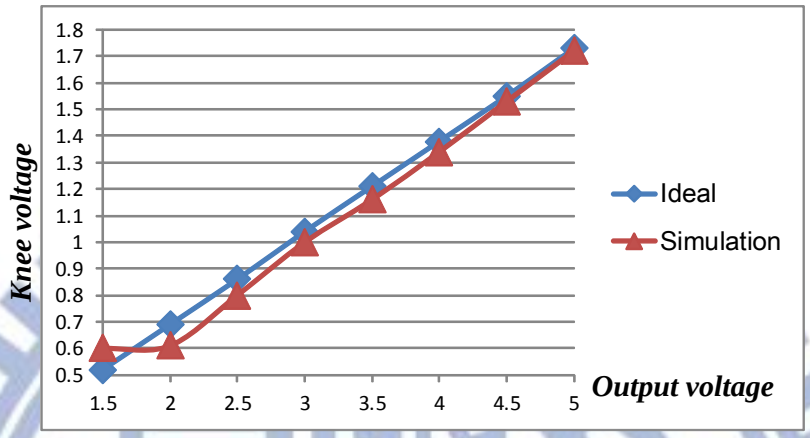


Fig. 35. The output voltage versus the knee voltage.

Chapter 6

Conclusions and Future Works

6.1 Conclusions

To achieve isolated charger for high input voltage, PSR is proposed to apply for this application. But the most difficult to design PSR is how to sensing the correct value of output voltage. In other words, the knee voltage must be found in each cycle. The KVD technique with the self-calibrator is proposed to find precise knee voltage. The current calculator is also used to regulate the current loop. In the CV regulation, the switching frequency is adaptive according to the valley selection mode or the green mode to improve the efficiency.

6.2 Future Works

The thesis proposed a technique to realize the isolated charger. However, the constant current regulation is still operating in constant frequency. The ZVS cannot apply in constant frequency. It will make the efficiency poor than that of the CV regulation due to the constant switching frequency. How to imply ZVS to CC regulation becomes an interesting topic.

References

[1] K.B. Park, C.E. Kim, G.W. Moon, M.J. Youn, "PWM Resonant Single-Switch Isolated Converter," *IEEE Trans. Power Electron*., vol.24, no.8, pp.1876-1886, Aug. 2009.

[2] Khan I.A., "Synthesis and Analysis of Transformer-Isolated Converters," *IEEE Trans. Power Electron*., vol.10, no.4, pp.409-418, Jul 1995.

[3] M. Chen, G.A. Rincón-Mora, "Accurate, Compact, and Power-Efficient Li-Ion Battery Charger Circuit," *IEEE Trans. Circuits and Systems II*, vol. 53, no. 11, pp. 1180-1184, Nov. 2006.

[4] M.J. Isaacson, R.P. Hollandsorth, P.J. Giampaoli, F.A. Linkowaky, A. Salim, V.L. Teofilo, "Advanced Lithium Ion Battery Charger," *The Fifteenth Annual Battery Conference on Applications and Advances*, pp. 193-198, Jan. 2000.

[5] C.C. Tsai, C.Y. Lin, Y.S. Hwang, W.T. Lee and T.Y. Lee, "A multi-mode LDO-based Li-ion battery charger in 0.35μm CMOS Technology," *IEEE Asia-Pacific Conference on Circuits and Systems*, pp. 49-52, Dec. 2004.

[6] K.B. Park, C.E. Kim, G.W. Moon; M.J. Youn, "PWM Resonant Single-Switch Isolated Converter," *IEEE Trans. Power Electron*., vol.24, no.8, pp.1876-1886, Aug. 2009.

[7] Torrico-Bascop R., Barbi N., "A double ZVS-PWM active-clamping forward converter: analysis, design, and experimentation," *IEEE Trans. Power Electron*., vol.16, no.6, pp.745-751, Nov. 2001.

[8] Yuh-Shyan Hwang, Shu-Chen Wang, Fong-Cheng Yang, Jiann-Jong Chen, "New Compact CMOS Li-Ion Battery Charger Using Charge-Pump Techniques for Portable Applications," *IEEE Trans. Circuits and Systems I*, vol. 54, no. 4, pp. 705-712, April 2007.

[9] J. Buxton, "Li-Ion battery charging requires accurate voltage sensing," *Anal. Devices Anal. Dialog.*, vol. 31, no. 2, 1997.

[10] M.T. Zhang, M.M. Jovanovic, and F.C. Lee, "Design considerations and performance evaluations of synchronous rectification in flyback converters," *IEEE Trans. Power Electron.*, vol.13, no.3, pp.538-546, May 1998.

[11] S. Howimanpom, C. Bunlaksananusom, "Performance comparison of continuous conduction mode (CCM) and discontinuous conduction mode (DCM) flyback converters," in *Proc. IEEE Power Electron. Drive Syst. Conf.*, vol.2, pp. 1434-1438, Nov. 2003.

[12] Ferdowsi M., Emadi A., Telefus M., Davis C., "Pulse regulation control technique for flyback converter," *IEEE Trans. Power Electron*., vol.20, no.4, pp. 798- 805, July 2005.

[13] T.Y. Tang, C.L. Chen, J.Y. Lin, S.Y. Lin, "Flyback Power Converter Having a Constant Voltage and a Constant Current Output Under Primary-Side Pwm Control," US 6862194 B2, Jun. 18, 2003.

[14] T.Y. Tang, C.C. Li, F.Y. Tsao, "Primary-Side Controlled Switching Regulator," US 20070103134 A1, Nov. 8, 2005.

[15] T.C. Lin, "Apparatus and Method for Regulating Constant Output Voltage and Current on Primary Side in Flyback Converter," US 7859862 B2, Dec. 28, 2010.

[16] Chen T.H., Lin W.L., Liaw C.M., "Dynamic modeling and controller design of flyback converter," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 35, no. 4, pp. 1230–1239, Oct. 1999.

[17] Irving B.T., Panov Y., Jovanovic M.M., "Small-signal model of variable-frequency flyback converter," *in Proc. IEEE APEC'03*, vol.2, pp.977-982, Feb. 2003.

[18] Panov Y., Jovanovic M.M., "Small-signal analysis and control design of isolated power supplies with optocoupler feedback," *IEEE Trans. Power Electron*., vol.20, no.4, pp. 823-832, July 2005.

[19] Suntio T., "Average and small-signal modeling of self-oscillating flyback converter with applied switching delay," *IEEE Trans. Power Electron*., vol.21, no.2, pp. 479- 486, Mar. 2006.

[20] C. Basso, “Understanding Loop Compensation with Monolithic Switchers” *ON Semiconductor*, Application Note, AND8334/D.