

國立交通大學

電信工程研究所

碩士論文

在 LTE 系統下保證服務品質的非連續接收機制週期調整方法

A DRX Cycles Adjustment Scheme with QoS Guarantee in LTE System

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中華民國壹佰零壹年柒月

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摘要

在長期演進計畫(LTE)系統中，為了節省用戶端設備 (UE) 的耗電，使待機時間延長，系統使用了非連續接收機制 (DRX)。本論文中，我們將簡單介紹非連續接收機制並進一步利用突發性封包模型 (bursty packet traffic model) 來表現此機制的運作情形。對於不同流量的情況，我們藉由調整非連續傳輸機制週期 (DRX Cycles) 來加強節電效能。接著基於數學模型分析，探討非連續接收機制參數選取對於封包延遲的影響。最後透過模擬結果顯示利用此方法確實可以降低能源消耗並滿足封包延遲的要求以及如何在上述兩者之間權衡取捨。

關鍵字： 非連續接收機制，封包延遲，能源消耗

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ABSTRACT

In the Long Term Evolution (LTE) system, Discontinuous Reception (DRX) has been introduced for power saving to extend the battery life of the User Equipment (UE). In this thesis, we take an overview of the DRX mechanism and further analysis the mechanism with bursty packet traffic model. We propose a scheme for DRX Cycle adjustment to enhance the power saving performance in different traffic conditions. Based on the analytical model, effects of the DRX parameters on the packet delay performance are also investigated. Simulation results show that the scheme can reduce the power consumption with satisfying the packet delay requirement and a trade-off relationship between power saving and packet delay performance.

Keywords: DRX, packet delay, power consumption

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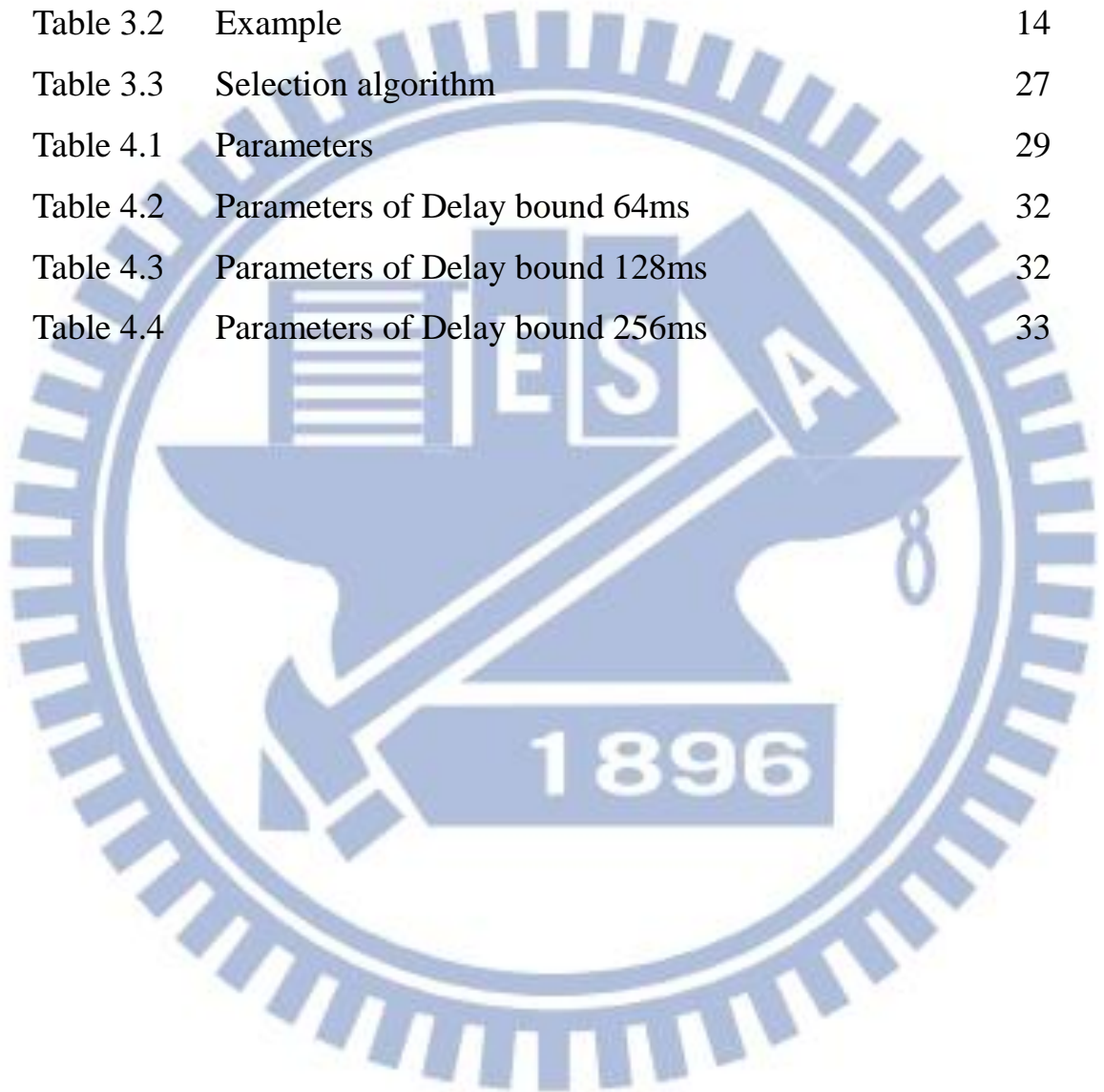
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Chapter 1.

Introduction

The 3rd generation partnership project (3GPP) is currently in the process of defining the long term evolution (LTE) as a mobile communication standard from the former 3G systems. UE energy saving is going to be an important issue of wireless network in recent years. Hence, in the released 3GPP specifications, LTE supports the power saving operation called Discontinuous Reception (DRX) mechanism to prolong the battery life of handset. The traffic status and DRX setting will directly influence the UE's energy consumption.

UE can run many applications over time. Although user has no interaction with device, there exists background traffic due to open applications. In the view point of UE's behavior, as seen in Figure 1.1, we characterize UE's traffic by two states, i.e., active and background state. For background traffic, it doesn't need high delay requirement. Therefore, we can set the DRX parameters to maximize the UE power saving. In active state, active traffic and background traffic coexist, but active traffic dominates this state. Based on different traffic types, active traffic may have various kinds of QoS requirements. For delay-sensitive traffic, we need to configure DRX parameters to meet the delay budget. Because of high traffic variability, using the same DRX parameters may not always be suitable. Switching parameters in each state and the impact of choosing different DRX parameters on packet delay should be considered.

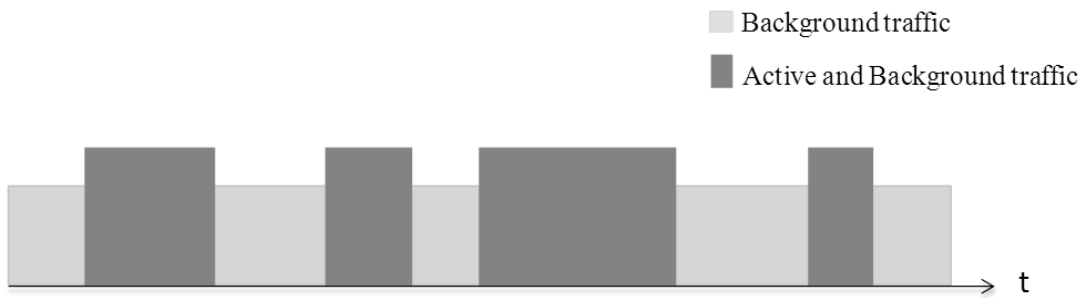


Figure 1.1: UE's traffic behavior

The outline of this article is organized as follows. Chapter 2 briefly introduces the DRX mechanism and the related works which we are going to adopt our system. System model, problem formulation and proposed algorithm are introduced in chapter 3. The following chapter 4 gives the performance evaluation. After that, a conclusion is drawn in chapter 5.

Chapter 2.

Preliminary

2.1 Discontinuous Reception Mechanism

A UE monitor a *physical downlink control channel* (PDCCH) in every subframe to determine whether resources are allocated in either downlink or uplink direction. The DRX mechanism is described in 3GPP LTE MAC specification [1]. It determines when the UE should monitor the PDCCH channel, or when should go to power saving mode. In the power saving mode, UE turns off its circuit to decrease the power consumption when there are no packet which needs to be transmitted or be received.

3GPP LTE specifies two radio resource control (RRC) states for UE, RRC_IDLE and RRC_CONNECTED states. DRX mode can be enabled in both RRC_IDLE and RRC_CONNECTED states. In the RRC_IDLE state, UE listens to the PDCCH, and receives the paging message from eNodeB about incoming call. Therefore, DRX mechanism in RRC_IDLE is used for non-consecutive listening to the call message in order to achieve the purpose of power saving.

In the RRC_CONNECTED state, when UE is initially establishing a radio resource link with eNodeB in the radio resource control link building process, the eNodeB will inform DRX mechanism parameters to UE. Besides, the initial values from RRC link setup, DRX parameters also can be updated via RRC connection reconfiguration

procedure. Therefore, in this state, UE power saving depends on the DRX parameter settings.

In this thesis, it focuses on DRX always in RRC_CONNECTED state (Full Connected DRX mode [2]). It means that UE will always stay in RRC_CONNECTED state with the proper DRX configuration. It has some advantages such as UE's always-on service seems to have the guarantee and RRC signaling overhead on state transition is avoided completely. Respectively, the disadvantage is the increased power consumption. Therefore, we must use discontinuous reception mechanism in RRC_CONNECTED state to achieve the power saving.

The DRX mechanism contains several different parameters to control DRX operation [3]. These parameters are described in detail as follows and the DRX operation is illustrated in simplified form in Figure 2.1.

- DRX Cycle: The DRX cycle specifies the periodic repetition of the On Duration followed by an inactive period. The mechanism provides two DRX Cycles that can be set for each UE, i.e. Long DRX Cycle (T_{LC}) and Short DRX Cycle (T_{SC}). The former is necessary, and the latter is optional.
- On Duration Timer (T_{ON}): The On Duration Timer specifies the number of consecutive PDCCH subframe(s) at the beginning of a DRX Cycle. The UE will listen to the scheduling message on PDCCH during the period T_{ON} . If the UE successfully decodes a scheduling message on PDCCH during the period T_{ON} , the UE will start or restart the Inactivity Timer.

- Inactivity Timer (T_{IN}): The Inactivity Timer specifies the number of consecutive PDCCH subframe(s) after successfully decoding a PDCCH indicating an initial UL or DL user data transmission for this UE. Whenever a scheduling message is successfully received while the Inactivity Timer is running, the UE restarts the Inactivity Timer. If no scheduling message is received on PDCCH during the period T_{IN} , the Inactivity Timer expired.
- Short Cycle Timer (N_{SC}): The Short Cycle Timer specifies the number of consecutive subframe(s) the UE shall follow the Short DRX cycle. After the Short DRX Cycle is enabled, it will start or restart when the Inactivity Timer expired. When the Short Cycle Timer expires, the UE moves into a Long DRX Cycle.

In LTE standard, there are two-leveled unit of time: (1.) Frame (Radio frame) , and (2.) Subframe. Each frame is divided into ten subframes, and each frame has its own System Frame Number (SFN). Each subframe has their own subframe number from 1 to 10. These two units are used in DRX mechanism. Starting the On Duration Timer in every DRX Cycle has a rule which should be obeyed. This is shown in Table 2.1.

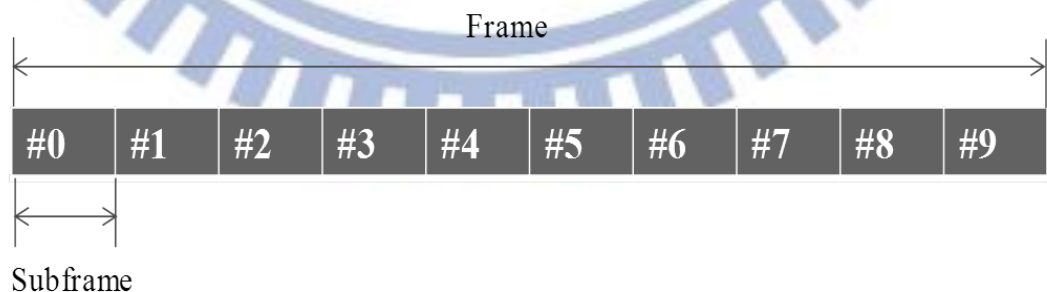


Figure 2.1: Frame structure

Table 2.1: Rule of On Duration Timer [1]

- If the Short DRX Cycle is used and $[(SFN * 10) + \text{subframe number}] \bmod (\text{Short DRX Cycle}) = (\text{DRX Start Offset}) \bmod (\text{Short DRX Cycle})$; or
- if the Long DRX Cycle is used and $[(SFN * 10) + \text{subframe number}] \bmod (\text{Long DRX Cycle}) = \text{DRX Start Offset}$:
 - start On Duration Timer.

The DRX Start Offset is used to obtain the starting subframe number for DRX Cycle.

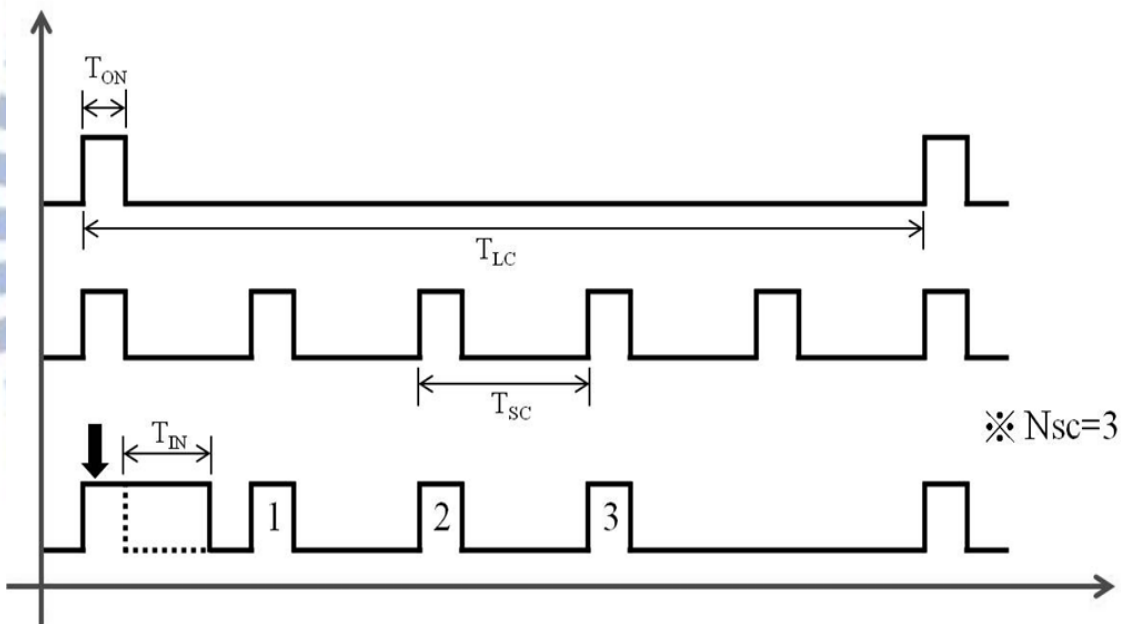


Figure 2.2: Simple illustration of DRX operation

2.2 Packet Traffic Model

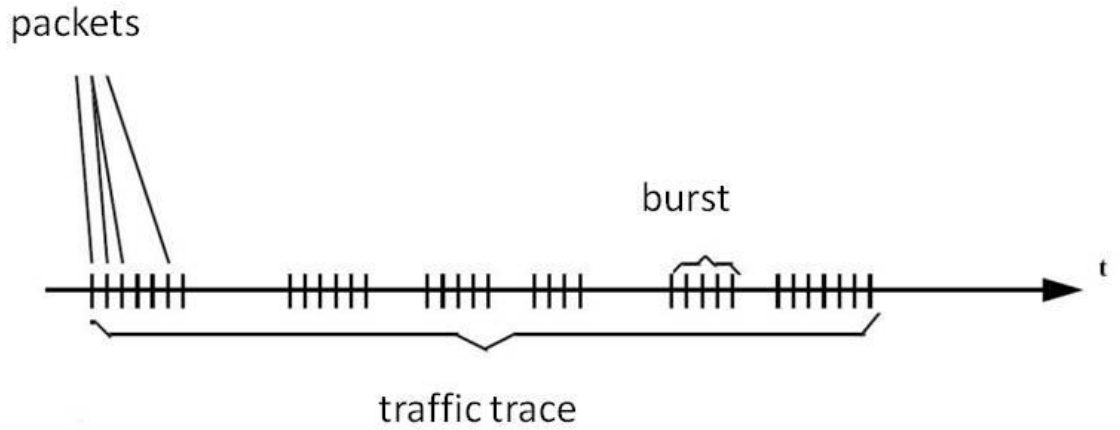


Figure 2.3: Bursty packet traffic model [4]

In this thesis, we measure the network traffic, and model it by a bursty packet traffic model [4], i.e. Figure 2.2. For this traffic model, an inter-packet arrival time and an inter-burst arrival time are generated by an exponential distribution. Each burst consists of several packets being generated by geometric distribution. The statistical distributions of the parameters in our traffic model are summarized in Table 2.2.

Table 2.2: Bursty packet traffic parameter distributions [6]

Parameter	Distribution	Mean Value
Inter-burst arrival time t_{ib}	Exponential	$1/\lambda_{ib}$
Number of packets per burst N_p	Geometric	μ_p
Inter-packet arrival time t_{ip}	Exponential	$1/\lambda_{ip}$

2.3 Related Work

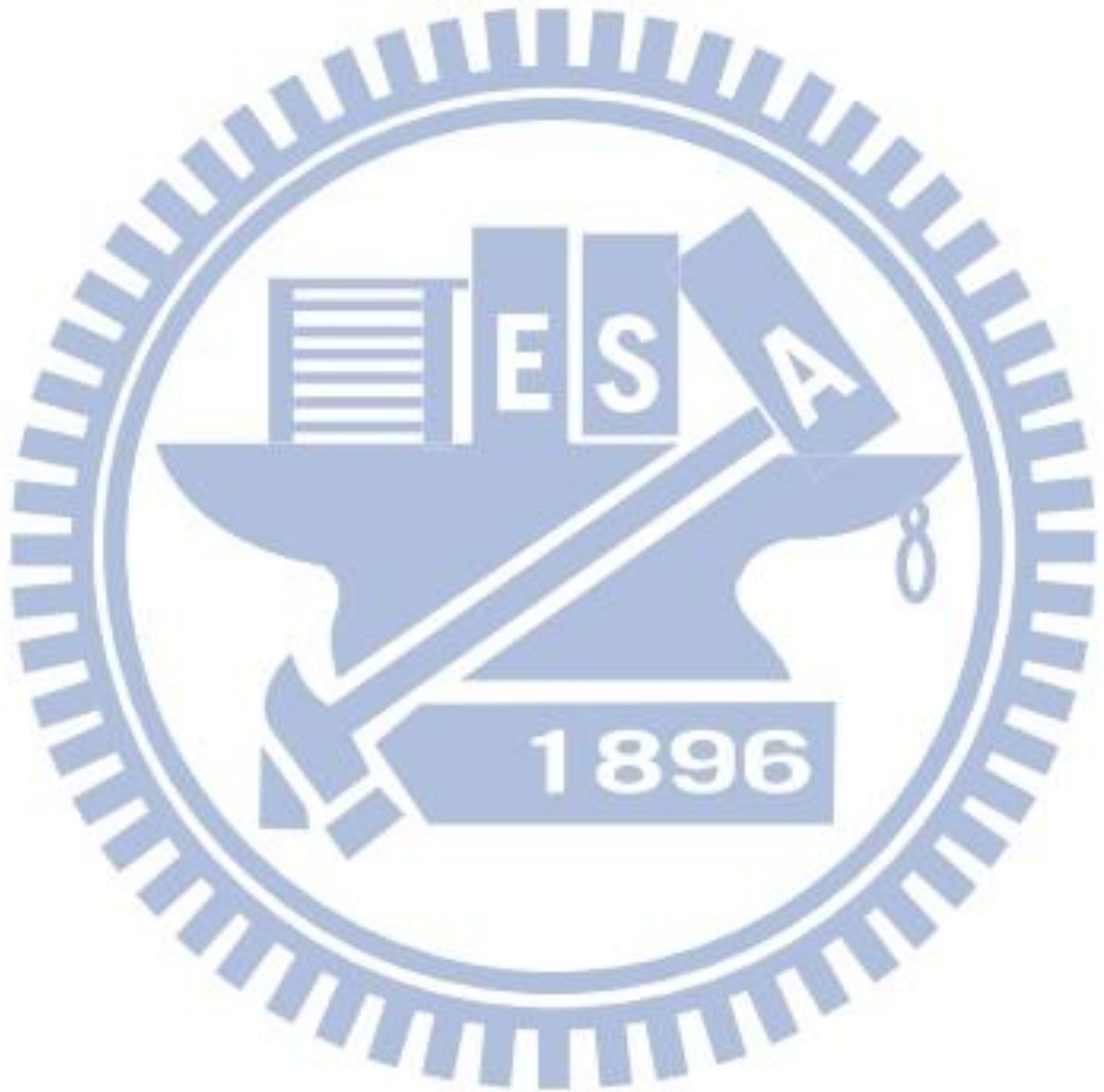
In DRX parameters configuration, the ideal situation to save the energy consumption is that a packet needs to be transmitted during UE's on-duration and no packet needs to be sent in non-transmission period. Therefore, DRX mechanism should be compatible with traffic so that DRX mechanism can determine the parameters to achieve better energy saving.

In recent studies, the work [8][9][10] for DRX parameters impact have been proposed. The following is an overview of the study: The On Duration Timer and the Inactivity Timer are adopted to control UE's power activity. When the length of the DRX cycle stays unchanged, the on-duration time (caused by On Duration Timer and Inactivity Timer) increasing makes UE power consumption increasing. In multi-user environment, considering the eNodeB resource scheduling, the On Duration Timer as well as the Inactivity Timer increasing will benefit the UE's throughput. Using Short DRX Cycle, UE do not have to wait for the next regular Long DRX Cycle on-duration incoming.

[12] points out that the increasing of time to turn off the receiver will get a better power saving efficiency, but may increase the transmission delay between the UE and eNodeB. Hence, setting parameters in DRX configuration not only have to consider the packet interval, but also have to consider the quality of service requirements of each application.

The works in [5] have analyzed and modeled the UMTS power saving operation. Moreover, the performance of LTE DRX operation with bursty data traffic is discussed

in [6] and [7]. In these works, they analyzed that the power factor and the mean packet delay based on Poisson process, but they did not provide a selection algorithm for DRX configuration.



Chapter 3.

Proposed scheme for DRX Cycle adjustment

Noted from chapter 2, the DRX parameters will significantly influence the performance of DRX operation under different traffic loads. In order to take appropriate adjustment, it is necessary to evaluate the performance over different parameter combinations in any traffic state. In this chapter, we are going to address the system model and the problem formation and then illustrate our analytical model and DRX parameter selection algorithm in detail.

3.1 System Model

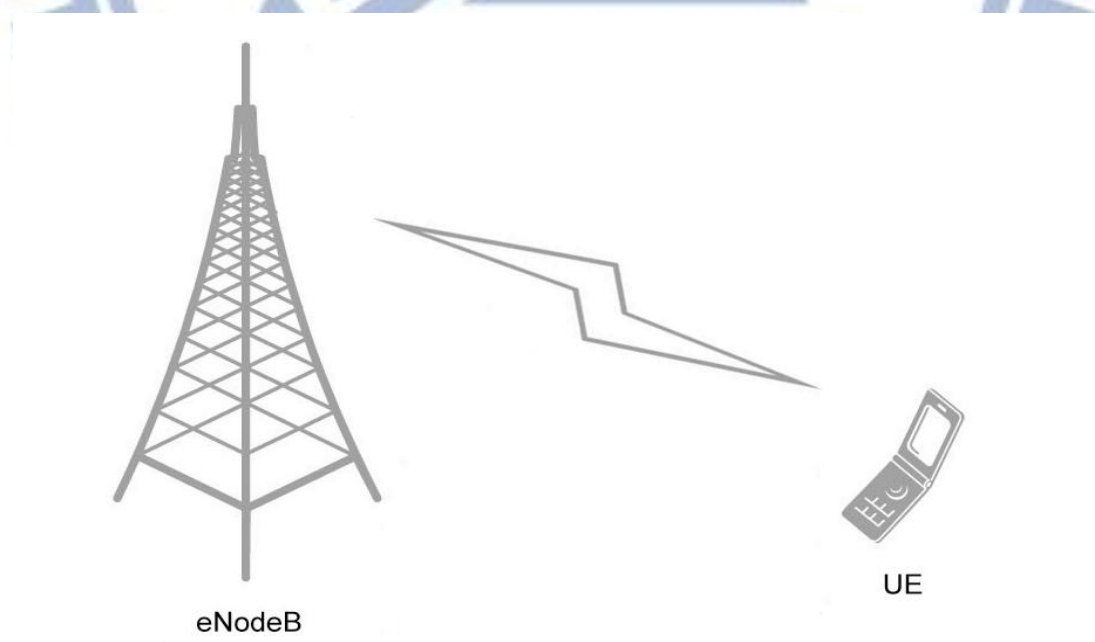


Figure 3.1: System model

Our system model is shown in Figure 3.1. A Single eNodeB with a single UE is considered in this environment. Therefore, from the discussion in Section 2.3, we set the On Duration Timer and the Inactivity Timer enough value to operate DRX mechanism. It means when eNodeB has a packet in the buffer, it can successfully transmit the packet to UE during these enough value of time. In multi-user environment eNodeB should determine the scheduling of resource allocation. These two parameter values are based on the system load in the network. Now we just consider a single pair UE/eNodeB, so we choose the minimum value for On Duration Timer and the Inactivity Timer.

From Figure 1.1, we assume that we know the traffic characteristics in both two states. The background traffics generally have low data rate and large inter-arrival time, so we only use Long DRX Cycle with minimum Inactivity Timer and On Duration Timer to guarantee the packet delay bound in the background state. Then, we enable Short DRX Cycle to reduce the packet delay to meet the delay requirement in active state.

As seen in Figure 3.2, the packet delay is produced by using the DRX mechanism. If a packet arrives in eNodeB on UE's off-duration of DRX Cycle, it will be stored in the buffer of eNodeB and will be transmitted to UE on the next on-duration of DRX Cycle. We define the time between packet arrival in eNodeB and the beginning of next on-duration DRX Cycle as packet delay.

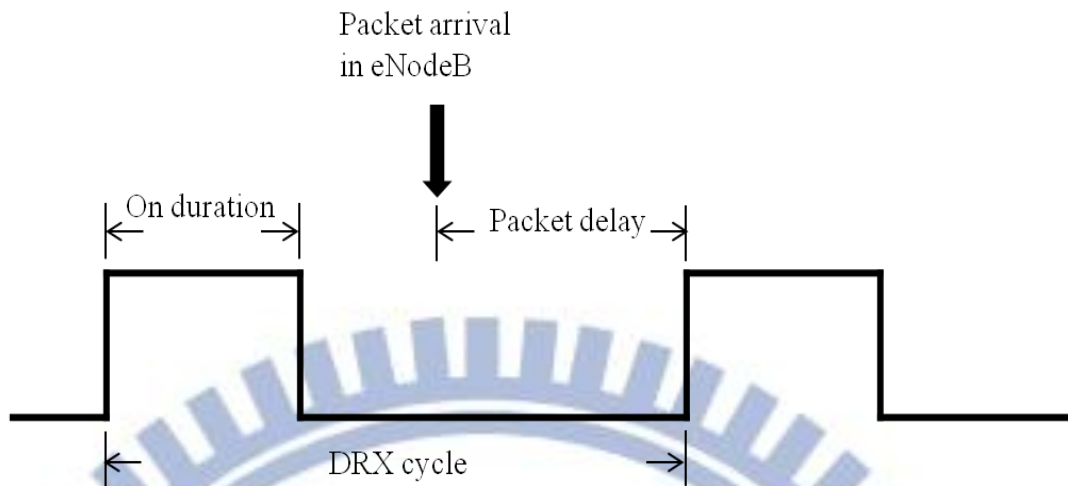


Figure 3.2: Packet delay by DRX

The problem formulation is as following:

Given the possible values of T_{LC} , T_{SC} , and N_{SC} , adjust the DRX parameters to minimize the energy consumption under downlink traffic. The packet delay requirement (90% packet delay under the delay bound δ) should be obeyed. The DRX parameter values are shown in Table 3.1.

Table 3.1: DRX parameter values [12]

DRX parameters	Values
DRX Long Cycle (T_{LC})	[10,20,32,40,64,80,128,160,256,320,512,640,1024,1280,2048,2560]ms
DRX Short Cycle (T_{SC})	[2,5,8,10,16,20,32,40,64,80,128,160,256,320,512,640]ms
Short Cycle Timer (N_{SC})	Integer [1..16]

3.2 Analytical Model

Based on the traffic model of section 2.2, we assume that an inter-packet arrival time is shorter than an inter-burst arrival time. Therefore, if $1/\lambda_{ib} \gg \mu_p/\lambda_{ip}$, the burst packet traffic model can be simplified to Compound Poisson Process with parameter λ_{ib} . And one burst contains μ_p packets on average.

We define t as inter-burst arriving time. Since the memoryless property of exponential distribution, it is true that

$$\Pr(t > X + T_{SC} | t > X) = \Pr(t > T_{SC}) \quad (3.1)$$

For this reason, we can calculate two probabilities. The probability of no burst arrives in one short cycle is $\Pr(t > T_{SC})$, and the probability of bursts arrive in one short cycle is $\Pr(t \leq T_{SC})$. We summarize as follows,

$$\begin{cases} \Pr(t > T_{SC}) = 1 - s = e^{-\lambda_{ib}T_{SC}} \\ \Pr(t \leq T_{SC}) = s = 1 - e^{-\lambda_{ib}T_{SC}} \end{cases} \quad (3.2)$$

Whenever a packet arrives in the serving eNodeB while UE is in the short cycle length and the Short Cycle Timer is running, the UE receives the packet in the next on-duration of short cycle and restarts the Short Cycle Timer. If no scheduling message is received on PDCCH during total short length, the Short Cycle Timer will expire and UE will move to long cycle. Therefore, the number of short cycle can be extended by the traffic. We define N_k is the number of total short cycle when $N_{SC} = k$. And then, we

will derive it in next paragraph.

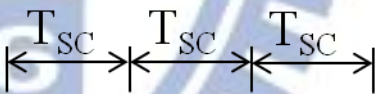
We can derive $E[N_k]$ by

$$E[N_k] = (1-s)(E[N_{k-1}] + 1) + s(E[N_{k-1}] + 1 + E[N_k]) \quad (3.3)$$

where $1-s$ is the probability of no burst arrives in one short cycle. And it is calculated by (3.2). Based on Equation (3.3) and $E[N_0] = 0$, we can show the recursive equations as follows

$$\begin{cases} E[N_k] = \frac{1}{1-s} E[N_{k-1}] + \frac{1}{1-s} \\ E[N_0] = 0 \end{cases} \quad (3.4)$$

Then $E[N_k]$ can be obtained from Equation (3.3). For example $N_{SC} = 3$, we can see in Table 3.2.

A
B
C

Table 3.2: Example

Ex: $N_{SC} = 3$	Probability	Expected number
Burst arrives in interval A	s	$E[N_3] + 1$
Burst arrives in interval B	$s(1-s)$	$E[N_3] + 2$
Burst arrives in interval C	$s(1-s)^2$	$E[N_3] + 3$
No burst arrives	$(1-s)^3$	3

From the example, we summarize $E[N_3]$ by

$$E[N_3] = s(E[N_3] + 1) + s(1-s)(E[N_3] + 2) + s(1-s)^2(E[N_3] + 3) + (1-s)^3 \times 3$$

$$\Rightarrow E[N_3] = \frac{s + 2s(1-s) + 3s(1-s)^2 + 3(1-s)^3}{1-s-s(1-s)-s(1-s)^2} \quad (3.5)$$

Now, we can represent the general form shown in (3.6).

$$E[N_k] = \frac{\sum_{n=1}^k ns(1-s)^{n-1} + (1-s)^k \times k}{1 - \sum_{n=1}^k s(1-s)^{n-1}} \quad (3.6)$$

From (3.6), we obtain the expected number of short cycle. Then, we derive the expected number of short cycle length by

$$E[N_k] \times T_{SC} \quad (3.7)$$

Accordingly, we define $m = \lceil E[N_k] \times T_{SC} / T_{LC} \rceil$. It means that total short cycle length $E[N_k] \times T_{SC}$ ends in m th long cycle, and UE moves to long cycle, i.e. Figure 3.3. In Figure 3.3, δ is the delay bound and it shows that the packet arrivals in the gray blocks do not obey the delay requirement.

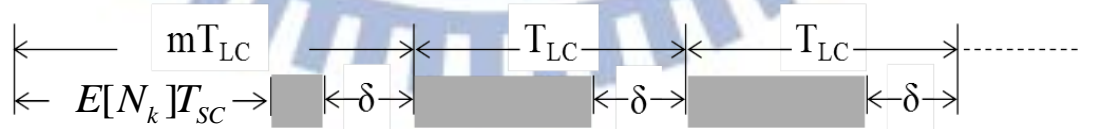


Figure 3.3: illustration of delay by DRX

When a packet arrives in eNodeB on any UE's Long DRX Cycle, it will be transmitted to UE during the next on-duration of long cycle. Then, UE starts the Short Cycle Timer once again. It forms a regenerate cycle as Figure 3.4.

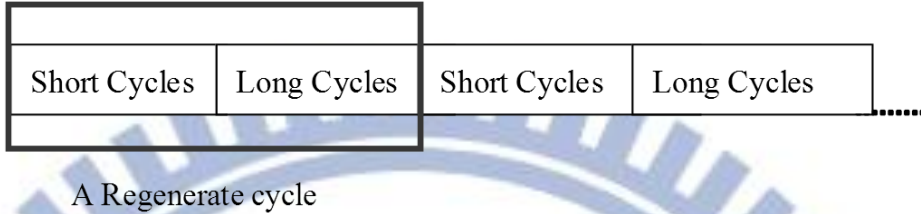


Figure 3.4: Regenerate cycle representation

It can be divided into two conditions as shown in Figure 3.5 and 3.7 by whether the burst arrives in the gray block in Figure 3.5.

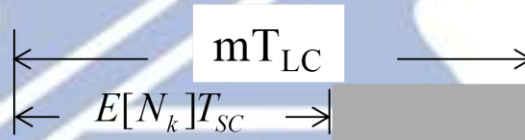


Figure 3.5: Case 1: next burst arrives in $mT_{LC} - E[N_k]T_{SC}$

Case 1 is the condition of next burst arrives in the gray block, that is, in the period $mT_{LC} - E[N_k]T_{SC}$. By DRX mechanism, the regenerate cycle will stop at the end of m -th T_{LC} . The average number of bursts arrive in this case can be derived by

$$\lambda_{ib} \times mT_{LC} \tag{3.8}$$

where mT_{LC} is the average regenerate cycle length of this case. Then, we derive the average number of bursts arrive in the gray block of Figure 3.5 as shown by

$$\lambda_{ib} \times (mT_{LC} - E[N_k]T_{SC}) \quad (3.9)$$

Accordingly, in Figure 3.6 the probability of burst arrives in the gray block which means these bursts do not meet the delay requirement is derived by

$$\frac{(T_{LC} - \delta)}{T_{LC}} \quad (3.10)$$

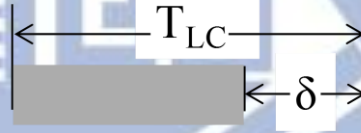


Figure 3.6: illustration of the probability of burst arrives in the gray block

The probability of bursts arrives in the gray block in case 1 is smaller than (3.10).

Hence, the average number of bursts arrive in the gray block of Figure 3.5 and does not satisfy the delay requirement is shown in (3.11)

$$\lambda_{ib} \times (mT_{LC} - E[N_k]T_{SC}) \times y$$

$$\text{where } y = \begin{cases} 0 & , \quad mT_{LC} - E[N_k]T_{SC} - \delta \leq 0 \\ \frac{mT_{LC} - E[N_k]T_{SC} - \delta}{mT_{LC} - E[N_k]T_{SC}} & , \quad mT_{LC} - E[N_k]T_{SC} - \delta > 0 \end{cases}$$

$$(3.11)$$

Based on the properties of Poisson Process, we can calculate the probability of case 1 occur by

$$1 - e^{-\lambda_{ib}(mT_{LC} - E[N_k]T_{sc})} \quad (3.12)$$

Now, we consider case 2 , no burst arrives in the gray block of Figure 3.4. As shown in Figure 3.6, it may cause the regenerate cycle extending until bursts arrival.

We define L as the number of extended long cycles . Whenever a burst arrives in long cycle length, UE restarts short cycle. Based on memoryless property, the probability of bursts arrive in a long cycle length is $1 - e^{-\lambda_{ib}T_{LC}}$. Thus, we can drive $E[L]$ by using the same method in (3.6).

$$E[L] = \left[(1 - e^{-\lambda_{ib}T_{LC}}) \times 1 + e^{-\lambda_{ib}T_{LC}} \times (E[L] + 1) \right] \times T_{LC}$$

$$E[L] = \frac{1}{1 - e^{-\lambda_{ib}T_{LC}}} \times T_{LC} \quad (3.13)$$

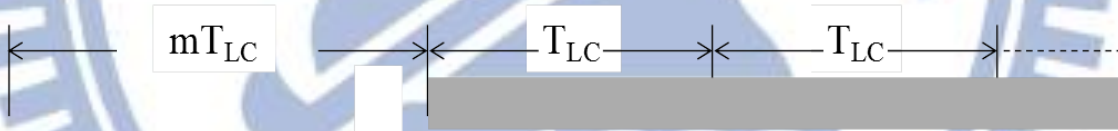


Figure 3.7: Case 2 : next burst arrives not in mT_{LC}

The average length of case 2 is

$$(m + E[L]) \times T_{LC} \quad (3.14)$$

From (3.14), we derived the average number of bursts arrive in case 2 by adding the average number of bursts arrive in the gray block of case 2 with the average number of bursts arrive in mT_{LC} .

The average number of bursts arrive in the gray block of case 2

$$\begin{aligned}
 &= \lambda_{ib} T_{LC} + (1 - e^{-\lambda_{ib} T_{LC}}) \lambda_{ib} T_{LC} + (1 - e^{-\lambda_{ib} T_{LC}})^2 \lambda_{ib} T_{LC} + (1 - e^{-\lambda_{ib} T_{LC}})^3 \lambda_{ib} T_{LC} + \dots \\
 &= \frac{\lambda_{ib} T_{LC}}{1 - e^{-\lambda_{ib} T_{LC}}} \\
 &= E[L] \lambda_{ib} T_{LC}
 \end{aligned} \tag{3.15}$$

Finally, we combine (3.8) and (3.15), then we have the average number of bursts arrive in case 2 in (3.16)

$$\lambda_{ib} \times (m + E[L]) \times T_{LC} \tag{3.16}$$

Thus, we can derive the average number of bursts which fails to meet delay requirement and arrive in the gray block of Figure 3.7 by

$$\lambda_{ib} \times \frac{1}{1 - e^{(-\lambda_{ib} T_{LC})}} \times T_{LC} \times \frac{(T_{LC} - \delta)}{T_{LC}} \tag{3.17}$$

We calculate the probability of case 2 occur by

$$e^{-\lambda_{ib} (m T_{LC} - E[N_k] T_{SC})} \tag{3.18}$$

Due to (3.11), (3.12), (3.17), and (3.18), the average number of bursts fail to meet delay requirement in one regenerate cycle is less than

$$\lambda_{ib}(mT_{LC} - E[N_k]T_{SC})y + \lambda_{ib} \times xE[L]T_{LC} \times \frac{T_{LC} - \delta}{T_{LC}}$$

where $x = e^{-\lambda_{ib}(mT_{LC} - E[N_k]T_{SC})}$

$$y = \begin{cases} 0 & , \quad mT_{LC} - E[N_k]T_{SC} - \delta \leq 0 \\ \frac{mT_{LC} - E[N_k]T_{SC} - \delta}{mT_{LC} - E[N_k]T_{SC}} & , \quad mT_{LC} - E[N_k]T_{SC} - \delta > 0 \end{cases} \quad (3.19)$$

By (3.9), (3.12), (3.14), and (3.18) we derive the average number of bursts arrive in one regenerate cycle by

$$\lambda_{ib} \left[(1 - e^{-\lambda_{ib}(mT_{LC} - E[N_k]T_{SC})})m + (e^{-\lambda_{ib}(mT_{LC} - E[N_k]T_{SC})})(m + E[L]) \right] T_{LC} \quad (3.20)$$

Finally, we summarize the Equation (3.19) and (3.20). The probability P is shown in (3.21)

$$P \triangleq \frac{\text{The average number of bursts fail to meet the delay bound requirement in one regenerate cycle}}{\text{The average number of bursts arrive in one regenerate cycle}}$$

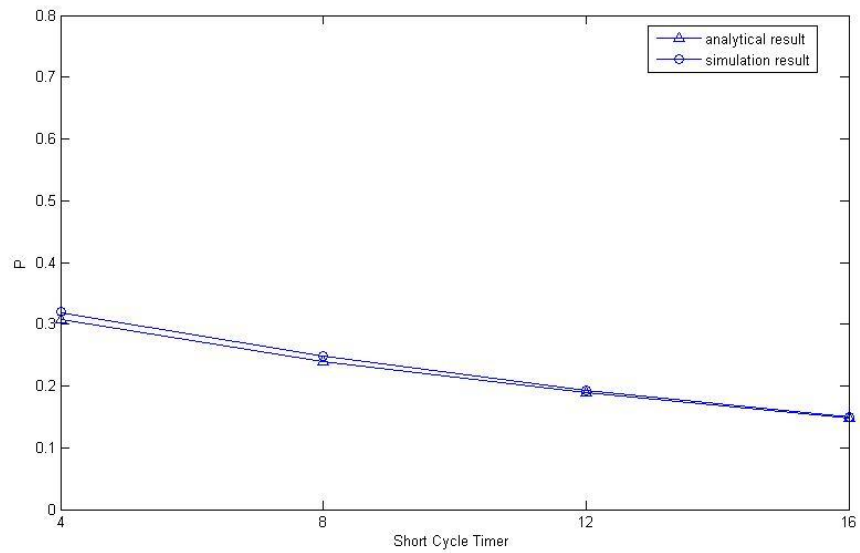
$$= \frac{\lambda_{ib}(mT_{LC} - E[N_k]T_{SC})y + \lambda_{ib} \times xE[L]T_{LC} \times \frac{T_{LC} - \delta}{T_{LC}}}{\lambda_{ib} [(1-x)m + x(m + E[L])]T_{LC}}$$

where $x = e^{-\lambda_{ib}(mT_{LC} - E[N_k]T_{SC})}$

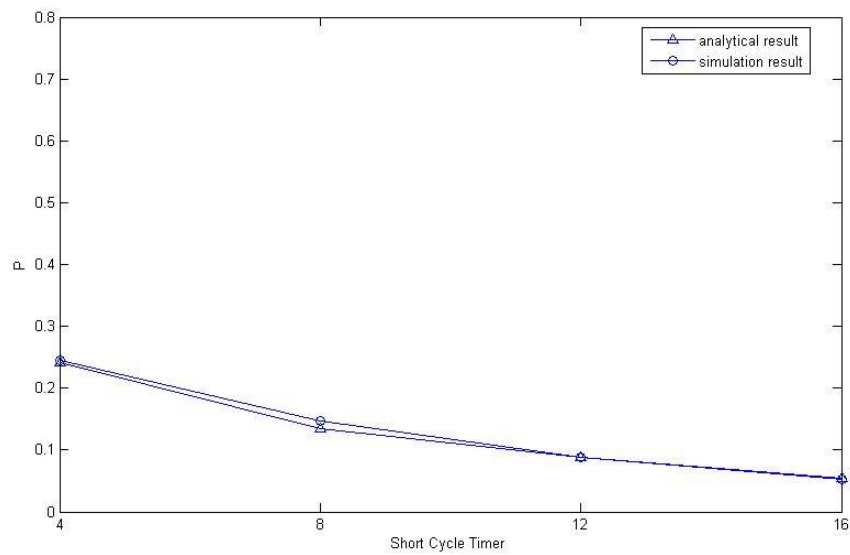
$$y = \begin{cases} 0 & , \quad mT_{LC} - E[N_k]T_{SC} - \delta \leq 0 \\ \frac{mT_{LC} - E[N_k]T_{SC} - \delta}{mT_{LC} - E[N_k]T_{SC}} & , \quad mT_{LC} - E[N_k]T_{SC} - \delta > 0 \end{cases} \quad (3.21)$$

3.3 Comparison between Analytical and Simulation Result

We have validated the analytical model against simulation experiments.



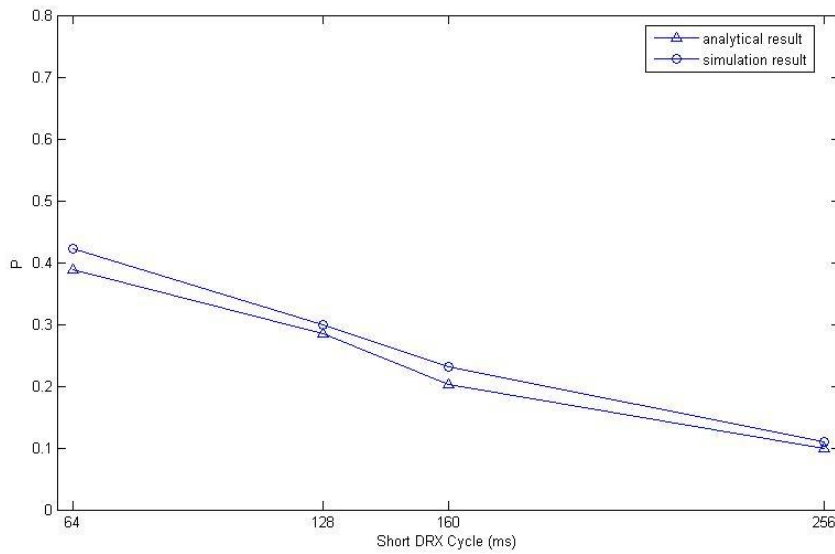
(a)



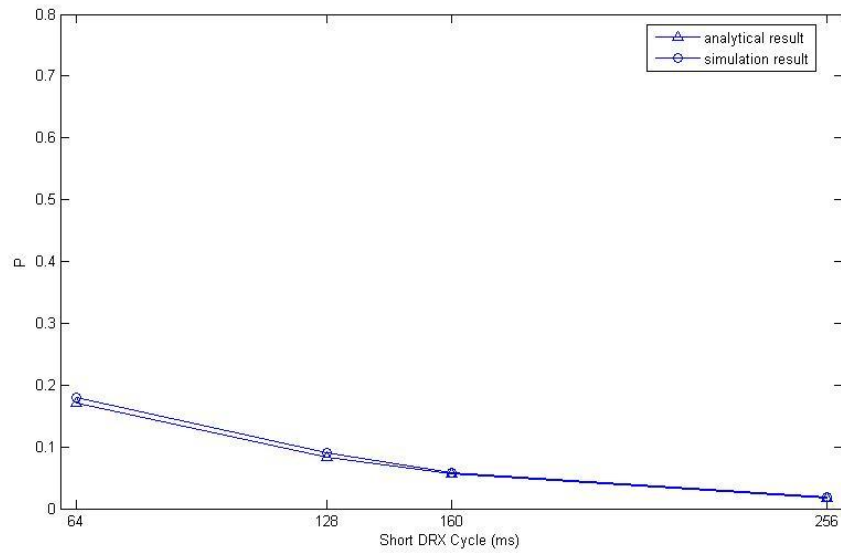
(b)

Figure 3.8: Performance comparison among analytical results and simulation results for different N_{SC} .

Figure 3.8 (a) shows the performance comparison among analytical results and simulation results, where $T_{LC}=256\text{ms}$, $T_{SC}=64\text{ms}$, $\delta=150\text{ms}$, $\lambda=0.001$. Figure 3.8 (b) shows the performance comparison among analytical results and simulation results, where $T_{LC}=256\text{ms}$, $T_{SC}=128\text{ms}$, $\delta=150\text{ms}$, $\lambda=0.001$. We can see that when the number of Short Cycle Timer increases, the probability of packet delay under the delay bound decreases. The reason is that using a bigger Short Cycle Timer tends to extend total Short Cycle Length. Therefore, UE takes more time in short cycles. It will reduce the probability of packet delay over the delay bound



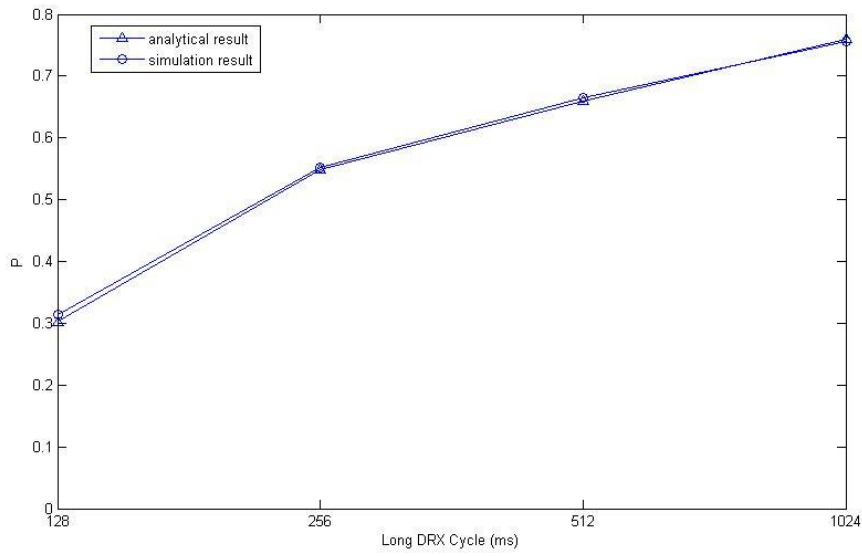
(a)



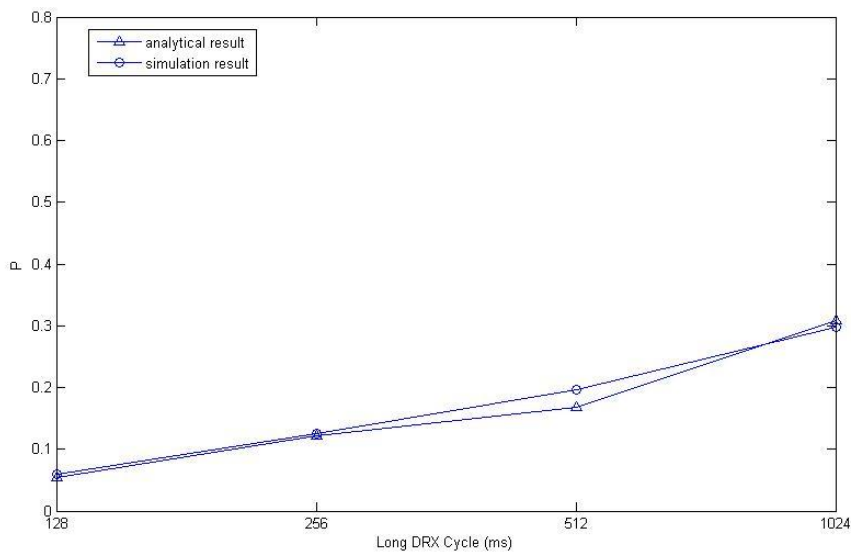
(b)

Figure 3.9: Performance comparison among analytical results and simulation results for different T_{SC} .

Figure 3.9(a) is the performance comparison among analytical results and simulation results, where $T_{LC}=1024ms$, $N_{SC}=8$, $\delta=300ms$, $\lambda=0.001$. Figure 3.9(b) is the performance comparison among analytical results and simulation results, where $T_{LC}=512ms$, $N_{SC}=12$, $\delta=300ms$, $\lambda=0.001$. It shows that the longer Short DRX Cycle is, the lower probability of packet delay under the delay bound is. As mentioned above, it will reduce the probability of packet delay over the delay bound, too.



(a)



(b)

Figure 3.10: Performance comparison among analytical results and simulation results for different T_{LC} .

Figure 3.10(a) shows the performance comparison among analytical results and simulation results, where $N_{SC}=4$, $T_{SC}=64ms$, $\delta=75ms$, $\lambda=0.001$. Figure 3.10(b) shows the performance comparison among analytical results and simulation results, where

$N_{SC}=6$, $T_{SC}=64\text{ms}$, $\delta=75\text{ms}$, $\lambda=0.005$. As the Long DRX Cycle increases, the probability of packet delay over the delay bound increases. Using longer Long DRX Cycle make the waiting time of packets increasing. Therefore, the number of packets which have to wait longer than the delay bound will rise.

From Figure3.8, Figure 3.9 and Figure3.10, we can find that the analytical results are slightly bigger than the simulation results. The reasons why the analytical results are bigger are that we use a bigger average number of packets fail to meet delay requirement and that we ignore the influence of On Duration Timer and Inactivity Timer in analytical model.

Note that the analytical results usually slightly smaller than the simulation results because the probability of case 2 occur we use is $e^{-\lambda_{ib}(mT_{LC}-E[N_k]T_{SC})}$ which is likely a geometric mean. By the inequality of geometric and arithmetic mean, geometric mean is smaller than arithmetic mean. So, the analytical probability of case 2 occur is smaller than simulation results. However, the number of burst arrives in case 2 is bigger than the number of bursts arrives in case 1. Thus, the analytical average numbers of bursts arrive is smaller than simulation results. It will lead the probability of bursts fail to meet the delay requirement decrease.

The other reason is the calculation errors of average number of bursts fail to meet

the delay requirement in case 1. We use $\lambda_{ib} \left(\left[\frac{E[N_k] \times T_{SC}}{T_{LC}} \right] \times T_{LC} - E[N_k] T_{SC} - \delta \right)$ to

approach the actual average number $\lambda_{ib} \times E \left[\left[\frac{N_k \times T_{SC}}{T_{LC}} \right] \times T_{LC} - N_k T_{SC} - \delta \right]$.

3.4 Selection Algorithm

In this section, according to the analytical model derived in previous section, a selection policy for DRX Cycles is shown in Figure 3.11.

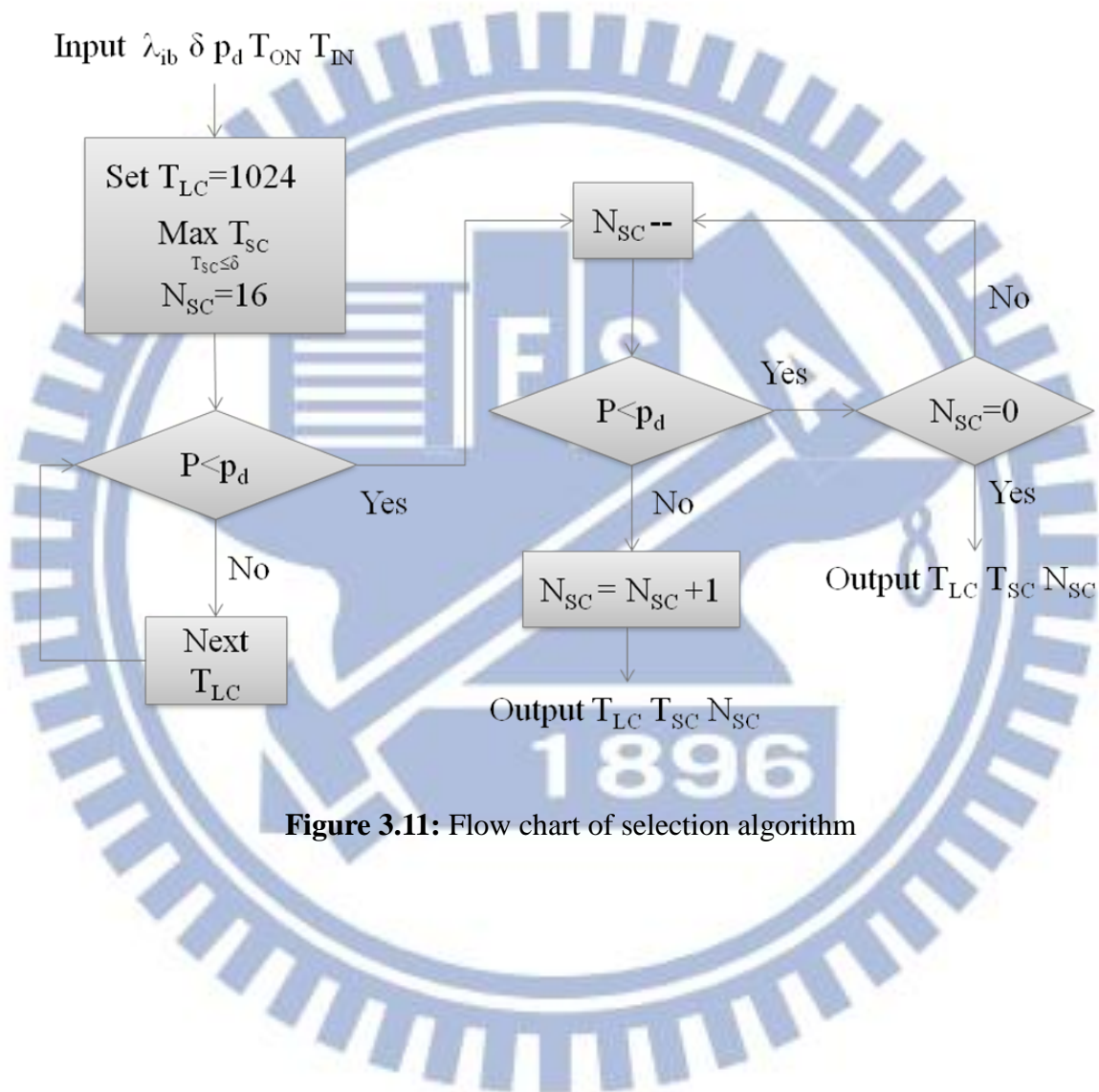


Figure 3.11: Flow chart of selection algorithm

After illustrating the ideas of our algorithm, the following table is pseudo codes of our algorithm.

Table 3.3: Selection algorithm

Algorithm : Proposed scheme for DRX Cycle
adjustment

Inputs : λ_{tb} δ p_d T_{ON} T_{IN}

1. *default*
 - set* $T_{LC} = 1024$
 - Max* T_{SC}
 $T_{SC} \leq \delta$
 - $N_{SC} = 16$
2. *calculate* P
 - while* ($P \geq p_d$)
 - update* T_{LC} *value to Next* T_{LC}
 - end while*
3. *while* (1)
 - calculate* P
 - if* ($P < p_d$)
 - update* $N_{SC} = N_{SC} - 1$
 - else if* ($P \geq p_d$)
 - update* $N_{SC} = N_{SC} + 1$
 - end if*
 - break if* $P \geq p_d$ *or* $N_{SC} < 0$
 - end while*

Outputs : T_{LC} T_{SC} N_{SC}

Chapter 4.

Performance Evaluation

In this chapter, simulations are conducted to evaluate the performance of proposed scheme, which will be compared with the fixed DRX operation without adaptively adjusting DRX parameters.

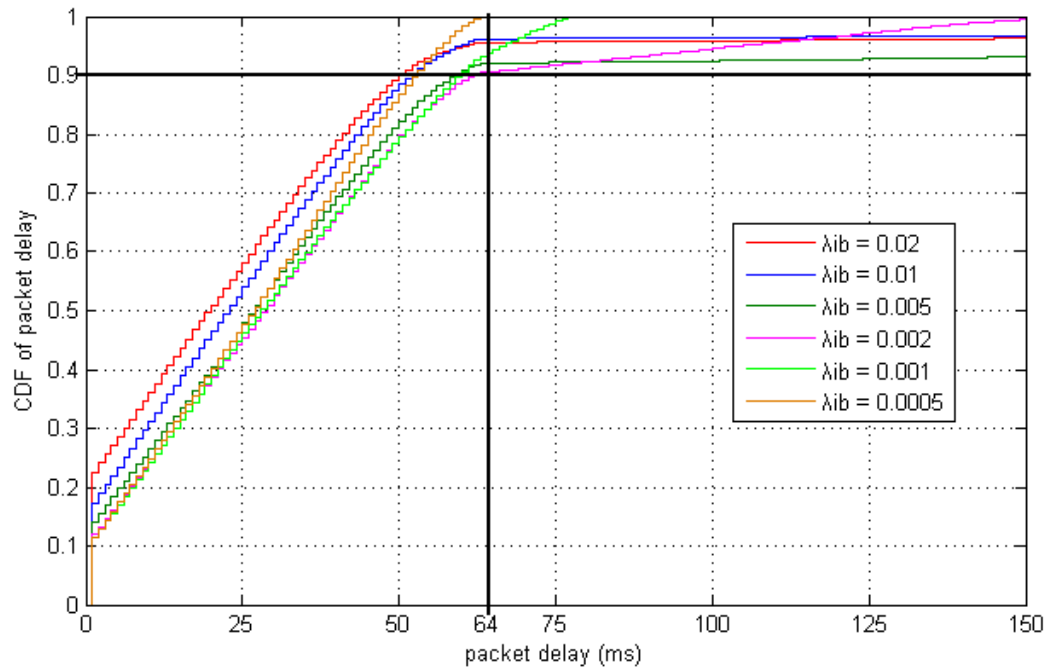
4.1 Parameters

The probability of packet delay over the delay bound δ , p_d , is set to 0.9. And the delay bound δ is set to 64ms, 128ms, and 256ms. The parameters of the numerical simulation are listed in Table 4.1. A Single eNodeB and a single UE with downlink traffic is considered in this simulation environment. The On Duration Timer and Inactivity Timer are set as 2ms and 10ms for all cases. The value of Long Cycle based on the delay requirement in background state is assumed to be 1024ms, so we set the initial Long Cycle value as 1024ms.

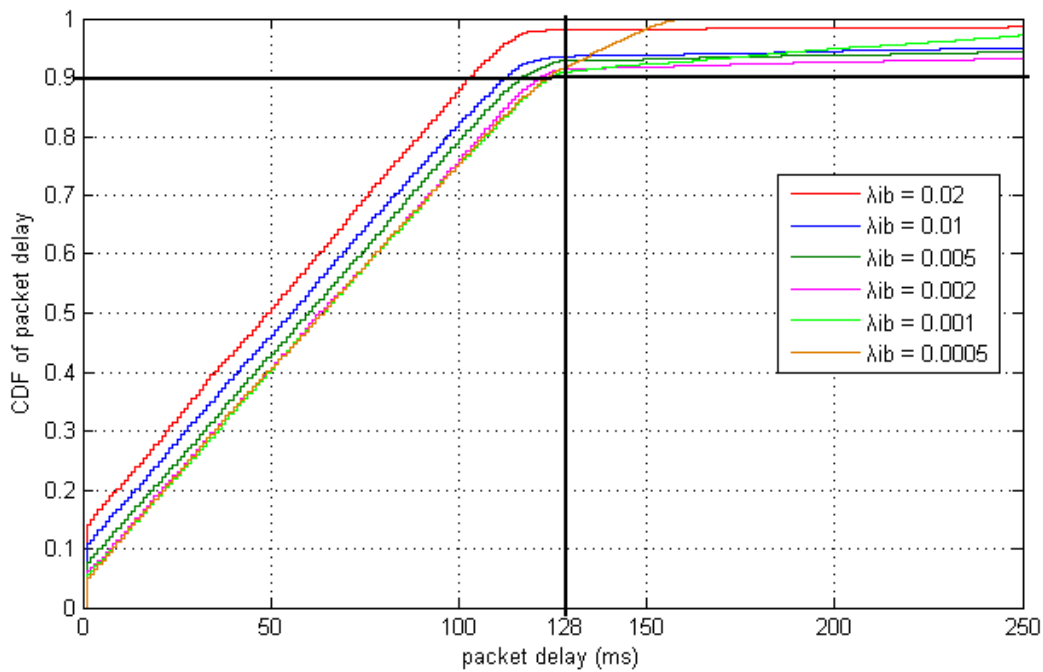
Table 4.1: Parameters

- $p_d=0.1$
- The delay bound $\delta = 64, 128, 256\text{ms}$
- $T_{ON}=2\text{ms}, T_{IN}=10\text{ms}$
- Initial $T_{LC} = 1024\text{ms}$
- $\lambda_{ip}=1$ arrivals/ms, $\mu_p=6$
- Number of bursts in simulation = 10000

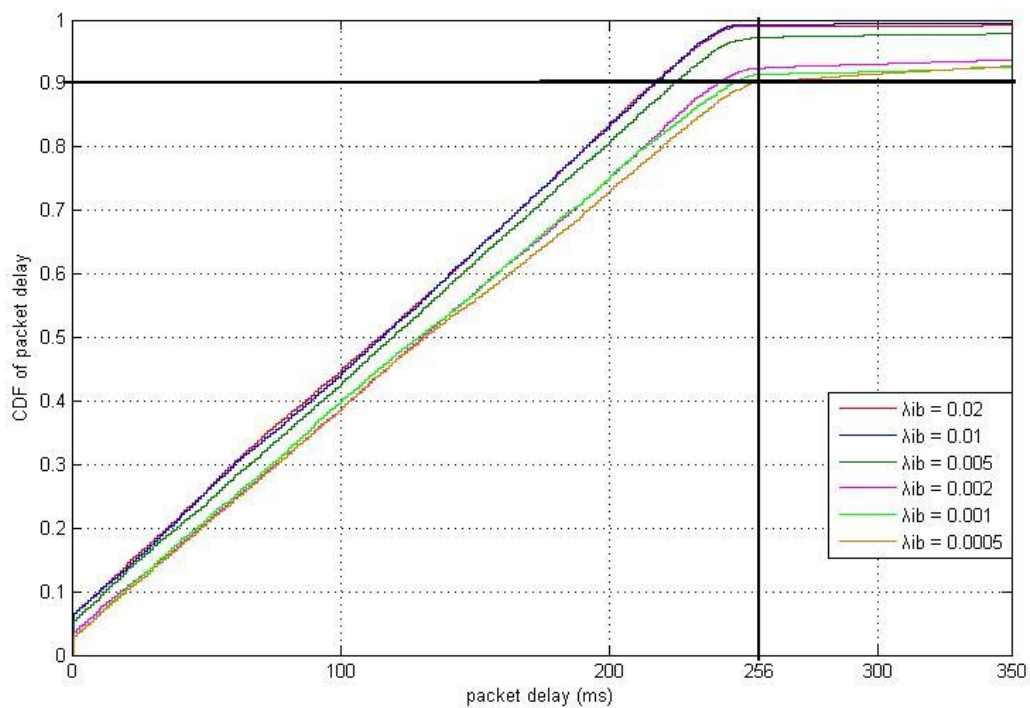
4.2 Simulation Results



(a) Delay bound 64ms



(b) Delay bound 128ms

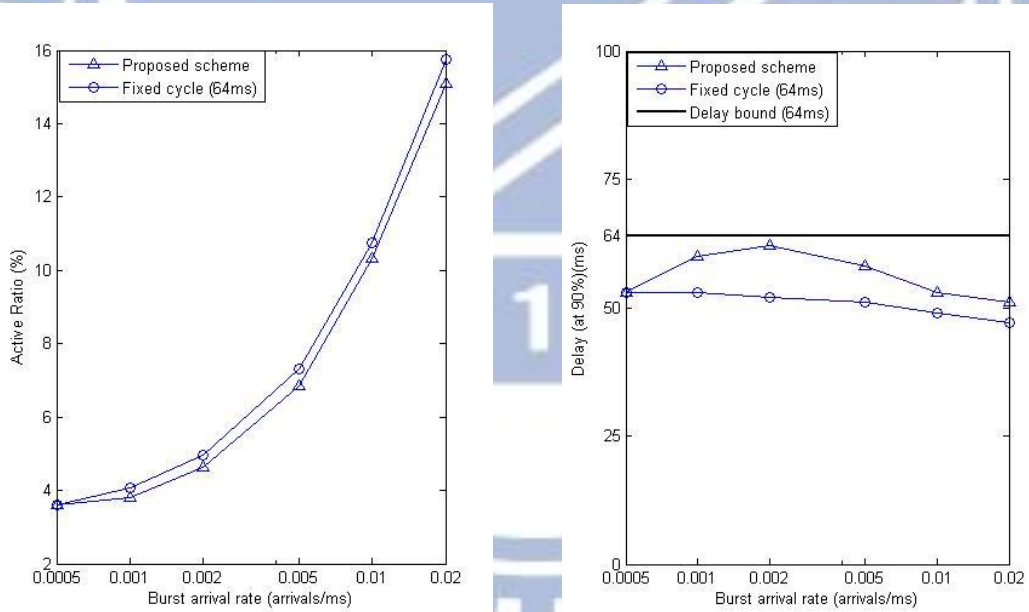


(c) Delay bound 256ms

Figure 4.1: The packet delay CDF of proposed scheme

The packet delay CDF of proposed scheme is shown in Figure 4.4. In our scheme, we prove that the delay requirement (90% packet delay under the delay bound δ) in different inter-burst arrival time is obeyed. From the figure, we can see the packet delay CDF has linear-like relationship with delay. And the turning points of these lines occur in the delay value $T_{SC} - T_{ON}$.

In the following figures, we show that the active ratio and delay probabilities respectively compare with fixed cycle scheme in different delay requirement δ as well as burst arrival rate λ_{tb} . Fixed cycle does not use Short Cycle in DRX operation, and use smaller fixed Long Cycle than delay bound δ instead.



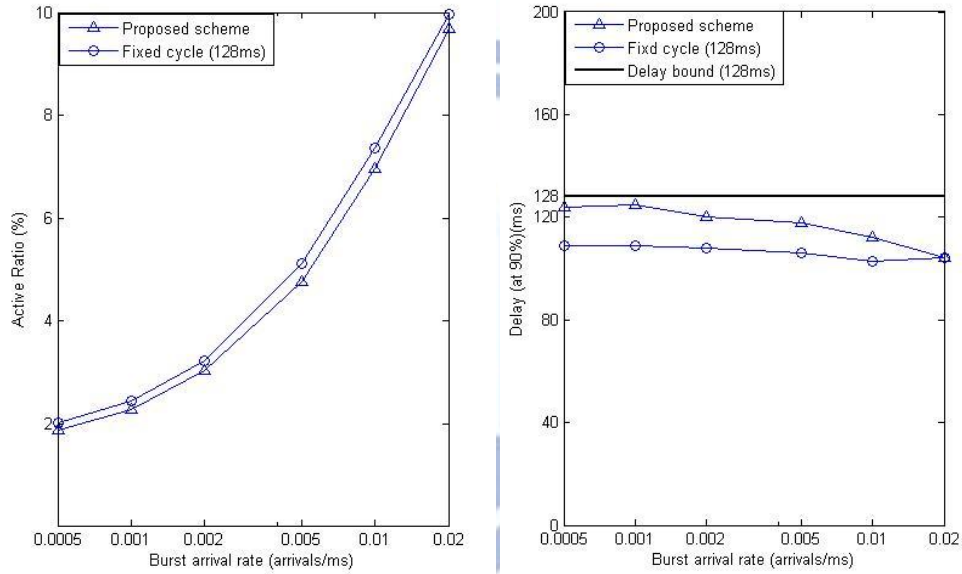
(a) Active ratio (Delay bound 64ms)

(b) Packet delay at 90% (Delay bound 64ms)

Figure 4.2: Performance comparison among proposed scheme and fixed cycle in delay bound 64ms

Table 4.2 Parameters of Delay bound 64ms (T_{SC} 64ms)

λ_{ib}	0.0005	0.001	0.002	0.005	0.01	0.02
T_{LC}	64	80	160	1024	1024	1024
N_{SC}	0	11	14	11	7	4



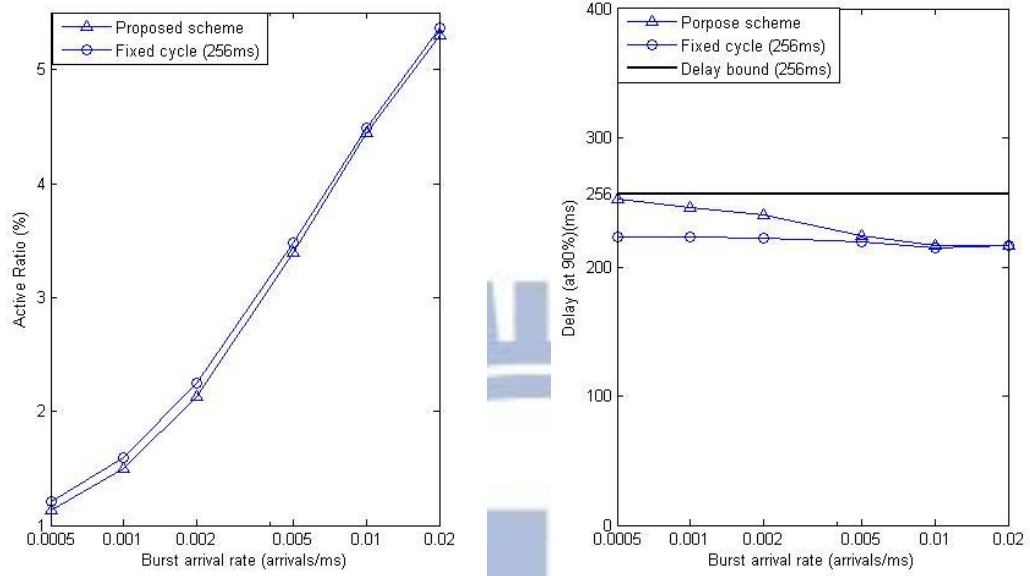
(a) Active ratio (Delay bound 128ms)

(b) Packet delay at 90% (Delay bound 128ms)

Figure 4.3: Performance comparison among proposed scheme and fixed cycle in delay bound 128ms

Table 4.3 Parameters of Delay bound 128ms (T_{SC} 128ms)

λ_{ib}	0.0005	0.001	0.002	0.005	0.01	0.02
T_{LC}	160	320	1024	1024	1024	1024
N_{SC}	11	14	11	5	3	2



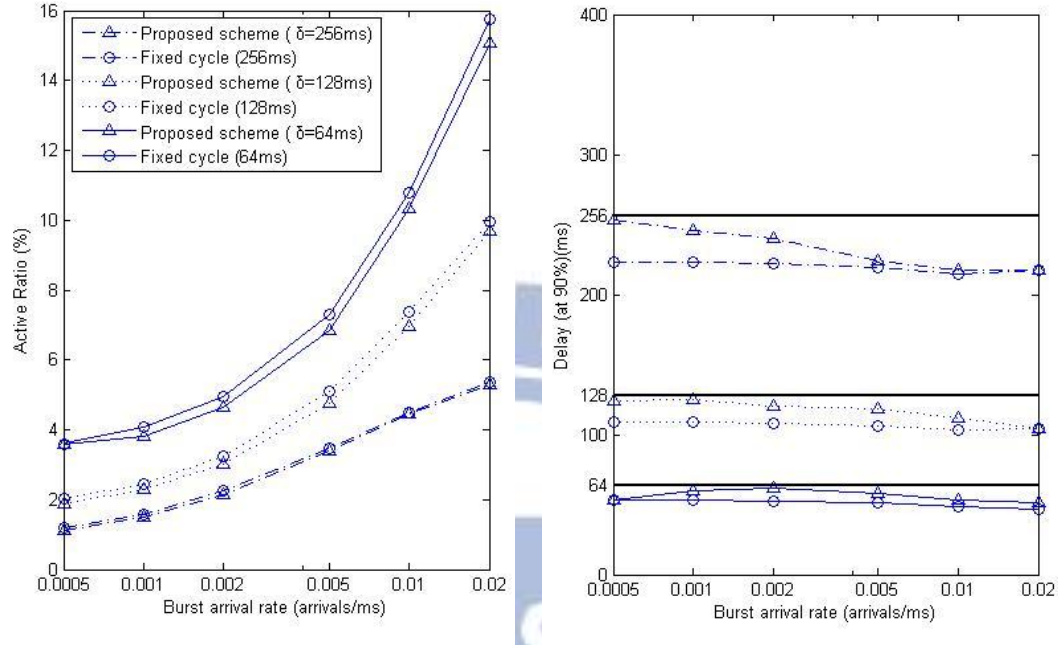
(a) Active ratio (Delay bound 256ms)

(b) Packet delay at 90% (Delay bound 256ms)

Figure 4.4: Performance comparison among proposed scheme and fixed cycle in delay bound 256ms

Table 4.4 Parameters of Delay bound 256ms (T_{SC} 256ms)

λ_{ib}	0.0005	0.001	0.002	0.005	0.01	0.02
T_{LC}	640	1024	1024	1024	1024	1024
N_{SC}	14	9	5	3	2	1



(a) Active ratio

(b) Packet delay at 90%

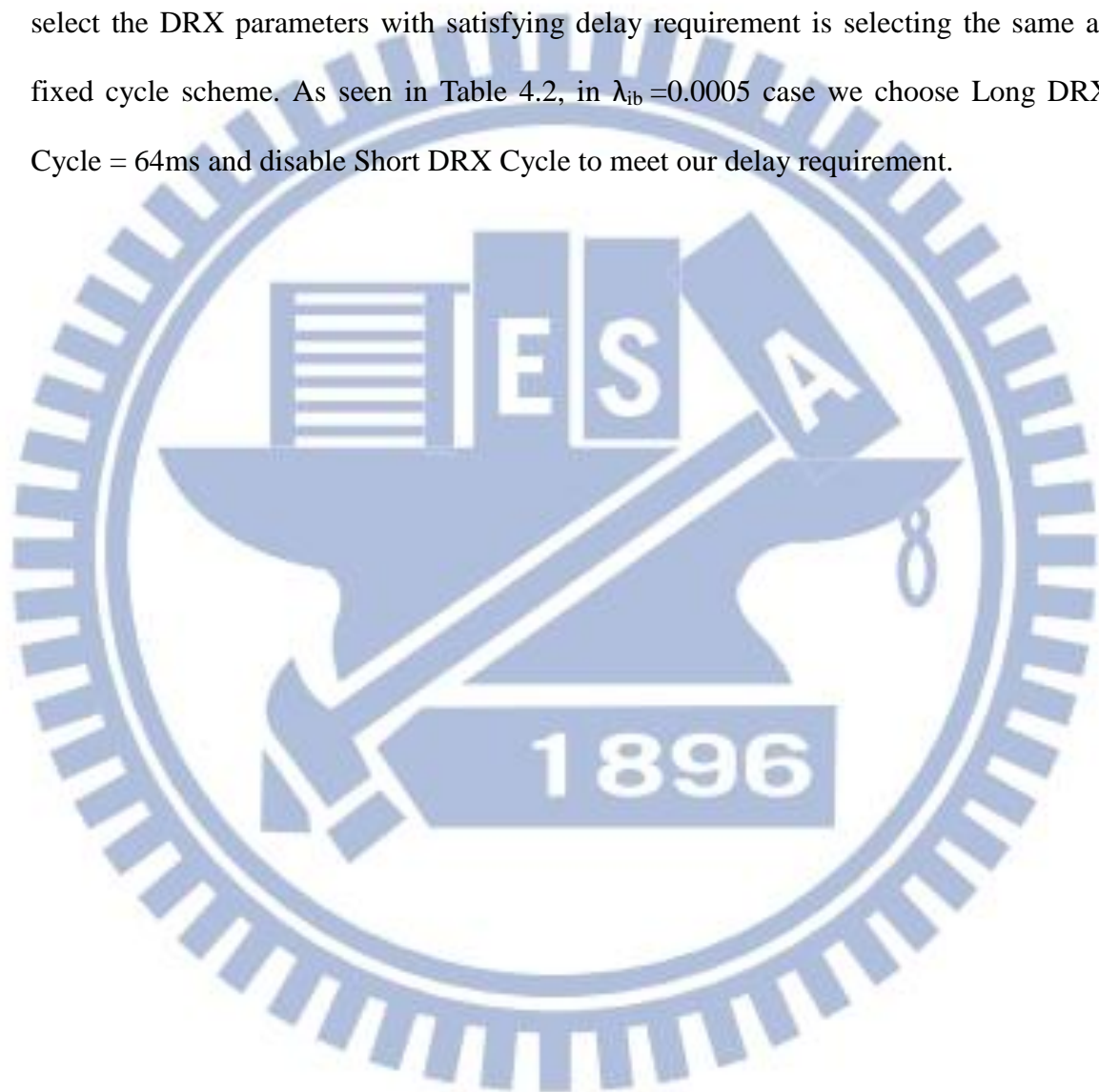
Figure 4.5: Performance comparison among proposed scheme and fixed cycle in different delay bound

From Figure 4.5, it can be observed that the active ratio of proposed scheme is lower than the compared fixed cycle scheme but the packet delay is higher than the compared fixed cycle scheme. In other words, we sacrifice some packet delay to reduce the active ratio. From Table 4.2, Table 4.3, and Table 4.4, it is clear that instead of decreasing the Long DRX Cycle, enabling Short DRX Cycle with appropriate Short Cycle Timer can effectively decrease packet delay.

Then, we should note that as the value of λ_{ib} increases, active ratio will increase because the Inactivity Timer extends UE's on-duration. When the value of delay bound is small, meeting the delay requirement will lead to increase in active ratio.

Note that the proposed scheme has similar performance as the compared fixed

cycle scheme. That is because as the value of p_d increases, the time UE operates in short cycles also increases. When UE almost operates in short cycles, the performance will approach the fixed cycle scheme (the Short Cycle value used by our scheme is equal to the cycle value of fixed cycle scheme). The worst situation of our algorithm to select the DRX parameters with satisfying delay requirement is selecting the same as fixed cycle scheme. As seen in Table 4.2, in $\lambda_{ib} = 0.0005$ case we choose Long DRX Cycle = 64ms and disable Short DRX Cycle to meet our delay requirement.



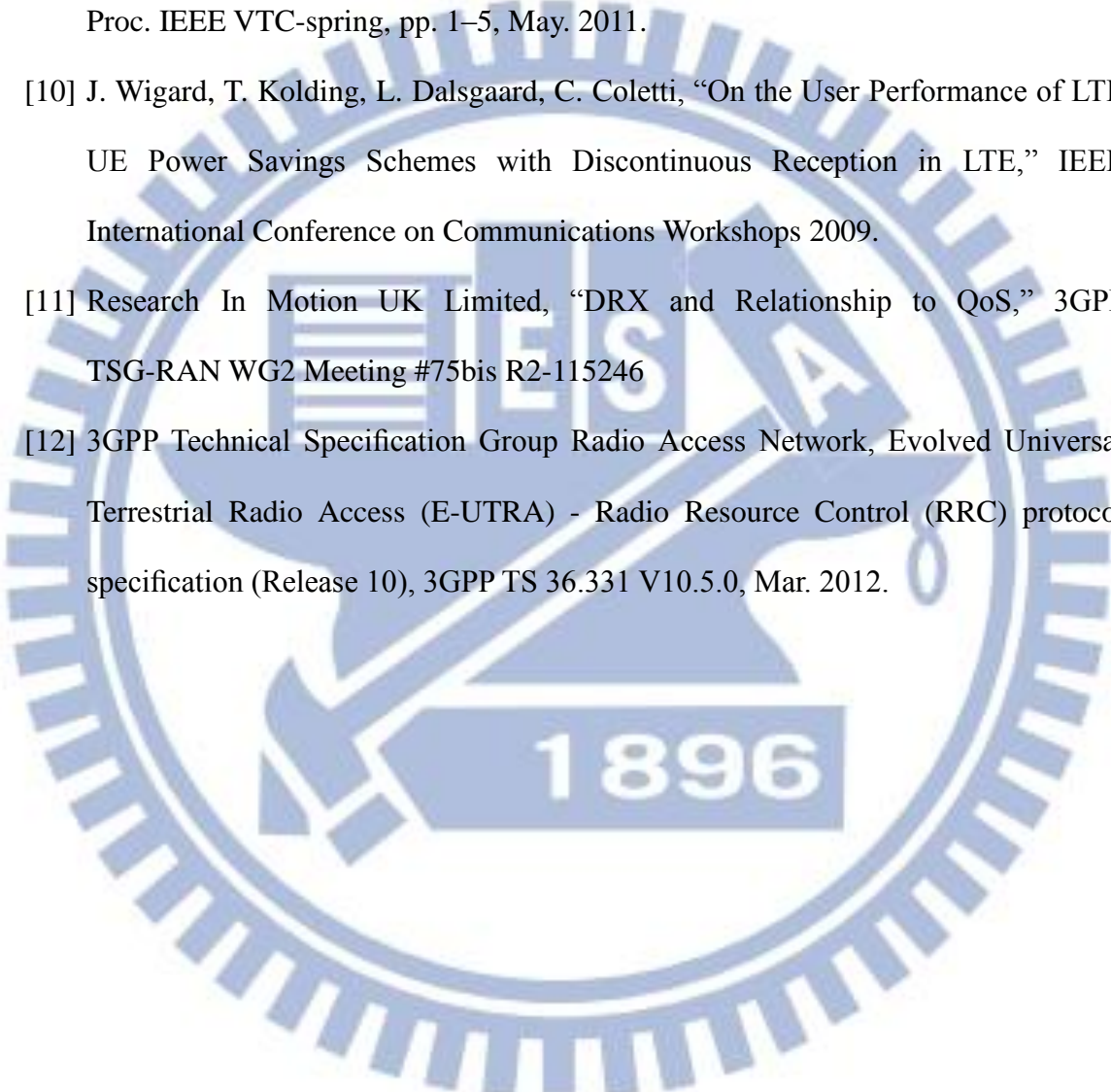
Chapter 5.

Conclusion

In this thesis, we take an overview of LTE DRX mechanism with adjustable DRX cycles and derive a mathematical model based on bursty packet traffic model. The analytical results match the simulation results. Through this model, we propose an algorithm for choosing DRX parameters. This algorithm tends to choose bigger long DRX cycle with smaller short cycle timer to satisfy the quality of service. Despite it may not have the guarantee to minimize the power consumption, it provides a simple way to choose DRX parameter with satisfying the delay requirement.

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Appendix

Based on Section 3.1, we set the On Duration Timer and the Inactivity Timer minimum enough value to operate DRX mechanism. So we ignore the influence of On Duration Timer and Inactivity Timer in Section 3.2. In this chapter, we try to consider the influence of Inactivity Timer. When a burst arrives in the period of Inactivity Timer, it will restart another Inactivity Timer. If the longer T_{in} we use, the bigger impact of Inactivity Timer it will be. Therefore, we must consider the impact of Inactivity Timer within big T_{in} .

Now, we define R as the total time of T_{in} extended until T_{in} expires. By using the same method in Equation (3.6) we have

$$E[R] = \frac{\sum_{n=1}^{T_{in}} nq(1-q)^{n-1} + (1-q)^{T_{in}} \times T_{in}}{1 - \sum_{n=1}^{T_{in}} q(1-q)^{n-1}}$$

where q is the probability of bursts arrive in one subframe. Then, we want to calculate a new $E[N_k]$ to replace $E[N_k]$, where $E[N_k]$ is the average number of total short DRX cycle length in one generating cycle with considering the Inactivity Timer. We define W as the extended short DRX cycle after initial Inactivity Timer expired. As seen in Table A.1, if a burst arrives in the interval A, B, or C, it will start the Inactivity Timer and reset the Short Cycle Timer.

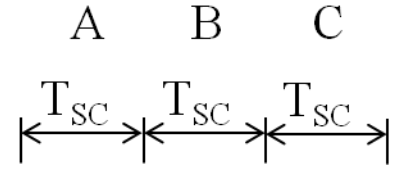


Table A.1: Example

Ex: $N_{SC} = 3$	Probability	Expected number
Burst arrives in interval A	s	$E[W] + 1 + \frac{E[R]}{T_{SC}}$
Burst arrives in interval B	$s(1-s)$	$E[W] + 2 + \frac{E[R]}{T_{SC}}$
Burst arrives in interval C	$s(1-s)^2$	$E[W] + 3 + \frac{E[R]}{T_{SC}}$
No burst arrives	$(1-s)^3$	$3 + \frac{E[R]}{T_{SC}}$

From the example, we summarize $E[W]$ by

$$\Rightarrow E[W] = \frac{s + 2s(1-s) + 3s(1-s)^2 + 3(1-s)^3}{1-s-s(1-s)-s(1-s)^2} + \frac{s + s(1-s) + s(1-s)^2}{1-s-s(1-s)-s(1-s)^2} \frac{E[R]}{T_{SC}}$$

Thus, we have $E[N_3]$

$$\begin{aligned} E[N_3] &= E[W] + \frac{E[R]}{T_{SC}} \\ &= \frac{s + 2s(1-s) + 3s(1-s)^2 + 3(1-s)^3}{1-s-s(1-s)-s(1-s)^2} + \frac{s + s(1-s) + s(1-s)^2}{1-s-s(1-s)-s(1-s)^2} \frac{E[R]}{T_{SC}} + \frac{E[R]}{T_{SC}} \end{aligned}$$

Now, we can represent the general form

$$E[N_k] = \frac{\sum_{n=1}^k ns(1-s)^{n-1} + (1-s)^k \times k}{1 - \sum_{n=1}^k s(1-s)^{n-1}} + \frac{1}{1 - \sum_{n=1}^k s(1-s)^{n-1}} \frac{E[R]}{T_{sc}}$$

It can be applied to modify our Equation 3.21 with longer Inactivity Timer.

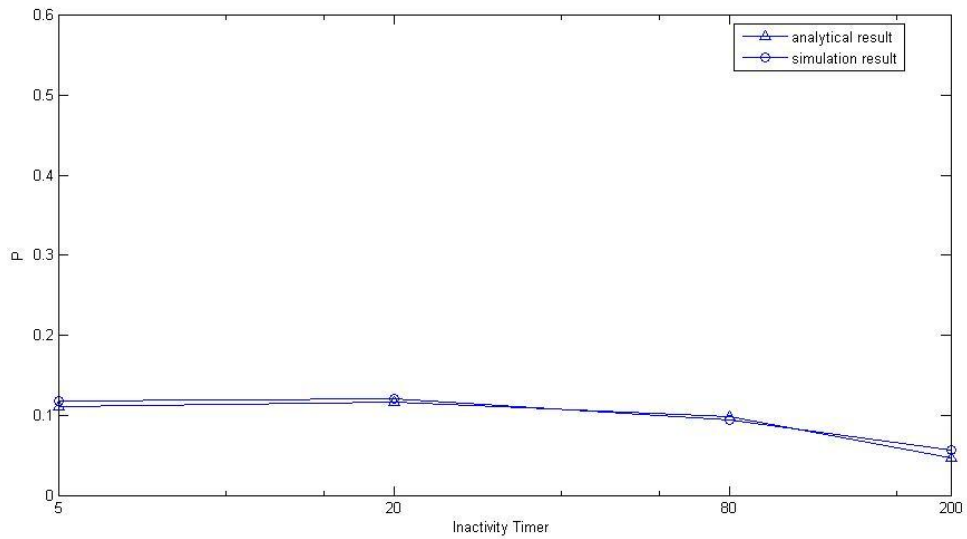


Figure A.1: Performance comparison among analytical results and simulation results for different T_{IN} .

Figure A.1 shows the Performance comparison among analytical results and simulation results for different T_{IN} where $N_{SC}=6$, $T_{SC}=64ms$, $\delta=75ms$, $\lambda=0.005$, $T_{LC}=256ms$. As we can see, the simulation results are similar to the analytical results. Furthermore, the probability of bursts fail to meet the delay requirement will decrease with T_{IN} increase.

Note that when T_{IN} is small, they have similar probability of bursts fail to meet delay requirement. Thus, while using a small T_{IN} , we can neglect the influence of T_{IN} in analytical model.