國 立 交 通 大 學

電信工程研究所

碩 士 論 文

設計低相位雜訊四相位震盪器與高增益降頻混頻器

Design of Low Phase Noise Quadrature VCO and High Gain

Down Conversion Mixer

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中 華 民 國 一 百 零 一 年 七 月

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中 文 摘 要

　　本論文討論分為兩部分，其中所提出電路之晶片製作皆由 TSMC 0.18 μm mixed-signal/RF CMOS 1P6M 製程來實現。

　　第一部分為結合電流再利用電路並利用考畢茲電容耦合產生四相位之震盪器。此四相位震盪器存有這兩種電路的優點，且從模擬中可得到利用電容耦合產生四相位並不會產生額外的相位雜訊之結論。根據量測結果顯示:本 QVCO 震盪頻率為 4.57~5.02 GHz，在供應電壓為 1.8 V 之條件下，功率損耗約為 8.46 mW，相位雜訊為-119 dBc/Hz @1 MHz，而 figure-of-merit (FOM)則為-183.7 dBc/Hz。

　　第二部分則提出低雜訊放大器運用在混頻器的射頻轉導級的高增益混頻器，這種整合型態的混頻器，利用低雜訊放大器的功能，可以同時在一個混頻器中達成高增益與低功率損耗的優點，並且減少面積使用以及避免多個電路整合到單一晶片時所遇到的匹配問題。第三章電路從分析混頻器各個區塊以達到高增益以及低雜訊，量測時，匹配的 S 參數 14~20 GHz 皆在 -10 dB 以下，12~16 GHz 增益頻段中有 18.327 dB 的最高轉換增益，而雜訊指數最小值 13.2 dB，三階截斷點為 - 7.5 dB，而功率損耗為 7.56 mW，FOM 為 191.42；第四章中除了包含第三章設計方法外，在射頻轉導級並接兩個 CCC CG-LNA 和 CS-LNA 以達到寬頻中也具有高增益與低雜訊，量測的 S 參數從 4 GHz 到 20 GHz 皆在 -8 dB 之下。在 2.7~17.8 GHz 增益頻段中只有 22.7 dB 的最高轉換增益，而雜訊指數最小值 10.45 dB，三階截斷點為 -10 dB，而功率損耗為 12.058 mW，FOM 為 192.04。

Design of Low Phase Noise Quadrature VCO and High Gain Down Conversion Mixer

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Abstract

This paper consists of two parts. All the proposed circuits were implemented in TSMC 0.18μm mixed-signal/RF CMOS 1P6M technology.

Part I presents a Colpitts current-reused QVCO based on capacitor coupling. The proposed QVCO exists the advantages of Coltpitts and current-reused circuit. Furthermore, using capacitor coupling to generate quadrature signals doesn't make extra phase noise. According to the measured results, the oscillation frequency is 4.57~5.02 GHz, and the power consumption is about 8.46 mW at the supply voltage of 1.8 V. The phase noise at 1 MHz offset is -119 dBc/Hz and the figure-of-merit (FOM) of the proposed QVCO is about -183.7 dBc/Hz.

Part II proposes a high gain mixer with low noise amplifier (LNA) in the RF trans-conductance stage of mixer. Using the ability of LNA, this integrated mixer can achieve high conversion gain and low power consumption in one circuit. Furthermore, it reduces the area and avoids the problem of matching that many components integrate in SOC. In chapter 3, analyzing each block of mixer achieve high conversion gain and low noise figure. During measurement, the matching s-parameter is below -10 dB in 14~20 GHz. The measured bandwidth of conversion gain ranges from 12 to 16 GHz and the maximum gain is 18.3 dB at

14 GHz. The minimum noise figure is 13.2 dB. The measured linearity shows that IIP3 is -7.5 dB. The power consumption is 7.56 mW and the FOM is 191.42；In chapter 4, including the analytic method of chapter 3, constructing cascade construction by CCC CG-LNA and CS-LNA at the RF trans-conductance stage achieves high conversion gain and low noise figure in wide band. The measured s-parameter is below -8 dB in 4~20 GHz. The measured bandwidth of conversion gain covers from 2.7 to 17.8 GHz and the maximum gain is 22.7 dB at 4 GHz and 16 GHz. The minimum noise figure is 10.45 dB. The measured linearity shows that IIP3 is -10 dB. The power consumption is 12.058 mW and the FOM is 192.04。

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賴星翰

於　新竹交通大學

2012 年　夏

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Chapter 1

Introduction

1.1   Background and Motivation

As increasing demand for wireless communications system, the requirements of low-cost and low power consumption for wireless system have dramatically increased. Also, it is required to reduce the circuit size and cost. Thus, we need an advanced integration to design Integrated Circuit (IC) in small area. In addition to area and cost, it is very significant to decrease the voltage supply and the power consumption. Wireless systems for many standards, including GSM, Bluetooth, WLAN, and Wireless Personal Area Network (WPAN) require low power consumption design techniques to enhance the battery lifetime and to improve their integration. Moreover, the development of advanced CMOS technology with the short-channel length is achieving higher cut-off frequency. Instead of BJT and GaAs (Gallium Arsenide), CMOS is very attractive for RFIC due to the capability of system-on-chip (SOC) implementation. Furthermore, scaling CMOS technology also satisfies the requirement of low-cost and smaller size.

In one kind of communication systems, downlink is a term in telecommunications that is used to refer to a data transmission in which data flows from an orbital satellite receiver to a ground-based transmitter. When a ground-based transmitter transmits data to a satellite in Earth's orbit, shown in Fig. 1 -1, the satellite stores the information until it can decide what to do with it. Downlink is usually used in astronomy, radio science, and telecommunications [1].

Downlink transmits to the C Band (3.7~4.2 GHz), the Ku Band (11.7~12.7 GHz), and the Ka Band between (18.3~20.2 GHz). The downlink applications in C Band radio frequencies are used to transmit data through thick rain clouds and other adverse weather conditions, which can often disrupt data. Ku Band radio frequencies are used to transmit data to small ground-based satellite dishes, such as those found on rooftops, and generally use more energy than C Band frequencies. Likewise, Ka Band radio frequencies are used to transmit data to small satellite dishes, but are specifically used for broadcasting satellite television and Internet [1].
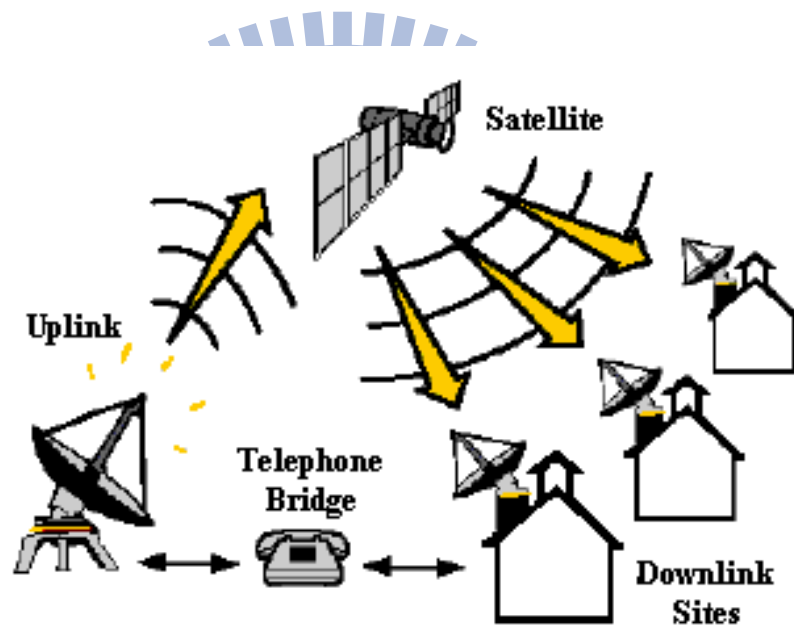
Fig. 1 - 1　The diagram of downlink [1]

The wireless communication standards generally use phase or frequency modulation, which require quadrature local signals mixing to extract the information contained in both sides of the spectra [2]. Phase-locked loop (PLL) is widely utilized to be a source of local oscillation signal, as shown in Fig. 1 - 2.
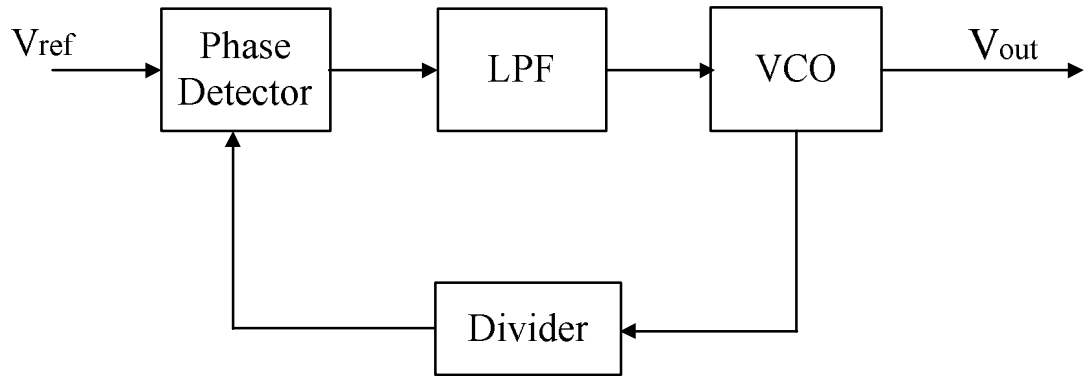
Fig. 1 - 2   Block diagram of phase-locked loop

Voltage-controlled oscillators (VCO) play a oscillatory component in the PLL circuits and the phase noise of the VCO directly affect the performance of the PLL circuits. Due to the requirements of quadrature generation for communication system, a low phase noise VCO with quadra-phase outputs becomes a important topic.

The other topic of direct conversion that is a communication system technology is radio-frequency (RF) front-end circuit. In recent years, the evolution of wireless systems has interested toward the development of multi-band applications or better performance. Within this direction, the RF front-end circuit with CMOS process also is a natural choice to design a new structure. A merged CMOS LNA and mixer for direct conversion system [16] develop to improve the integrated front-end circuit. This idea uses LNA circuit in the RF trans-conductance stage of mixer to achieve the performance of front-end circuit. The main challenge of this structure is to achieve high conversion gain and low noise figure in wide frequency range.

1.2　Phase Noise
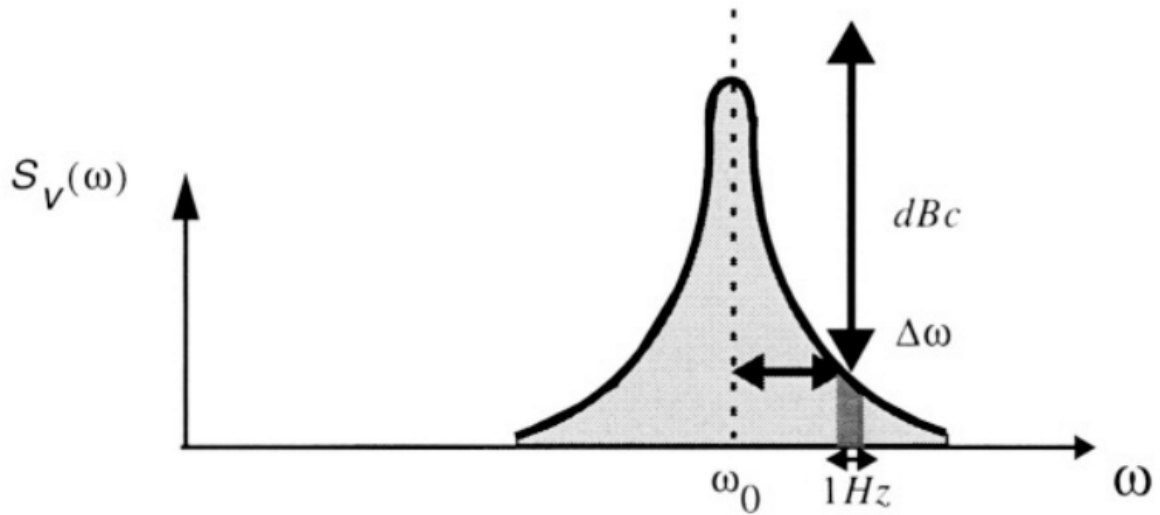
Fig. 1 - 3　The phase noise per unit bandwidth

The output purity of VCOs is quantified as phase noise, i.e., the cyclic uncertainty induced by the noise of the active and passive devices. The phase noise is defined as "the relative noise power per unit bandwidth at certain offset with respect to the carrier power". That is,

$$L_{total}\{\Delta\omega\} = 10 \cdot \log\left[\frac{P_{sideband}(\omega_o + \Delta\omega, 1Hz)}{P_{carrier}}\right] \quad (1.1)$$

where $P_{sideband}(\omega_o + \Delta\omega, 1Hz)$ represents the single sideband power at a frequency offset, $\Delta\omega$, from the carrier in a measurement bandwidth of 1Hz, as shown in Fig. 1 - 3, and $P_{carrier}$ is the total power under the power spectrum.

Phase noise is the most critical parameter in the design of a high performance voltage controlled oscillator (VCO). Any practical oscillator has fluctuations in both the amplitude and the phase. Such fluctuations are caused by both the internal noise generated by passive and

active devices and the external interference coupled from the power supply or substrate. The amplitude noise is usually less important in comparison with the phase noise for oscillators, since it is suppressed by the intrinsic nonlinear nature of oscillators. Therefore, wireless communication systems usually impose strict specifications on the phase noise performance. If one plots $L_{total}\{\Delta\omega\}$ for a free-running oscillator as a function of $\Delta\omega$ on logarithmic scales, regions with different slopes may be observed as shown in Fig. 1 - 4, [33]. At large offset frequencies, there is a flat noise floor. At small offsets, one may identify regions with a slope of $1/f^2$ and $1/f^3$, where the corner between $1/f^2$ and $1/f^3$ regions is called ω_{1/f^3}. Finally the spectrum becomes flat again at very small offset frequencies.
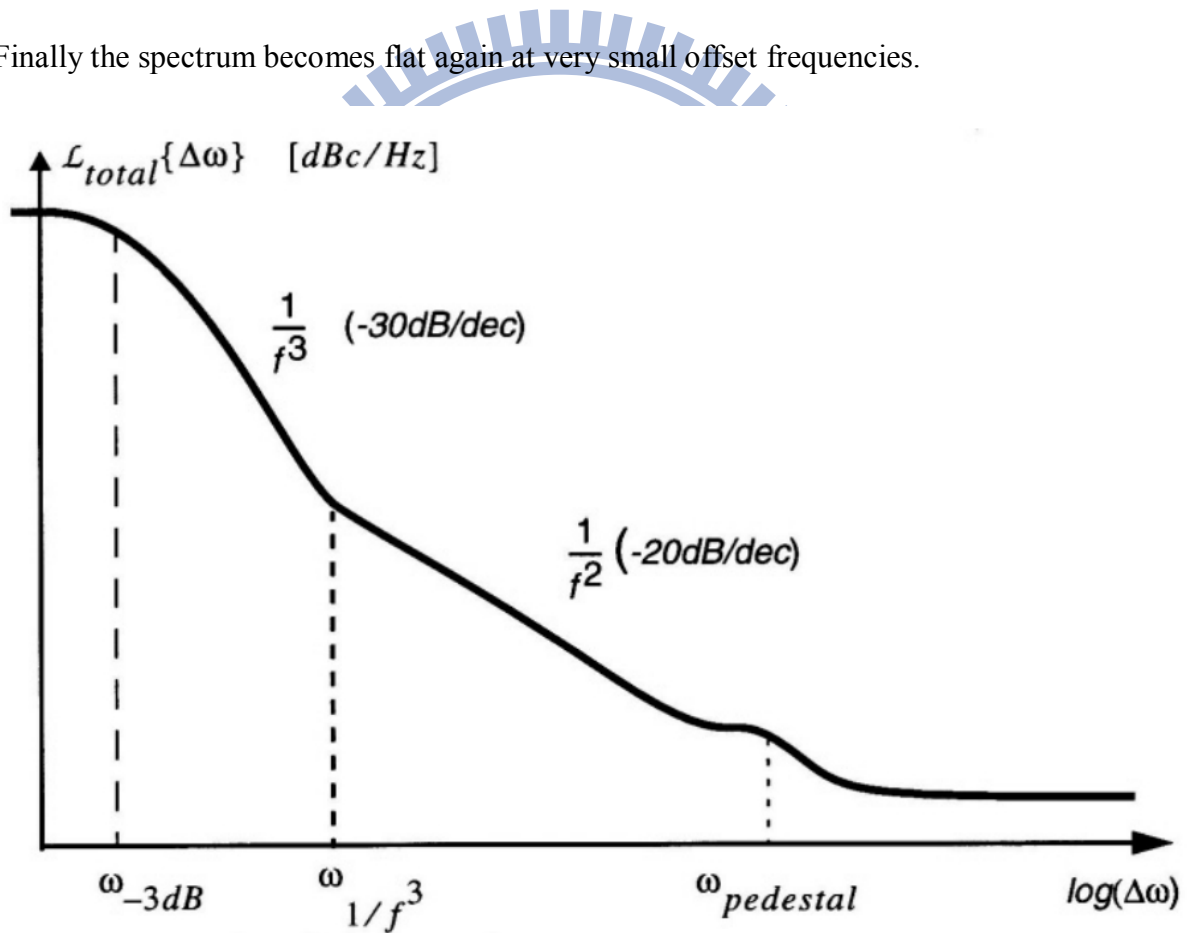
Fig. 1 - 4   A typical phase noise plot for a free running oscillator, [33]
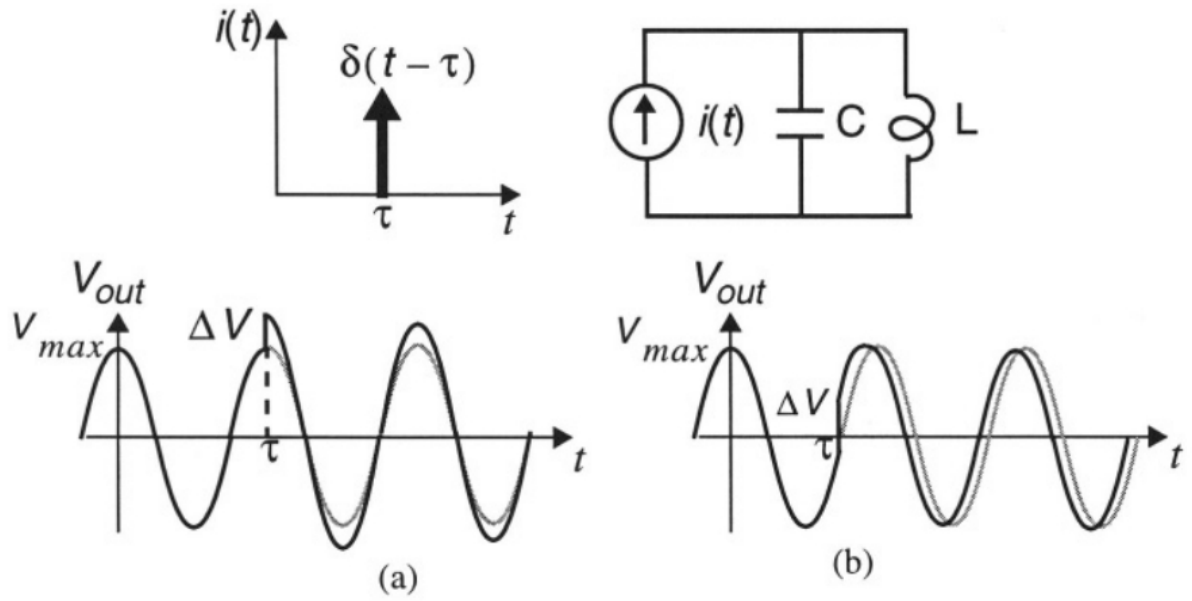
Fig. 1 - 5 Impulse response of an ideal LC oscillator, [33]

The phase-noise model proposed by Hajimiri and Lee in [33] is based on the impulse sensitivity function (ISF), which is a measure of the sensitivity of the oscillator to an impulsive input. It is a dimensionless periodic function in 2π that is independent of the output frequency and amplitude, describing phase shift result from applying a unit impulse at any point in time. Fig. 1 - 5 illustrates this sensitivity for an LC resonator with the impulse applied at the zero crossing and the peak of its output waveform [33]. If one injects an impulse of current at the voltage maximum, only the voltage across the capacitor changes; there is no effect on the current through the inductor. Therefore, the tank voltage changes instantaneously, as shown in Fig. 1 - 5 (a). On the other hand, if this impulse is applied at the zero crossing, it has the maximum effect on the excess phase, $\phi(t)$, and the minimum effect on the amplitude, as depicted in Fig. 1 - 5 (b).

For a small injected charge Δq, the resulting phase shift $_\Delta\phi$ is proportional to the voltage change, ΔV, and hence to the injected charge, Δq. Therefore $_\Delta\phi$ can be written as

$$_\Delta\phi = \Gamma(\omega_O\tau)\cdot\frac{\Delta V}{V_{max}} = \Gamma(\omega_O\tau)\cdot\frac{\Delta q}{q_{max}} \qquad \Delta q \ll q_{max} \qquad (1.\,2)$$

where V_{max} is the voltage swing across the capacitor and q_{max} is the maximum charge swing. The function, $\Gamma(\omega_O\tau)$, is the so-called impulse sensitivity function (ISF). As long as the injected charge is small, the equivalent systems for amplitude and phase can be fully characterized using their linear time-variant unit impulse response, $h_\phi(t,\tau)$ and $h_A(t,\tau)$. Note that the introduced phase shift persists indefinitely, the unity phase impulse response can be easily calculated from above equation to be

$$h_\phi(t,\tau) = \frac{\Gamma(\omega_O\tau)}{q_{max}} \cdot u(t-\tau) \tag{1.3}$$

Therefore, the output excess phase can be calculated using the superposition integral as

$$\phi(t) = \int_{-\infty}^{\infty} h_\phi(t,\tau) \cdot i(\tau)\,d\tau = \int_{-\infty}^{\infty} \frac{\Gamma(\omega_O\tau)}{q_{max}} \cdot i(\tau)\,d\tau \tag{1.4}$$

where $i(\tau)$ represents the input noise current injected into the node of interest. Since the ISF is periodic, it can be expanded in a Fourier series as

$$\Gamma(\omega_O\tau) = c_O + \sum_{n=1}^{\infty} c_n \cos(n\omega_O\tau + \theta_n) \tag{1.5}$$

where the coefficients c_n are real-valued, and θ_n is the phase of the nth harmonic. Using equation (1.5) for $\Gamma(\omega_O\tau)$ in the superposition integral and exchanging the order of summation and integration, the following is obtained

$$\phi(t) = \frac{1}{q_{max}} \left[c_O \int_{-\infty}^{t} i(\tau)\,d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i(\tau)\cos(n\omega_O\tau)\,d\tau \right] \tag{1.6}$$

Equation (1.6) identifies individual contribution to the total $\phi(t)$ for an arbitrary input

current i(t) injected into any circuit node, in terms of various Fourier coefficients of the ISF. The decomposition implicit in equation (1.6) can be better understood with the equivalent block diagram shown in Fig. 1 - 6, [33].
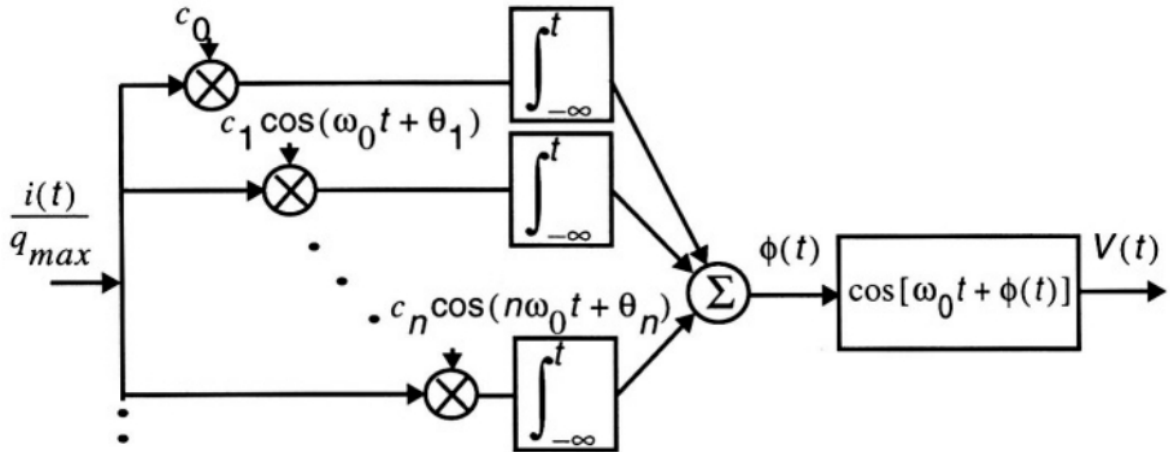
Fig. 1 - 6   The equivalent system for ISF decomposition, [33]

To investigate the effect of low frequency perturbations on the oscillator phase, a low frequency sinusoidal perturbation current, $i(t) = I_0 \cos(\Delta\omega t)$, is injected into the oscillator at a frequency of $\Delta\omega \ll \omega_O$. The arguments of all the integrals associated with c_n, n=1,...∞ in equation (1.6) are at frequency higher than $\Delta\omega$ and are significantly attenuated by the averaging nature of the integration, except the term arising from the first integral (the first branch in the equivalent block diagram of Fig. 1 - 6), which involves c_0. Therefore, the resulting excess phase can be approximated as

$$\phi(t) = \frac{I_0 \sin(\Delta\omega t)}{q_{\max} \cdot \Delta\omega} + \sum_{n=1}^{\infty} \frac{I_0 c_n}{2 \cdot q_{\max}} \left[\frac{\sin((n\omega_O + \Delta\omega) \cdot t)}{n\omega_O + \Delta\omega} + \frac{\sin((n\omega_O - \Delta\omega) \cdot t)}{n\omega_O - \Delta\omega} \right]$$

$$\phi(t) \cong \frac{I_0 c_0 \sin(\Delta\omega t)}{q_{\max} \cdot \Delta\omega} \tag{1.7}$$

As a result, there will be two impulses at $\pm\Delta\omega$ in the power spectral density of $\phi(t)$, denoted as $S_\phi(\omega)$ as shown in Fig. 1 - 7, [33].
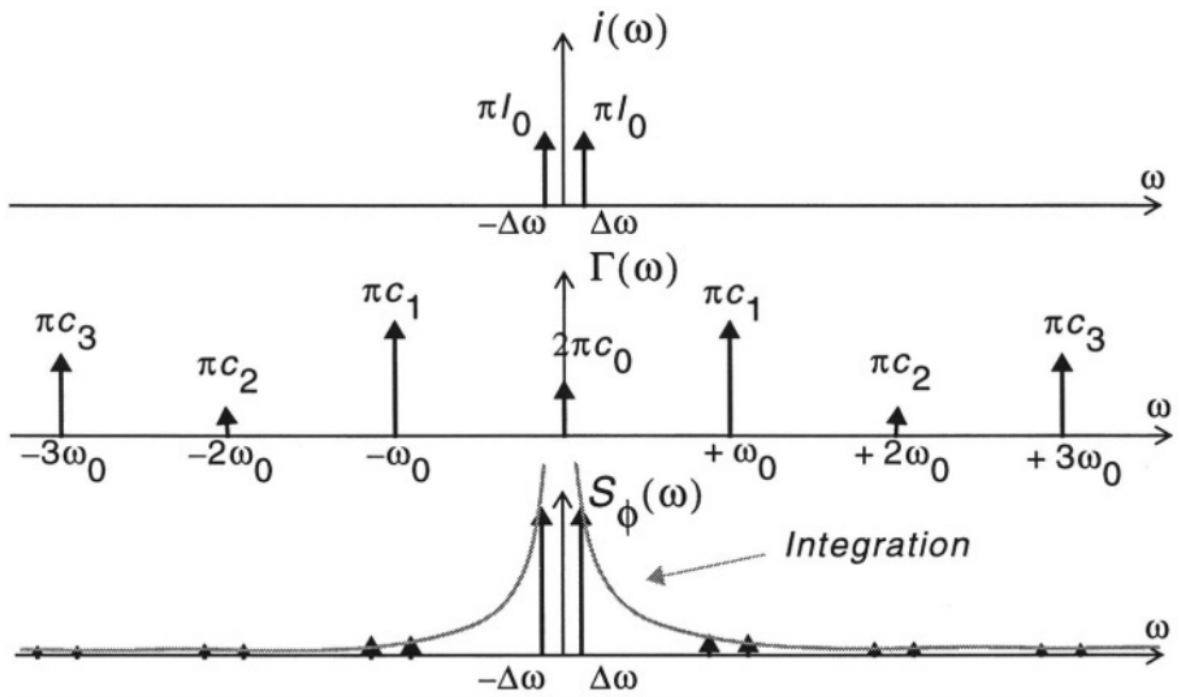
Fig. 1 - 7   Conversion of a low frequency sinusoidal current to phase, [33]
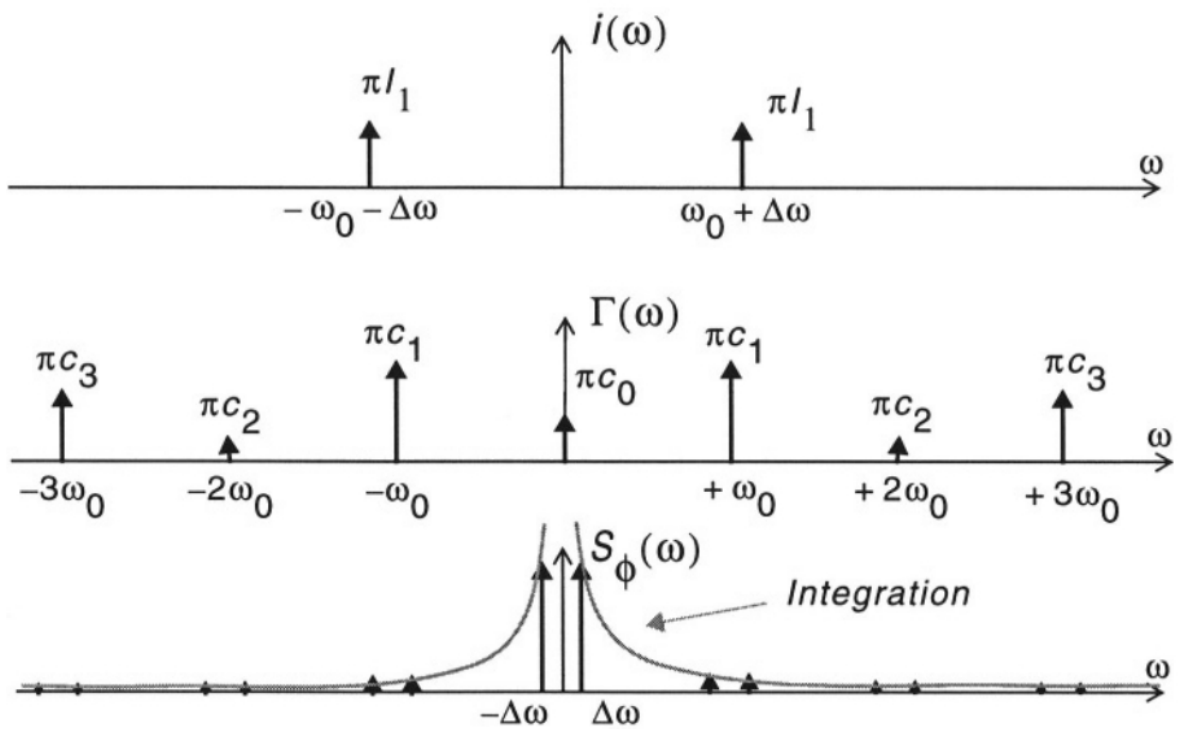
Fig. 1 - 8   Conversion of a tone in the vicinity of ω_o, [33]

As another important special case, consider a current at a frequency close to the

oscillation frequency given by $i(t) = I_0 \cos\left[(\omega_O + \Delta\omega)t\right]$. A process similar to that of the previous case occurs except that the spectrum of i(t) consists of two impulses at $\pm(\omega_O + \Delta\omega)$, as shown in Fig. 1 - 8, [33]. This time the dominate term will be the second integral corresponding to n=1. Therefore, $\phi(t)$ is given by

$$\phi(t) \cong \frac{I_1 c_1 \sin(\Delta\omega t)}{q_{max} \cdot \Delta\omega} \tag{1. 8}$$

which again results in two equal sidebands at $\pm\Delta\omega$ in $S_\phi(\omega)$.

The amount of phase error due to a given sinusoidal current can thus be calculated using equation (1.7) and equation (1.8). Computing the power spectral density (PSD) of the oscillator output voltage, $S_v(\omega)$, requires knowledge of how the output voltage relates to the excess phase variations. The phase-to-voltage conversion process for a single tone is now considered. For small value of $\phi(t)$, $\cos\left[\omega_O t + \phi(t)\right]$ can be approximate as

$$\cos\left[\omega_O t + \phi(t)\right] = \cos(\omega_O t)\cos[\phi(t)] - \sin(\omega_O t)\sin[\phi(t)]$$

$$\cos\left[\omega_O t + \phi(t)\right] \cong \cos(\omega_O t) - \phi(t)\sin(\omega_O t) \tag{1.9}$$

$$\cos\left[\omega_O t + \phi(t)\right] \cong \cos(\omega_O t) + \frac{I_n c_n}{4 \cdot q_{max} \Delta\omega}\left[\cos((\omega_O + \Delta\omega)t) - \cos((\omega_O - \Delta\omega)t)\right] \tag{1.10}$$

where it is assumed that $\cos[\phi(t)] \cong 1$ and $\sin[\phi(t)] \cong \phi(t)$ for small values of $\phi(t)$. The excess phase is then converted to a pair of equal sidebands at $\omega_O + \Delta\omega$. The sideband power relative to the carrier can be calculated as

$$L(\Delta\omega) = 10\log\left[\frac{I_0^2 c_0^2 + 2\sum_{n=1}^{\infty} I_n^2 c_n^2}{8 q_{max}^2 \Delta\omega^2}\right] \tag{1.11}$$

Consider a random noise current source $i_n(t)$, whose power spectral density has both a flat region and a $1/f$ region, as shown in Fig. 1 - 9, [33]. Equation (1.6) shows that noise components located near integer multiples of the oscillation frequency are weighted by Fourier coefficients of the ISF and integrated to form the low noise frequency noise sidebands for $S_\phi(\omega)$. These sidebands in turn become close-in phase noise in the spectrum of $S_v(\omega)$ through phase modulation (PM), as shown in Fig. 1 - 9. The definition of the ISF can be expanded to take into account the presence of cyclostationary noise sources such as the channel noise of a MOS transistor. Its statistical properties vary with time in a periodic manner because the noise power is modulated by the gate-source overdrive voltage.
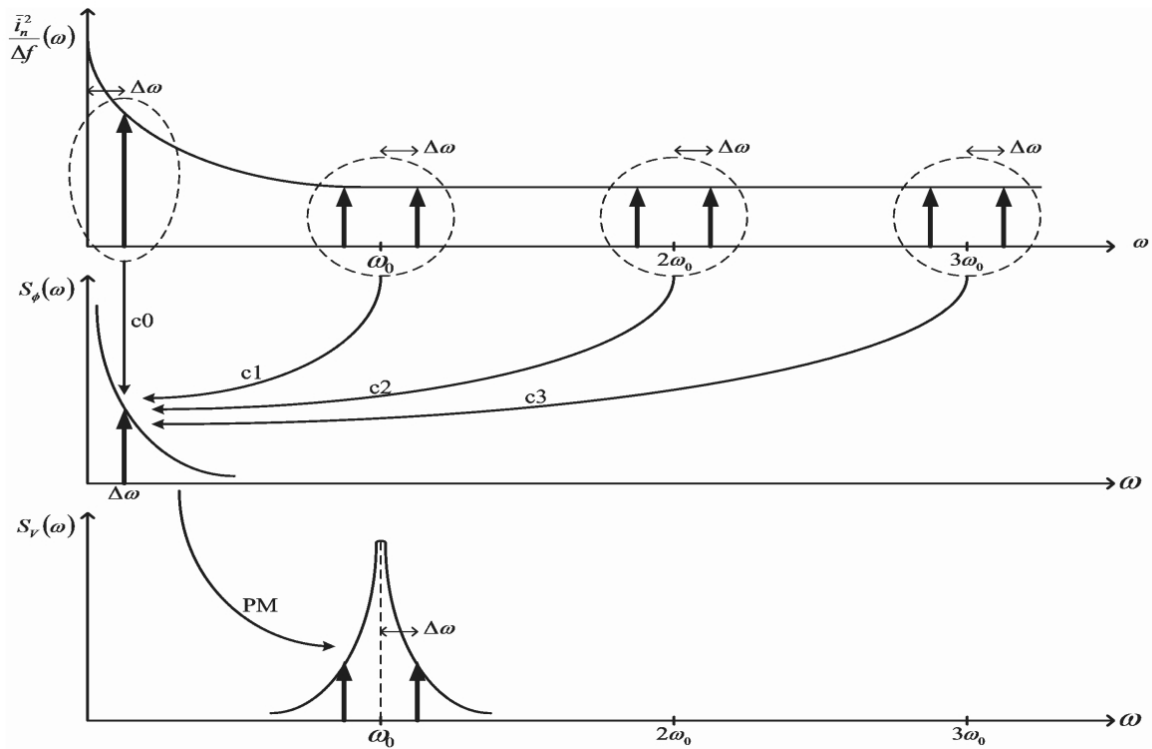
Fig. 1 - 9   Conversion of circuit noise to excess phase, and then to phase-noise sideband

Now consider with a white input noise current with power spectral density $i_n^2 / \Delta f$. Note that I_n in equation (1.11) represents the peak and not the rms amplitude, hence, $I_n^2 / 2 = \overline{i_n^2} / \Delta f$ for $\Delta f = 1 \mathrm{Hz}$. Noise power around the frequency $n\omega_O + \Delta\omega$ causes two

equal sidebands at $\omega_O \pm \Delta\omega$, as shown in Fig. 1 - 8. However, it is important to recognize that noise power at $n\omega_O - \Delta\omega$ also has a similar effect. Therefore, twice the power of noise at $n\omega_O + \Delta\omega$ should be taken into account, and hence equation (1.11) becomes

$$L(\Delta\omega) = 10\log\left[\frac{\left(c_0^2 + 2\sum_{n=1}^{\infty} c_n^2\right) \cdot \frac{\overline{i_n^2}}{\Delta f}}{8q_{max}^2 \Delta\omega^2}\right] \tag{1.12}$$

According to Parseval's relation,

$$2\Gamma_{rms}^2 = \frac{1}{\pi}\int_0^{2\pi} |\Gamma(x)|^2 dx = \frac{c_0^2}{2} + \sum_{n=1}^{\infty} c_n^2 \tag{1.13}$$

where Γ_{rms} is the rms value of $\Gamma(x)$. As a result equation (1.12) becomes

$$L(\Delta\omega) = 10\log\left[\frac{\Gamma_{rms}^2 \cdot \frac{\overline{i_n^2}}{\Delta f}}{2q_{max}^2 \Delta\omega^2}\right] \tag{1.14}$$

This equation gives the phase noise spectrum of an arbitrary oscillator in the $1/f^2$ region of the phase noise spectrum.

Many active and passive devices exhibits low frequency noise with a power spectrum that is approximately inversely proportional to the frequency. It is for this reason that noise source with this behavior are referred to as $1/f$ noise. Noting that device noise in the $1/f$ region can be described by

$$\overline{i_{n,1/f}^2} = \overline{i_n^2} \cdot \frac{\omega_{1/f}}{\Delta\omega} \qquad \Delta\omega < \omega_{1/f} \tag{1.15}$$

where $\omega_{1/f}$ is the corner frequency of device $1/f$ noise. Hence, the sideband power relative to the carrier in the $1/f^3$ portion of the phase noise spectrum can be expressed as

$$L(\Delta\omega) = 10\log\left[\frac{c_0^2 \cdot \dfrac{\overline{i_n^2}}{\Delta f} \cdot \dfrac{\omega_{1/f}}{\Delta\omega}}{8q_{max}^2\Delta\omega^2}\right] \qquad (1.\,16)$$

The phase noise $1/f^3$ corner, $\Delta\omega_{1/f^3}$, is the frequency where the sideband power due to the white noise given by equation (1.14) is equal to the sideband power arising from the $1/f$ noise given by equation (1.16), as shown in Fig. 1 - 10.
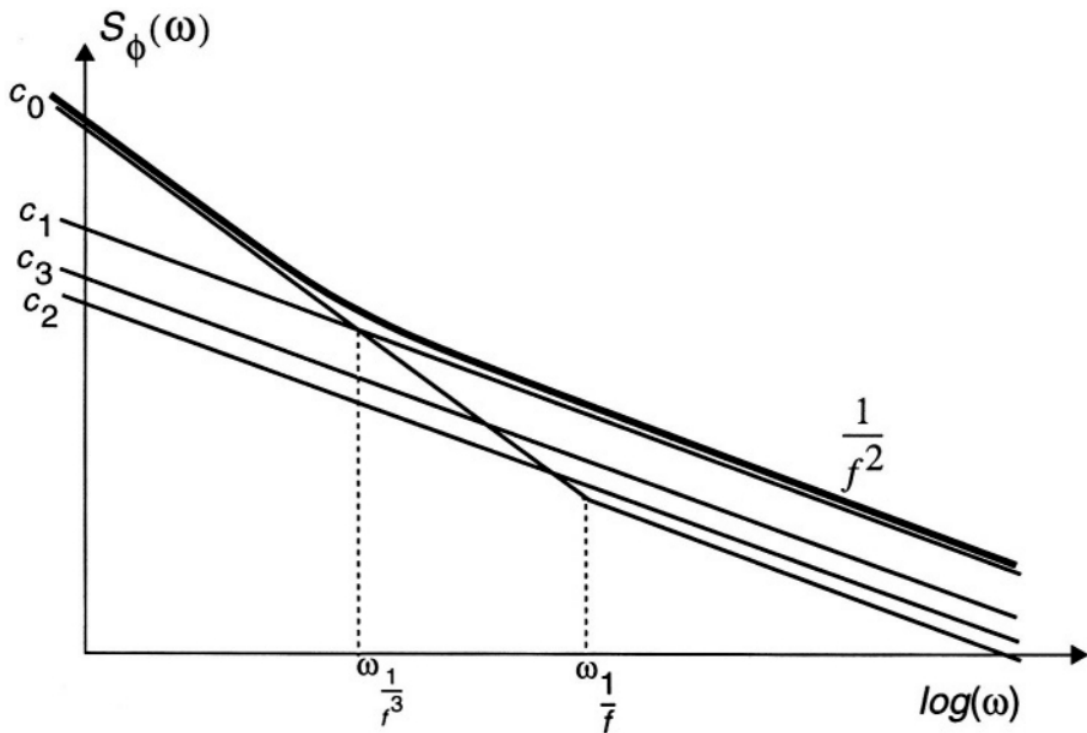
Fig. 1 - 10 $S_\phi(\omega)$ on a log-log axis, [33]

Solving for $\Delta\omega_{1/f^3}$ resulting in the following expression for the $1/f^3$ corner in the phase noise spectrum:

$$\Delta\omega_{1/f^3} = \omega_{1/f} \cdot \left(\frac{c_0}{\Gamma_{rms}}\right)^2 \tag{1.17}$$

As can be seen, the $1/f^3$ phase noise corner is not equal to the $1/f$ device noise corner but smaller by a factor equal to $\left(\dfrac{c_0}{\Gamma_{rms}}\right)^2$, where c_0 is the dc value of ISF,

$$c_0 = \frac{1}{2\pi}\int_0^{2\pi}\Gamma(x)dx \tag{1.18}$$

Therefore, if the circuit can be designed such that the ISF corresponding to each transistor noise source has no DC component, the flicker noise will not have any effect on the phase noise of the VCO.

A white cyclostationary noise current $i_n(t)$ can always be decomposed as

$$i_n(t) = i_{n0}(t)\cdot\alpha(\omega_O t) \tag{1.19}$$

where $i_{n0}(t)$ is a white stationary process and $\alpha(\omega_O t)$ is a deterministic periodic function describing the noise amplitude modulation and therefore is referred to as the noise modulating function (NMF). The NMF is normalized to a maximal value of one and can be easily derived from the device noise characteristics and noiseless steady-state waveform. Therefore, the expression for the excess phase resulting from a cyclostationary noise source can be written as

$$\phi(t) = \int_{-\infty}^{t} i_{n0}(\tau)\frac{\alpha(\omega_O t)\cdot\Gamma(\omega_O \tau)}{q_{max}}d\tau \tag{1.20}$$

As can be seen, cyclostationary noise can be treated as a stationary noise applied to a system with a new ISF given by $\Gamma_{NMF}(x) = \Gamma(x)\cdot\alpha(x)$ where $\alpha(\omega_O t)$ can be derived easily from device noise characteristics and the noiseless steady-state waveform.

In summary, the linear time-variant phase-noise model proposed by Hajimiri and Lee can

accurately predict phase noise of most practical oscillators by taking into account the cyclostationary properties of the random noise sources. The introduced ISF accurately describes the contribution to phase perturbation by each individual noise   source, allowing efficient optimization of phase noise performance.

1.3   Thesis Organization

In this thesis, a Colpitts current-reused quadrature VCO on capacitor coupling and a high gain down conversion mixer are implemented in TSMC 0.18 μm mixed-signal/RF CMOS 1P6M technology.

Chapter 1 discusses the background of low phase noise CMOS QVCO and high gain mixer , and gives a brief introduction to phase noise.

Chapter 2 presents a quadrature VCO on capacitor coupling which combine current-reused oscillator with Colpitts structure. This method is able to exist low phase noise and generate quadrature signals. Compared with conventional P-QVCO, it doesn't trade off phase noise and phase error. Furthermore, using capacitor coupling to generate quadrature signals doesn't make extra phase noise.

Chapter 3 will propose a high gain down conversion mixer. The proposed mixer with current bleeding circuit constructs common mode feedback (CMFB) circuit in active load and CS-LNA in RF trans-conductance stage. Besides, the inductor connecting with switch pairs can reduce indirect noise. By these methods, the propose mixer can achieve high conversion gain at low noise figure easily.

Chapter 4 presents a broadband high gain down conversion mixer with cascade structure. The cascade structure in RF trans-conductance stage combines CS-LNA with capacitor cross-coupled CG-LNA (CCC CG-LNA). Compared with the traditional CG-LNA in cascade structure, the CCC CG-LNA not only matches input impedance widely but also improves the performance of noise figure and the effective trans-conductance that is almost twice as large as general CG-LNA. Hence, the proposed mixer can achieve high conversion gain and low noise figure in broadband.

Chapter 5 gives the conclusions, summary of contributions, and future work plan.

Chapter 2

A Colpitts Current-Reused QVCO Based on Capacitor Coupling

2.1 Introduction

Modern RF receivers and transmitters require oscillators with accurate phase and low phase noise. Since most of the current wireless communication systems are employing quadrature modulation, there have been various research to obtain accurate quadrature local oscillator (LO) signals with low phase noise. For quadrature signals, in-phase and quadrature-phase (I/Q) match is an important requirement while meeting the requirements of low-phase noise and low power consumption for integrated VCOs. Coupling two differential VCOs to generate quadrature signals is called quadrature coupling technology, as shown in Fig. 2 - 1, and is widely used because of its better phase noise. So, we use the quadrature coupling method to generate the quadrature signals in this chapter.
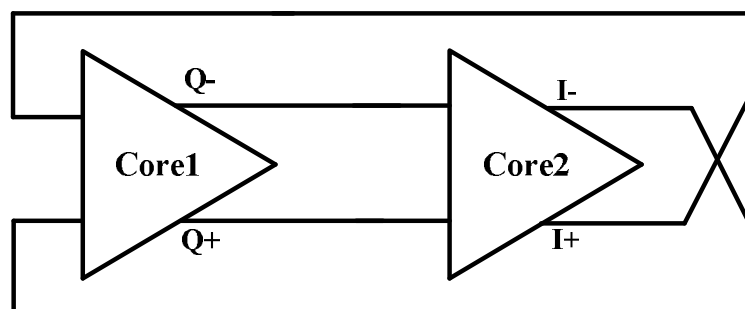
Fig. 2 - 1   Examples of quadrature signal generation methods - quadrature coupling
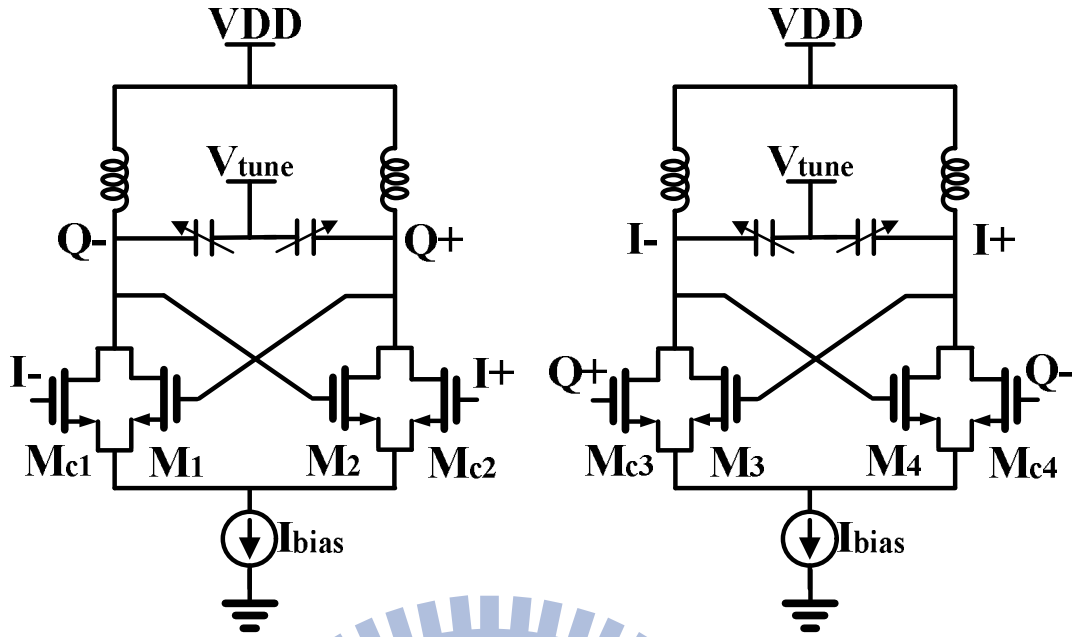
Fig. 2 - 2   Schematic of the parallel-coupled QVCO (P-QVCO) topology

In communication systems, the quadrature VCO plays a major block in generating local oscillation (LO), a wide-used structure is the parallel-QVCO (P-QVCO) [4]. Fig. 2 - 2 shows the conventional parallel QVCO (P-QVCO) where I and Q signals are generated by coupling two differential VCOs through coupling transistors M_{c1} - M_{c4} in parallel with switching transistors M_1 - M_4. The coupling factor S is defined as the ratio of channel width of parallel coupling transistor W_c to the channel width of cross coupled transistor W, i.e, S = Wc /W [5]. The coupling factor value makes P-QVCO difficult to optimize the performance parameters like phase noise and phase accuracy. It means the P-QVCO suffers from a trade-off between phase noise and phase accuracy. The phase noise degradation is induced by the increase in transconductance of the coupling transistors. In addition, the increase in S leads to a higher amount of power dissipation.

In order to achieve low power consumption, current-reused VCO (CR-VCO) configuration is one of the most widely used solutions. Fig. 2 - 3 shows the schematic of the conventional NMOS-based current-reused VCO (CR-VCO) by stacking switching transistors in series like a cascode [6].
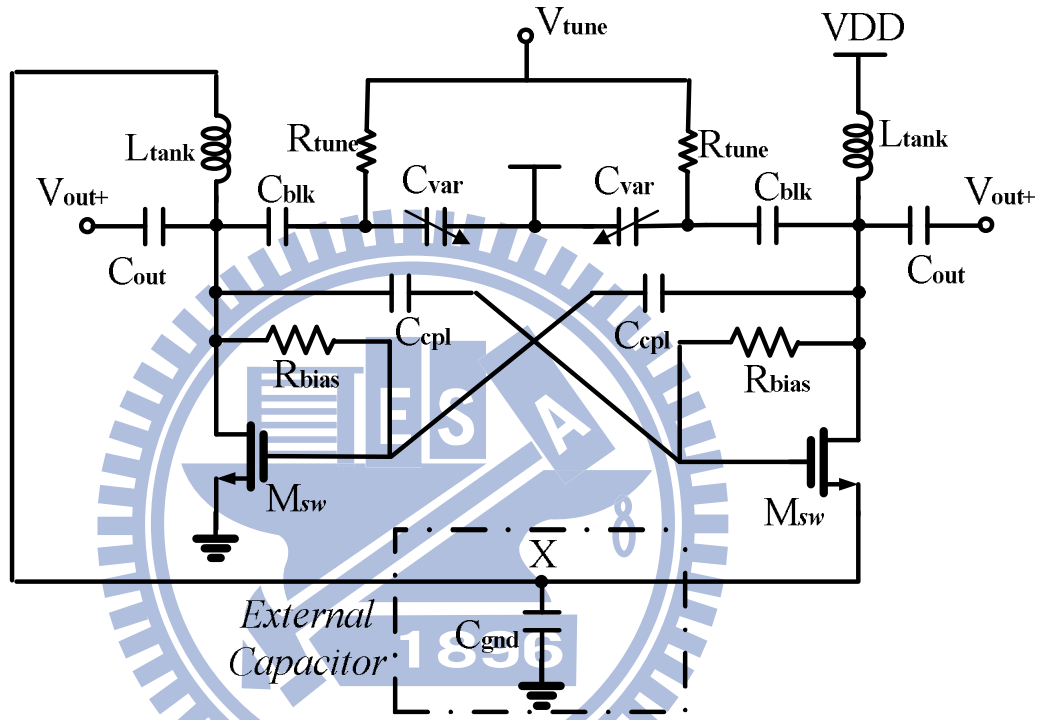
Fig. 2 - 3   Schematic of the conventional current-reused topology

Unfortunately, there are three drawbacks of this type CR-VCO. First, compared with the general VCO, the frequency tuning range of this type CR-VCO is narrower. Because the DC levels at the two sides of the varactors are different, the capacitors C_{blk} must be added for dc block and ac short to have the identical voltage drop across the varactors. Besides, the capacitors C_{cpl} and resistors R_{bias} should be added to bias the transistors properly. Therefore, the capacitance tuning range C_{max} / C_{min} will be smaller due to the addition of extra capacitors. Involving too large number of capacitors and higher capacitive load at the output node also restrict the oscillation frequency. Second, a large capacitor C_{gnd}, even an external one, should be

attached at the node X. Because the node X is pulled up when each one of the differential NMOS turns on, the frequency at the node X is twice as the frequency at the VCO output. A large capacitor C_{gnd} should be used to have a tight ground effect, symmetric differential output swing and suppress the high frequency noise at node X. Third, the amplitude imbalance of the output signals is relatively larger than the conventional cross-coupled VCO due to the unsymmetric circuit structure.
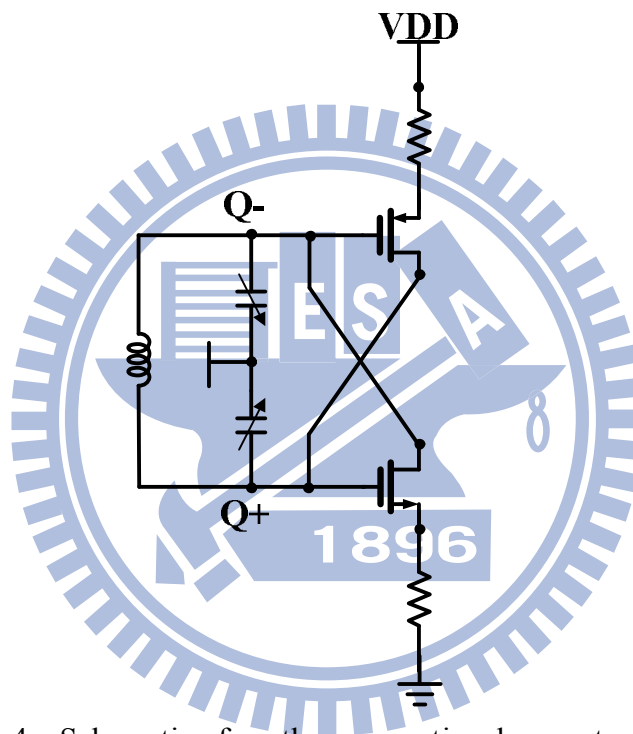
Fig. 2 - 4　Schematic of another conventional current-reused topology

Another type of CR-QVCO has been reported in [7], as shown in Fig. 2 - 4. This structure exists three advantages, low phase noise、half power consumption of standard LC-VCO and easily start-up oscillation. This technology replaces one NMOS in conventional cross-coupled pair by PMOS. Using PMOS transistors in the cross-coupled pair can additionally reduce the phase noise due to lower flicker noise and hot carrier effects. And the series stacking of NMOS and PMOS allows the current to be reduced about half of standard VCO. Also, it is easy to start-up oscillation. The biasing of this complementary current-reused VCO (CR-VCO)

topology is much easier than the NMOS-based cascode current-reused VCO (CR-VCO) topology. That is, the DC levels at the two sides of the varactors are the same and no extra capacitors are needed. Therefore, the problem of involving large number of capacitors and higher capacitive load at the output node can be solved.

Although the CR-QVCO using the configuration shown in Fig. 2 - 4 has excellent low power consumption, there is a drawback that the amplitude imbalance of the output signals is relatively larger than the conventional cross-coupled VCO due to the asymmetric circuit structure. To solve this problem, a passive degenerative resistor is added at the source node of the NMOS transistor to balance the different trans-conductance between PMOS and NMOS transistor.
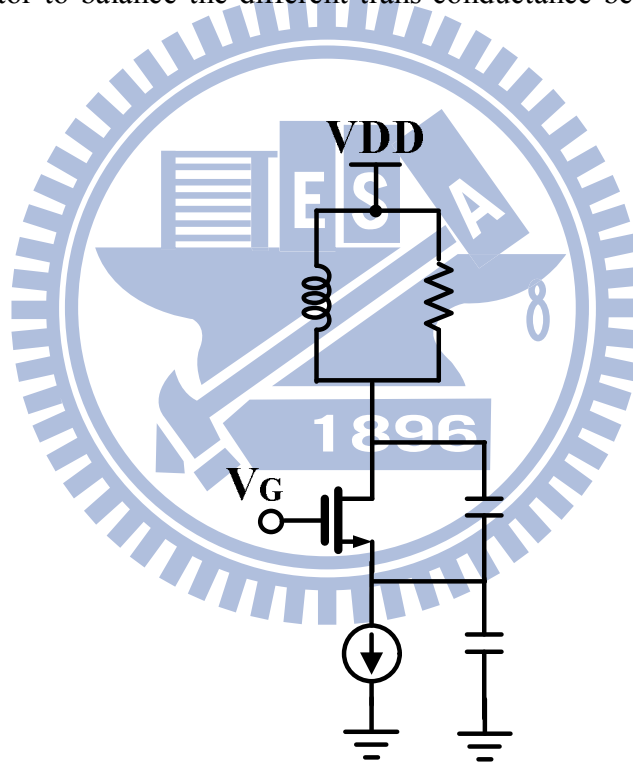
Fig. 2 – 5 Schematic of Colpitts VCO topology

Fig. 2 - 5 is shown Schematic of Colpitts VCO topology. According to Colpitts technology, it shows a better phase noise performance due to large output voltage swing and better cyclostationary noise property [5]. However, the drawback of Colpitts is hard to oscillate because the transistor of Colpitts must need high gain to start up oscillator.

2.2　Circuit Design Consideration

The circuit was simulated and optimized using Agilent ADS. The design procedure can be divided in two steps. First, it analyses the parameters of inductor and chooses the optimal inductor. Finally, a large signal analysis was performed with the harmonic balance to simulate the performance of proposed circuit and output power of the fundamental signal as well as the harmonic signals. In the $1/f^2$ region, the phase noise is given as [8] :

$$L\{f_{off}\} = \frac{1}{8\pi^2 f^2_{off} q^2_{max}} \sum_n \left(\frac{\overline{i^2_n}}{\Delta f} \cdot \Gamma^2_{rms,n} \right)$$

$$(2.1)$$

where f_{off} is the offset frequency from the carrier and $q_{max} = CV_{tank} = V_{tank}/(L_{tank}\omega^2_{osc})$ is the total charge swing of the tank. The impulse sensitivity function (ISF), Γ, represents the time-varying sensitivity of the oscillator's phase to perturbations. Equation (2.1) can be easily interpreted by $V_{tank} = I_{bias}/G_{tank} \approx I_{bias}/G_L$, G_L is the conductance of inductor. Setting to oscillation frequency f_{osc} and DC current I_{bias}, equation(2.1) will be used define a design strategy [8] :

$$L\{f_{off}\} \propto (L_{tank} \cdot G_L)^2$$

$$(2.2)$$

Fig. 2 - 6 to Fig. 2 - 7 show the performance of the inductor that be implemented in TSMC 0.18 μm mixed-signal/RF CMOS 1P6M process. Using the data of Fig. 2 - 6, it can be seen the factor $(L_{tank} \cdot G_L)^2$ in equation (2.2) increasing with an enhancing inductance. However, it needs more DC power to compensate the loss of tank if we choose minimum inductance to achieve better phase noise, as shown Fig. 2 - 7. So, it is important to choose optimal inductor from Fig. 2 - 6 to Fig. 2 - 7.
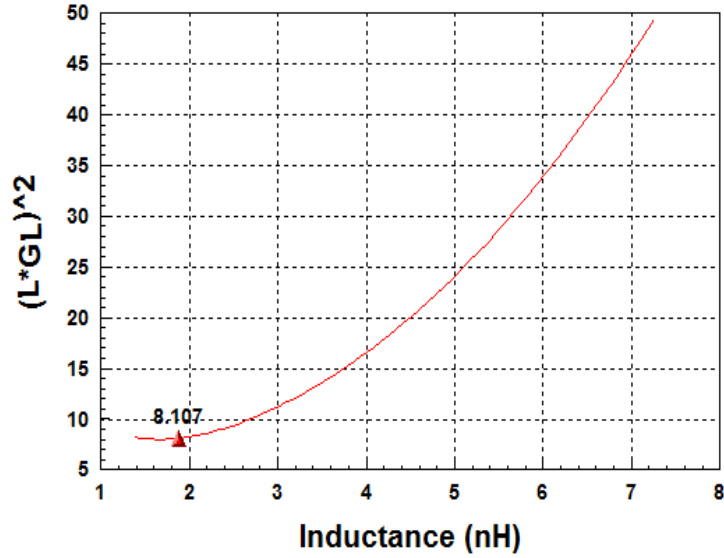
Fig. 2 − 6   The equation (2.2) of inductor
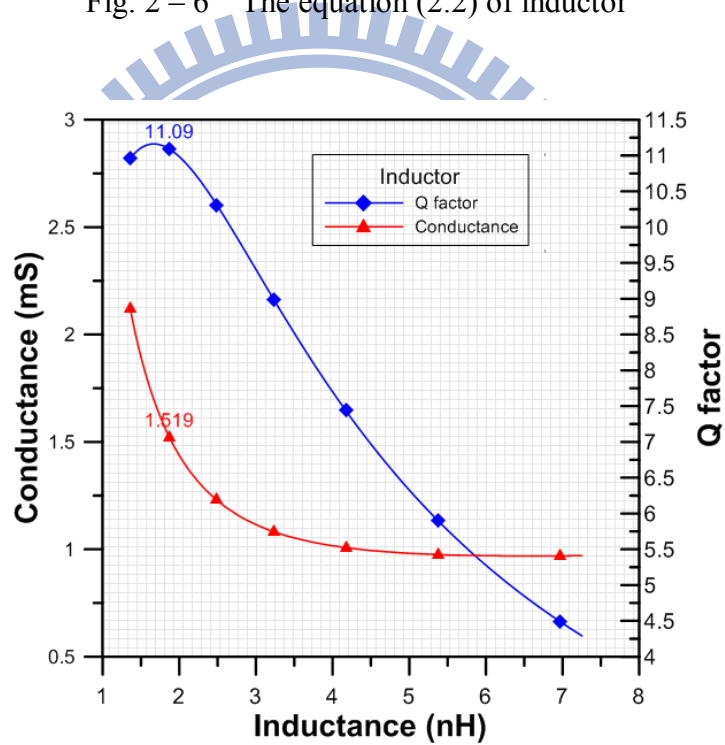
Fig. 2 − 7   The inductance and conductance of inductor

Fig. 2 - 2 shows a schematic of the P-QVCO which is proposed by [4]. In general, the QVCO consists of the two VCO cores and these two VCOs cores are connected through active device. This structure uses coupling transistors $Mc_1 \sim Mc_4$ which are parallel with cross-coupled transistors $M_1 \sim M_4$ to generate quadrature signals. However, compared with a standard VCO [4] (the P-QVCO with no coupling transistor), the P-QVCO not only consumes

more than twice power of the standard VCO but also exhibit poor phase noise due to the additional components $Mc_1 \sim Mc_4$.
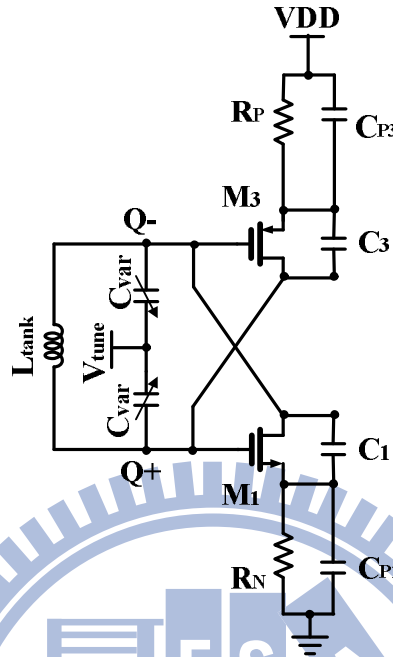
Fig. 2 - 8   Schematic of proposed half circuit

In order to achieve better performance of the QVCO, we should make the VCO cores that have low phase noise at setting power consumption, Fig. 2 - 8 shows a schematic of proposed half circuit, in which M_1 and M_3 are cross-coupled pair and C_1, C_3 , C_{p1} and C_{p3} are Colpitts capacitors. In Fig. 2 - 8, the cross-coupled pair of M_1 and M_3 is a structure that reuses the dc current so that only consumes the half power of a standard VCO. Besides, this proposed VCO exhibits a better phase noise than standard VCO because PMOS (M_3) in complementary cross-coupled pair owns lower flicker noise and hot carrier effects [7]. However, the amplitudes of oscillation signals are asymmetric due to the trans-conductance of PMOS and NMOS are mismatch. In order to solve this problem, the source degeneration resistances R_N, R_P used to balance voltage swings. Beside, these resistances control the DC current and lead current-reused VCOs into current-limited region [7]. The proposed VCO is used to design QVCO in this chapter. This structure can get the advantages of current-reused VCO. Besides, combining Colpitts technology with current-reused structure also makes better phase noise.

Fig. 2 - 9   Schematic of a Colpitts current-reused QVCO based on capacitor coupling

Fig. 2 - 9 shows a schematic of the proposed QVCO, in which through Colpitts coupling capacitors C_{p1}~C_{p4}, the two VCO core are connected with each other for generating quadrature signals. Using passive Colpitts capacitors C_{p1}~C_{p4} to couple two VCO cores as a QVCO instead of using conventional active devices has three advantages as below:

(1) This capacitor coupling method can reduce the power consumption.

(2) It can improve phase noise performance.

(3) It doesn't consider the trade-off of phase noise and phase accuracy.

The first is that the additional power consumed by active device such as Mc_1~Mc_4 in P-QVCO can be removed. So, it can reduce the power consumption of proposed QVCO by capacitor coupling method. The second is to avoid phase noise degradation because the passive devices are noiseless. The third is that the active coupling transistors Mc_1~Mc_4 make P-QVCO difficult to optimize phase noise and phase accuracy. The technique using capacitor to generate quadrature signals doesn't consider the coupling factor that defines as traditional P-QVCO.

2.3   Chip Layout and Simulation Results

Fig. 2 - 10 shows the chip layout photograph of the proposed QVCO which is implemented in TSMC 0.18 μm mixed-signal/RF CMOS 1P6M process. The chip size is 1×0.78 mm^2 including all pads and bypass capacitances. Each buffer of the QVCO output is designed as a common-source amplifier with bias-tee model. The core power consumption is 6.462 mW at 1.8 V supply.
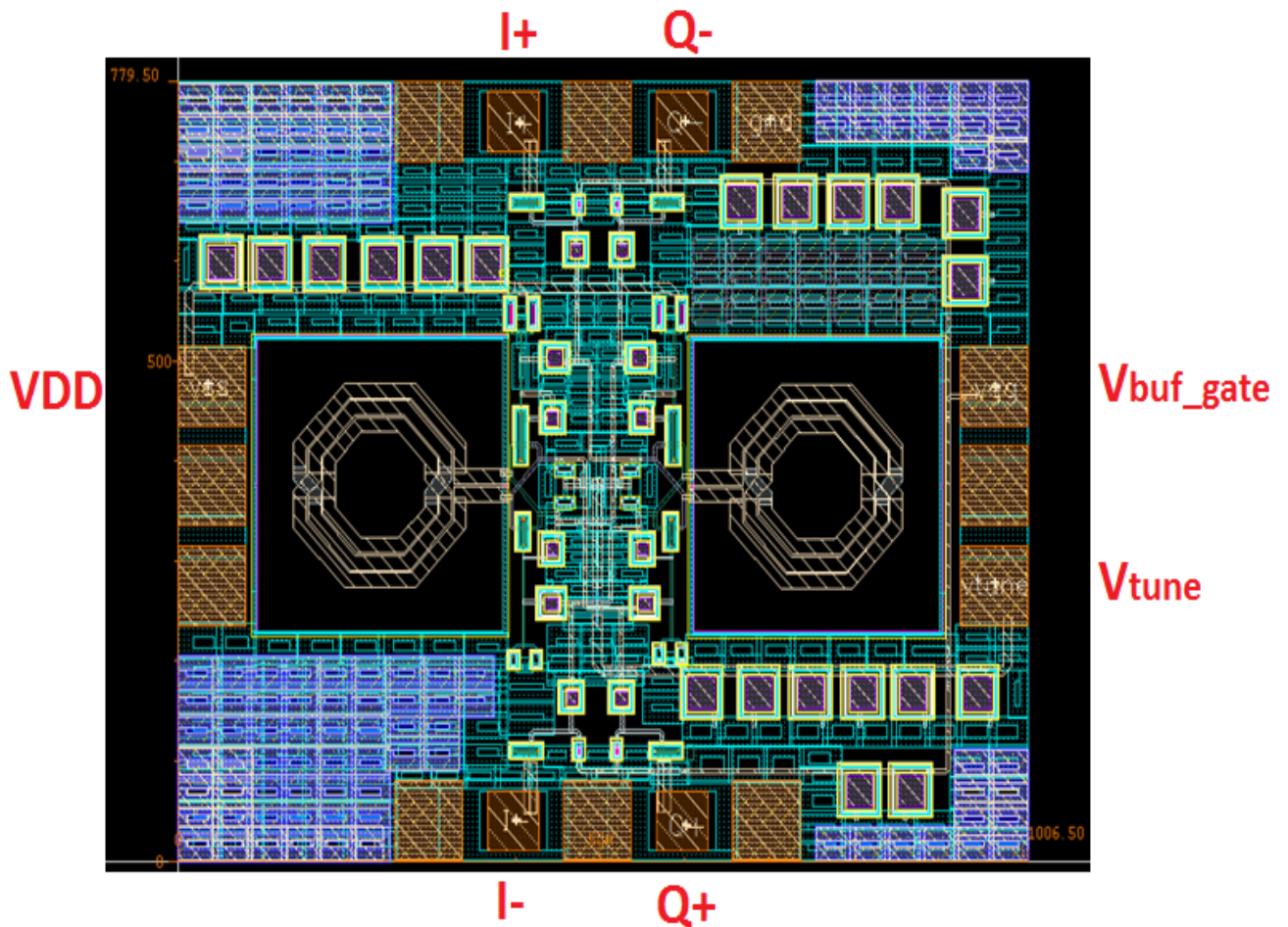

Fig. 2 - 10   Chip layout of the proposed QVCO

Compared with P-QVCO, as shown Fig. 2 - 2, the proposed QVCO has three advantages:

(1) Low phase noise

(2) It doesn't consider the trade-off of phase noise and phase error.

(3) Reducing power consumption.

The first combines current-reused VCO with Colpitts structure. And also it makes better phase noise by passive device coupling than active devise. Second, the active coupling transistors Mc_1 to Mc_4 make P-QVCO difficult to optimize phase noise and phase error. Using capacitor to generate quadrature signals doesn't consider the coupling factor that defines as traditional P-QVCO. Finally, proposed QVCO only uses two branch currents to get desired trans-conductance. However, P-QVCO needs four branch currents to get same trans-conductance.
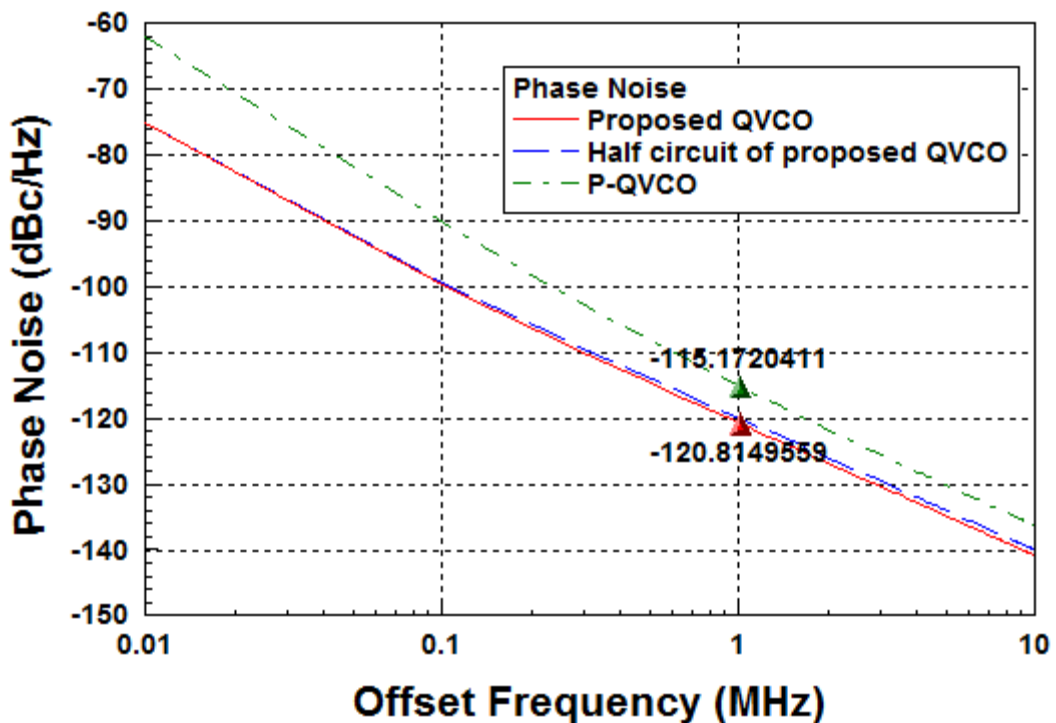

Fig. 2 - 11   The comparison of pre-simulated phase noise at 5GHz

Fig. 2 - 11 shows the pre-simulated phase noise performances of proposed QVCO, a stand-alone VCO of Fig. 2 - 6 and the P-QVCO of Fig. 2 - 2. Under supplied voltage of 1.8 V for all simulations at 5 GHz, the power consumption of the proposed QVCO is equal to the P-QVCO and is twice of the stand-alone VCO. In Fig. 2 - 11, the phase noise at 1MHz offset frequency of proposed QVCO is quite close to that of the stand-alone VCO. Compared with the phase noise of P-QVCO, the phase noise of proposed QVCO is better about 5 dB. Consequently, using Colpitts capacitor to couple quadrature signals doesn't make extra phase noise.

To consider EM effect, the simulated tuning range 、voltage swing at 5GHz and phase noise is shown in Fig. 2 - 12 to Fig. 2 - 14, respectively. The po-simulated tuning range covers from 4.7826 to 5.316 GHz with control voltage supplying from 0 V to 1.8 V shown in Fig. 2 - 12. When oscillatory frequency is 5.316 GHz, the po-simulated phase noise of proposed QVCO at 1 MHz offset frequency is -119.45 dBc/Hz shown in Fig. 2 – 13. Fig. 2 - 14 shows output voltage swing of proposed QVCO that exist a little amplitude error due to MOS mismatch. In addition, the po-simulated quadrature phase errors and differential phase error are below 4° shown in Fig. 2 - 14.
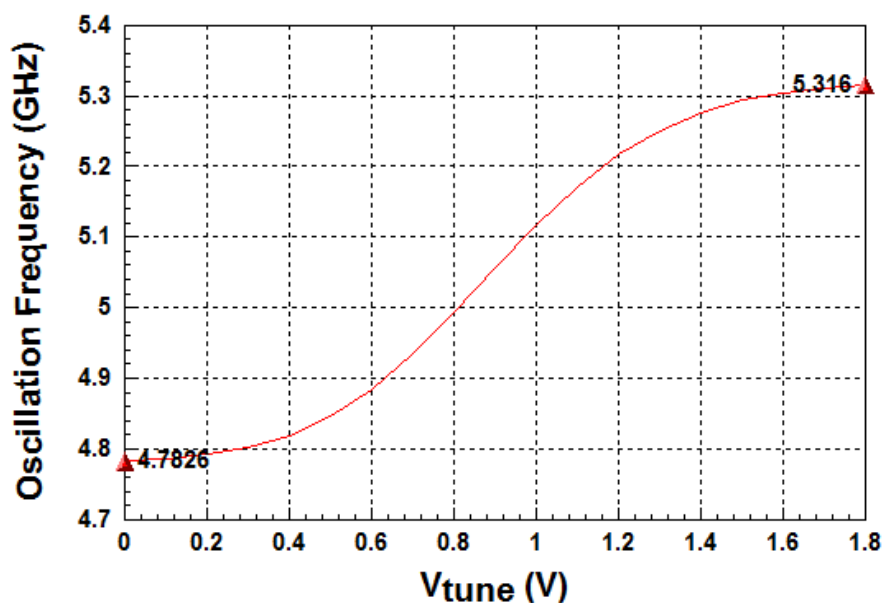

Fig. 2 - 12   Simulated tuning range of the proposed QVCO
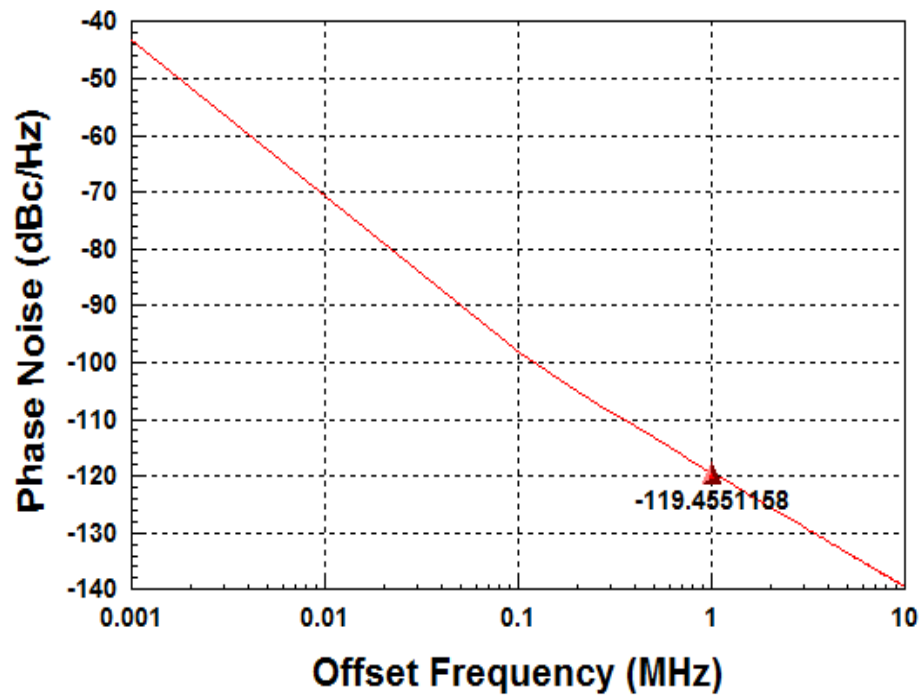
Fig. 2 - 13   Simulated phase noise of the proposed QVCO
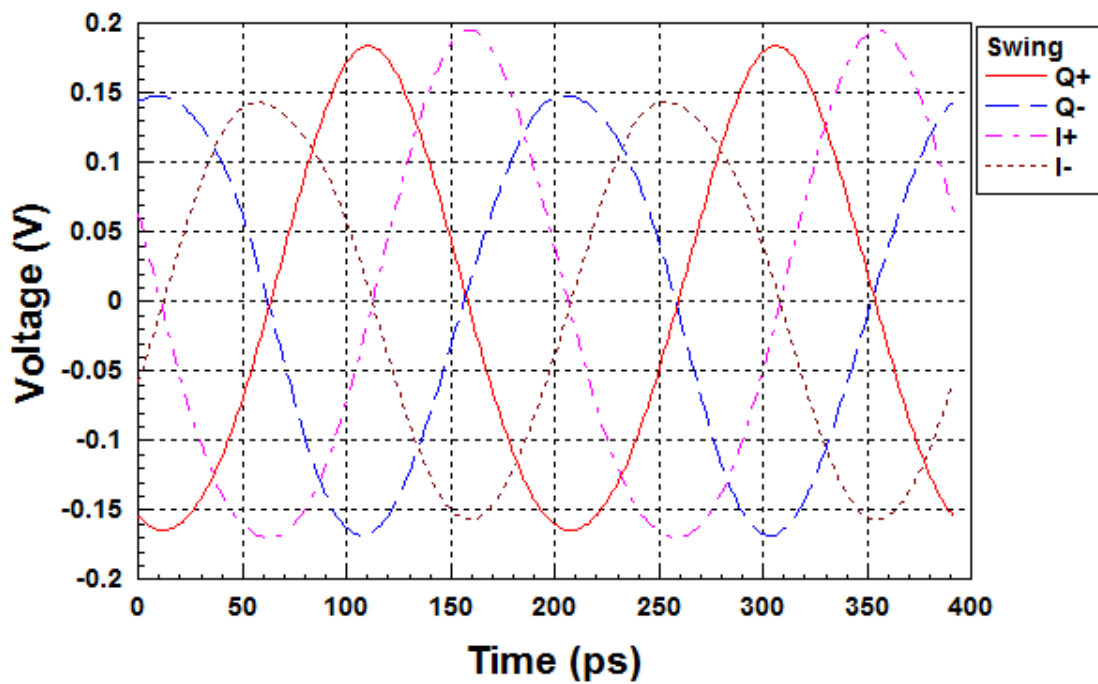
Fig. 2 - 14   Simulated swings of the proposed QVCO

2.4　Measurement Results and Comparison

2.4.1 Measurement Consideration

The proposed QVCO are designed for on-wafer testing, and the DC voltage are supplied by two sets of three-pin probe, so that the distance between each DC pad is 100um to satisfy the probe testing rules. The output buffer of each quadrature output is designed using common-source amplifier, and the drain end of each buffer is connected to the RF pad. For measurement, we connect four bias-tee terminals to the corresponding RF pads.

The phase noise, tuning range and output spectrum are measured by signal source analyzer (Agilent E5052B) shown in Fig. 2 - 15. The output voltage swing is measured by digital signal analyzer (Agilent DSA91204A) shown in Fig. 2 - 16.

Fig. 2 - 15　Signal Source Analyzer (Agilent E5052B)
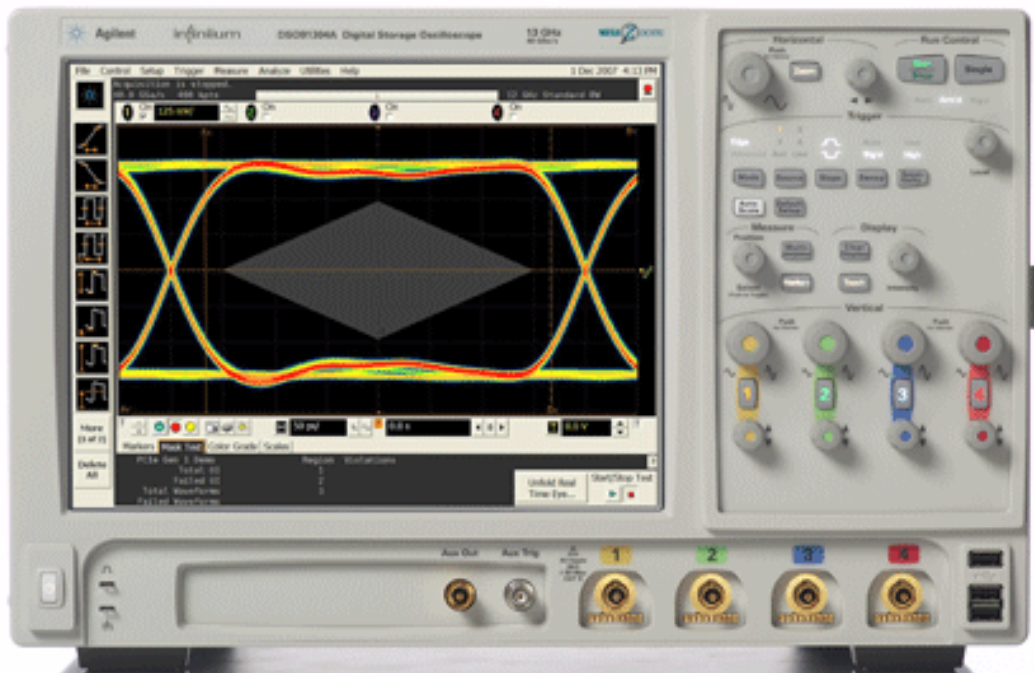
Fig. 2 - 16   Digital Signal Analyzer (Agilent DSA91204A)
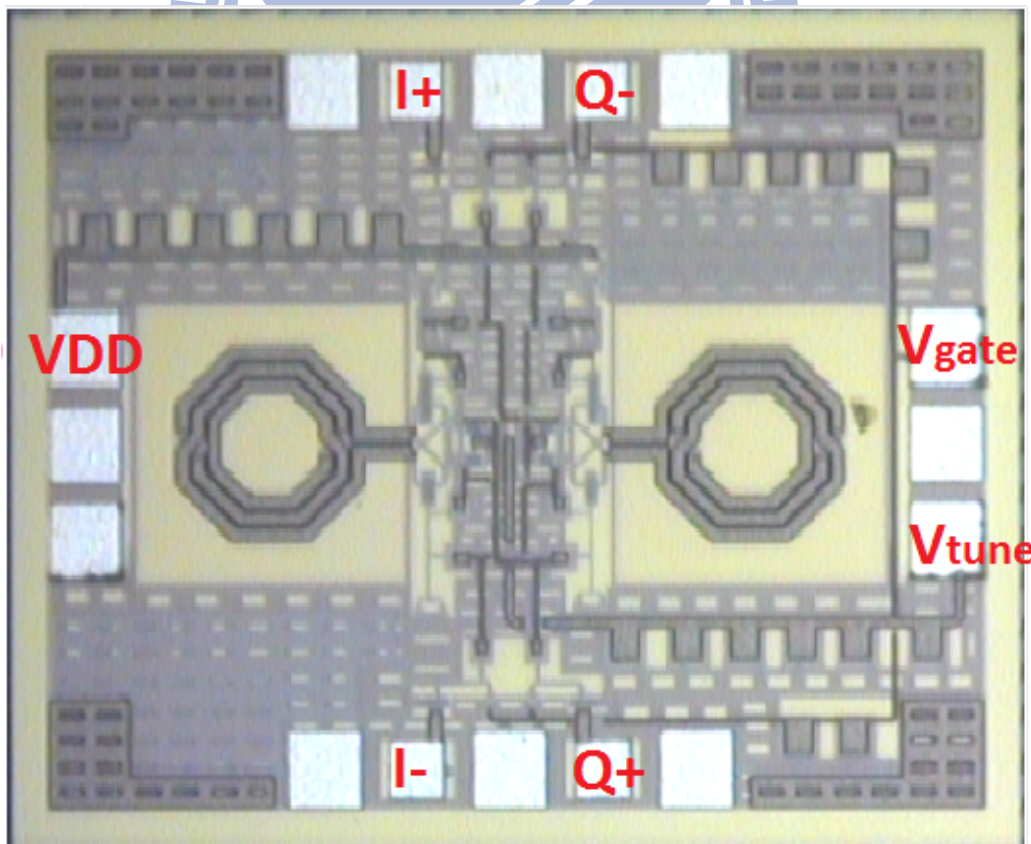
Fig. 2 - 17   Chip photo of the proposed QVCO

The Chip photo of the proposed QVCO is shown in Fig. 2 - 17. Fig. 2 - 18 shows the arrangement of DC and RF probes. The core DC consumption is 8.46 mW with 1.8 V. The measured phase noise at 1 MHz、output spectrum、output swings and tuning range, was shown in Fig. 2 - 19 to Fig. 2 - 22, respectively. When oscillatory frequency is 5 GHz, the measured phase noise of proposed QVCO at 1 MHz offset frequency is -119 dBc/Hz shown in Fig. 2 - 19. As shown in Fig. 2 - 20, the output power at 5 GHz is -8 dBm without compensating buffer effect and the loss of coaxial cables line. Measured output swings are shown in Fig. 2 - 21. According to measured swings data, the average phase error of quadrature signals and different signals is 8° and 9° respectively. The measured tuning range covers from 4.57 GHz to 5.02 GHz with control voltage supplying from 0 V to 1.8 V shown in Fig. 2- 22.
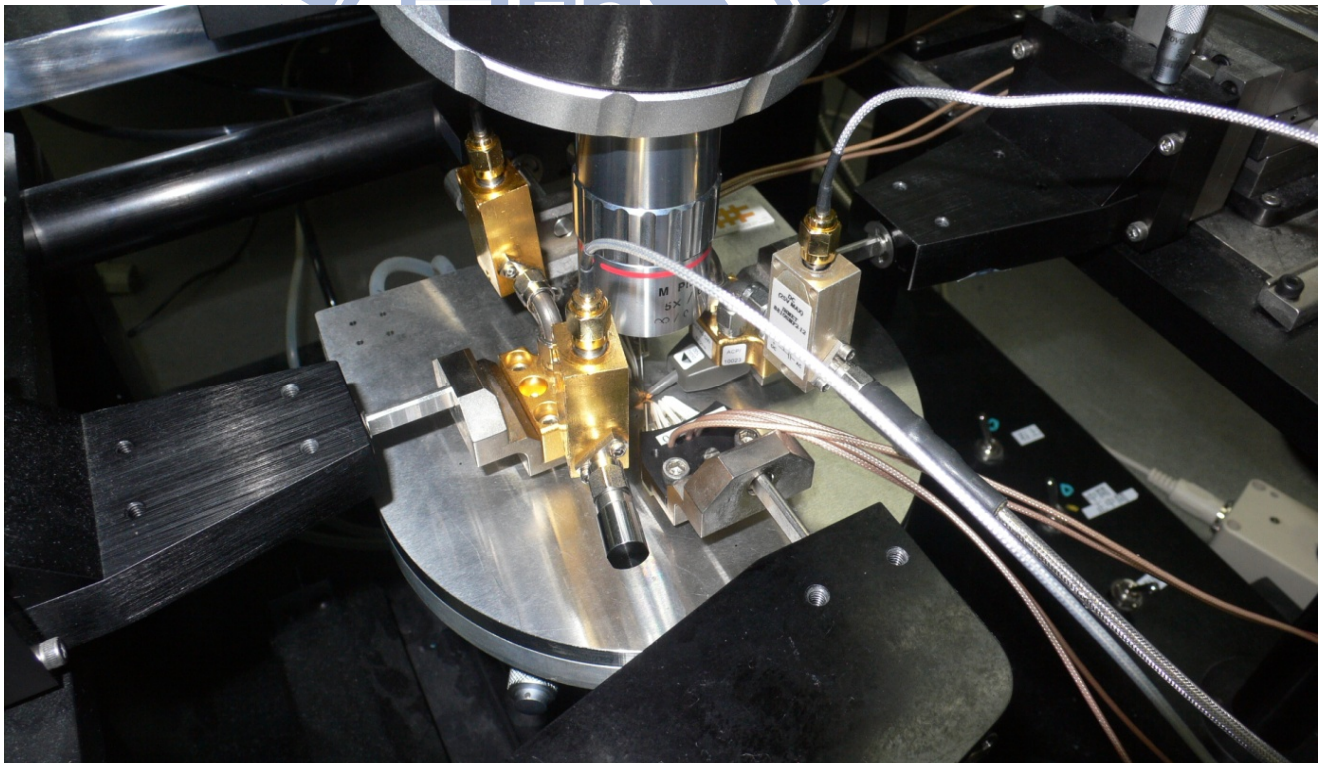
Fig. 2 - 18   Photograph of the probe station
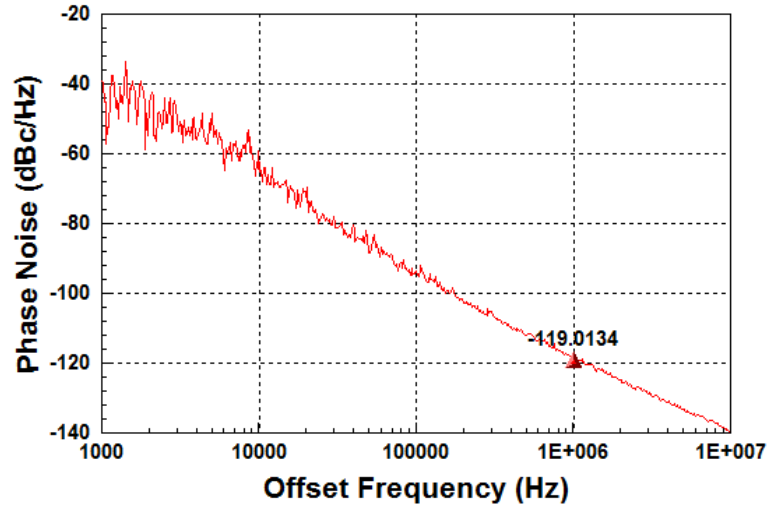
Fig. 2 - 19   Measured phase noise of the proposed QVCO
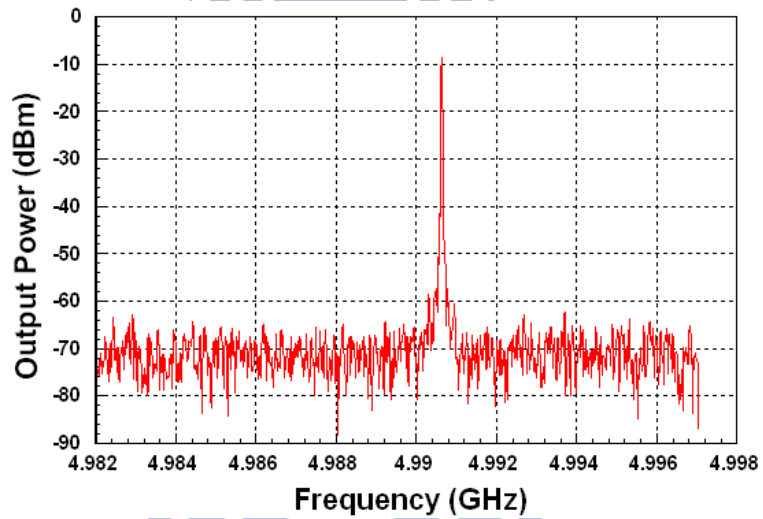
Fig. 2 - 20   Measured output spectrum of the proposed QVCO
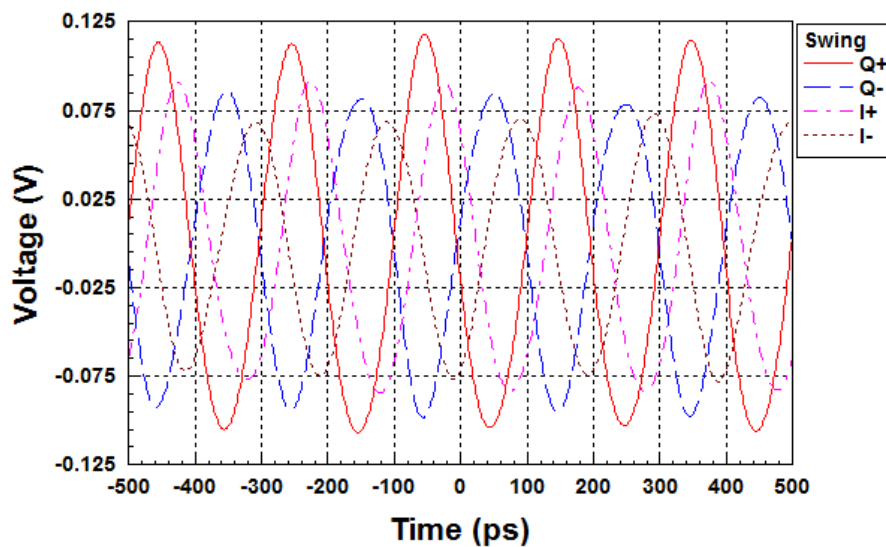
Fig. 2 -21   Measured voltage swings of the proposed QVCO
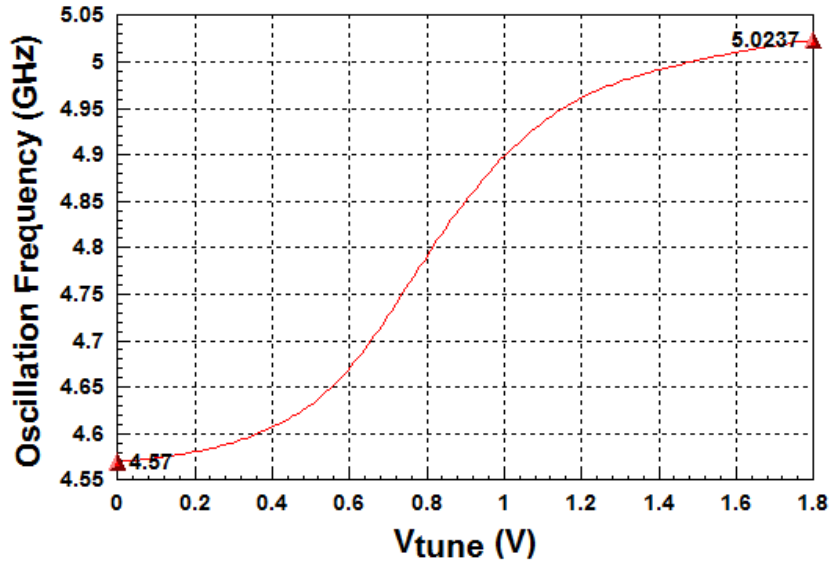
Fig. 2 -22 Measured tuning range of the proposed QVCO

The figure of merits (FOM) for oscillators summarizes the important performance parameters, i.e., phase noise and power consumption , to make a fair comparison is defined in [40] as :

$$FOM = L(\Delta\omega) - 20\log\left(\frac{\omega_O}{\Delta\omega}\right) + 10\log(\frac{P_{DC}}{1mW})$$

(2.3)

where Δf is offset frequency, $L(\Delta\omega)$ is phase noise at offset frequency, ω_O is the oscillation frequency, P_{DC} is the power consumption of core circuit. Table 2 - 1 summarizes the simulated and measured results of the proposed QVCO. Every measured performance is close to simulated results except frequency range. Table 2 - 2 shows the comparison of the measured results of proposed QVCO with the published papers of QVCOs. From Table 2 - 2, it can get proposed QVCO making better performance than other QVCO at same frequency and process

Table 2 - 1 Simulated results of the proposed QVCO

	Po-simulation	Measurement
Process	TSMC 0.18um CMOS	
Tuning Range (GHz)	4.7826 - 5.316	4.57 - 5.023
Bandwidth (MHz)	533.4	453
PhaseNoise@1MHz (dBc/Hz)	-119.45	-119
Output Power (dBm)	-5.9	-8
Supply Voltage (V)	1.8	1.8
Core Power (mW)	8.586	8.46
FOM	-184.04	-183.6

Table 2 - 2 Comparison of QVCO performance

	Process	Tuning Range	Phase Noise @1MHz	Supply Voltage	Core Power	FOM
This work (Chapter 2)	0.18μm CMOS	4.57-5.02 GHz	-119 dBc/Hz	1.8V	8.46mW	-183.7
[9] MWCL, 2009	0.18μm CMOS	4.39-5.26 GHz	-113.65 dBc/Hz	1.8V	6.3mW	-180.0
[10] MWCL, 2005	0.18μm CMOS	5.50-6.70 GHz	-115 dBc/Hz	1.8V	1.84mW	-182.2
[11] RFIC, 2002	0.18μm CMOS	6/9 GHz	-106 dBc/Hz	1.8V	6.8mW	-173.2
[12] PIERS 2007	0.18μm CMOS	5.15-5.75 GHz	-107 dBc/Hz	1.8V	1.5mW	-177
[13] EDSSC, 2007	0.18μm CMOS	5.25-5.58 GHz	-113 dBc/Hz	1.8V	21.6mW	-174.6

Chapter 3

A High Gain Down Conversion Mixer in Ku Band

3.1   Introduction

Mixer is an essential component of an RF system and translates the IF signal to a carrier frequency for transmission. Mixer operates either the trans-conductance of an amplifier or the resistance of a switch to produce the mixing action through time-varying mechanism. There are many structures of active mixers (single-balanced、double-balanced, etc.), the double-balanced circuit have been popularly appearing in microwave and millimeter wave applications for its good isolations because it solves the problem of LO-IF feed-through from single-balanced circuit.

Fig. 3 - 1   Conventional double-balanced mixer

For example, as indicated in Fig. 3 - 1, the schematic is a typical double balanced mixer. In order to enhance the conversion gain, it is perhaps to use large R_L. However, as R_L increasing, the voltage headroom will decrease and minimize the output swing to drive next stage hardly. Increasing the power supply V_{DD} is a solution but it will consume more power. Another solution is additionally current bleeding by using the two current sources as indicated in Fig. 3 - 2. Bleeding can achieve a higher conversion gain through the higher load because part of the trans-conductance stage current steers from the switching pairs. Furthermore, the transistors of switch pairs could be operated at a lower overdrive voltage and smaller size transistors could be used. In either case, for setting power of local signal, bleeding improves the conversion efficiency when lower charges are necessary to turn them on and off. However, bleeding degrades at high frequency performance of the trans-conductance stage due to the higher impedance at the output as the smaller DC currents through the switching pairs reduce their trans-conductance [14].
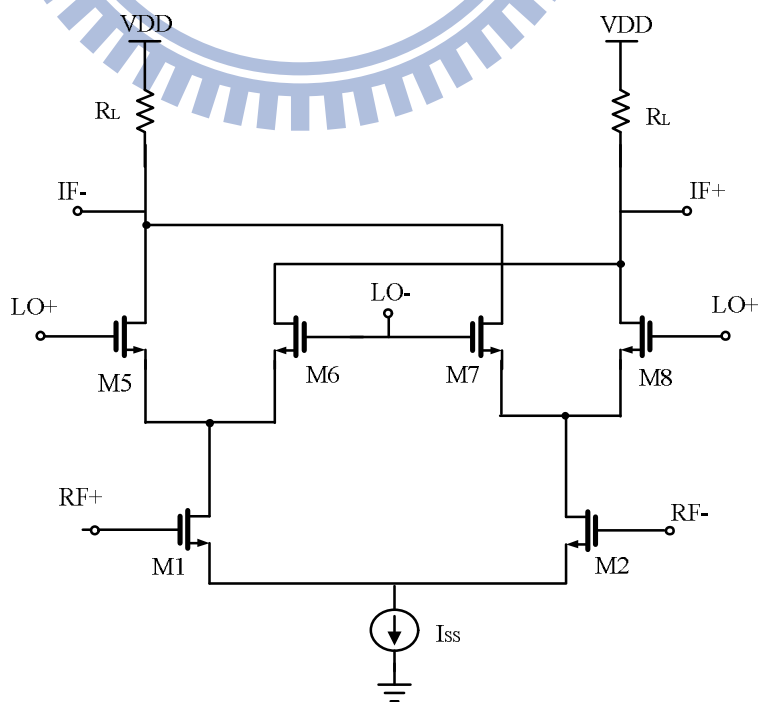
Fig. 3 - 2 Conventional double-balanced mixer with current bleeding

3.2   Circuit Design Consideration

The proposed high gain mixer is shown in Fig. 3 - 3. It can be divided mixer into three blocks, active load, switch pairs and radio frequency (RF) trans-conductance stage like Fig. 3 - 4 and discuss each block respectively.
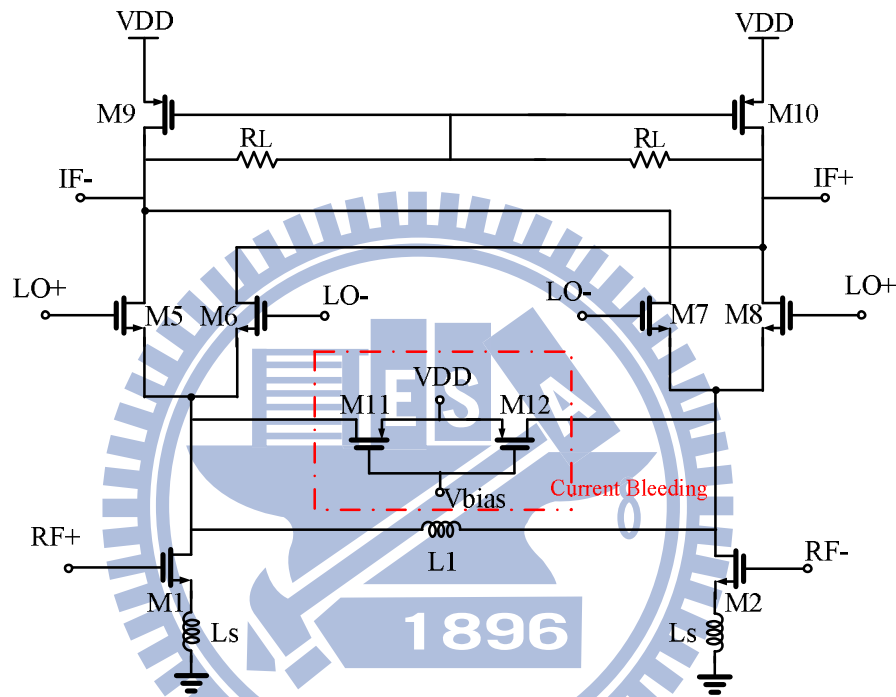

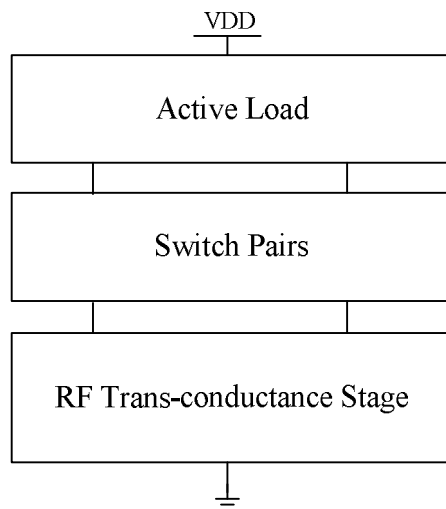Fig. 3 - 3   The proposed high gain mixer

Fig. 3 - 4   The block diagram of conventional mixer

The active load is shown Fig. 3 - 5. The transistors M_9 and M_{10} are the active load of the mixer replacing passive load resistors of conventional mixer. Furthermore, using M_9 、 M_{10} and R_L to construct common mode feedback circuit (CMFB) can stabilize the IF ports (IF+、 IF-) and restrain the common mode signal from the IF ports. R_L also can prevent the IF ports dropping as it is increased to provide more conversion gain. This will provide a better linearity than passive load structure even if the conversion gain is increased [27].
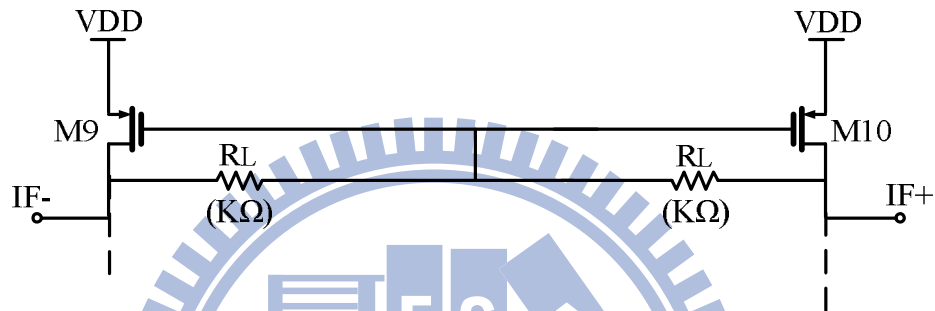

Fig. 3 - 5 The active load by CMFB circuit

The switching pairs are formed by four transistors M_5-M_8 and the current-bleeding circuit is composed of transistors M_{11}-M_{12}, shown Fig. 3 - 6. The current-bleeding circuit [14] plays an important component in the operation of the down-conversion mixer. First, it improves the conversion gain. Second, the switching pairs can be biased with a low overdrive voltage that reduces the local signal power needed for switching and makes the switching more ideal [14].
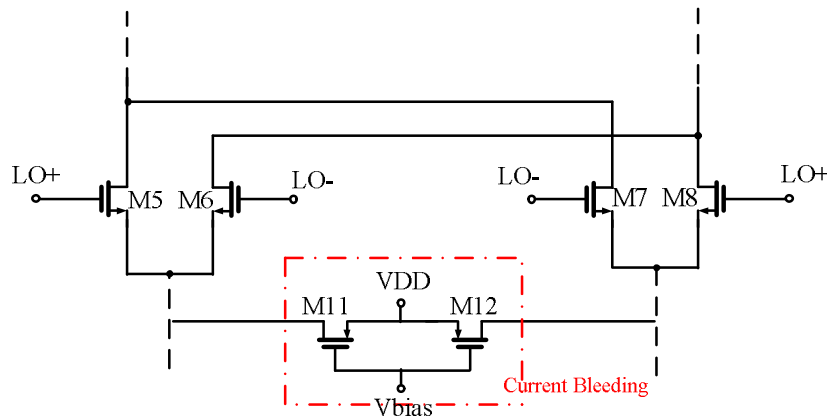

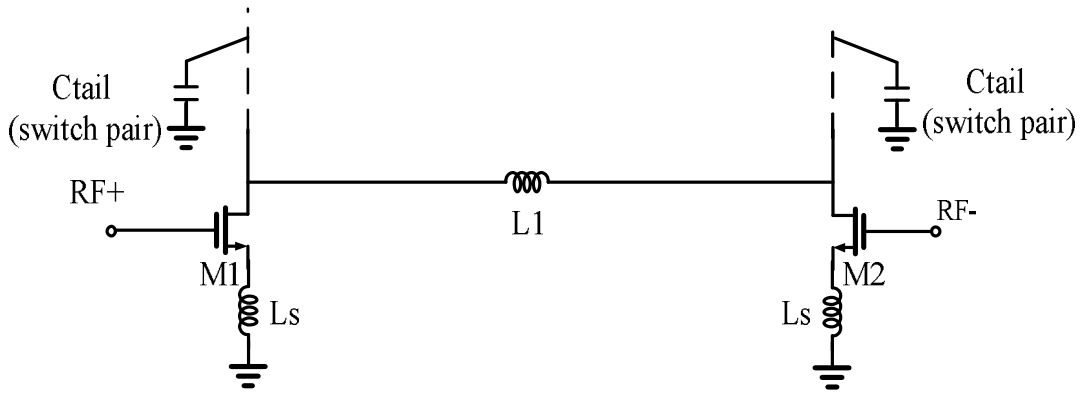Fig. 3 - 6 The switch pairs and current bleeding circuit

Fig. 3 - 7   The LNA trans-conductors for mixer

The LNA trans-conductors with inductor Ls is used to design RF trans-conductance stage [16] shown in Fig. 3 - 7. It is used the LC match input T-model network to simulate optimal noise and impedance matching. This match method yields good input matching and achieves minimum noise figure at the same time easily. Optimum the fingers of transistors and gate bias voltage are needed to get a minimum noise figure for the LNA. But, in mixer, the flicker noise of the switching pairs translates to output due to the direct and indirect mechanism that is explained in [15]. To minimize the noise effect of the direct mechanism, the current-bleeding circuit is used to decrease the dc current through the switch pairs. However, the current-bleeding circuit also adds noise to mixer. To minimize the noise of the current-bleeding circuit, PMOS transistor is chosen and biased at the optimum overdrive voltage for minimum noise. The size of switch transistors increases for getting high conversion gain as soon as tail capacitances of the switching pairs increase. It results extra flicker noise translating to the output indirectly [25]. This phenomenon is called noise in indirect mechanism. If parallel inductor L_1 be used to resonate out the tail-capacitance, the flicker noise in indirect mechanism will decrease.

3.3   Simulated and Measured Results

The proposed high gain mixer is simulated and optimized using Agilent ADS. Fig. 3 - 8 shows the chip layout of the proposed high gain mixer which is implemented in TSMC 0.18 μm mixed-signal/RF CMOS 1P6M process. The mixer size is 0.7×1.4 mm^2 including all pads and bypass capacitances. Each buffer of the IF ports were designed as a common-source amplifier.
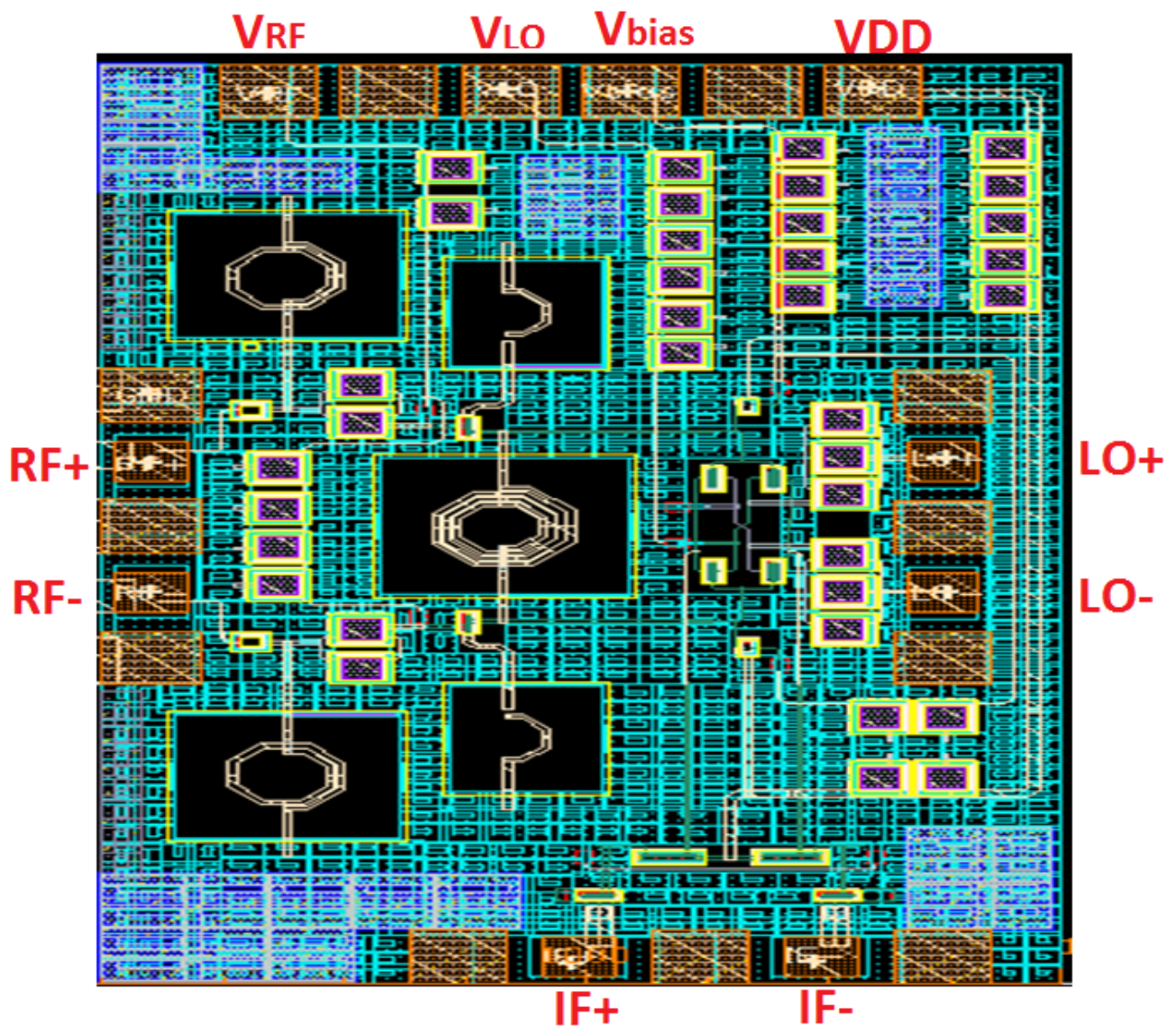

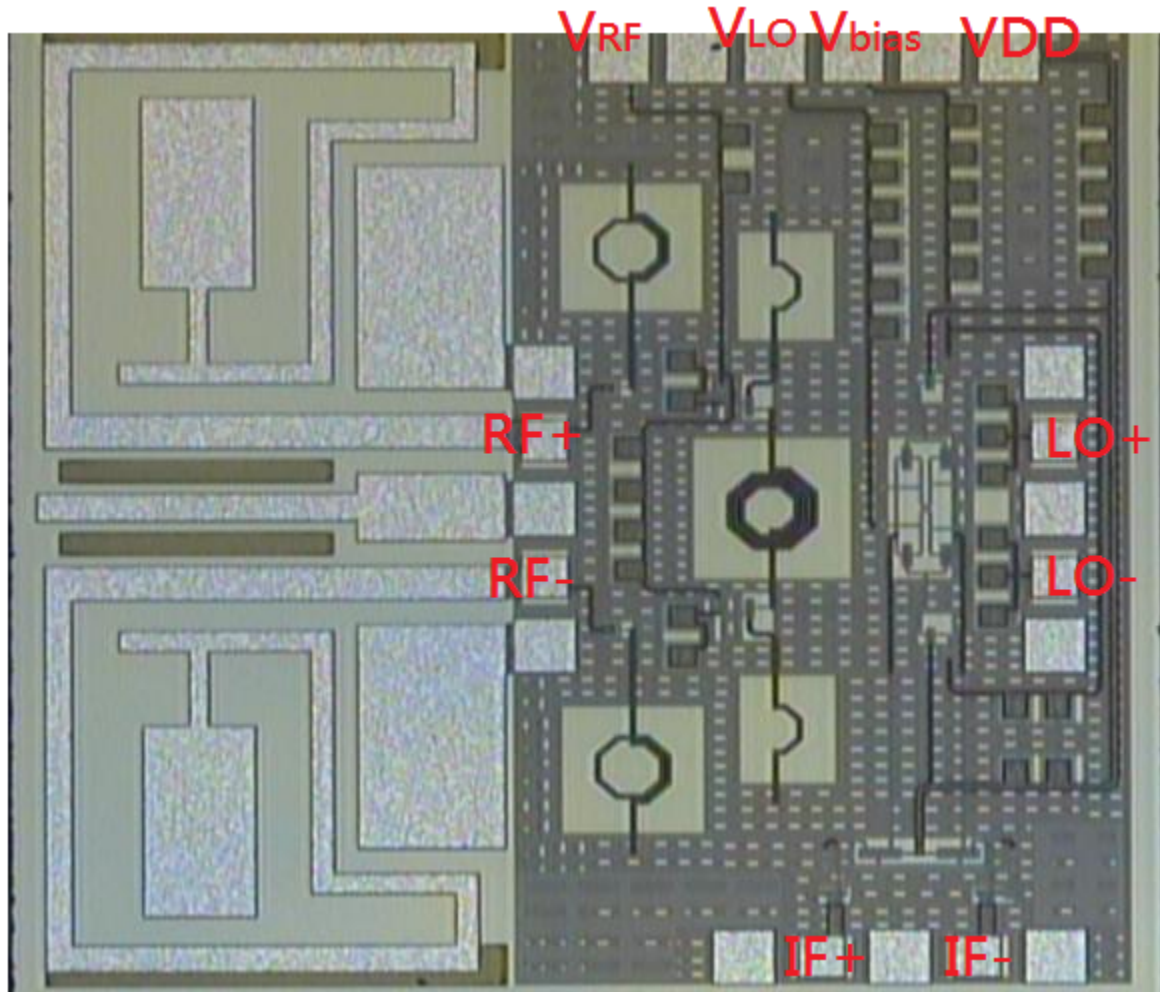Fig. 3 - 8   The chip layout photograph of the proposed high gain mixer

Fig. 3 - 9　The full chip photograph of integrated circuit

Fig. 3 - 9 shows the chip photograph of integrated circuit that includes antenna (0.7×1.4 mm^2) and high gain mixer (0.7×1.4 mm^2). Fig. 3 - 10 shows the simulated and measured s-parameter of RF ports. The simulated result without antenna is an exact performance of proposed mixer. However, it cannot cut the antenna to get the true results of mixer when the probe contacts the pad of mixer to measure performance. So, the matching s-parameter of mixer shifts to high frequency because the load of antenna affects matching impendence that smaller than standard impendence during measurement. As shown Fig. 3 - 10, the simulated s-parameter without antenna is below -10 dB in 12.5~15 GHz and with antenna is below -10 dB in 13~20 GHz. The measured s-parameter is averagely below -10 dB in 6~20 GHz.

Fig. 3 - 11 shows the simulated and measured the bandwidth of conversion gain while radio frequency down converts to 100 MHz. The simulated result with antenna or not exhibits the 3 dB gain bandwidth from 11.5 to 14.8 GHz and the maximum conversion gain is 22.285 dB at 13 GHz. However, the measured result decreases 4 dB approximately. The maximum conversion gain is 18.3 dB at 14 GHz and bandwidth covers from 12 to 16 GHz. As shown Fig. 3 - 12, the simulated noise figure without antenna is below 9 dB in 12~15.5 GHz and with antenna is below 12.3 dB in 12~16 GHz. The measured noise figure is below 16 dB in 12~16 GHz and the minimum is 13.214 dB at 13.5 GHz.
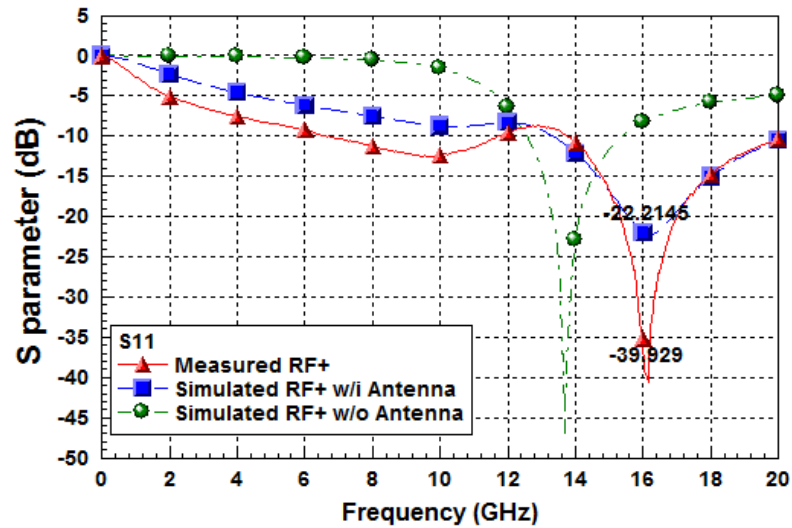

Fig. 3 - 10   The input return loss of the proposed high gain mixer
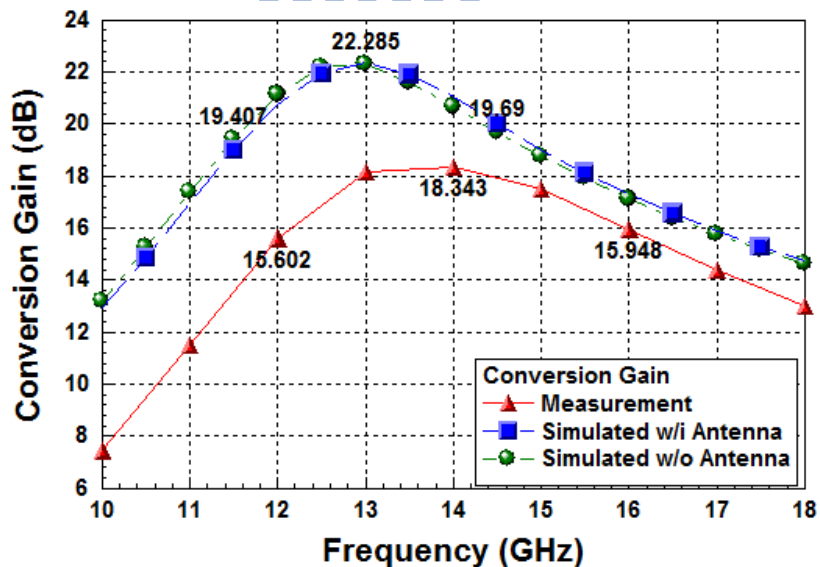

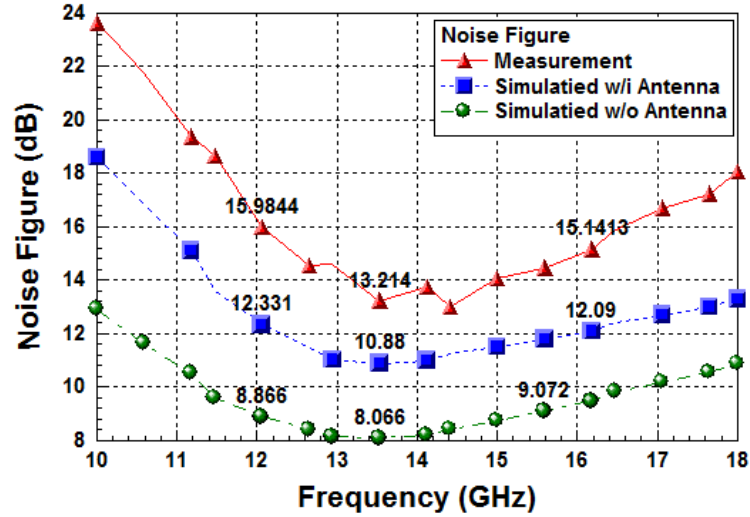Fig. 3 - 11   The conversion gain of the proposed high gain mixer

Fig. 3 - 12   The noise figure of the proposed high gain mixer

Fig. 3 -13 and Fig. 3 - 14 show the simulated and measured linearity at 14 GHz that is the radio frequency of the maximum conversion gain. The simulated linearity shows that P1dB is -26 dB and IIP3 is -15 dB. The measured linearity shows that P1dB is -16 dB and IIP3 is -7.5 dB. Fig. 3 -15 shows the measured isolation from 9.9 to 18 GHz. The LO-IF isolation is below -35 dB, the LO-RF isolation is below -55 dB and the RF-IF isolation is below -35 dB. The figure of merits (FOM) for mixer summarizes the important performance parameters and formula is defined as:

$$FOM_{Mixer} = 20\log(f_{RF}) + CG - NF(DSB) + IIP3 - 10\log(P_{Consumption}) \tag{3.1}$$

where f_{RF} is the center frequency. CG is the conversion gain. $NF(DSB)$ is noise figure at double-side band. $IIP3$ is input third-order intercept point. $P_{Consumption}$ is power consumption. Table 3 - 1 summarizes the simulated and measured results of the proposed high gain mixer. The simulated FOM is 193.7 by equation (3.1). However, the measured FOM drops to 191.42.

Including the antenna load effect, the simulated power consumption is not equal to the measured power consumption. This condition must be process variation. Also, the proposed mixer is used by idea balun to generate different signals and drive proposed mixer. The performance of idea balun is obviously different from the real balun that used in measurement because real balun exists phase error but idea balun doesn't. So, from Fig. 3 – 11 to Fig. 3 – 15, the simulated results are not fit measured results perfectly due to process variation and using real balun.
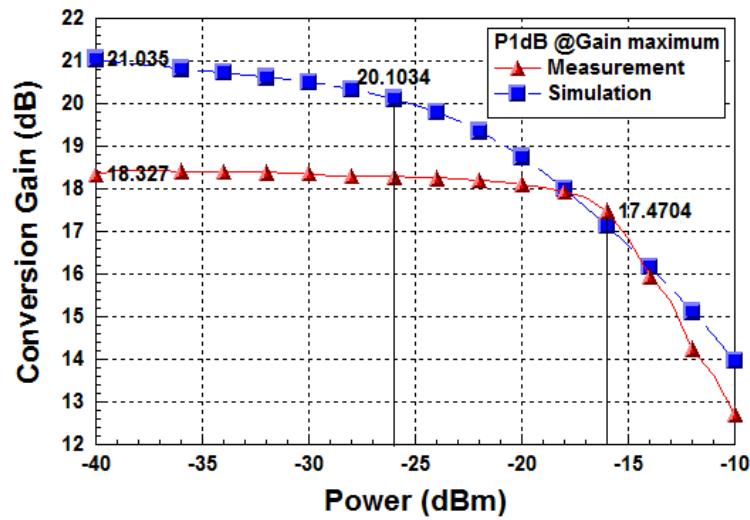
Fig. 3 - 13　　The P1dB of the proposed high gain mixer
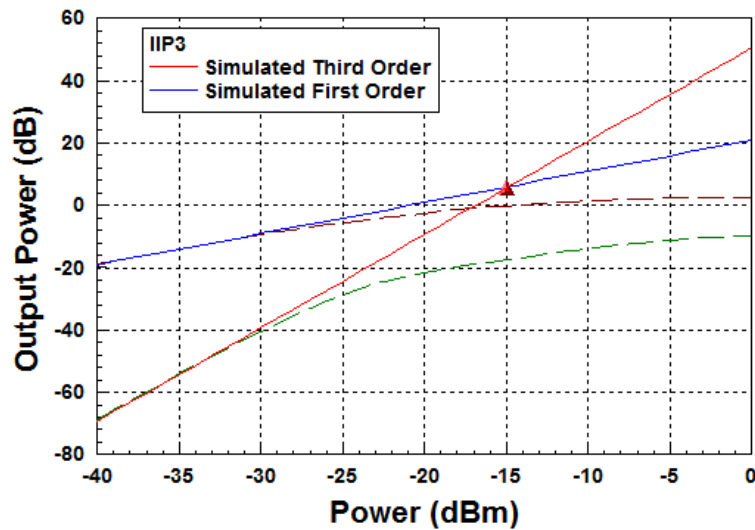
(a) Simulation
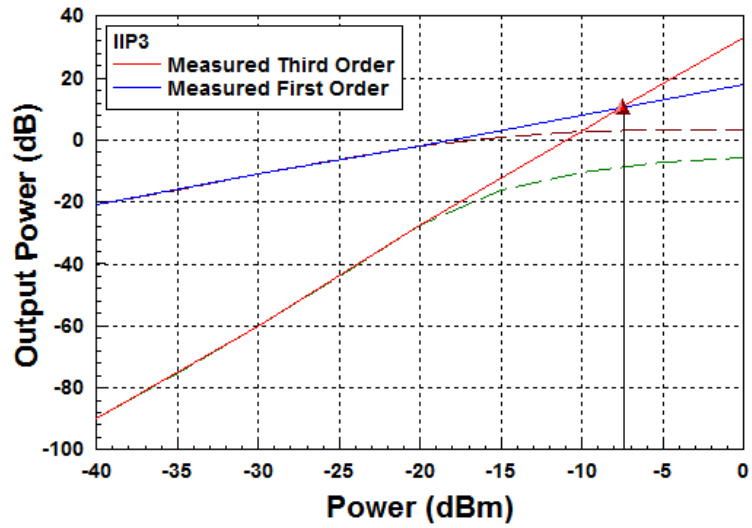
(b) Measurement

Fig. 3 - 14   The IIP3 of the proposed high gain mixer
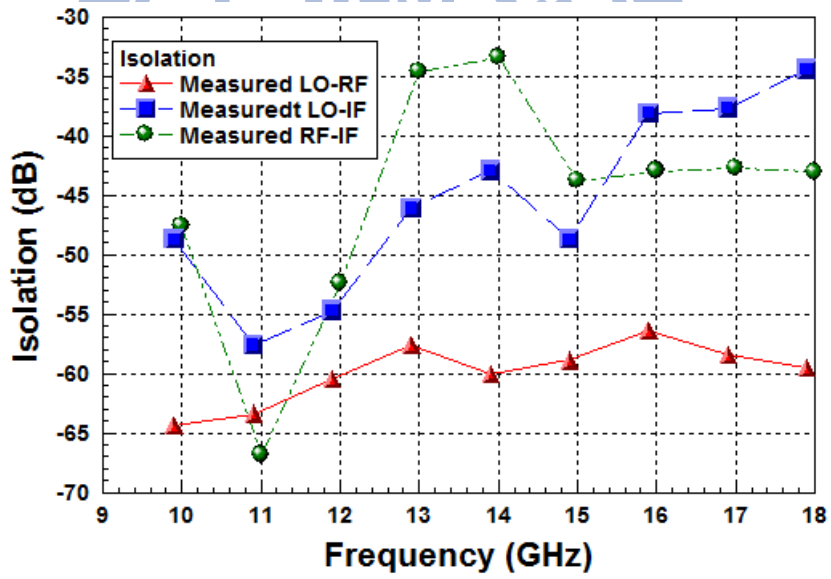
Fig. 3 - 15   The isolation of the proposed high gain mixer

Table 3 -1 Simulated results of the proposed high gain mixer

	Simulation	Measurement
Technology	TSMC 0.18um CMOS	
RF Freq.	11.5~14.8 GHz	12~16 GHz
IF Freq.	100 MHz	100 MHz
LO Power	0 dB	0 dB
Conversion Gain,max	22.285 dB	18.327
NF	8~9	13.2~15.9
P1dB	-26 dB	-16 dB
IIP3	-15 dB	-7.5 dB
LO-to-RF isolation	< -40 dB	< -55 dB
LO-to-IF isolation	< -35 dB	< -35 dB
RF-to-IF isolation	< -35 dB	< -35 dB
Power Consumption	6.12 mW	7.56 mW
FOM	193.7	191.42

Table 3 -2 Comparison of mixer performance

	This Work (Chapter 3)	[27]	[28]	[29]	[30]
Process	TSMC 0.18 um CMOS	TSMC 0.18 um CMOS	0.18um CMOS	0.18um CMOS	TSMC 0.18 um CMOS
RF Bandwidth(GHz)	12 ~15	12~18	6 ~9	6 ~10	5.725~5.825
Conversion Gain (dB)	15.3~18.3	6.52~8.12	14~14.8	8	11.06
Noise Figure (dB)	13.2~15.9	17.26	15.1	13.5	12.8
P1dB (dB)	-16	NA	NA	NA	-16.4
IIP3 (dB)	-7.5	3.5	-13.9	NA	-7.5
Power Consumption (mW)	7.56	6.36	17.4	10.5	3.6
FOM	191.42	189.84	170.9	182.34+ NA	180.43

Chapter 4

4-17 GHz Wideband High Gain Down Conversion Mixer with Cascade Structure

4.1 Introduction

Direct conversion front-end circuit is a very important component in wireless communication system. Generally, front-end circuit must be constituted by low-noise amplifier (LNA) and mixer. The mixer is a key block to translate signals in the system. In the development of modern wireless applications, wideband frequency range, low power consumption and small chip area are the aims of work. For these topics, the idea of high gain mixer is proposed and replaced conventional front-end circuit further. The double-balance mixer is commonly used because the advantage of this active mixer is good isolation [14]. However, the main challenge in double-balanced mixer is to decrease noise figure and extend frequency range for more applications at steady high conversion gain.

In this chapter, a broadband high gain mixer is presented for many bands applications such as C band (4~8 GHz)、X band (8~12 GHz) and most part of ultra-wide band (3.1~10.6 GHz) and Ku band (12~18 GHz). The RF trans-conductance stage of proposed mixer uses cascade structure that the capacitor cross-coupled wideband amplifier at first stage replaces passive LC input match network to design high gain mixer at wide frequency range.

4.2   Circuit Design Consideration

Radio frequency designs are increasingly used in advance CMOS process that makes the integration of complete communications systems possibly [17]. The proposed mixer at this chapter is shown in Fig. 4 − 1. In high gain mixer, the blocks of active load and switch pair are discussed at chapter 3. This section focuses on RF trans-conductance stage how to achieve high gain and low noise figure in wideband. The RF part can be divided into CS-LNA [17] at second stage and CCC CG-LNA [20] at first stage.
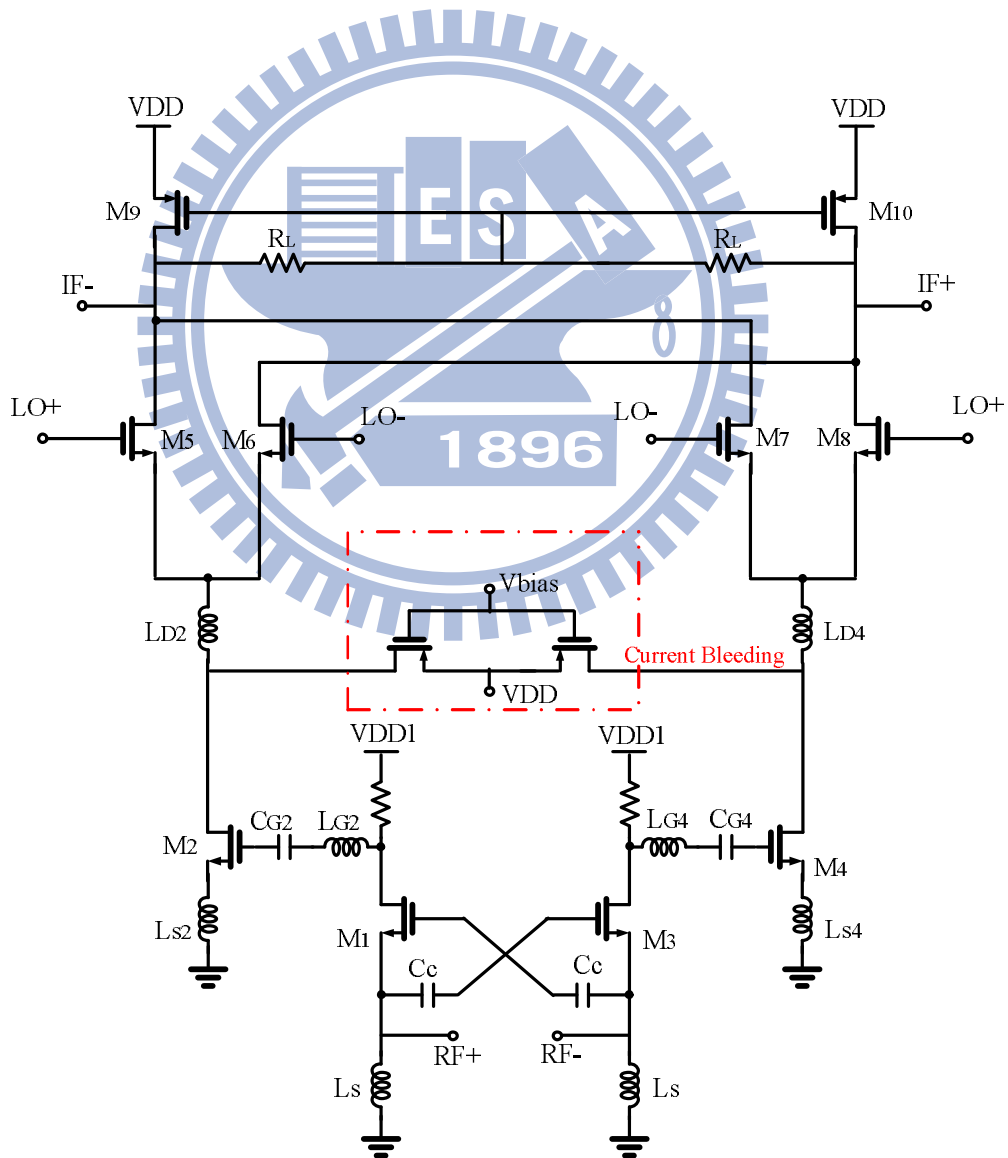

Fig. 4 - 1   The proposed high gain mixer with wideband amplifier

A. Common Source Low Noise Amplifier (CS-LNA)

As shown Fig. 4 – 2, it is a popular structure of low noise amplifier that is inductive generation common-source LNA (CS-LNA). In a CS-LNA, degenerated inductor L_{S2} is used to generate the real part impedance needed to match the LNA easily. Using L_{G2} is called series RLC network circuit can possibly match the input impedance to 50Ω in narrow band. A simple analysis of input impedance is defined as [17]:

$$Z_{in} = s(L_{G2} + L_{S2}) + \frac{1}{sC_{tot}} + (\frac{G_{m2}}{C_{tot}})L_{S2}$$ (4.1)

At the series resonance frequency of the input network circuit, the impedance is purely real and proportional to L_{S2}. The gate inductor L_{G2} is used to set the resonance frequency as it is chosen to satisfy the criterion of 50 Ω input impedance [17]. C_{tot} is the capacitance of $C_{GS,2}$ and C_{G2} in series. The large gate capacitance C_{G2} is used to be a DC block so the capacitance of C_{tot} almost equals to $C_{GS,2}$.
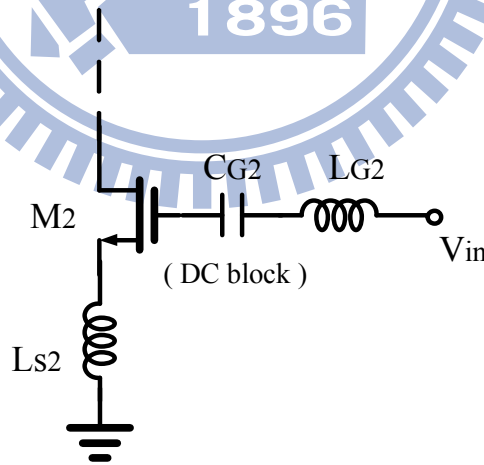

Fig. 4 - 2   The CS-LNA with series RLC input match network

However, the degenerated inductor common source LNA with a series RLC input match network only can enhance effective trans-conductance to increase gain and reduce the noise figure in narrowband [19].

B. Capacitor Cross-Coupled CG-LNA (CCC CG-LNA)

In order to extend bandwidth, common gate amplifier (CGA), shown Fig. 4 - 3, is used to match wideband input impedance generally. The simple input admittance and noise factor analysis of CGA is defined as [20]:

$$Y_{in} = s(C_{GS1}) + \frac{1}{sL_S} + G_{m1}$$

(4.2)

$$F_{CGA} \approx 1 + \frac{\gamma}{\alpha}$$

(4.3)

α,γ are bias-dependent parameters [26]. According Equation (4.2), the CGA at first stage can achieve to 50 Ω because the input impedance looking into the source of transistor M_1 is approximate $1/G_{m1}$. However, the CGA suffers from poor noise figure comparison to CS-LNA [20]. To solve this problem, a capacitive cross-coupling method can boost the trans-conductance of transistors M_1 and M_3 with the passive component of capacitors [20]-[22]. As shown in Fig. 4 – 4, it is called capacitor cross-coupled common-gate low noise amplifier (CCC CG-LNA).
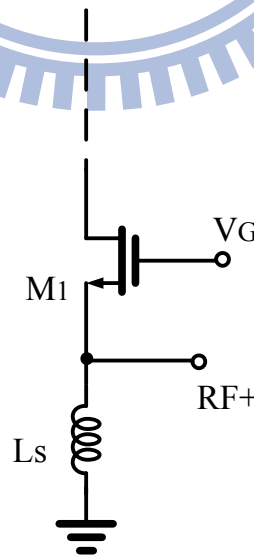

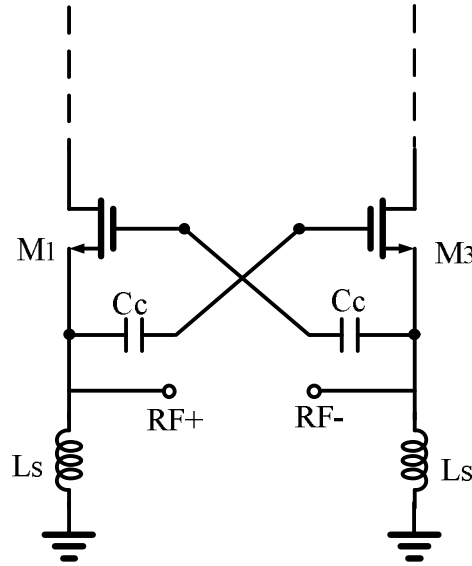Fig. 4 - 3   The structure of common gate amplifier

Fig. 4 - 4   The structure of CCC CG-LNA

According to Fig.4 – 4, the small signals analysis of CCC CG-LNA can prove the effective trans-conductance and noise factor better than CGA by following formula:

$$G_{m,eff} = (\frac{C_{GS} + 2C_C}{C_{GS} + C_C})G_{m1} \approx 2G_{m1} \tag{4,4}$$

$$F_{CCC,CG-LNA} \approx 1 + \frac{\gamma}{2\alpha} \tag{4,5}$$

Due to capacitors cross-coupling, the noise factor decreases and the effective trans-conductance is double if C_C is much larger than C_{GS}. So, the CCC CG-LNA is fit for wideband differential topology.

The RF trans-conductance stage of proposed mixer combines CCC CG-LNA with CS-LNA to design a cascade structure. The CCC CG-LNA at first part achieves wideband input matching to improve applications and supplies the RF gain of low frequency band. The CS-LNA at second part includes both the RF gain of high frequency band and translating voltage signals into current signals that provides switch pair down-conversion. L_{D2} and L_{D4} resonate out the tail capacitance of switch pairs to reduce flicker noise in indirect mechanism more [15] [23] [25].

4.3 Simulated and Measured Results

The proposed high gain mixer is simulated and optimized using Agilent ADS. Fig. 4 - 5 shows the chip layout of the proposed high gain mixer which is implemented in TSMC 0.18 μm mixed-signal/RF CMOS 1P6M process. The chip size is 1.19×1.17 mm^2 including all pads and bypass capacitances. Each buffer of the IF ports were designed as a common-source amplifier.
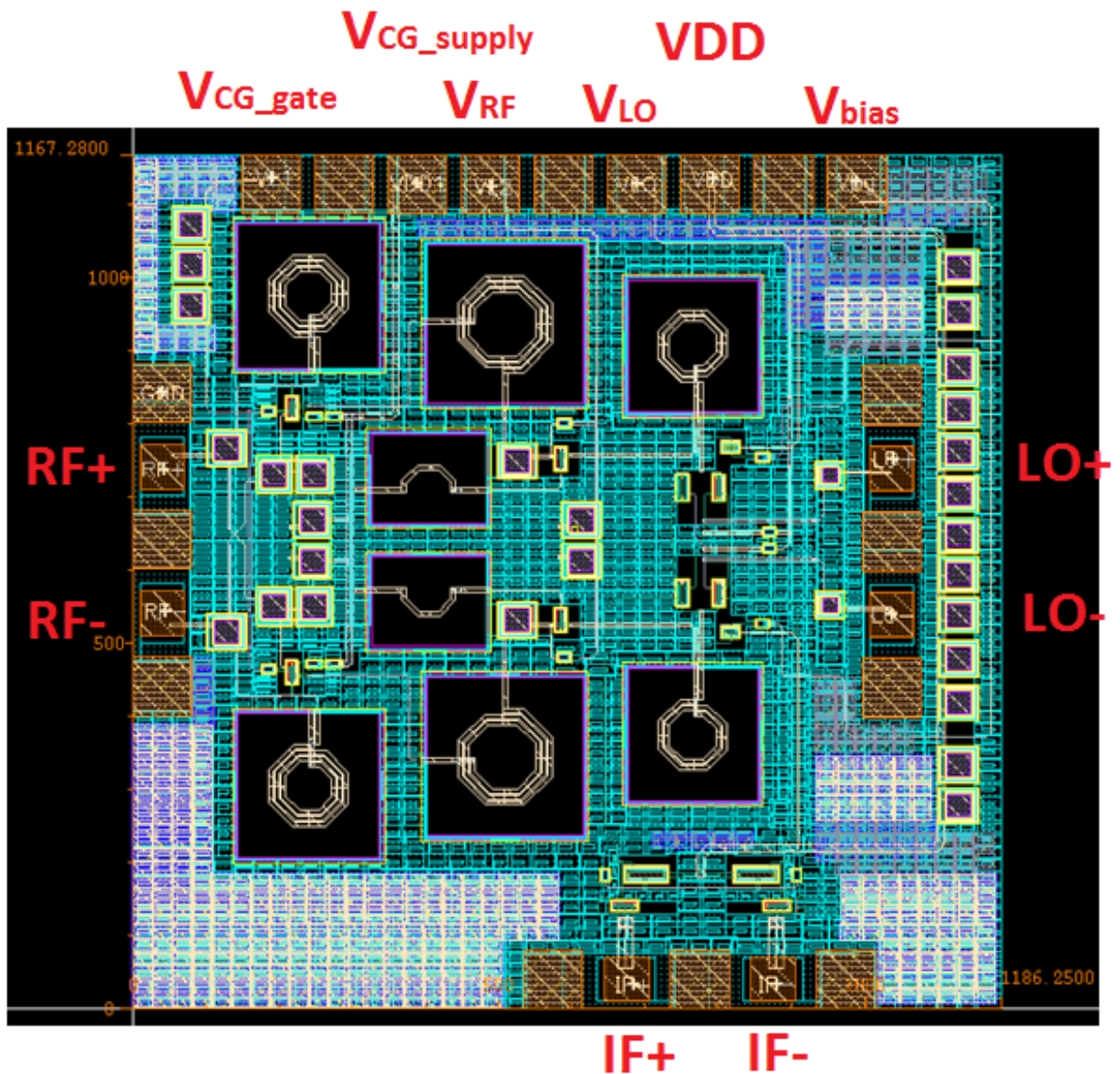

Fig. 4 - 5　The chip layout of the proposed mixer
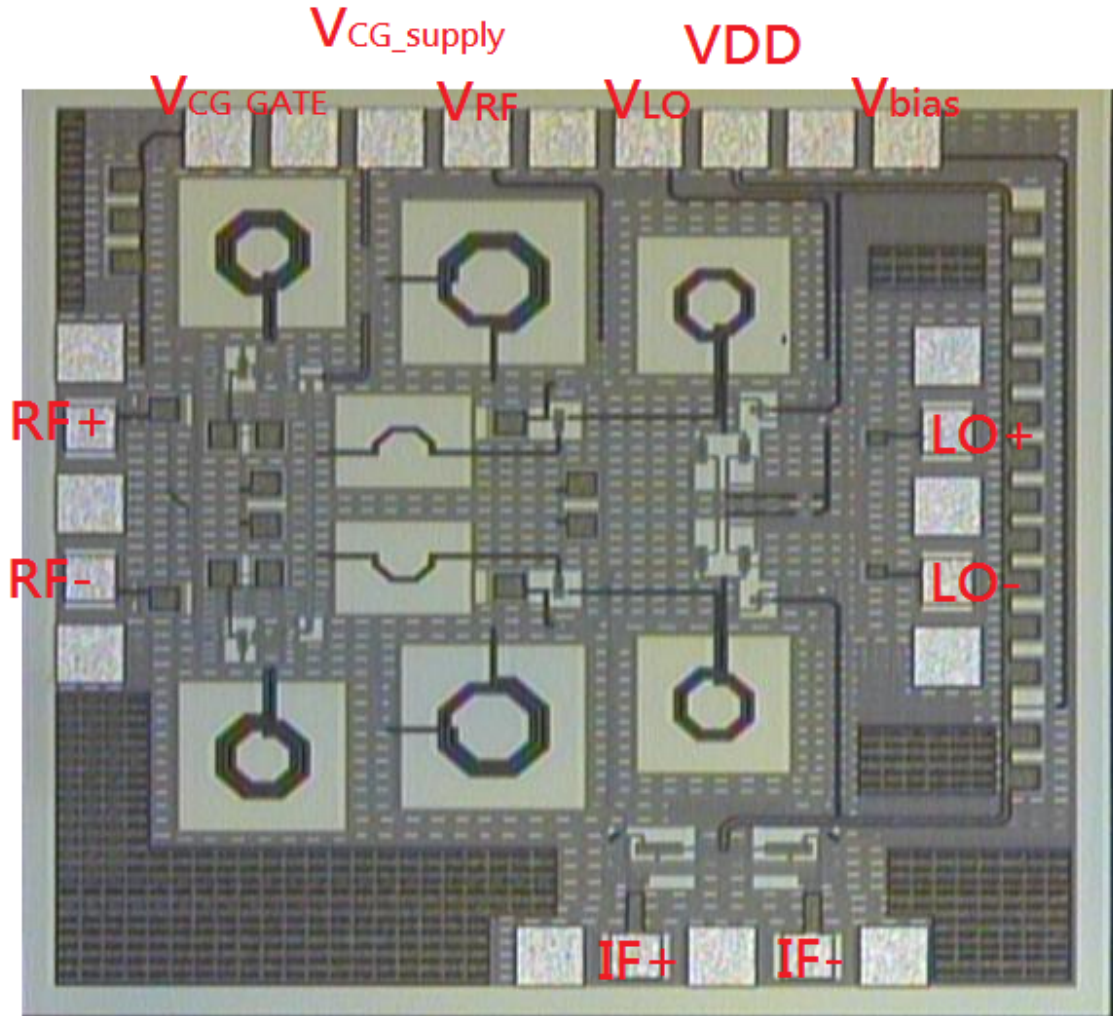
Fig. 4 - 6　The chip photograph f the proposed mixer

Fig. 4 - 6 shows the chip photograph of proposed mixer. As shown in Fig. 4 -7, the simulated and measured return losses of RF ports are below -8 dB in 4~20 GHz. Fig. 4 - 8 shows the simulated and measured the bandwidth of conversion gain when radio frequency down converts to 100 MHz. The simulated result exhibits the 3dB gain bandwidth from 2.7 to 17.8 GHz and the maximum conversion gain is 27 dB at 4 GHz and 15 GHz. But, the measured result decreases 4 dB approximately and the maximum conversion gain is 22.7 dB at 4 GHz and 16 GHz. The simulated noise figure is below 8 dB in 4~17 GHz and the measured noise figure is below 12 dB in 4 ~16 GHz shown in Fig. 4 - 9.

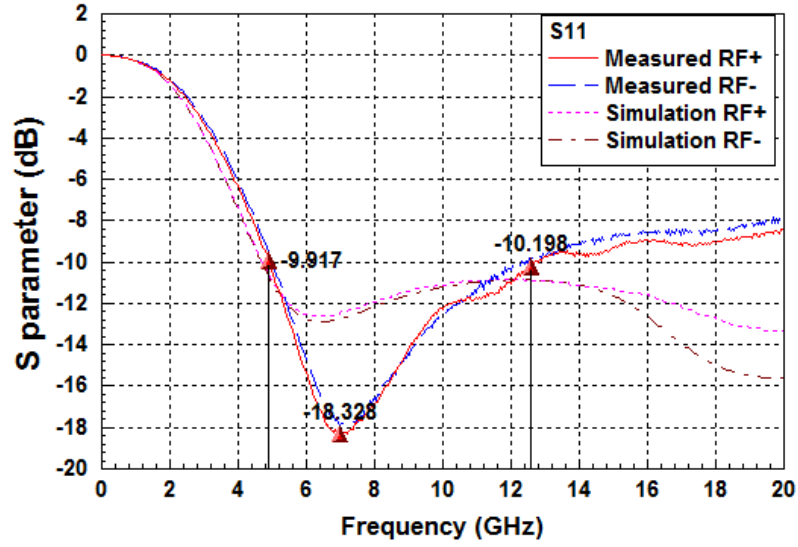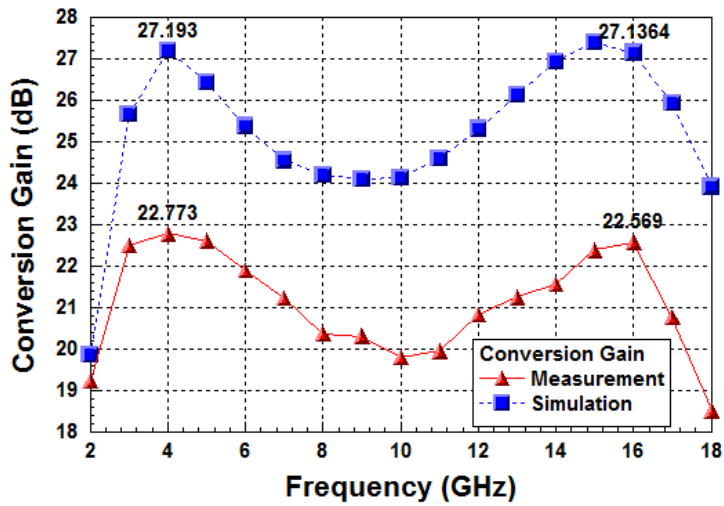Fig. 4 - 7   The input return loss of the proposed mixer

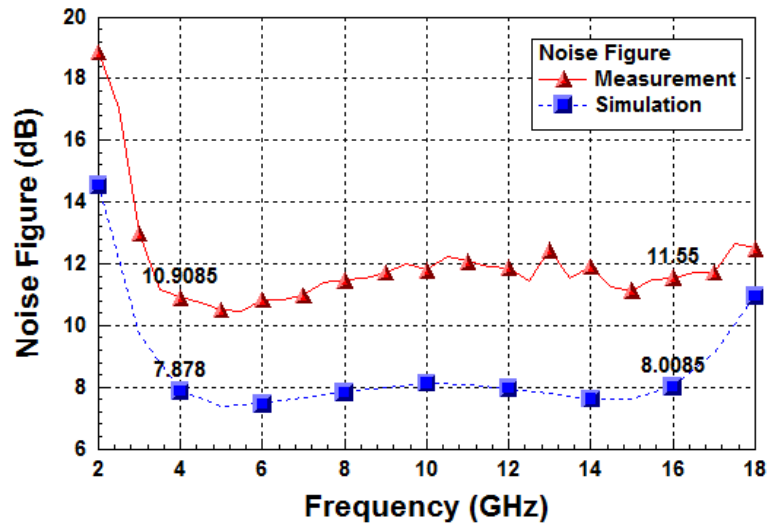Fig. 4 - 8   The conversion gain of the proposed mixer

Fig. 4 - 9   The noise figure of the proposed mixer

Fig. 4 - 10 and Fig. 4 - 11 show the simulated and measured linearity at 16 GHz that is the radio frequency of the maximum conversion gain. The simulated linearity shows that P1dB is -28 dB and IIP3 is -17 dB. The measured linearity shows that P1dB is -20 dB and IIP3 is -10 dB. Fig. 4 - 12 shows the measured isolation from 0.9 to 20 GHz. The LO-IF isolation is below -40 dB, the average LO-RF isolation is below -60 dB and the average RF-IF isolation is below -30 dB. Table 4 - 1 summarizes the simulated and measured results of the proposed high gain mixer. The simulated FOM is 192.84 by equation (3.1). However, the measured FOM drops to 192.04.

Compared with the simulated power consumption, the measured power consumption is 12.058 mW and is more than the simulated power consumption which is 9.012 mW. This condition must be process variation. Also, the proposed mixer is used by idea balun that generates different signals and that drive proposed mixer. The performance of idea balun is obviously different from the real balun that is used during measurement because real balun exists phase error but idea balun doesn't. So, from Fig. 4 – 7 to Fig. 4 – 12, the simulated results are not fit measured results perfectly due to process variation and using different balun.
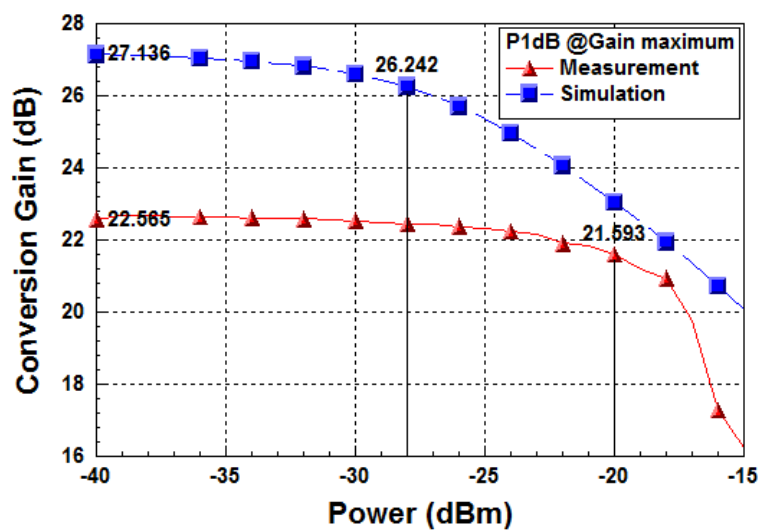
Fig. 4 - 10   The P1dB of the proposed mixer
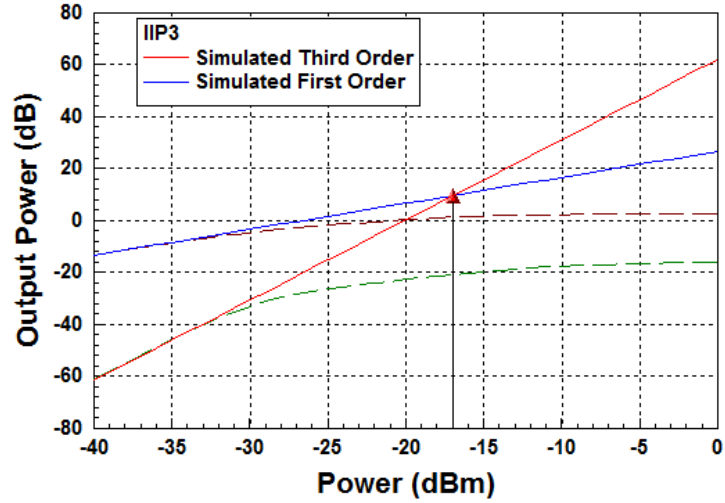
(a) Simulation
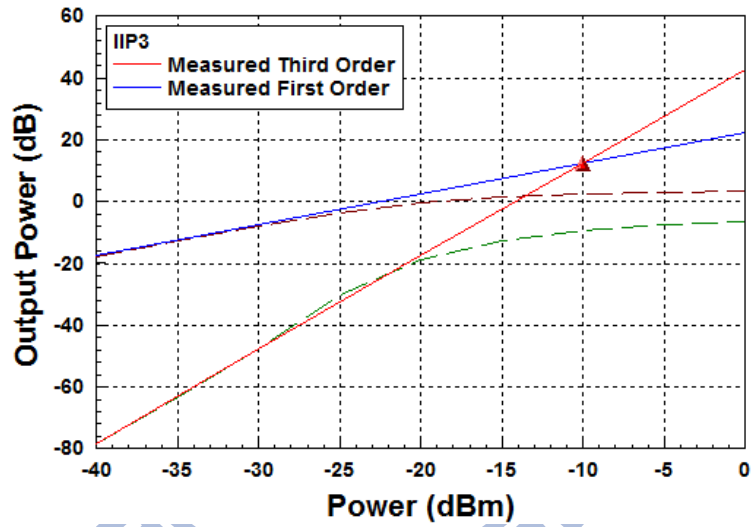
(b) Measurement

Fig. 4 - 11   The IIP3 of the proposed mixer
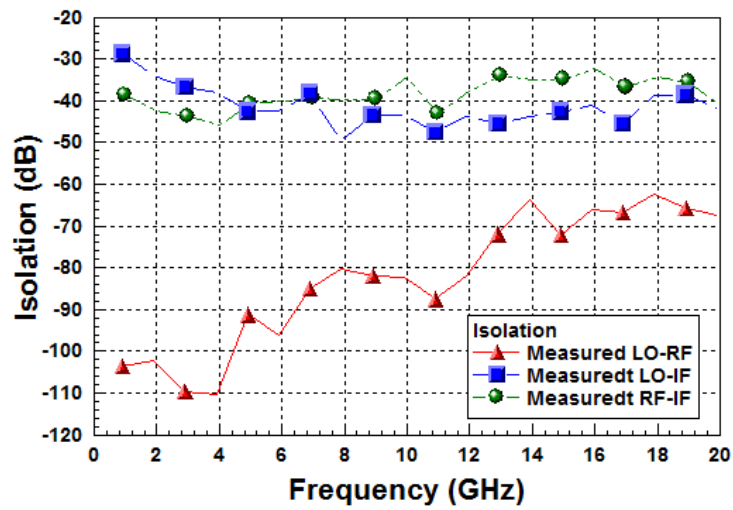
Fig. 4 - 12   The isolation of the proposed mixer

Table 4 -1 Simulated and measured result of the proposed mixer

	Simulation	Measurement
Technology	TSMC 0.18um CMOS	
RF Freq.	4~16 GHz	4~17.8 GHz
IF Freq.	100 MHz	100 MHz
LO Power	0 dB	0 dB
Conversion Gain,max	27.19 dB	22.565
NF	7.8~8 dB	10~12 dB
P1dB	-28 dB	-20 dB
IIP3	-17 dB	-10 dB
LO-to-RF isolation	< -60 dB	< -60 dB
LO-to-IF isolation	< -40 dB	< -40 dB
RF-to-IF isolation	< -30 dB	< -30 dB
Power Consumption	9.012 mW	12.058 mW
FOM	192.84	192.04

Table 4 -2 Comparison of broadband mixer Performance

	This Work (Chapter 4)	[34]	[35]	[36]	[37]
Process	TSMC 0.18 um CMOS	0.13 um CMOS	GaAs HBT	0.13 um CMOS	0.13 um CMOS
RF Bandwidth(G Hz)	4~17.8	3.1~10.6	1.5~14	3.1~10.6	3.1~10.6
Conversion Gain (dB)	20~22.565	9.8 ~ 14	20	18~22.3	19.5~23.3
Noise Figure (dB)	10.9~12	14.5~19.6	23	5.7~9.6	5.2~9.1
P1dB (dB)	-20	-24~-19	NA	-21.5	NA
IIP3 (dB)	-10	NA	-3	-9.6	-10.4
Power Consumption (mW)	12.058	1.85	16.32	46.5	42
FOM	192.04	193.54+NA	179.66	187.04	188.18

Chapter 5

Conclusion and Future Work

5.1　Conclusion

In chapter 2, I proposed a new structure for low phase noise QVCO: Colpitts current-reused QVCO based on capacitor coupling. This technology not only generates quadrature signals easily but also uses passive coupling capacitor instead of active coupling transistors to solve the trade-off of phase noise and phase error in P-QVCO. Furthermore, using Colpitts capacitor to couple quadrature signals doesn't make extra phase noise. The measured phase noise at 1 MHz offset frequency is -119 dBc/Hz at 5 GHz. The FOM is -183.7.

In Chapter 3, I proposed architecture for high conversion gain mixer. To design each part of mixer, active load, switch pairs and RF driver stage, and add current-bleeding circuit to mixer, it can achieve high performance in narrow band. Furthermore, using parallel inductor that resonates out the tail capacitance of switch pairs can decrease noise in indirect mechanism effectively. The measured conversion gain with antenna is the maximum 18.3 dB at 14 GHz and bandwidth covers from 12 GHz to 16 GHz. Also, the measured noise figure with antenna is below 16 dB in 12~16 GHz and the minimum is 13.2 dB. The FOM is 191.42.

In Chapter 4, I further proposed a wideband and high conversion gain mixer with cascade structure. In RF stage of proposed mixer, the CCC CG-LNA at first part achieves broadband input matching to enhance application and supplies the RF gain of low frequency

band. The CS-LNA at second part includes both supplying the RF gain of high frequency band and translating voltage signals to current signals that provides switch pairs to down convert. Also inductors that are between switch pairs and the RF stage reduces flicker noise in indirect mechanism more. The measured gain bandwidth covers from 2.7 to 17.8 GHz. In the meantime, the measured conversion gain is the maximum 22.7 dB at 4 GHz and 16 GHz. The measured noise figure is below 12 dB in 4~16 GHz and the minimum is 10.45 dB. The FOM is 192.04.

5.2 Future Work

This paper focus on how to design a better component, at same time, I also study the theory of phase-locked loop and simulate PLL by ADS、Hspice and Matlab. For enhancing the performance, I add QVCO that is proposed in this paper to PLL. According to simulated results, it shows better performance than other PLL certainly. As to high conversion gain mixer, it can integrate with differential antenna being a front-end circuit without LNA. In chapter 3, the integrated circuit is the first step to plan how to make better performance for integration. So, the circuit will be measured completely, shown as Fig. 5 - 1, and improving performance will be my future research.
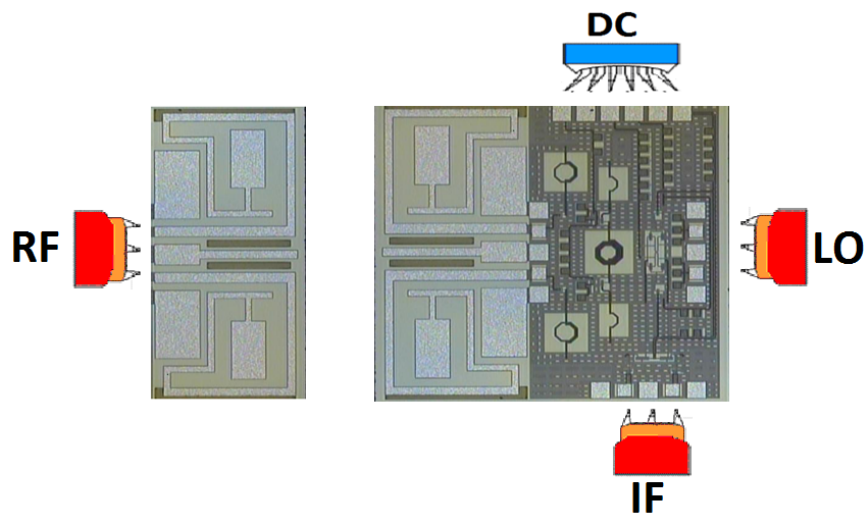

Fig. 5 - 1   The measured diagram of integrated mixer with antenna

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