Correspondence

A High-Density MOS Static RAM Cell Using the Lambda Bipolar Transistor

CHUNG-YU WU AND YIH-FANG LIU

Abstract—**Based upon the common-collector lambda bipolar transistor (LBT), which is built with p-well NMOS, and the parasitic n-p-n BJT in a CMOS IC, a novel MOS static RAM cell called the LBT cell is proposed. In this new cell, the LBT and two poly-Si resistors form a bistable element with a PMOS access transistor. With the minimum feature size F, the optimal cell area of 32 F^2 can be realized by using the silicide contact and small p-well spacing. The READ-WRITE operation is simulated. Due to the need of precharging before reading and the rather slow recovery after reading, suitable peripheral circuits should be designed.**

Compared with dynamic MOS RAM, static MOS random access memory (RAM) has the advantages of simple operation with no refreshing required. However, the static RAM suffers from low packing density which is caused by the complex cell circuitry. This problem becomes more severe as the memory bit capacity increases. Two methods are applied to solve the problem. One is the use of advanced fabrication technologies to reduce the chip area. The other is the use of new devices or circuits for the cell. The latter method is effective since the total cell area usually occupies 60–70 percent of the total memory chip area. Therefore the efforts of searching for a new cell which has high packing density and good speed-power performance have been increased recently [1]–[6].

This correspondence describes a new MOS static RAM cell which is constructed by using a negative resistance device called the lambda bipolar transistor (LBT) [7], [8]. The proposed new cell, which is called the LBT cell, consists of one PMOS access transistor and one bistable storage element. The storage element is designed by using two poly-Si resistors and one common-collector type n-p-n lambda bipolar transistor, which consists of an NMOS merged with an n-p-n bipolar junction transistor (BJT). Since the PMOS, NMOS, and n-p-n BJT are compactly merged, the LBT cell has the highest packing density among all MOS static RAM cells. Moreover, it gives a good balance between process complexity, operation complexity, and performance.

The proposed new static RAM cell circuit is shown in Fig. 1(a) where the BJT Q_2 and the NMOSFET M_1 form a lambda bipolar transistor [7]–[8] as marked by the dashed line. The collector of the LBT is connected to V_{DD}, while the base and the emitter are connected to V_{DD} and ground through poly-Si resistors R_1 and R_2, respectively. This common-collector type of LBT, together with R_1 and R_2, serves as a bistable storage element which is accessed through the PMOSFET M_3. The typical integrated structure of the LBT cell is shown in Fig. 1(b). It may be seen that the p-well in M_1 also serves as the base of Q_2 and the source of the M_3.

The bistable characteristics of the storage element in the cell can be understood by superimposing the current-voltage

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The authors are with the Institute of Electronics, National Chiao Tung University, Hsin-Chu, Taiwan, Republic of China.

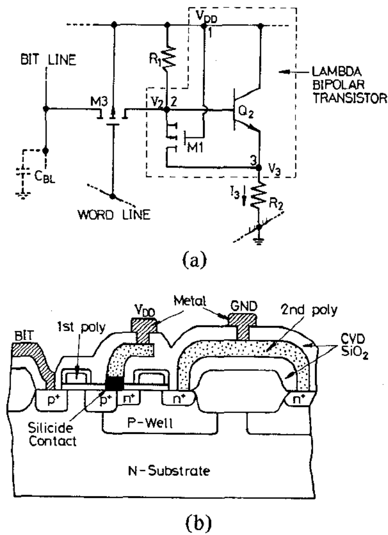

Fig. 1. (a) Schematic circuit diagram of an LBT cell. (b) Cross-sectional view of the integrated LBT cell.

characteristics of the common-collector LBT and its source resistor R_2, as shown in Fig. 2. The characteristics shown by the solid curve are the simulation results using the SPICE program [9] with the device parameters which were measured from actual devices fabricated by Si-gate CMOS technology with 3.5 μm design rule. The common-collector characteristic of the LBT may be divided into four regions. In region I, the emitter node voltage V_3 is near V_{DD} (5 V) so that the base-emitter voltage is not enough to turn on Q_2 and the gate–source voltage is small enough to keep the M_1 in the OFF state. Thus the node current I_3 is nearly zero. When the voltage V_3 is decreased below the voltage V_{DD} - $V_{BE,\mathrm{on}}$ but above the peak voltage V_p, as shown in region II of the characteristic in Fig. 2, the BJT Q_2 is operated in its active state and the NMOS M_1 is still off. Therefore the current I_3 can be approximately written as

$$I_3 = (\beta + 1)(V_{DD} - V_{BE,\mathrm{on}} - V_3)/R_1 \tag{1}$$

where β is the current gain of Q_2 and $V_{BE,\mathrm{on}}$ is the base-emitter turn-on voltage. Setting $\beta = 100$ and $V_{BE,\mathrm{on}} = 0.8$ V, the calculated result of (1) is shown to be consistent with the simulated result in Fig. 2. For smaller β, I_3 is decreased.

As the voltage V_3 is further decreased below the peak voltage V_p, the NMOS M_1 is turned on. The voltage V_p is larger than the voltage V_{DD} - V_{TO} due to the positive substrate bias effect [7]–[8]. Moreover, V_p must be smaller than the voltage V_{DD} - $V_{BE,\mathrm{on}}$ in order to turn on Q_2. Thus the threshold voltage V_{TO} of M_1 at zero substrate bias should be higher than a conventional NMOS. In this case, we have V_{TO} = 3 V which can be achieved by introducing another implanting process for threshold voltage adjustment.

As soon as M_1 is turned on, the base–emitter voltage of Q_2 is decreased and its base current is partly bypassed. Therefore the current I_3 is decreased as shown in region III of Fig. 2. Finally, when the node voltage V_3 is decreased to the valley voltage V_V, all the base current is taken out and the base-emitter voltage is $V_{BE,\text{cut-in}}$, the cut-in voltage. Since R_1 is as high as 10 MΩ, the current through the NMOS M_1 is very much smaller than it can conduct. Thus, the valley point is

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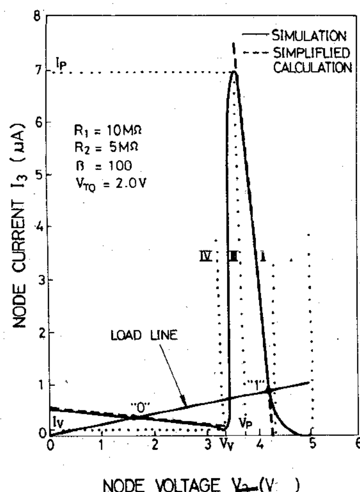

Fig. 2. The current-voltage characteristics of the common-collector lambda bipolar transistor and its load resistor.

near its threshold point and the valley voltage V_V can be expressed similarly as the peak voltage V_p [7], [8]. Further decreasing V_3 quickly decreases the base-emitter voltage to zero and the current I_3 can be written as

$$I_3 = (V_{DD} - V_{BE,\text{cut-in}} - V_3)/R_1 \simeq (V_{DD} - V_3)/R_1. \quad (2)$$

The calculated result of (2) is also shown by the dashed line in region IV of Fig. 2. It agrees with the simulated result.

The load characteristic of R_2 is plotted and the resultant two stable points are indicated. At these points, the voltage at nodes 3 and 2 can be accurately determined from (1) and (2) and expressed as

$$V_2(0) = V_3(0) = V_{DD}/(1 + \gamma) \quad (3)$$

$$V_3(1) = (\beta + 1)(V_{DD} - V_{BE,\text{on}})/(\gamma + \beta + 1) \quad (4)$$

$$V_2(1) = [(\beta + 1) V_{DD} + V_{BE,\text{on}}]/(\gamma + \beta + 1) \quad (5)$$

where γ is the resistance ratio R_1/R_2. The voltages of the two stable points are seen to depend on the resistance ratio of the two poly-Si resistors rather than their resistance magnitudes. Such characteristics guarantee cell stability with large resistance variations in fabricating the poly-Si resistors.

To obtain the bistable characteristic, the load current cannot be larger than the peak current I_p or smaller than the valley current I_V, as may be seen from Fig. 2. This gives the ratio γ a constraint which can be obtained from (1) and (2). For smaller β, I_p is smaller and the permitted range of γ is decreased.

Since the collectors of all LBT's are connected to V_{DD}, no isolation is needed for each BJT. Therefore the packing density of the new cell is mainly determined by two factors. One is the n^+-p^+ contact in the LBT. The other is the p-well–p-well spacing. If the n^+-p^+ contact is directly formed by the silicide [6], the cell area can be decreased considerably. However, this will add extra process complexity to the conventional Si-gate CMOS technology.

The p-well–p-well spacing is related to the bulk latch-up effect. In the new cell, since the large resistors R_1 and R_2 limit the current flow, latch-up due to parasitic p-n-p-n structures within the cell array can be avoided. Being free from the latch-up effect, the p-well–p-well spacing can be reduced.

Based on these considerations, a cell area of $4F \times 8F$ can be realized with a p-well–p-well spacing of $2F$. When the minimum feature size F is 3 μm (2.5 μm), the cell area is 288 μm^2 (200 μm^2) which has been the smallest among the cells reported so far [1]–[6]. The number of contacts per cell is $3\frac{11}{12}$ while the number of interconnection lines per cell is 3.

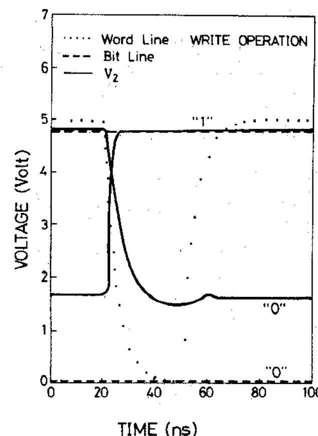

Fig. 3. Simulated WRITE transients of the LBT cell.

To write a binary 1(0), the bit-line voltage is first increased to nearly 5 V (0 V). Then the access PMOSFET in the selected cell is turned on by the word-line negative pulse applied to its gate, and the bit-line voltage charges (discharges) the cell nodes and changes the cell stable point to the desired one. Using the actual device parameters, the write transients of the new cell are simulated by the SPICE program. The results are demonstrated in Fig. 3. Note that the voltage of the low stable state is designed to be equal to the threshold voltage V'_{TP} of the PMOS under substrate bias $V_{DD} - V_2$. Thus, the WRITE 0 operation can be quickly achieved. On the other hand, to avoid the overshooting of the voltage at node 2, which decreases the base current and possibly destroys the cell stability, the bit-line voltage during the WRITE 1 operation is kept at a voltage equal to that of the high stable state.

The bit-line capacitance C_{BL} in the LBT cell is dominated by the capacitance of the p^+-n substrate junction of the access PMOS. Since the n-type substrate impurity concentration is low, such junction capacitance is small. Therefore for a 16 K (64 K) static RAM with 64 (128) cells per line, C_{BL} may be as low as 0.2 (0.4) pF.

To read the cell, which has only one bit line, the bit line voltage should be precharged to some level to prevent the cell from reaching its switching voltage on node 2. Otherwise, destructive read-out is possible. Using the SPICE program with the actual device parameters, the range of the precharged voltage in this cell is determined to be from 2.9 to 3.1 V. Choosing 3 V as the precharged voltage, the simulated read transients are shown in Fig. 4. For C_{BL} = 0.2 pF, the swing of bit-line voltage is nearly 400 mV. For C_{BL} = 0.4 pF, the swing reduces to nearly 200 mV. Note that the increase of bit-line voltage during the READ 1 operation is mainly due to the charging current provided by the node capacitance on cell node 2.

As shown in Fig. 4, the recovery of the binary 1 is rather slow because the charging through the large resistor R_1 and the large forward-junction capacitance C_{BE} to increase the node voltage V_2 is difficult. On the other hand, the recovery of the binary 0 involves only large resistors and thus is a little faster than that of the binary 1. This slow recovery will lead to a large memory cycle time.

The small range of the precharged voltage in the above case may be extended by reducing the disturbance on node 2 of M_3. This is achieved by decreasing the word-line voltage to 2 V rather than 0 V during the selected period. In this case, the simulated range is between 2.5 V and 3.6 V. Taking 3 V as the precharged voltage, the simulated READ transients are shown in Fig. 5. In the READ 0 operation, the access PMOS

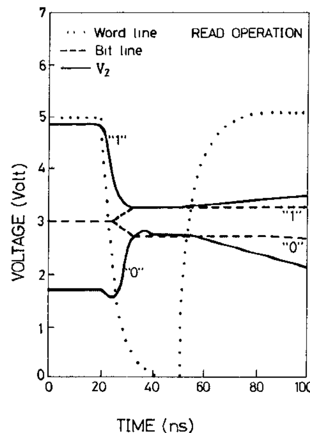

Fig. 4. Simulated READ transients of the LBT cell with word-line voltage down to 0 V.

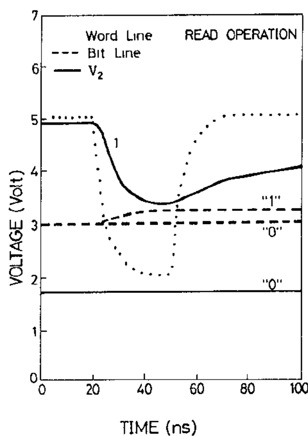

Fig. 5. Simulated read transients of the LBT cell with word-line voltage down to 2 V.

with its gate at 2 V and its source at 3 V cannot be turned on. Thus both the bit-line voltage and the cell node voltage remain unchanged. In the READ 1 operation, the recovery of V_2 is faster than that in Fig. 4 because the voltage V_2 is not as severely lowered as that in Fig. 4.

Although the new cell has the smallest area, its recovery after reading is rather slow. One of the possible ways to solve this problem is to design suitable peripheral circuits which aid the cell to restore its original stored data. Another kind of peripheral circuit is also needed to provide the precharging voltage before reading. With these peripheral circuits, the design of high-density large static RAM's using the proposed new cell may be practicable.

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Frequency Modulation of Gunn Oscillator by Low Magnetic Flux

T. KORYU ISHII

Abstract—It was found that when a low magnetic flux density was applied transversely to a commercial Gunn oscillator under rated bias voltage deep beyond the threshold, the oscillation frequency was modulated. This phenomenon was theoretically explained by employing new concepts of simplified magnetodynamic effect, successive collision effect, and successive collisions with a variable number of collisions.

I. INTRODUCTION

The purpose of this correspondence is to report on the observations and theoretical explanations of oscillation frequency modulation of a Gunn oscillator MA86501 by low magnetic flux. Magnetic effects on the characteristics of various kinds of Gunn diodes have been reported in past literature [1]-[9]. Borodovskii *et al.* [1] reported the reduction of oscillation frequency with increasing dc magnetic flux density on one of their experimental Gunn diodes. They attributed the observed results to both the increase in the device length and the decrease in the drift velocity of the high field domain. Another one of their diodes showed an increase in oscillation frequency with an increasing dc magnetic field. They attributed it to the decrease in device capacitance. Kennedy [2] also reported a decrease in oscillation frequency when a dc magnetic field was applied on his experimental Gunn oscillator. His study was limited within a neighborhood of threshold bias voltage. According to Foyt *et al.* [3], near the threshold the oscillation can be quenched by an application of a dc magnetic field. Decreasing the threshold voltage by a magnetic field was reported by Guetin *et al.* [4]. Contrary observation was reported by Vorobyev [5]. Gunn reported a threshold current is not affected by a moderate magnetic field [6]. There are many works published about magnetic effects on a high field domain near the threshold [7]-[9]; but to the author's knowledge, none of the published works involves investigation at the nominal rated working bias voltage which

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The author is with the Department of Electrical Engineering and Computer Science, Marquette University, Milwaukee, WI 53233.

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