experimentally by the results described in the section "Current-voltage characteristics" (Fig. 4).

Following the law of conservation of energy, the order of magnitude of the fluid flow velocity can be estimated by equating the electrostatic energy and the kinetic energy of the fluid, which yields

$$v \approx \frac{\overline{U}}{d} \cdot \sqrt{\frac{\epsilon\epsilon_0}{\rho}} \quad [8]$$

With the experimental value of the threshold voltage of convection of about 3V and a span of the oxidation and reduction potential of 2.5V, approximatively, one obtains $\overline{U} = 0.5V$. For an electrode spacing of 50 μm, a solvent density of $\rho = 1$ g/cm^3, and a dielectric constant of $\epsilon = 3.5$, the averaged flow velocity should be of the order of 0.2 cm/sec just above the onset of convection. Equation [8] shows that the velocity has to increase linearly with increasing voltage beyond that point, which is in agreement with the linear increase of the current in the convection region. Accordingly, the interpretation of the experimental results, described in Fig. 3a, leads to the conclusion that the overall degree of ionization of the rubrene solution should be constant in the linear range of the current/voltage curve. The degree of ionization can be estimated under these conditions. With $d = 60$ μm, $\bar{i}(3V) = 0.1$ mA/cm^2 or $\bar{i}(5V) = 0.6$ mA/cm^2 one obtains $v(3V) = 0.16$ cm/sec, $v(5V) = 0.78$ cm/sec, respectively, and the degree of ionization, β, is then ($C = 4 \cdot 10^{-6}$ mol/cm^3)

$$\beta = \frac{\bar{i}}{z\mathbf{F} \cdot C \cdot v} \approx 1.5\%$$

This rather low value of β must not be considered to be the absolute fraction of rubrene radical ions in the solution in any case; it indicates, however, the fraction of rubrene molecules that is active in charge transport during electrohydrodynamic convection flow in the thin-layer cells.

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Post-Epitaxial Polysilicon and Si_3N_4 Gettering in Silicon

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ABSTRACT

Substantial improvement of the quality of silicon epitaxial films by post-epitaxial polysilicon back-side gettering has been observed. This improvement is displayed by the reduction of defect counts revealed by the Wright etch and anodic etch and the increase of carrier lifetime characterized by the improved MOS retention time. Correlation between the defect etch pit counts and the retention time of MOS devices fabricated is reported.

High quality epitaxial (epi) films are essential for achieving high yields in semiconductor devices and integrated circuit processing. Various gettering schemes have been proposed (1-5) to insure a sufficiently high quality of substrates and films. Most of these gettering procedures share a common feature, that is, they all aim at creating a form of strain and/or lattice disorder to the backsurface of substrate wafers

* Electrochemical Society Active Member.
Key words: MOS retention time, defects.

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that is followed by annealing at an elevated temperature. It is generally understood that gettering implies that defects and impurities move and are trapped at these back-side treated regions and are prevented from further movement to front surfaces. Previous investigations have shown that deep level impurities near the surface can reduce MOS retention time.

There are several methods of characterizing the effectiveness of gettering in silicon epitaxial films. The simplest of these include decoration with chemical preferential etches such as Wright etch (6) and anodic etch techniques (7). The chemical preferential etches decorate surface as well as bulk defects existing in the material, most notably epitaxial stacking faults (SF_{epi}), oxidation stacking faults (OSF), hillocks, and slip lines. The etched decorations can be observed using an optical microscope with Nomarski interference attachments. The anodic etch decorates selectively the electrically active defects from among the above. Although defect decoration techniques are good indicators of gettering effectiveness, the most sensitive test of silicon quality improvement is MOS retention time. We therefore measured capacitors formed on the epi films in both gettered and ungettered regions to evaluate improvement and compare results (8).

This study has examined the effectiveness of polysilicon, Si_3N_4, and combinations of polysilicon/Si_3N_4 as getterers when used as a post-epitaxial procedure to reduce defects already introduced in the epi films through inadequate pre-epitaxial surface cleaning. Observations were made on the gettered samples of defect counts in device areas using the etching techniques and these results were correlated with the MOS retention time measurements.

Experimental

The epi films were deposited by the hydrogen reduction of silicon tetrachloride ($SiCl_4$) at 1050°C in an AMC-1200 reactor. The depositions were made on Si wafers following procedures known to produce film defects at levels greatly above normal in epitaxial films, *i.e.*, poor pre-cleaning, rinsing, and drying. Both n^+ and p^- <100> oriented, 5.7 cm diam, 0.038 cm thick, silicon substrates were employed. The epitaxial films were from 1.3 to 3.9 μm thick. Only n-type epitaxial films were deposited using AsH_3 as a dopant source. The resistivities of the films ranged within 0.2-2.0 Ω-cm. Samples that were examined for defects were first given a 10 sec BHF etch followed by a Wright etch of from 40 to 120 sec. Electrically active defects in the epitaxial films were decorated using anodic etch techniques previously described (5). The typical voltage used for the present experiments was 3V bias in a 5% HF electrolyte. Gettering films were deposited on the back-side of substrate wafers. Anneals followed the back-side gettering treatments. The annealing consisted of 5 min at 1000°C in O_2 and 25 min in N_2. In these experiments the gettering treatments were applied to selected sectors on the back-sides leaving one area in an ungettered form for comparison purposes (Fig. 1). The details on these gettering films are given below.

Polysilicon; polysilicon/Si_3N_4; Si_3N_4 gettering films.—A polycrystalline silicon layer of 500 nm thick was deposited on one-half of the wafer back-side by chemical vapor deposition at 650°C employing a mechanical mask. This was followed by a deposition of an Si_3N_4 film at 700°C also in a half-wafer fashion. For this second deposition of Si_3N_4, the mask was rotated 90° such that the Si_3N_4 edge was perpendicular to the previously formed polysilicon/silicon boundary. This resulted finally in a quartered wafer as shown in Fig. 1 labeled to indicate the back-side gettering films present for each sector. Following the routine anneals a 500Å SiO_2 layer was thermally grown on the epitaxial film using a dry oxygen atmosphere at 1000°C. MOS structures were completed on this oxide by forming Al gate electrodes. Wafers having no epi were included as controls.

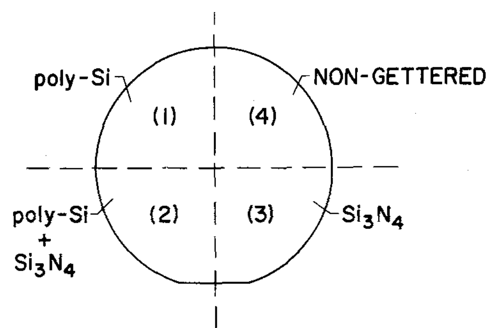

Fig. 1. Designation of back-side gettering treatments according to sectors (front-side view of wafer).

Results and Discussion

Surface morphology by Wright etch and anodic etch.—In nongettered wafers, hazy patterns as shown in Fig. 2 were always clearly visible by reflected light when epi films were treated with Wright etch (Fig. 2a) or anodic etch (Fig. 2b). These hazy surfaces were found both with or without a high temperature steam oxidation. The hazy regions in Fig. 2 are found to consist of high density aggregations (up to 10^7 cm^{-2}) of hillock-type etch pits shown in Fig. 3 at high magnification. These same hazy regions as developed from anodic etch exhibit high density aggregations (up to 10^6 cm^{-2}) of anodic etching artifacts of varying size as

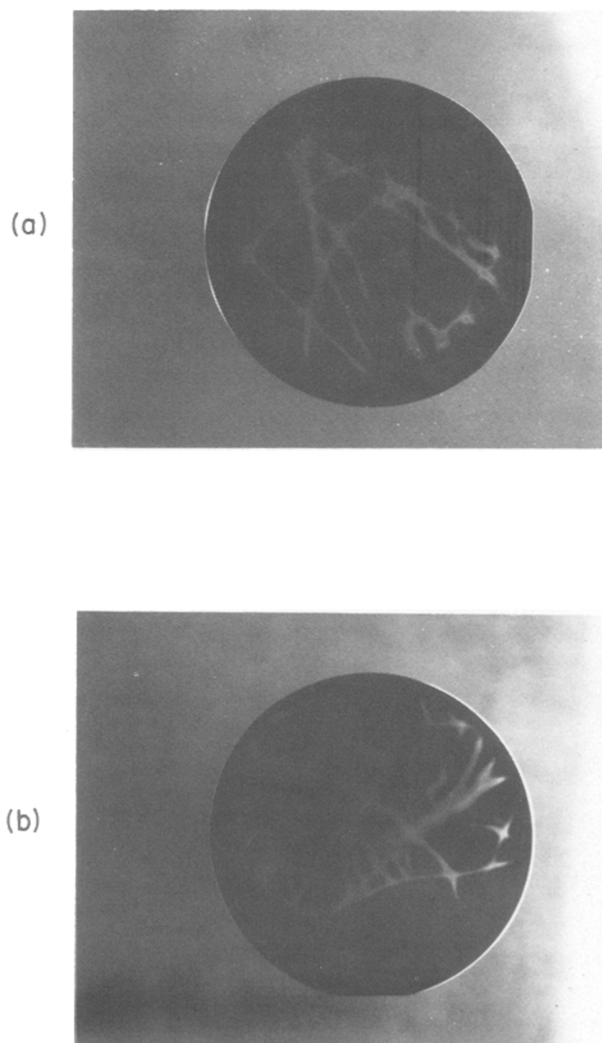

Fig. 2. Hazy patterns observed on the surface of epi wafers following Wright etch (a) or anodic etch (b).

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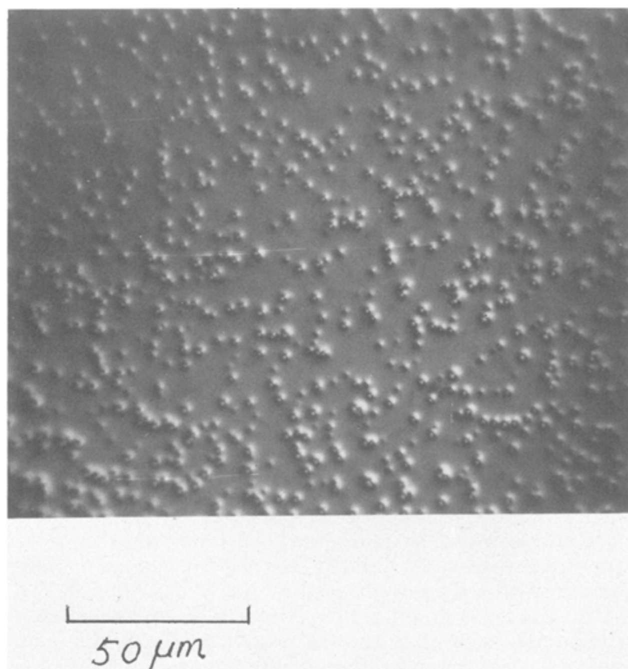

Fig. 3. Hillocks-type etch pits within the hazy region (Fig. 2a) after Wright etch for 40 sec shown at higher magnification.

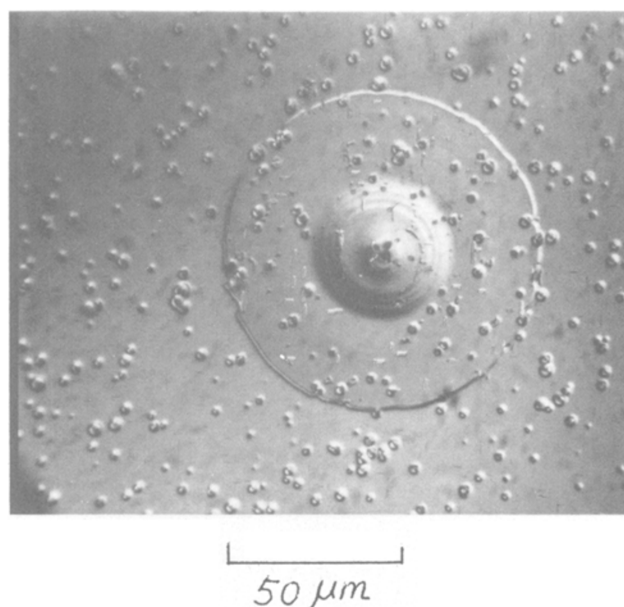

Fig. 5. Characteristic anodic etching artifacts on the surface of n/p^- epi wafer within the hazy regions (similar to Fig. 2b) after 2 min anodic exposure (3V bias in 5% HF).

shown in Fig. 4 and 5. Similar hazy regions after high temperature steam oxidation treatments plus Wright etch display local clusters of high density aggregation (up to 10^7 cm^{-2}) of either solely oxidation induced stacking faults (OSF) (Fig. 6a) or a mixture of OSF and hillocks as shown in Fig. 6b.

Figure 7 shows some typical anodic currents generated during the anodic etching process for two n-type epitaxial films of differing thickness on n^+ substrates (n/n^+) and n-type epi on p-type substrates (n/p). The epi surface exposed to the anodic etch included a circular area of approximately 5 cm in diameter. The higher current initially observed in Fig. 7 is due to the presence of surface defects. For the n/p wafers the current stabilizes and remains at a level of 10-15 mA. For the n/n^+ wafers, there is a rapid current increase following the initial current decay resulting from etch "punch through" to the n^+ substrate. The anodic decorations were examined using a Nomarski interference microscope and typical examples are shown in Fig. 4 and 5. Figure 4 shows the typical anodic etching artifacts on the surface of n/n^+ epi wafers located within a high haze region and is shown following 30 sec of anodic etch treatment. Figure 5 shows a typical anodic etching artifact observed on the surface of n/p wafer located within a dense haze area shown after 2 min of anodic etch. In addition to the smaller artifact collections that are found in the hazy regions, some totally different anodic artifacts are also found scattered on the wafer overall. The density of the largest artifacts shown in the figure also varies, but they are typically less than 100 cm^{-2}. A small square-shaped structure can usually be observed at the center of the very largest anodic decorations. These defects are always electrically active and arise from epitaxial stacking faults. The stacking fault defects can be present both with or without oxidation treatments.

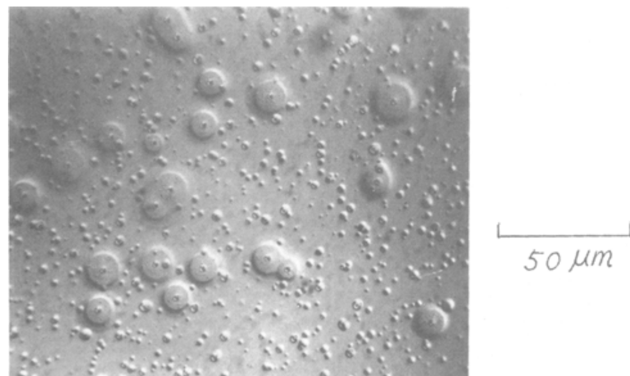

Fig. 4. Representative anodic etch artifacts at higher magnification on the surface of n/n^+ epi wafer within the hazy regions (as in Fig. 2b) after 30 sec anodic exposure (3V bias in 5% HF).

Polysilicon back-side deposition and annealing was found to be an effective gettering technique. Figure 8 shows three consecutive microphotographs covering the boundary region between the nongettered and gettered wafer sectors. It should be noted that the reduction in hillock density is gradual across this boundary occurring over approximately 500 μm. The gradual reduction in hillock density observed is believed to result from the silicon wafer mask overlay employed for forming gettered structures. Deposition of polysilicon has been observed to occur in a graded fashion beneath such a mask and gettering effectiveness is probably tied to the thickness of the polysilicon occurring over this 0.5 mm gradation.

Figure 9 shows a wafer back-side gettered in the manner of Fig. 1 photographed tilted under overhead light. A clear demarkation between nongettered and gettered sides can be observed by the sharp disappearance of the haze pattern in the gettered sections when properly tilted, Fig. 9a. The less effective gettering in the Si_3N_4 sector is also obvious in Fig. 9b where the same wafer is tilted in a slightly different way.

MOS retention time.—The quality of silicon can be characterized by the measurement of the minority carrier lifetime. The lifetime value reflects the amount of impurity centers and crystalline imperfections existing in the crystalline material. The transient response of MOS capacitors was used to measure the lifetime of carriers (9) in these studies. The method consists of measuring the MOS capacitance as a function of time by driving the device from accumulation into deep depletion and observing the decay back into inversion. The recovery time T_R from the deep depletion state to the inversion state and the lifetime τ can be approximated by the relation (10)

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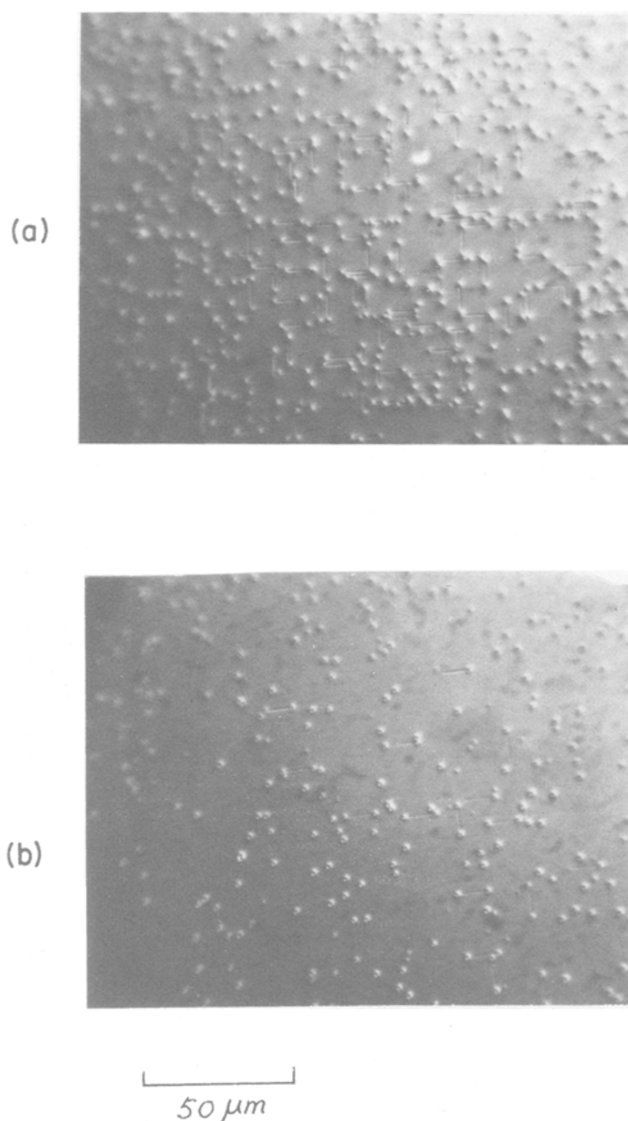

Fig. 6. Representative oxidation-induced stacking faults and hillocks-type etch pits within the hazy region of wafers of the type in Fig. 2 after 40 sec Wright etch. The epi wafer had undergone 1100°C steam oxidation for 1 hr.

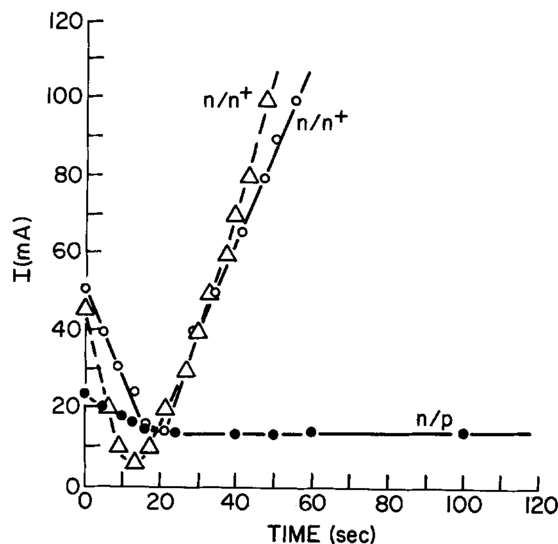

Fig. 7. Typical anodic current as a function of time plotted during the anodic etching process. The epi surface exposed to the anodic etch is a circular area of 5 cm diam.

$$\tau = \frac{n_i}{8N_d}\frac{C_f}{C_o}\left(1 + \frac{C_i}{C_f}\right)T_R$$

where n_i is the intrinsic carrier concentration, N_d is the substrate concentration, C_o is the oxide capacitance, C_i is the initial deep depletion capacitance, and C_f is the final strong inversion capacitance. The gettering effects for the various treatments were made on both the epi wafers treated as in Fig. 1 and control wafers. The controls were n-type silicon wafers having no epi films. The MOS results for both follows below.

Typical results of MOS retention time measurements for samples gettered as shown in Fig. 1 are summarized in Table I and II. Table I shows the measured retention times of a poly-Si gettered epitaxial wafer. Similarly, Table II summarizes the retention time data of the gettered control wafers having no epi film. The overall average retention is consistently lower for all sectors in the control. This is believed to be due to process differences experienced by control and gettered samples which can result in an overall difference sample to sample. However, the improvement between gettered and nongettered regions is obvious. In the gettered wafers, the T_r values overall are significantly higher in all quadrants. In general, both these sample types contained initially a large number of microdefects overall. This is reflected in the results which show a large number of devices with a very short retention time (*e.g.*, retention time less than 1 sec). If one starts out with a high defect count in the films, it appears that even in the most effectively gettered region, region 2, approximately 23% of the devices still fail to show a measurable retention time ≥ 1 sec (Table I).

It has been reported previously that silicon nitride back-side gettering is most effective employing 4000Å of Si_3N_4 (11). In the present work, it is also apparent that a moderate improvement of retention time was

Table I. MOS retention time (T_R) data of poly-Si gettered epi wafers

Areas	(1)	(2)	(3)	(4)
Gettering arrangement	Poly-Si	Poly-Si plus Si_3N_4 (700Å)	Si_3N_4 (700Å)	None
Total No. of devices measured	69	47	48	55
Yield:* $T_R \geq 1$ sec	62.3%	76.6%	35.4%	23.6%
$T_R \geq 5$ sec	53.6%	72.3%	22.9%	12.7%
$T_R \geq 10$ sec	49.3%	68.1%	20.8%	7.3%
$T_R \geq 60$ sec	30.4%	51.1%	12.5%	1.8%
$T_R \geq 100$ sec	5.8%	29.8%	0	0
$T_R \geq 140$ sec	0	10.6%	0	0
Average T_R (sec), all measured devices	33.0	61.6	10.6	3.8
Devices with $T_R \geq 1$ sec only	52.9	80.4	30.7	15.8

* Yield means percentage of total number of measured devices with retention time $T_R \geq t$ sec.

Table II. MOS retention time (T_R) data of poly-Si gettered control wafer

Areas	(1)	(2)	(3)	(4)
Gettering arrangement	Poly-Si	Poly-Si plus Si_3N_4 (700Å)	Si_3N_4 (700Å)	None
Total No. of devices measured	29	26	29	26
Yield: $T_R \geq 1$ sec	100%	93.1%	88.5%	76.9%
$T_R \geq 5$ sec	100%	50.0%	62.1%	34.6%
$T_R \geq 10$ sec	100%	7.7%	41.4%	3.8%
$T_R \geq 15$ sec	100%	0	20.7%	0
$T_R \geq 20$ sec	93.1%	0	13.8%	0
$T_R \geq 30$ sec	82.8%	0	6.9%	0
$T_R \geq 40$ sec	41.4%	0	0	0
$T_R \geq 50$ sec	3.5%	0	0	0
Average T_R (sec)	35.7	4.3	9.7	3.6

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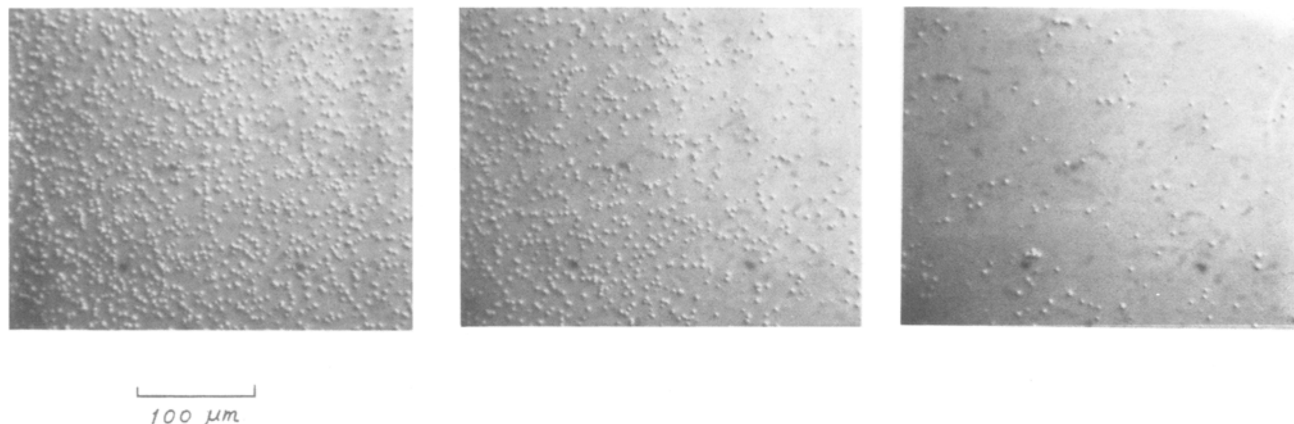

Fig. 8. Three consecutive microphotographs taken crossing the boundary between the poly-Si gettered region (on the right) and the non-gettered region (on the left).

achieved with even a thin (700Å) Si_3N_4 film (area 3, Table I). Based on the earlier work (11) thicker films would seem in order for epi films to achieve better gettering. In other studies (5) however, we observed severe wafer warpage on 57 mm diam wafers (0.038 cm thick) when 5000Å of Si_3N_4 was used as a getterer. This warpage observed in our work seemed implicated in reducing the total effectiveness of this gettering technique compared to other pre-epi techniques ($POCl_3$ and Ar I/I) at this 5000Å Si_3N_4 thickness.

Correlation between etch pits and MOS retention time.—Improvement of MOS retention time and reduction of hillock-type etch pit defects has been observed on the gettered parts of wafers. To investigate the relationship more closely, the individual MOS device areas were marked using reactive ion etching employing the Al contact as the mask for the dry etch as described in earlier work (5). The aluminum and underlying MOS oxide were then stripped, and the samples were Wright etched to delineate the etch pits in the active device area. Primarily hillock-type defects were exposed by the Wright etch. Figures 10a and b plot the relation of MOS retention time and the number of hillocks counted in the defined 32 mil diam MOS device dot areas. The data have been plotted on both a linear (Fig. 10a) and log scale (Fig. 10b). The counts included all etch pits that were observable by the Nomarski-interference microscope. The data show a somewhat scattered but consistent distribution. A practically hillock-free or etch pit-free region is required for retention time to achieve values of 30 sec (Fig. 10a), which in this study corresponds to approximately a 10 μsec carrier generation lifetime.

Anodic etching was also done on a few samples following MOS retention time measurements. With the aluminum and oxide stripped, the epi wafer was anodically etched using a 2V bias for 1 min to decorate the electrically active defects. The anodic etching was confined to essentially the upper half of a wafer as shown in Fig. 11. The presence of anodic defects were then assessed for each individual device region. The results are mapped on Fig. 11. The numbers given at

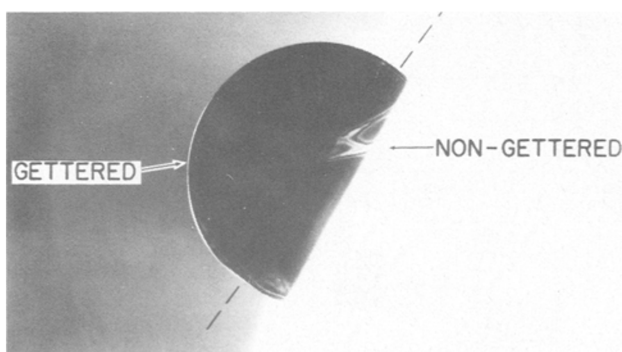

Fig. 9a. Photo indicating the effectiveness of gettering as viewed with overhead reflected light showing the abrupt change in haze for gettered and nongettered regions.

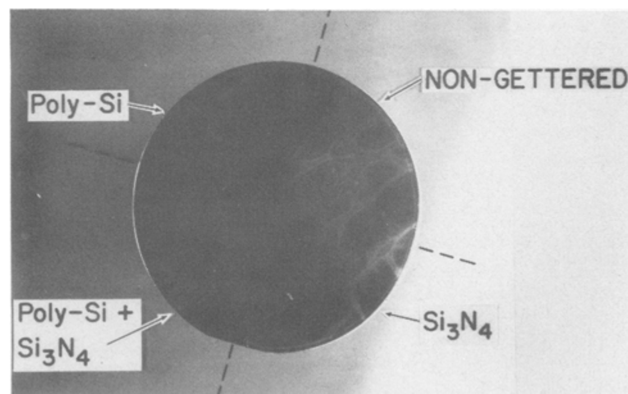

Fig. 9b. Sample in Fig. 9a tilted differently to show degree of haze disappearance in gettered regions.

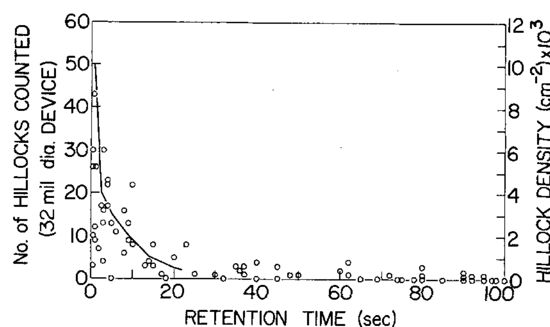

Fig. 10a. Hillock counts vs. retention time (linear plot)

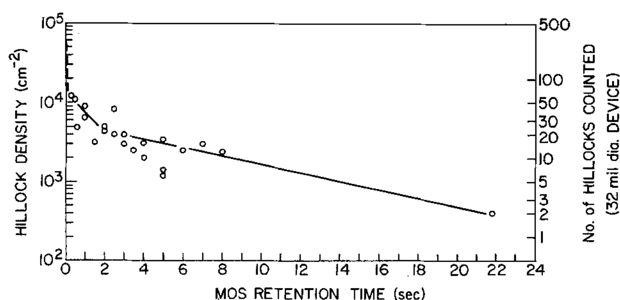

Fig. 10b. Hillock counts vs. retention time (log plot)

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Fig. 11.

each device location (square) in Fig. 11 represent the measured retention time in seconds observed previously at that site. A circled number indicates that no anodic artifacts could be observed at that specific device location. A noncircled retention time value in the figure indicates that at least one or more anodic artifacts were observed in the device region. The analysis shows that the existence of even a single electrically active defect can significantly reduce the MOS retention time irrespective of size. The data also show, however, that a "no artifact decoration observation" using anodic etch does not necessarily insure a high retention time will be obtained.

Conclusions

Polysilicon, polysilicon/Si_3N_4, and Si_3N_4 wafer back-side gettering were employed in a post-epi mode. The chemical preferential Wright etch and anodic etching technique were used to expose defects. MOS retention time measurements were made to evaluate the overall quality improvement of the epitaxial films. The films had high starting densities of hillock-type defects (up to 10^7 cm^{-2}) that could be easily observed by the Wright etch and anodic etching. High densities of OSF nucleation sites could be induced in such films following high temperature steam oxidation. As a result of these high densities, the majority of devices were found to exhibit very low retention times. Differences in the retention time and reduction of defect densities could be observed on the gettered regions even on these initially high background defect films. All gettering techniques tested yielded some improvements of the epi film quality. A correlation between the MOS retention time and the number of hillocks counted within the MOS device showed that for the retention time to be better than 30 sec, a practically hillock-free device is required. Further, the studies have shown that electrically active defects are significantly implicated in reducing the retention times.

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