國 立 交 通 大 學

電子物理研究所碩士班

碩 士 論 文

鎳金屬誘發側向結晶垂直通道
低溫複晶矽薄膜電晶體之研究

**The Study of Vertical Channel LTPS TFTs with
Metal-Induced Lateral Crystallization Method**

研 究 生：郭 柔 含

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鎳金屬誘發側向結晶垂直通道低溫複晶矽薄膜電晶體之研究

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摘要

多晶矽薄膜電晶體擁有較高的載子遷移率，被認為可廣泛應用於主動矩陣式液晶顯示器的主動開關元件上。為了提升元件特性，元件的通道長度的微縮是有必要的。然而，垂直通道結構的複晶矽薄膜電晶體的通道長度是以沉積的閘極厚度所決定，並不受微影機台的限制，因此具有高度的發展潛力可應用於三維垂直整合。但過多的晶粒界面及缺陷存在於通道中將大幅地劣化多晶矽薄膜電晶體的特性。

在本論文中，我們利用了金屬誘發側向結晶的方式製作垂直通道的多晶矽薄膜電晶體，其製程簡單，並不需要額外的光罩並與 CMOS 製程有高度相容性，且其具有等效的雙閘極結構，能有效地抑制汲極端的電場以降低漏電流並提升開關電流比。

本研究提出利用氨電漿處理及結晶過濾效應可有效地提升元件特性。研究中發現，較窄的結晶通道寬度具有較佳的結晶特性及較少的晶界缺陷，因此我們可利用較窄的結晶過濾寬度來有效地提升元件特性。此外，我們也比較了以鎳金屬誘發側向結晶及鎳金屬矽化物誘發側向結晶的差別。由結果顯示，兩種方式並沒有太大的差異。推論由鎳金屬矽化物誘發側向結晶的方式無法有效地進一步降低在通道中的鎳金屬含量。但藉由結晶過濾效應，兩種結晶方式都可利用通道個數的增加來提升元件的開關電路比，且並不影響其他電性表現。

The Study of Vertical Channel LTPS TFTs with Metal-Induced Lateral Crystallization Method

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Abstract

Polycrystalline silicon thin-film transistors (poly-Si TFTs) have attracted considerable attention because of its application in active matrix liquid crystal displays (AMLCDs), due to their higher mobility than amorphous silicon (a-Si) TFTs. There is a need to scale down poly-Si TFTs' channel length to achieve higher speeds and packing densities. Therefore, vertical-channel thin-film transistors (VTFTs) have been widely researched and developed to overcome the limits of photolithography. VTFTs have shown great potential for 3-D integration since the channel lengths are determined by the thicknesses of the poly-Si or SiO_2 film, instead of photolithographic process limitations.

In this thesis, we have fabricated the VTFTs with MILC technology. They are simple in structure and fabrication of VTFTs without any additional mask and compatible with the silicon technology. Moreover, VTFT structure which has the inherently own an effective dual-gate structure. And it can reduce the peak lateral electrical field in the drain depletion region, significantly reducing the leakage current and increasing the I_{on}/I_{off} current ratio.

We have proposed that the NH_3 plasma treatment and crystal filtering effect can improve the electrical performance of VTFTs. In our research indicates that the narrower channel width has the better the electrical performance and less intra-grain defects and grain boundary. Thus, the high performance VTFTs can be achieved by

reducing the channel width. Compare MILC-VTFTs with NSILC-VTFTs, we can observe that the electrical performance of them seems to be no significantly difference. The method of NSILC is not able to reduce the Ni and NiSi$_2$ efficient and further improve the device characteristics. Both the MILC-VTFTs and NSILC-VTFTs can be improved the crystal filtering effect and multiple channel structure.

最後，由衷地感謝我的家人。謝謝爸媽總不辭辛勞地教導養育我長大，所有的成就都是你們賜與我的；謝謝哥哥及弟弟在生活上的扶持，你們是我最堅強的後盾。希望這小小的成就可以帶給你們小小的驕傲！

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Chapter 1

Introduction

Low-temperature polycrystalline silicon (LTPS) thin-film-transistors (TFTs) have attracted considerable interest due to their wide applications in active matrix liquid crystal displays (AMLCDs) [1]-[3], driving circuit of system-on-panel (SOP) [4]-[5], nonvolatile memory, image sensors, photo-detector amplifier, and 3-D circuit integration [6], because they provide good electrical properties and can be integrated in peripheral circuits on inexpensive glass substrates. Among these applications, the application in the AMLCD was the major driving force to promote the developments of poly-Si TFTs technology. Therefore, how to improve the performance of LTPS TFTs is an interesting and important issue.

1.1 Overview of Poly-Si Thin-Film-Transistors

Thin film transistor (TFT) is one of the field-effect transistors, which is composed of three terminals including a gate, a source and a drain as shown in Fig. 1-1. The transistor may conduct current between the source and drain if a channel of carrier is created by making the gate voltage (V_G) sufficiently large. Thus, the magnitude of the current can be controlled by the gate voltage. Take n-type transistor for example. When the V_G becomes sufficiently positive, free electrons are attracted to the oxide/ Si interface, forming the conductive channel. We say the transistor is on. The gate potential at which the channel begins to appear is called the "threshold voltage" V_t. If the $V_G < V_t$, no channel exist, the device is off.

The TFT employ a thin semiconductor film on an insulating substrate as the active device channel. And the TFT was first demonstrated in 1961 by Dr. P. K. Wedsnimer.

With its simplicity in structure and fabrication, the applications of TFTs are becoming more and more popular.

In the beginning, the a-Si:H (hydrogenated amorphous silicon) TFTs were applied as the pixel switching device in the AMLCDs. The major advantage of a-Si TFTs is appropriate for large area glass substrate with the lower processing temperature (T < 350 ^{o}C). However, the application of a-Si TFTs is constrained in the aspect of pixel switching elements. Hence, it is difficult to integrate pixel switching elements and peripheral driving circuits on the same glass substrate for system-on-panel due to the low carrier field-effect mobility (below 1 cm^2/V-s generally) of the a-Si:H TFTs. In order to acquire devices suitable for system-on-panel, it is necessary to fabricate the devices with low cost, high electrical properties and reliability by low temperature process.

Since the first poly-Si TFTs were fabricated by Fa et al in 1966 [7], the electrical properties, conduction mechanism and fabrication process of poly-Si films were extensively studied [8]-[9]. Over the past three decades, poly-Si TFTs have been drawn much attention thanks to the fact that they can be fabricated with a low thermal budget and on large area substrates while achieving performances adequate for the realization of complex circuit. For this reason, they have many commercial applications.

Recently, poly-Si has been proposed as a very attractive alternative material for the AMLCDs because of their superior performance [10]-[12]. The mobility of poly-Si can reach 10 to 300 cm^2 /V-s, so the devices with considerable high driving current can be integrated of peripheral circuit on the same panel in AMLCDs [13]. However, the conduction mechanism and performance of poly-Si TFTs are strongly influenced by grain boundaries and intra-grain defects. The defects in the grain boundary would trap carriers and build a potential barrier which degrades the on-state current and subthreshold swing (S.S.). Moreover, the grain boundary also provides the path of

leakage current.

In order to enhance the performance of the poly-Si TFTs, several methods have been proposed to improve the device performance such as enlarging the grain size of poly-Si films and reducing the trap-state densities in the grain boundaries. It has been reported that the a-Si films can be crystallized by many techniques, such as Solid-Phase Crystallization (SPC) [13]-[15], Excimer Laser Crystallization (ELC) [16]-[17] and Metal-Induced Lateral Crystallization (MILC) [18]-[20] to obtain the large grain size of poly-Si to raise the field-effect mobility. Besides, there were other methods such as plasma treatment to passivate the defects in the channel or narrowing the channel width to reduce the trap state density. These techniques are described as follow.

1.1.1 Solid-Phase Crystallization (SPC)

The a-Si film was deposited at temperature below 600 ^{o}C, so the film was required thermal energy to convert amorphous silicon into the polycrystalline form. This method is called Solid-Phase Crystallization (SPC). The SPC technique is usually performed at 600 ^{o}C for 24~72 hours. The SPC method has many advantages, such as simplicity, low-cost batch process, and compatible with the silicon technology, large area capability, and smoother surface. However, such crystallized poly-Si films have high density of grain-boundary defects and intra-grain defects, which degrade the electrical properties of poly-Si TFTs. But the high crystallization temperature around 600 ^{o}C prevents SPC from commercial application. Because the maximum process temperature of the inexpensive glass substrate is limited to less than 600 ^{o}C. If temperature up to 600 ^{o}C, the substrate might be bending, it would affect the following process of fabrication.

1.1.2 Excimer Laser Crystallization (ELC)

Excimer Laser Crystallization (ELC) has investigated as an alternative crystallization technique to furnace annealing. And the standard gas mixtures and output wavelengths are ArF (193 nm), KrF (248 nm) and XeCl (308 nm). For fabricating high performance poly-Si TFTs on a glass substrate, Excimer Laser Crystallization method is very promising for the following reasons. First of all, the combination of strong optical absorption of the UV light in silicon ($\alpha > 10^6 \, \text{cm}^{-1}$) and small heat diffusion length (~100 nm) during the laser pulse (10 ns~30 ns) implies that high temperature can be produced in the silicon surface region. Therefore, we can obtain higher quality poly-Si film without damage of the glass substrate by serious thermal shrinkage. Second, it can crystallize the film selectively by partially irradiating the film surface, so both poly-Si TFTs and a-Si TFTs can be formed on the same substrate. Third, the throughput of the ELC process is higher than that of the SPC process and the large grain size translates to fewer defects.

However, there are many problems need to be resolved to obtain a mature ELC poly-Si TFT technology, such as high manufacturing cost, high process complexity, narrow laser process window, the roughness and uniformity of poly-Si films, and stability of electric performances.

1.1.3 Metal-Induced Lateral Crystallization (MILC)

There are many researches show that: the crystallization temperature of a-Si can be lowered by the addition some certain metal. The lower energy barrier of recrystallization was resulting from the reaction between the free electrons of metal and covalent of Si-Si bonds at the interface when the silicide is moving. This phenomenon is called "metal-induced crystallization (MIC)". And the various metals can be classified into two groups. One is silicide-forming metals such as Pd, Ti, Ni, and Cu [21]-[25]. The metal on the a-Si films are forming the crystalline metal silicide,

4

which acts as a heterogeneous nucleation site for Si crystallization. And the other is eutectic-forming metals such as Ag, Au, Al etc [26]-[29]. The metals could increase Si atomic mobility by forming interstitials which change the Si-Si bonding nature from covalent to metallic [30]-[31], or to form low temperature eutectic [32] or metal stable silicide compounds [33]-[35].

But this phenomenon has not been applicable to the fabrication of TFT's because of the grain size of poly-Si is small, and metal contamination into the crystallized Si films. These disadvantages of MIC might degrade the field-effect mobility and leakage current of poly-Si TFTs. Subsequently, metal-induced lateral crystallization (MILC) has been proposed as an alternative crystallization technique to MIC.

Take Nickel for example. When a Ni film is deposited on the a-Si film and annealed, the interaction follows two steps: first step is Ni_2Si to $NiSi$ and second step is $NiSi$ to $NiSi_2$. The $NiSi_2$ precipitates acts as a good nucleus of Si, which has similar crystalline structure (the fluorite type) and a small lattice mismatch of 0.4% with Si, which is shown in Fig. 1-2.

MILC is a silicide-mediated phase transformation process in which a tiny nodule of $NiSi_2$ exists between a crystallized silicon (c-Si) region and an a-Si region. The metal/silicon diffusion leads to the successive formation of the silicides, starting from the metal-rich to end up to the silicon-rich silicide. Fig. 1-3 shows that the Molar free-energy curves which is drawn for a-Si, c-Si, and $NiSi_2$. The driving force for the phase transformation is the reduction in free energy associated with the transformation of metastable a-Si to stable c-Si. The chemical potential of the Ni atoms is lower at the $NiSi_2$/a-Si interface, whereas the chemical potential of the Si atoms is lower at the $NiSi_2$/c-Si interface. There is a driving force for the forward diffusion of Ni atoms through the $NiSi_2$ and a driving force for the diffusion of Si atoms in the reverse direction through the $NiSi_2$. Hayzelden *et al*. proposed that "nodules" of $NiSi_2$ in an

a-Si host first initiated crystallization of Si on {111} faces of the nodule. They

observed that decomposition of $NiSi_2$ at the c-Si/$NiSi_2$ interface and Ni diffuses into

the a-Si from the precipitate, forming new $NiSi_2$ at the $NiSi_2$ /a-Si interface due to its

ability to lower the Ni atom chemical potential. Diffusion of Ni through $NiSi_2$ will

continue to occur dissociatively leaving epitaxial c-Si at the rear of the precipitate. This

transportation of Ni through the nodules resulted in the movement of the nodules away

from the crystallized Si region [36]. The growth mechanism of Ni-induced lateral

crystallization is shown in Fig. 1-4.

1.2 Overview of Vertical Channel Thin-Film-Transistors

Polycrystalline silicon (poly-Si) thin-film transistors (TFTs) have attracted much

attention because of its wide range of application in electronics, such as in the active

matrix liquid crystal display, organic light-emitting displays, due to their higher

mobility and lower threshold voltage than amorphous silicon (a-Si) TFTs. For further

system-on-panel and 3-D circuit applications with multi-function circuit and system

integration, there is a need to scale down poly-Si TFTs' channel length to achieve

higher speeds and packing densities. However, it is difficult to reduce channel length

due to the limits of photolithography resolution. Therefore, vertical-channel thin-film

transistors (VTFTs) have been widely researched and developed to overcome the limits

of photolithography. In these previous studies, VTFTs have shown great potential

VTFTs have shown great potential for 3-D integration since the channel lengths are

determined by the thicknesses of the poly-Si or SiO_2 film, instead of photolithographic

process limitations for 3-D integration since the channel lengths are determined by the

thicknesses of the poly-Si or SiO_2 film, instead of photolithographic process limitations

[37]-[39]. However, these works using asymmetric source/drain (S/D) have

encountered circuit design difficulties. S/D parasitic series resistance and contact

resistance remain problems for device scaling and reduce device performance.

Moreover, the performance of conventional top-gate poly-Si TFTs are not good enough in terms of speed and current drive capability, and the large leakage current of poly-Si TFTs is still a serious problem that leads to poor switching characteristics. The leakage current, which is caused by the high electric field in the drain region, is relatively large in short channel devices. To reduce the leakage current, many methods have been proposed to reduce the drain electric field, such as offset-gated, filed-induced drain, lightly doped drain (LDD) structure, high-k spacer and Si/Ge T-Gate structure [40]-[44]. But these structures need additional lithography process or other materials which makes the fabrication for the device rather complicated and difficult. VTFT structure which has the inherently own an effective dual gate structure. And the offset region was constructed by self-aligned oxide overetching without any additional photolithographic step and the fabricated device exhibited submicron device characteristics.

1.3 Motivation

Metal-induced lateral crystallization process has been introduced by which the a-Si thin films could be crystallized at a low temperature of below 500 ^{o}C. However, the applications of Ni-mediated lateral crystallization of a-Si to poly-Si TFTs have a critical issue because the leakage current are mostly high [45]. The Ni defects induced leakage current is directly related to the lateral electrical field in the drain region in the off-state [46]. Much research related to overcoming the problems in MILC poly-Si TFTs has been carried out, and the general consensus is that the presence of Ni-silicide in the channel region is the cause of these problems. Several methods have been proposed to reduce the amount of undesired metal impurity [47]-[49]. However, these methods are complicated and need of extra process.

Accordingly, we propose a more simple method to reduce the Ni silicide contamination in the MILC region and expect the applicability of the method to fabricate poly-Si TFTs with high performance.

In this thesis, we fabricate the symmetric vertical-channel NSILC-VTFT device with unilateral crystallization. Thus, the MILC/MILC grain boundary (LLGB) in the middle of the channel can be eliminated. Besides, the devices can reduce the metal contaminations on source and drain region due to the metal seed window is separated from the drain metallurgical junction [45]. We also hope that grain filtering effect occurred on the NSILC process when the width of a-Si film pattern was narrowed. Thus we can obtain the vertical channel region, which is composed of a single-orientated crystal. In addition, the NSILC-VTFTs which has the inherently own an effective dual gate structure and offset region. We hope that measured results shows the NSILC-VTFTs have high on-state current, high field effect mobility, steeper subthreshold swing, and low leakage current.

1.4 Organization of the Thesis

There are four chapters in this thesis. This thesis is organized as follows:

In Chapter 1, we introduce the development of thin-film transistors and comparison between poly-Si TFTs and a-Si TFTs. Some technique of manufacture the poly-Si TFTs are described in this chapter. Moreover, we also introduce the vertical channel thin-film transistors.

In Chapter 2, we describe the structure and the process of our vertical thin-film transistors. We also show the VTFTs cross-sectional photograph of TEM and optical microscopy photograph during different process time of MILC. Besides, the electrical parameters extraction are shown in the end of this chapter.

In Chapter 3, we discuss the electrical characteristic of VTFTs and the effect of post treatment. Then, we discuss the crystal filtering effect in the VTFTs and comparison between MILC-VTFTs and NSILC-VTFTs.

Finally, the main conclusions and future works are summarized in Chapter 4.
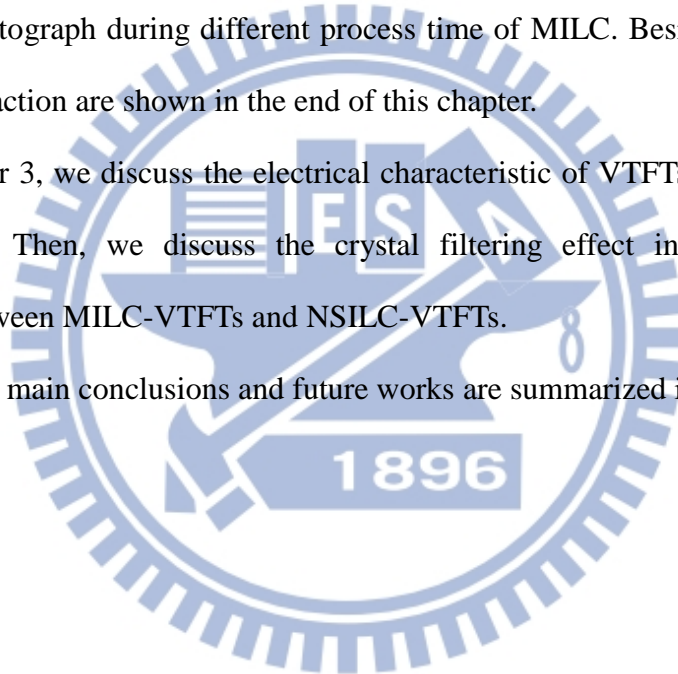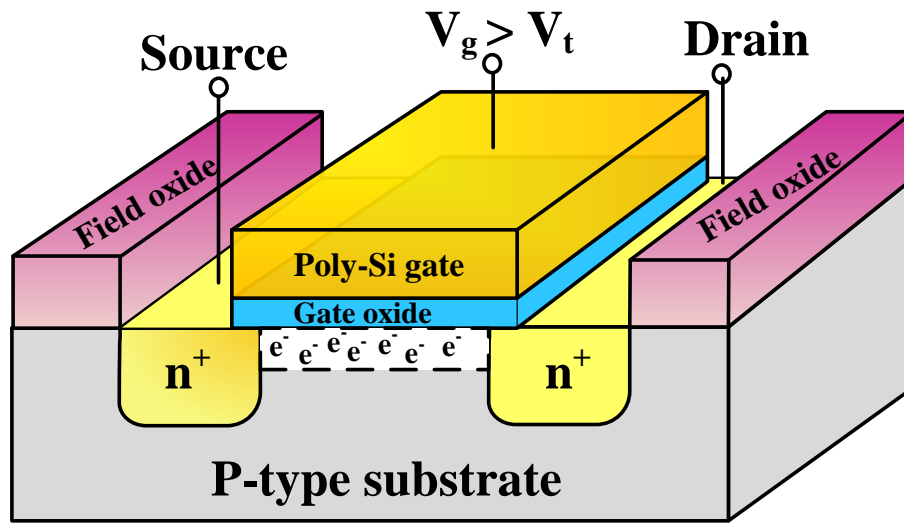
Fig. 1-1 Schematic of field-effect transistor.

Si Diamond structure
a = 5.430 Å

NiSi$_2$ Fluorite structure
a = 5.406 Å
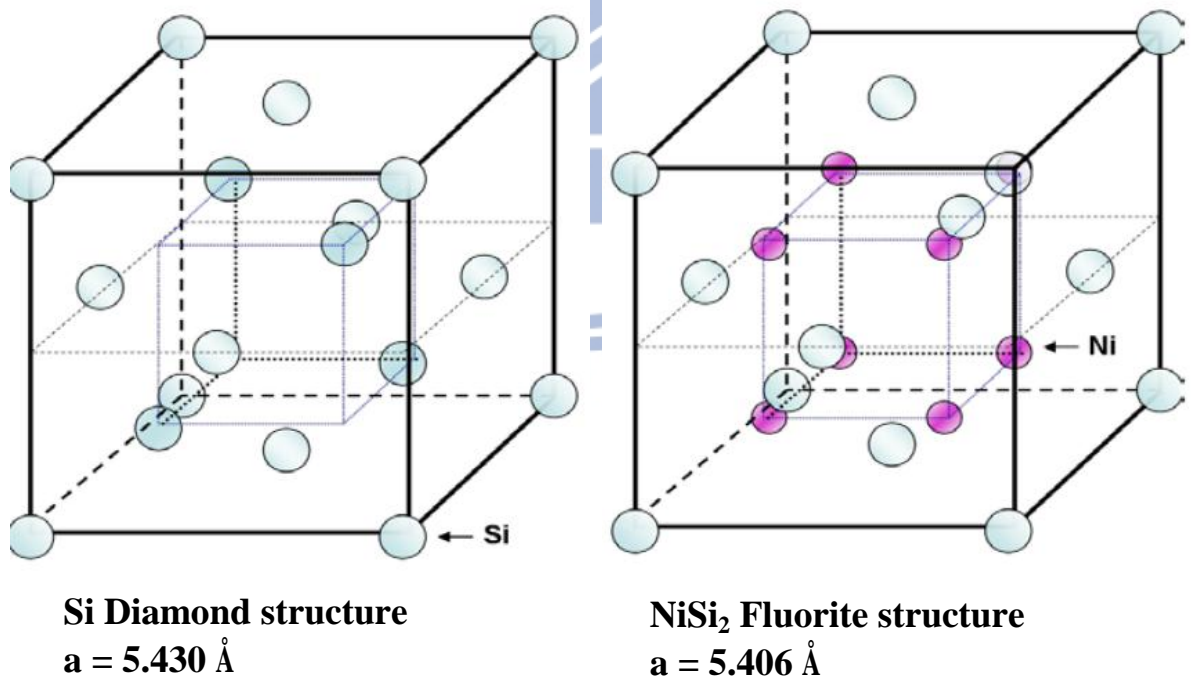
Fig. 1-2 The crystalline structure of Si and NiSi$_2$.
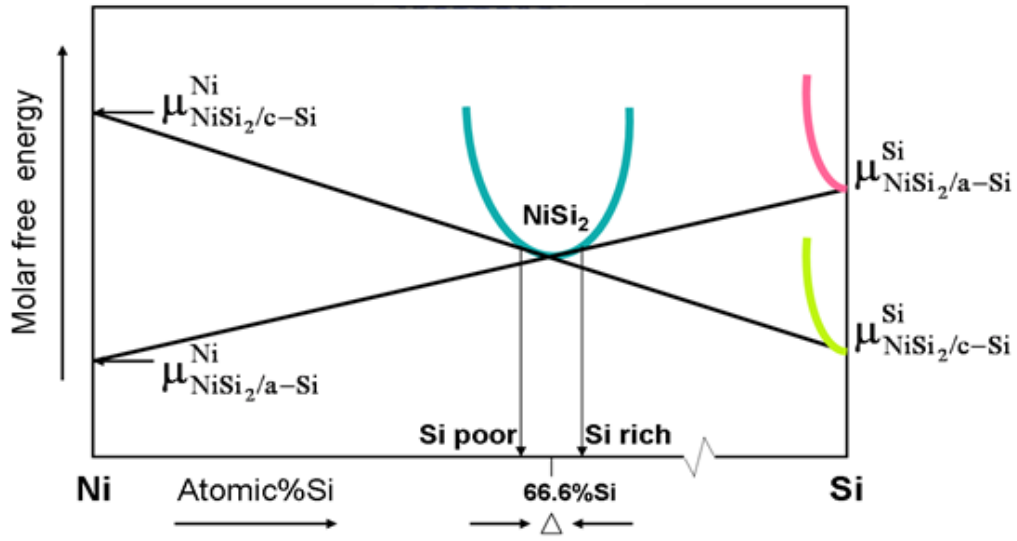
Fig. 1-3 Schematic equilibrium molar free-energy diagram for NiSi$_2$ in contact with a-Si and c-Si. [36]
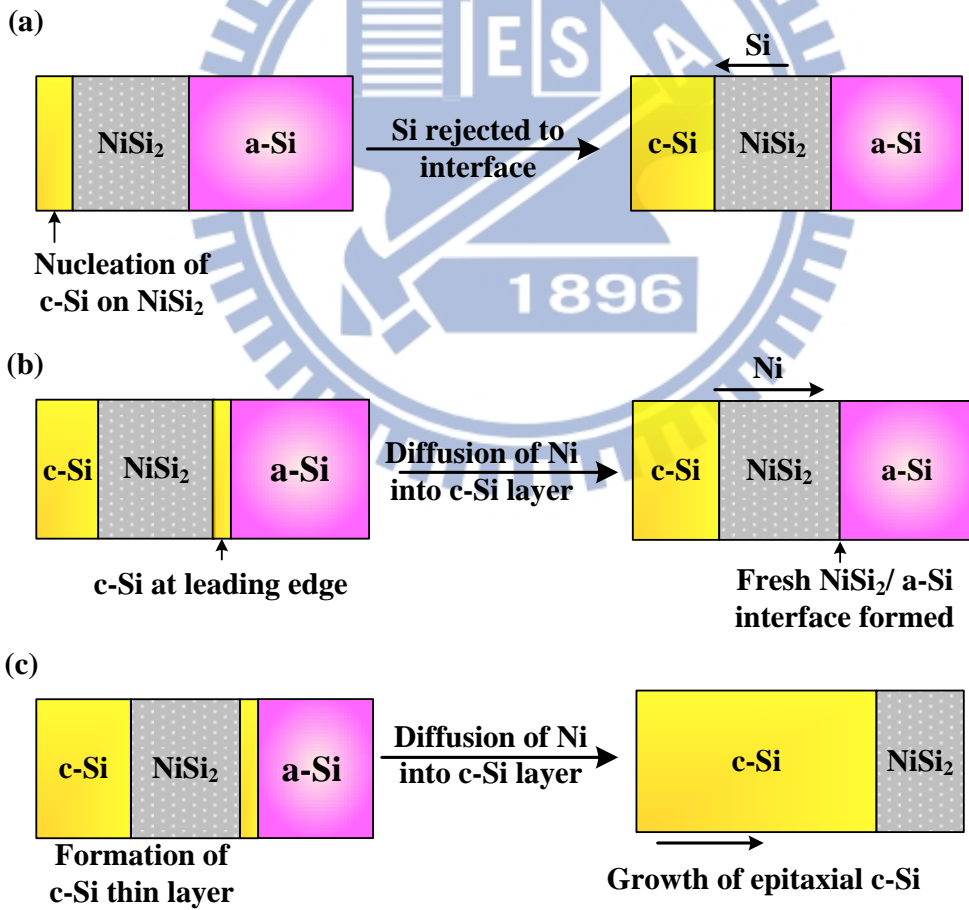
Fig. 1-4 Schematic of the growth mechanism of Ni-induced lateral crystallization [36].

Chapter 2

Device Fabrication and Electrical Parameters Extraction

2.1 Fabrication of the vertical channel thin-film-transistor

2.1.1 Fabrication Process

The overall fabrication process flow of the vertical thin-film-transistors (VTFTs) is shown in Fig 2.1.

First of all, the 550-nm thick thermal oxide was grown on Si wafer as starting substrate. Then 200-nm thick poly-Si layer was deposited for gate by low-pressure chemical vapor deposition (LPCVD) system using SiH_4 as source gas. The gate was implanted with phosphorous, the energy and the dose of the implantation were 40 keV and $5 \times 10^{15} \ cm^{-2}$, respectively. Subsequently, the dopants were activated by furnace at 600 ^{o}C for 24 hours.

After the gate patterning, the oxide was overetched to about 80-nm to form the offset region. Then, the 15-nm thick layer of tetraethoxysilane (TEOS) oxide and 50-nm thick undoped amorphous Si (a-Si) layer were deposited consecutively as gate oxide and active region by LPCVD. The deposition pressure and temperature of a-Si film are 350 mTorr and 560 ^{o}C, respectively. After active region patterning, Ni-window mask pattern was form on the top of the TFTs using photoresist. The 10-nm Ni film was deposited by electron-beam evaporation system and then Ni film on the photoresist was removed by the lift-off process. Ni contacts with a-Si only in the seeding window; other areas of wafers outside the seeding window are mostly free of Ni contamination.

We used two methods to complete the channel crystallization: MILC and NSILC. The MILC-VTFTs were fabricated without Ni-silicidation process by rapid thermal annealing (RTA). In the NSILC-VTFTs, the Ni-silicidation was carried out at 450 ^{o}C for 30 s by RTA. And then, the unreacted Ni film was removed by H_2SO_4 / H_2O_2

solution at 120 ^{o}C for 10 min. Next, both devices were crystallized subsequently at 500 ^{o}C for 48 hours in N$_2$ ambient.

Then, a 15-nm thick TEOS oxide was deposited and 15-keV, $5 \times 10^{15} \ cm^{-2}$ As$^+$ ion implantation to form self-aligned n$^+$ S/D and n$^+$ floating region. Then the dopants were activated by RTA at 750 ^{o}C for 30 s. The three-dimensional graph of the device structure is shown in Fig. 2-2.

2.1.2 Fabrication results

Fig. 2-3 and Fig. 2-4 show the cross-sectional transmission electron microscope (TEM) microphotograph of the NSILC-VTFTs and MILC-VTFTs. The integrity of the vertical poly-Si channel is verified by the transmission electron diffraction (TED) pattern inserted in TEM microphotograph. In the TEM images, the gate oxide and the poly-Si thickness in the channel are roughly 20-nm and 50-nm, respectively. The offset region between the gate and the S/D edges was achieved by wet-oxide overetched resulting in about 20-nm offset region. Fig. 2-5 displays the top-view schematic diagram of MILC-VTFTs with source, drain, bottom gate and Ni-window. And the schematic cross-sectional view and effective dual gate structure of MILC-VTFTs are shown in Fig. 2-6. The length of floating n$^+$ region (L_f) is defined by the mask channel length, and the mask channel width (W_{mask}) is equal to the effective channel width. The effective channel length L_{eff} is the vertical channel region, which is defined as $2 \times$ the total thickness of the poly-Si gate, which equals 0.4 μm. Moreover, the equivalent dual-gate structure can reduce the peak lateral electrical field in the drain depletion region, significantly reducing the leakage current and increasing the I$_{on}$/I$_{off}$ current ratio [1]-[2].

The Fig. 2-7 shows optical microscopy photograph of active pattern with the source, the drain, channels, bottom-gate and Ni-seeding window. The gate length is 1

µm, and the channel width is 2 µm. The optical micrograph of a sample heat treated for 3 h at 500 ℃, as in Fig. 2-8(a), the crystallization was seen to proceed laterally from the Ni-window and the MILC distance was around 5.98 µm from the Ni-seeding window. And the crystallization was completed in 12 h as in Fig. 2-8(b), the whole active channel was crystallized by the MILC process. Three distinct regions are visible: the rectangle with the brighter contrast was originally covered by Ni, which is MIC region. This is surrounded by the MILC region with the brightest contrast. And the darkest area in the out of MILC region is a-Si region. These results indicate that the active channel can be crystallized during the MILC process at 500 ℃ for 48 hours.

2.2 Method of Device Parameter Extraction

In this thesis, all of the electrical properties of proposed poly-Si TFTs were measured by semiconductor characterization system Keithley 4200. Many methods have been proposed to extract the characteristics of poly-Si TFT. In this section, extractions of various electrical parameters are introduced. These parameters include the subthreshold swing (S.S.), Filed-effect mobility (μ_{eff}), On-state current (I_{on}), and Off-state current (I_{off}).

2.2.1 Determination of Subthreshold swing

Subthreshold swing (S.S.) is an important parameter to describe the control ability of gate toward the channel, reflecting the switch speed of the device. It is defined as the amount gate voltage required to increase/ decrease drain current by one-order of magnitude. In general, the S.S. should be independent on drain voltage and gate voltage. However, there are many non-ideal effects in MOSFETs and TFTs. The degradation of the S.S. with increasing drain voltage is due to short channel effect, avalanche multiplication, and punch through effect. Moreover, the subthreshold swing

is related to gate voltage which attributes the undesirable factor, such as interface states and gate oxide thickness.

In this thesis, the S.S. is defined as a quarter of gate voltage required to increase drain current by four-orders of magnitude.

$$S.S. \equiv \frac{\partial V_G}{\partial (log I_D)} = (ln10)\frac{\partial V_G}{\partial (ln I_D)}$$

By neglecting the depletion capacitance in the active layer, Takashi Noguchi has reported that effective interface-trap-state-density (N_{it}) near the poly-Si/ SiO$_2$ interface can be extracted from the subthreshold swing [3]-[5].

$$N_{it} = [\left(\frac{S.S.}{ln10}\right)\left(\frac{q}{kT}\right) - 1](\frac{C_{ox}}{q})$$

2.2.2 Determination of Field Effect Mobility

Usually, the field effect mobility (μ_{eff}) is extracted from the maximum value of transconductance (g$_m$) at low drain voltage ($V_{DS} = 0.1$ V, V_{GS}-$V_{th} \gg V_{DS}$). The transfer characteristic of poly-Si TFTs is similar to traditional MOSFET, so the first order of I-V relation in the bulk Si MOSFETs can be applied to poly-Si TFTs. The drain current in linear region ($V_D < V_G - V_{th}$) can be approximated as the following equation:

$$I_D = \mu_{eff} C_{ox}\left(\frac{W}{L}\right)[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2]$$

Where W and L are channel width and channel length, respectively. C$_{ox}$ is the gate oxide capacitance per unit area and the V$_{th}$ is the threshold voltage. Thus, the transconductance g$_m$ is given by

$$g_m = \frac{\partial I_D}{\partial V_G}|_{V_{DS}=const.} = \mu_{eff} C_{ox}(\frac{W}{L})V_{DS}$$

Therefore, the field-effect mobility is obtained by

$$\mu_{FE} = \frac{L}{W C_{ox} V_{DS}} g_{m,max}$$

2.2.3 Determination of ON/ OFF current ratio

On/off current ratio is one of the most important parameters of poly-Si TFTs. An promising poly-Si TFT technique should not only provides high on-state current but also low off-state leakage current. For switching elements, as pixel cell, the off state is frequently operated in normal operation. Therefore, on/off current ratio is evidently a more appropriate evaluation parameter compared with on state current alone. The leakage current mechanism in the poly-Si TFTs is more complicated than single crystal device. For single crystal device, the channel film is composed of single crystalline and the leakage current is due to the tunneling of minority carrier from drain region to accumulation layer located in channel region. However, in poly-Si TFTs, the channel is composed of poly-Si grain, which has lots of inherence defects in the intra-grain and inter-grain site. And most of the density of states located within deep state close to the middle of the forbidden band-gap, and increase as the number of dangling bond increases. Thus, the leakage current due to trap-assisted tunneling and band-to-band tunneling is much larger in poly-Si TFTs than in the single crystal MOSFETs.

In this thesis, the on-state current is defined as the drain current when the gate voltage at 6V and drain voltage is 0.1V for n-channel TFT. The off-state current is defined as the minimum current when the drain voltage equals to 0.1V.

$$\frac{I_{on}}{I_{off}} = \frac{Drain\ current\ of\ I_{DS}-V_{GS}\ plot\ at\ V_{DS}=0.1\ V, V_{GS}=6V}{Minimum\ current\ of\ I_{DS}-V_{GS}\ plot\ at\ V_{DS}=0.1\ V}$$

Poly-Si
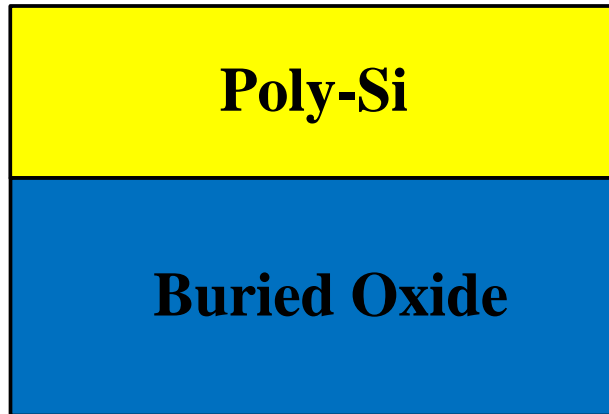
Buried Oxide

(1) 550-nm thick buried oxide was grown and 200-nm a-Si was deposited.

Phosphorous implant

↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓

Poly-Si
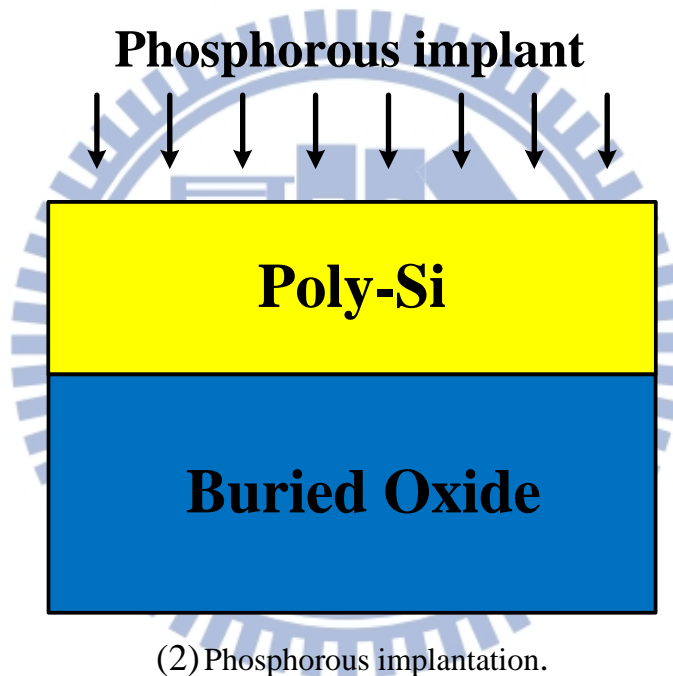
Buried Oxide

(2) Phosphorous implantation.

n$^+$ poly-Si
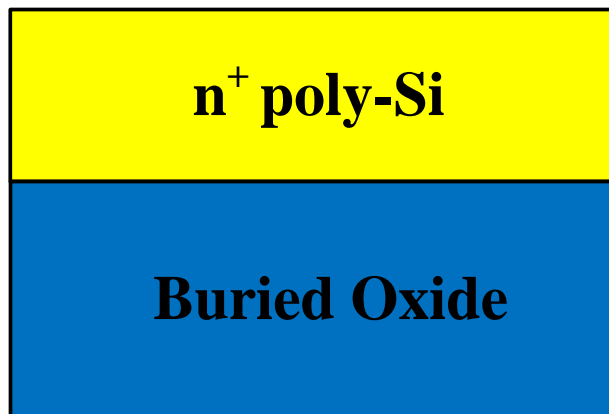
Buried Oxide

(3) 600 ℃ annealing for 24 hours was used to activate the dopants.

Poly-Si
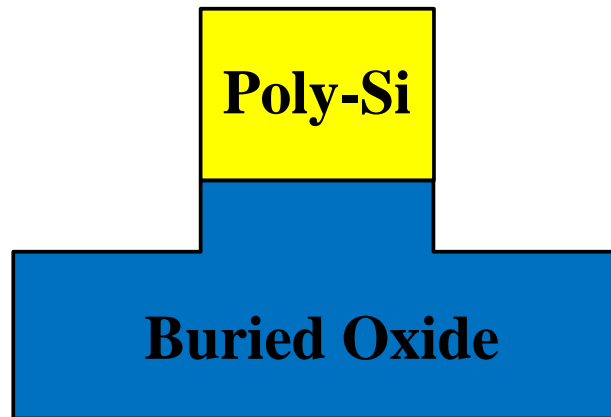
Buried Oxide

(4) Dry etching the poly-Si and 80-nm thick buried oxide to define the gate pattern.

a-Si

Poly-Si

Buried Oxide
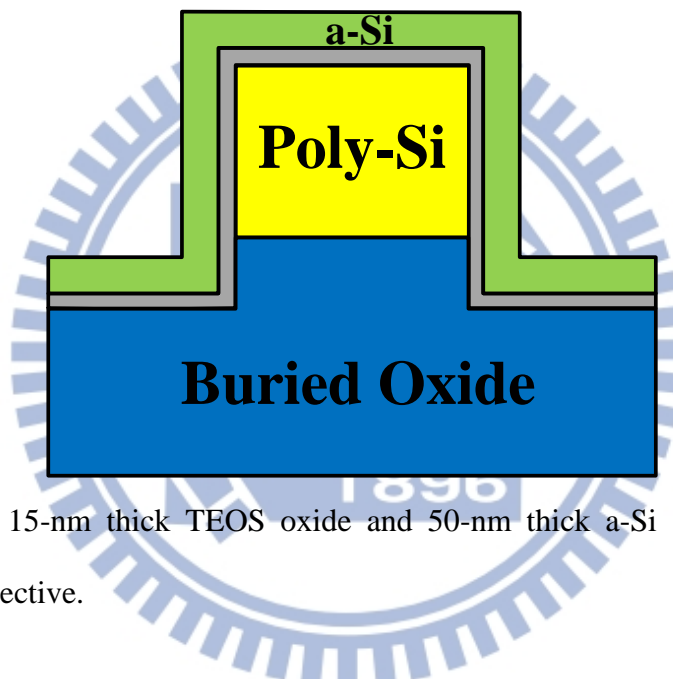
(5) Deposit the 15-nm thick TEOS oxide and 50-nm thick a-Si as gate oxide and channel respective.

Poly-Si

Ni

Buried Oxide
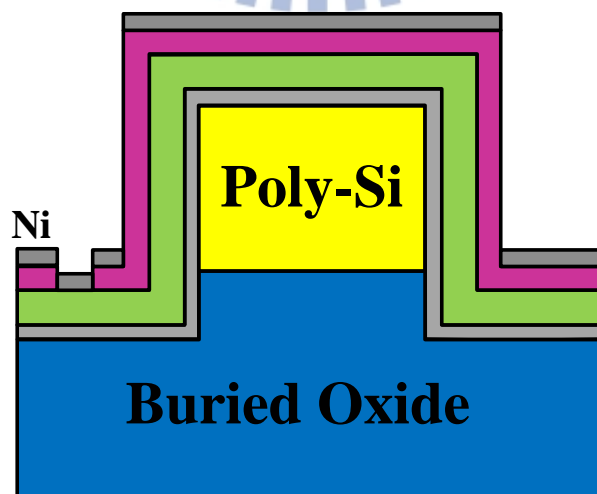
(6) Using photoresist to define the Ni-window and deposit 10-nm thick Ni.
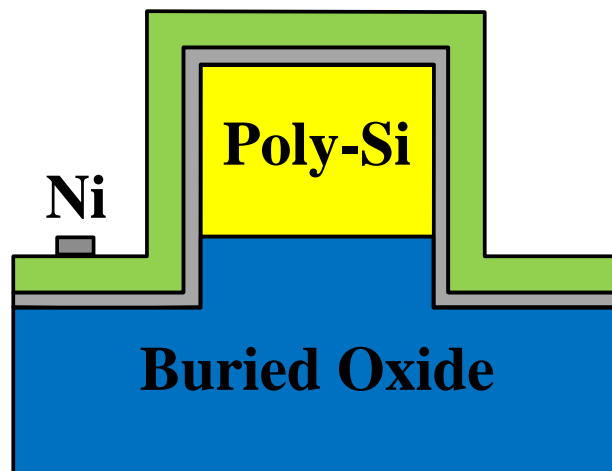
(7) The Ni film on the photoresist was removed by the lift-off process.
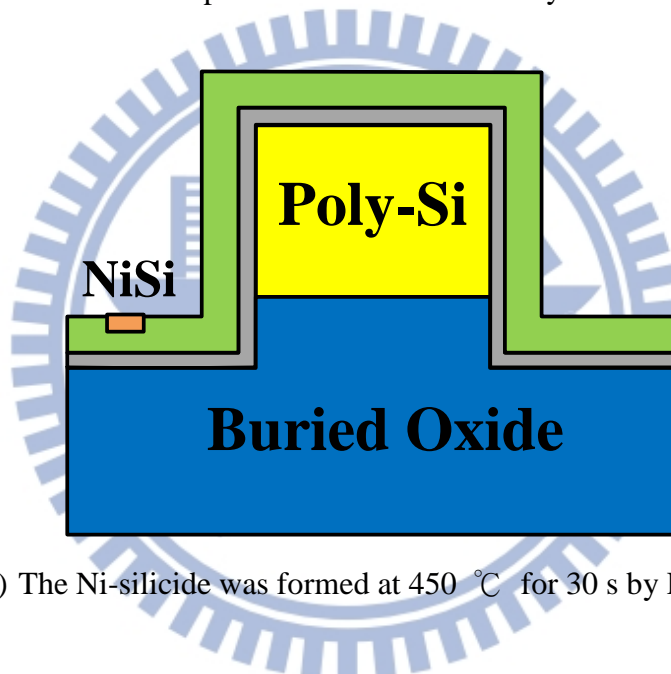
(8) The Ni-silicide was formed at 450 ℃ for 30 s by RTA.
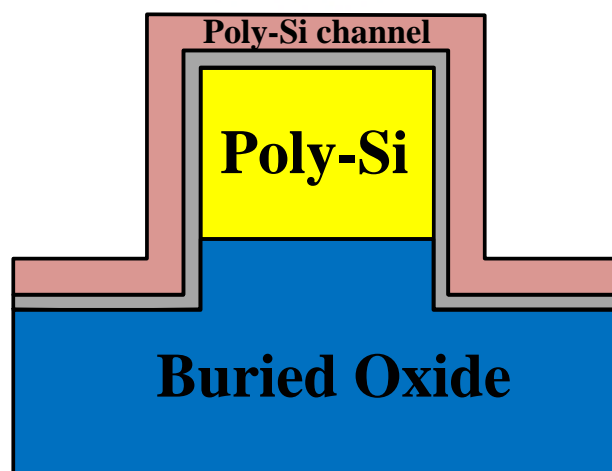
(9) To crystallize the channel during MILC process (500 ℃, 48 h)
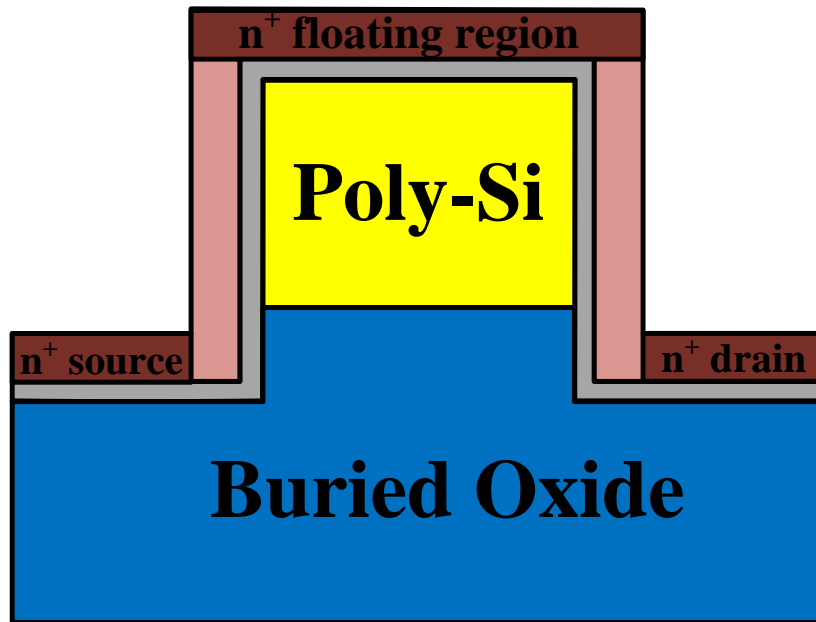
(10) As[+] ion Implantation to form n[+] source/drain and n[+] floating region.

Fig. 2-1 The schematic cross-section diagrams and key process flows of the devices.
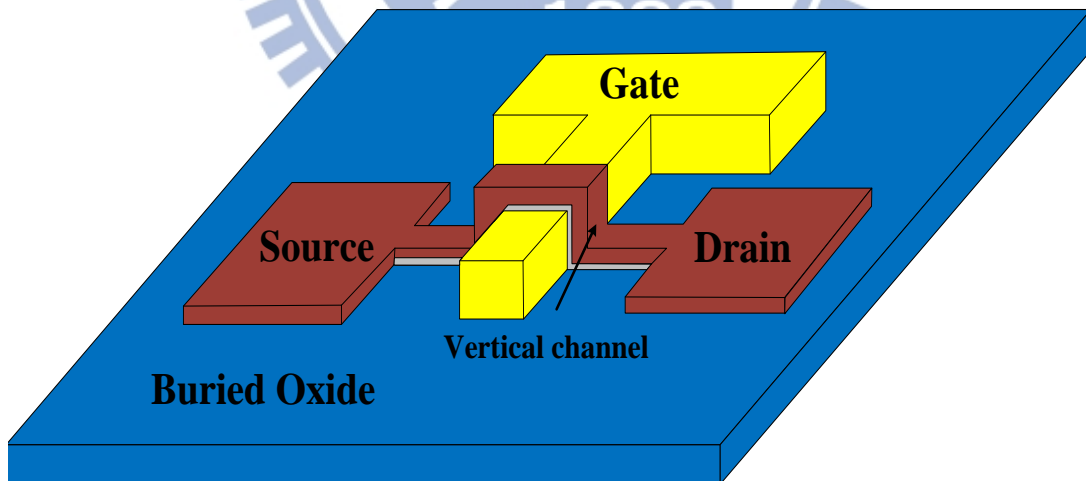
Fig. 2-2 Device structure of the proposed VTFT.
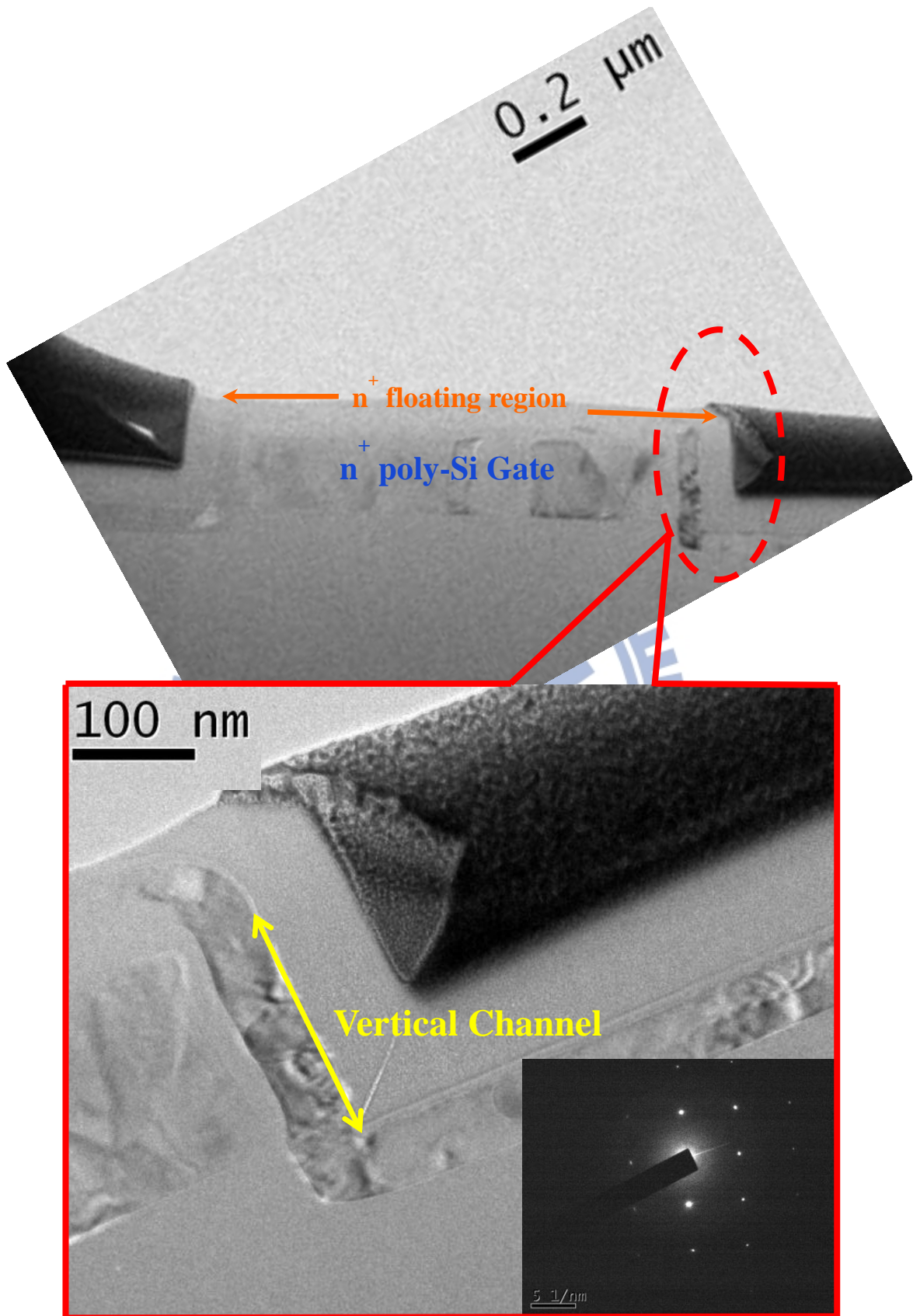
Fig. 2-3 The cross-sectional transmission electron microscope (TEM) microphotograph and TED pattern of the NSILC-VTFTs.
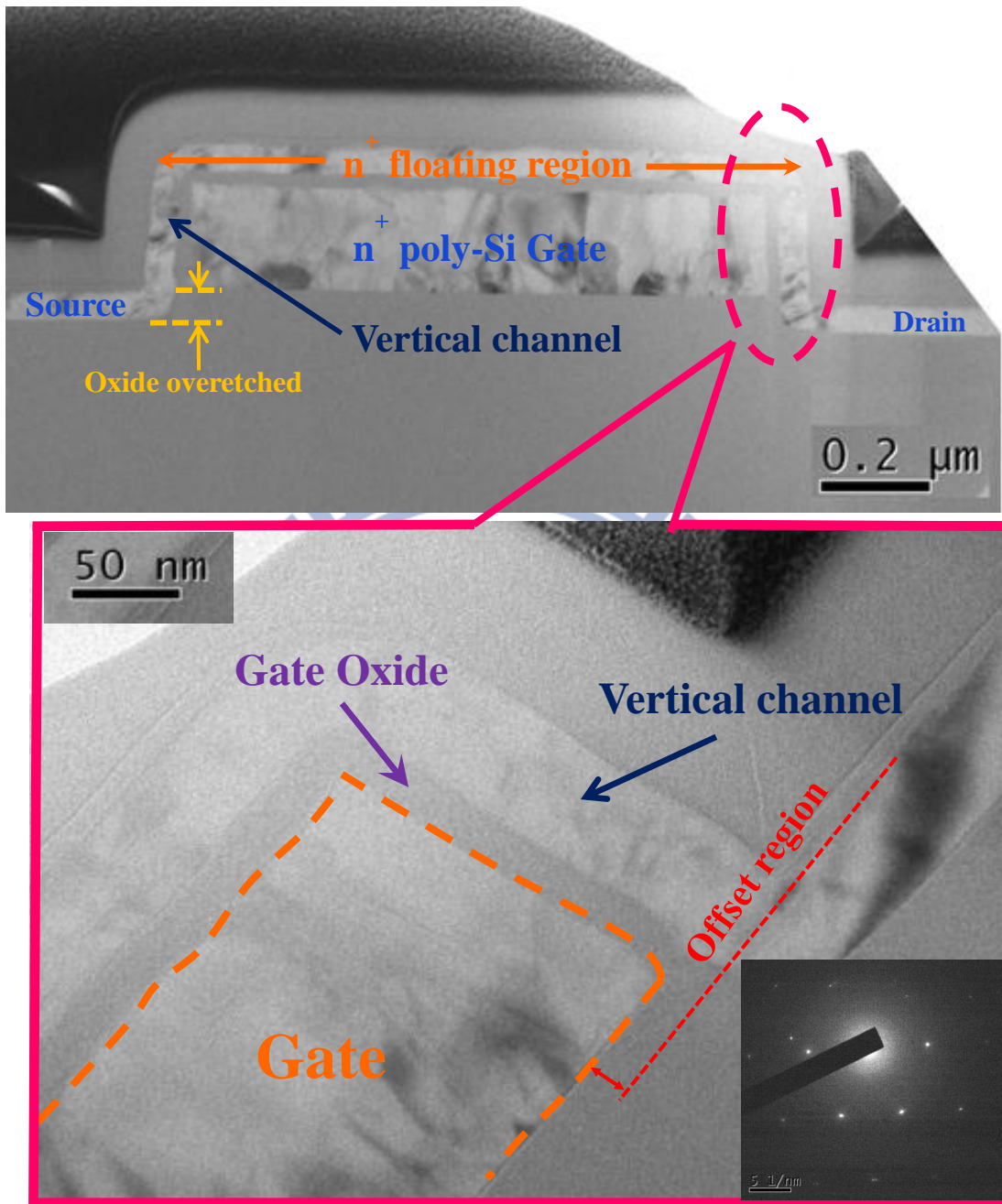
Fig. 2-4 The cross-sectional transmission electron microscope (TEM) microphotograph and TED pattern of the MILC-VTFTs.
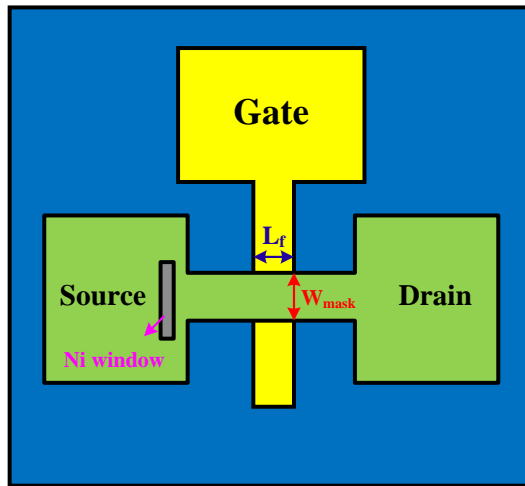
Fig. 2-5 The top-view schematic diagram of MILC-VTFTs with source, drain, bottom gate and Ni-window.
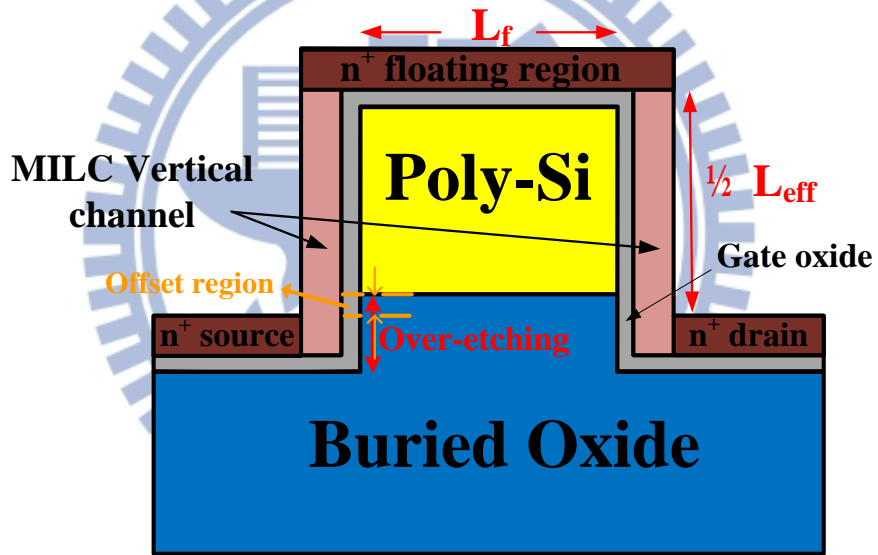
(a)
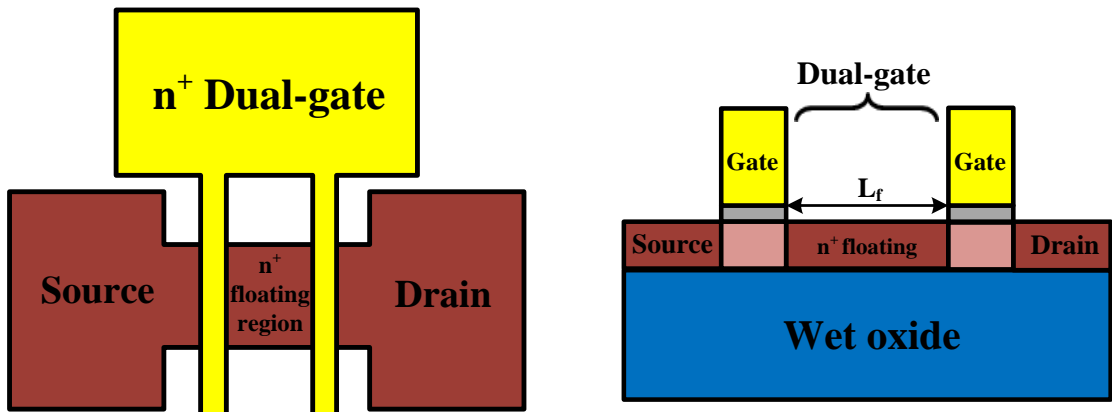
(b)

Fig. 2-6 (a) The cross-sectional schematic diagram of MILC-VTFTs and (b) Effective dual gate structure of MILC-VTFTs.

Fig. 2-7 Optical microscopy photograph of active pattern with the source, the drain, channels, bottom-gate and Ni-seeding window.
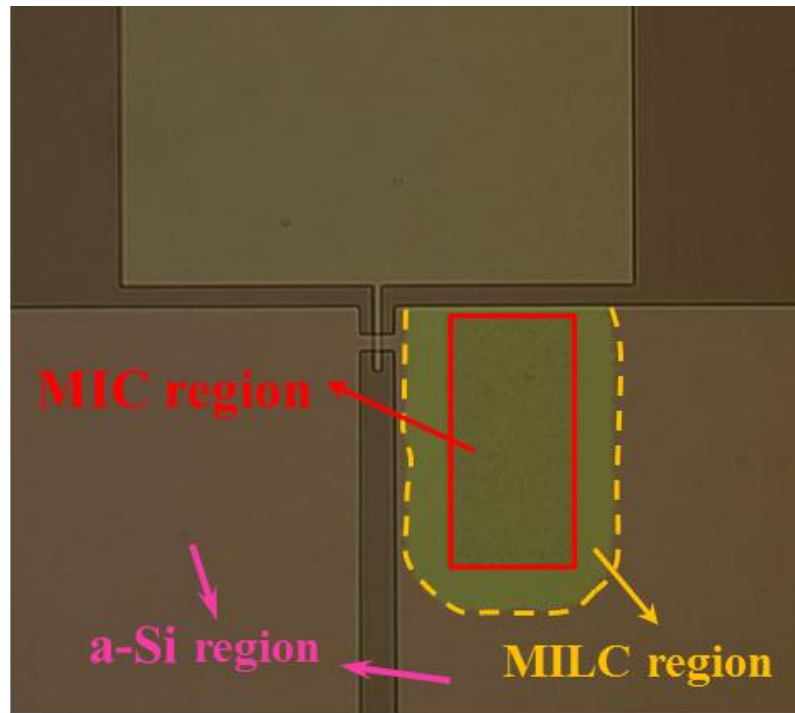
(a)
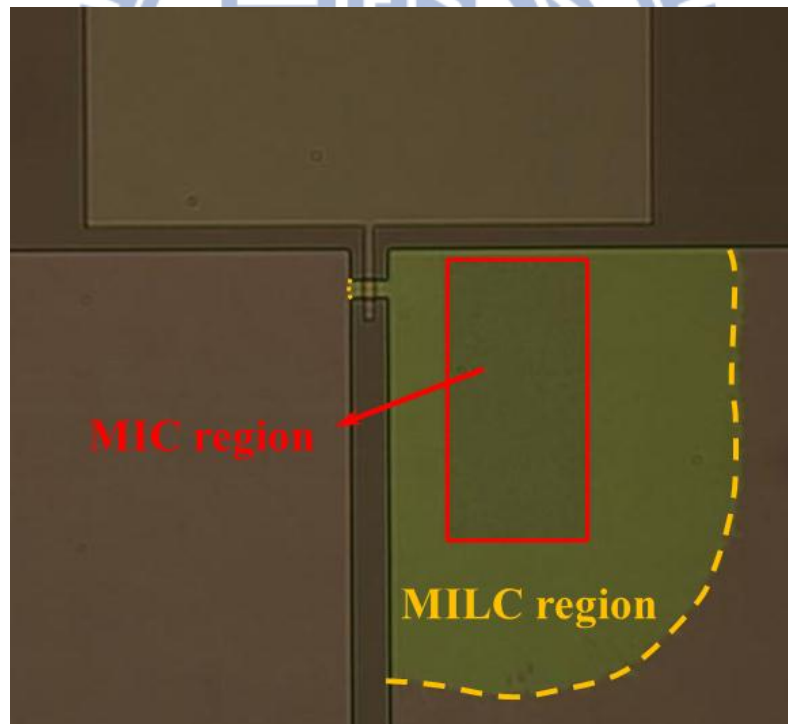
(b)

Fig. 2-8 The OM micrographs of a sample heat treated for (a) 3 h and (b) 12 h of heat treatment at 500 ^{o}C, and the whole active channel was crystallized by the MILC process.

Chapter 3

Characteristics of Vertical Channel Low Temperature

Nickel Induced Lateral Crystallization Poly-Si TFT

Poly-Si TFTs have attracted considerable interest due to their wide applications, such as driving pixels and peripheral circuits in AMOLEDs and system on panel (SOP). The most widely employed methods for poly-Si formation are solid-phase crystallization (SPC), excimer laser annealing (ELA) and metal-induced lateral crystallization (MILC). The a-Si thin films could be crystallized at a low temperature of below 500 $^{\circ}$C by MILC, and it has uniform poly-Si films and low-cost production. However, there are many intra-grain defects in poly-Si and the Ni and $NiSi_2$ precipitates are trapped in poly-Si grain boundaries. Both Ni and $NiSi_2$ act as trap sites for high leakage current at the junction boundary and as scattering sources that considerably reduce the filed-effect mobility. Therefore, Ni contamination inside the MILC poly-Si film should be reduced to improve the device performance.

In order to alleviate adverse effects to obtain high performance TFTs, plasma treatment and crystal filtering can be used to produce the uniform crystal orientation and enhance the device performance. Besides, several methods have been proposed to reduce the amount of undesired metal impurity [47]-[49]. But these methods are complicated and need extra process. Accordingly, we propose a more simple method to reduce the Ni and $NiSi_2$ contamination in the MILC region and expect the applicability of the method to fabricate poly-Si TFTs with high performance.

3.1 Effects of post treatment

It is well known that the grain boundaries exert a profound effect on device characteristic, because the charges trapped within grain boundaries and build up potential barriers to the flow of carrier subsequently. Moreover, the numerous intra-grain defects in poly-Si channel film also adversely influence on the device performance. Thus, poly-Si TFTs exhibit poor performance such as low mobility, large subthreshold swing, large threshold voltage, and large leakage current than the single-crystal counterparts. To obtain high performance poly-Si TFTs, both the grain enlargement techniques [1]-[2] and defect passivation processes have become increasingly important. In order to reduce the trap state densities in the poly-Si channel film, it can be performed by plasma treatment, including H_2, O_2, N_2, and NH_3 plasma [3]-[7]. Traditionally, H_2 plasma has been a very effective and popular method for passivation. However, it had been observed that the introduction of hydrogen would degrade the reliability due to the weak Si-H bonds. To attenuate the hot-carrier degradation and obtain comparable device performance, NH_3 anneal and NH_3 plasma passivation have been recently proposed, and the better hot-carrier reliability than using H_2 plasma passivation has been realized.

In this thesis, the NH_3 plasma treatment was performed for 10 min at 300 ^{o}C with RF power of 50 W. The flow-rate was 100 sccm at pressure of 67 Pa. The typical transfer characteristic and the transconductance of NSILC-VTFTs and MILC-VTFTs with and without NH_3 plasma treatment is shown in Fig. 3-1. The length of the floating region and channel width is 0.35 μ m and 1 μm respectively.

Accordingly, the subthreshold swing (S.S.) and the effective interface trap-state density (N_{it}) of the NH_3 plasma-treated NSILC-VTFT are 224.1 mV/dec. and $2.98 \times 10^{12}\ cm^{-2}$, respectively, which are superior to 1206.9 mV/dec. and $20.8 \times 10^{12}\ cm^{-2}$ of the control NSILC-VTFT. And the S.S and the N_{it} of the plasma-treated

MILC-VTFT are 256.8 mV/dec. and $3.57 \times 10^{12}\ cm^{-2}$, respectively. Moreover, the field-effect mobility of NILC-VTFT and MILC-VTFT with NH_3 plasma treatment for 10 min are 131.87 cm^2/V-s and 147.39 cm^2/V-s, respectively. It is evident that device characteristics are significantly improved by NH_3 plasma passivation. Detailed device parameters such as field-effect mobility (μ_{eff}), subthreshold swing (S.S.), effective interface trap-state density (N_{it}), off-state current (I_{off}), ON/OFF current ratio are summarized in Table 3-1. It has higher field mobility, higher ON/OFF current ratio, lower threshold voltage, and steeper subthreshold swing with NH_3 plasma treatment. The previous study had reported that the threshold voltage and subthreshold swing are related to the dangling-bond deep trap states. They have faster response to the plasma passivation. And the leakage current and field-effect mobility, which are related to strain-bond tail trap states of poly-Si channel, have slower improvement to plasma passivation [8]. NH_3 plasma passivation further improves the performance of these devices, suggesting that the NH_3 plasma effectively passivated the dangling bonds at the grain boundary by the H and N radicals coupling and the nitrogen pile up at the SiO_2/poly-Si interface resulting in the formation of strong Si-N bonds[6]-[8]. Moreover, the NH_3 plasma passivation reduces the barrier height (E_B) of the poly-Si grain boundary, the electrons can easily overcome E_B, producing a high current and allowing the TFT to be easily turned on.

3.2 Crystal Filtering Effect

The poly-Si TFTs have attracted much attention for driving pixels and peripheral circuits in AMOLEDs, due to their higher carrier mobility than a-Si TFTs. However, the presence of poly-Si grain boundary defects in the channel region of TFTs drastically influences on the electrical characteristics [9]-[10]. Therefore, the control of the orientation of the Si crystal grains enables us to control the alignment of grain

boundaries. Thus, the electrical performance can be improved by reducing the grain boundary defects and the randomly oriented grain boundaries from the device area. In this section, we propose the VTFTs with various crystal filter widths and multichannel structure to improve the electrical characteristics by crystal filtering effect.

In this thesis, the devices can be divided into two groups, EW2 and EW1, according to their effective widths listed in Table 3-2. The top view optical microscope microphotographs of MILC-VTFTs with various widths of crystal filter are shown in Fig. 3.2. The effective width of EW2 and EW1 are 2 μm and 1 μm respectively. Both the devices of the floating region length (L_f) were fixed at 1 μm. In the group EW2, one with crystal filter width of 2 μm and a single-channel (designed "W2C1"), one with crystal filter width of 1 μm and two channels (designed "W1C2"), one with crystal filter width of 0.5 μm and four channels (designed "W0.5C4"), and the other with crystal filter width of 0.4 μm and five channels (designed "W0.4C5"). In the group EW1, one with crystal filter width of 1 μm and a single-channel (designed "W1C1"), and another with crystal filter width of 0.5 μm and two-channels (designed "W0.5C2").

Fig. 3.3 shows the transfer characteristics of MILC-VTFTs with various widths of crystal filter. Compared with W2C1, W1C2, W0.5C4, W0.4C5 has better device performance than its counterparts. Moreover, the W0.5C2 also has the significant performance than other. These results indicate that the narrower the unit channel width is, the better the electrical performance is, including higher on-state current, steeper subthreshold swing, and lower off-state current. This is attributed to that lower probability of the channel region covers the grain boundary in narrower width devices and the channel region would have more uniform crystal growth direction than the unfiltered active layer of MILC-VTFT area. The narrower the widths of the crystal filters are, the more uniform the crystallographic orientation the MILC poly-Si is

[11]-[12]. In general, the c-Si grains grow toward the a-Si region with the migration of NiSi$_2$ and the individual crystallites form networks in Ni-MILC process. Moreover, if the NiSi$_2$ layer at the front of c-Si grain meets other crystal grains crystallized by the MILC process. Subsequently, the NiSi$_2$ cannot migrate through the c-Si anymore because there is no difference of chemical potential driving force for the phase transformation between the two c-Si grains [13]. Therefore, the captured NiSi$_2$ would increase silicide contaminations in the MILC region. For the crystal filtering method, there are few crystal Si grains, which has growth direction parallel to the crystal filter, can pass through the filter. Thus, the crystallized Si grains have longer grain lengths, similar crystal orientation and dense microstructure could be selected through crystal filter [14]-[15]. Therefore, the narrower crystal filter width has better grain crystallization, less intra-grain defects, less grain boundaries defects and NiSi$_2$ contaminations in the poly-Si channel. Hence, the device performance, including higher on-state current, steeper subthreshold swing, lower off-state current, will be improved by reducing the crystal filter width.

In order to further confirm the crystal filter effect is correct, we measured more than 20 devices to determine the statistical average values of on-state current (I_{on}), off-state current (I_{off}), subthreshold swing (S.S.), and transconductance (G_m) of group EW2 and EW1, shown in Fig. 3-4 – Fig. 3-11. Based on the statistical result, the narrower crystal filter width also has higher I_{on}, lower I_{off}, steeper S.S., and higher G_m than others wider crystal filter width. The statistical average values of some important parameters of all devices are summarized in Table 3-3. The W0.4C5 also has the highest field-effect mobility (μ_{FE}) as 87.5 cm^2/V·s in the group EW2. And the W0.5C2 has the best field-effect mobility as 96.3 cm^2/V·s in all devices. These results were similar to previous reports, indicating that the poly-Si grain lateral length increase as the channel width declines and the grain boundary defects of poly-Si would be reduced

to increase the mobility.

In addition, the longitudinal grains and their boundaries are parallel to the direction of carrier flow in the channel. The wide channel devices with grain boundaries traversing from source to drain provide extra current paths and cause punchthrough. However, the VTFTs inherently own an effective dual gate structure and the offset region, constructed by self-aligned oxide overetching. The previous study had reported that the OFF-state currents can be improved by increasing the oxide overetching depth and equivalent dual-gate structure [16]. This improvement on leakage current originates from reducing the lateral electrical field in the drain depletion region [17]-[20]. Thus, the OFF-state current of these device can be reduced below 1 pA/ μm.

3.3 Compare NSILC-VTFT with MILC-VTFT

According to the previous report [21], the excess Ni accumulation in the middle of the n+ floating region is found in the MILC-VTFTs, but it is not found in the NSILC-VTFTs. The Ni and $NiSi_2$ precipitates trapped in the grain boundary would act as trap sites which increase the leakage current and degrade the field-effect mobility.

In this section, we focus on discussing the different electrical characteristics between NSILC-VTFTs and MILC-VTFTs. Fig. 3-12 –Fig. 3-15 show the on-state current distribution, off-state current distribution, subthreshold swing distribution, and transconductance distribution of the NSILC-VTFTs and MILC-VTFTs with 1 μm of length of n^+ floating region and channel width from 0.35 μm to 1 μm, respectively. We can observe that the electrical performance of NSILC-VTFTs and MILC-VTFTs seems to be no significantly difference. No matter what size of device we choose, we still have the same conclusion: There are no difference between NSILC-VTFTs and MILC-VTFTs.

This observation can be possibly ascribed to the following explanations. In this work, we used the unilateral crystallization method to complete the channel crystallized. Therefore, there is no excess Ni accumulation found in MILC-VTFTs and NSILC-VTFTs. And the MILC/MILC grain boundary in the middle of the channel can be eliminated. If the Ni content is provided by an appropriate amount to complete the channel crystallization, even MILC-VTFTs will be no excess Ni remaining in the channel. Therefore, the NSILC-VTFTs with Ni-silicided seeding window to limit the Ni source is not able to further improve the device characteristics. Nevertheless, the leakage current still can be suppressed by the dual-gate structure and offset region due to reducing the lateral electrical field in the drain depletion region.

Moreover, as channel widths decrease, the I_{off} suppresses and the G_m, S.S. and I_{on} enhances. These results reflect the crystal filtering once more. The average values of some important parameters are summarized in the Table 3-4. The narrower the widths of the crystal filters are, the more uniform the crystallographic orientation the MILC poly-Si is. Thus, the high performance device can be achieved by reducing the channel widths.

Although the narrower the channel width is the better the electrical performance, the on-state current would be degrade due to the W/L factor reducing. In order to overcome this problem, we proposed a layout which given high performance VTFTs. The design of wide devices usually involves the breakdown of a wide transistor into a number of smaller transistors in parallel. In this experiment, we fabricated the multiple channels structure, which unit channel width of 0.35 μm. Fig. 3-16 shows the transfer characteristics of a MILC-VTFT with unit crystal width of 0.35 μm under various channel number. These results indicate that the multiple channel and crystal filtering effect can significant improve the on-state current, while maintaining the high performance of VTFTs. When the channel numbers are increased, the S.S. still remains

better performance about 300 mV/dec.. Moreover, the off-state current can significantly be reduced with both the equivalent dual-gate structure and offset region, and the on-state current and G_m can evidently be improved by multiple channels. In order to further verify the result is correct, more than 20 devices are measured to obtain the statistics. The average values of some important parameters such as I_{on}, I_{off}, S.S., G_m and their standard deviations with unit crystal width of 0.35 μm for various channel number are shown in Fig. 3-17- Fig. 3-20. As a result, the combination of narrower crystal width and multiple channels can successfully further optimize electrical characteristics of poly-Si TFTs, owning to the elimination of grain boundaries and defects.
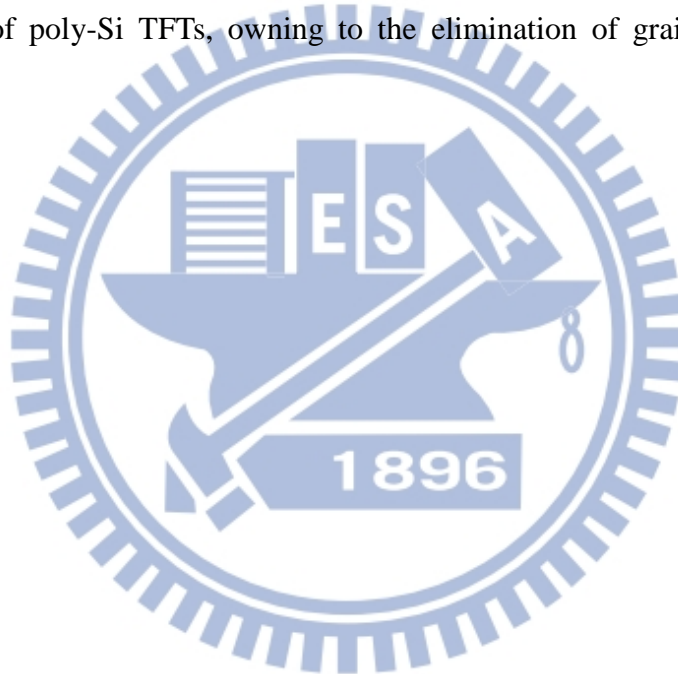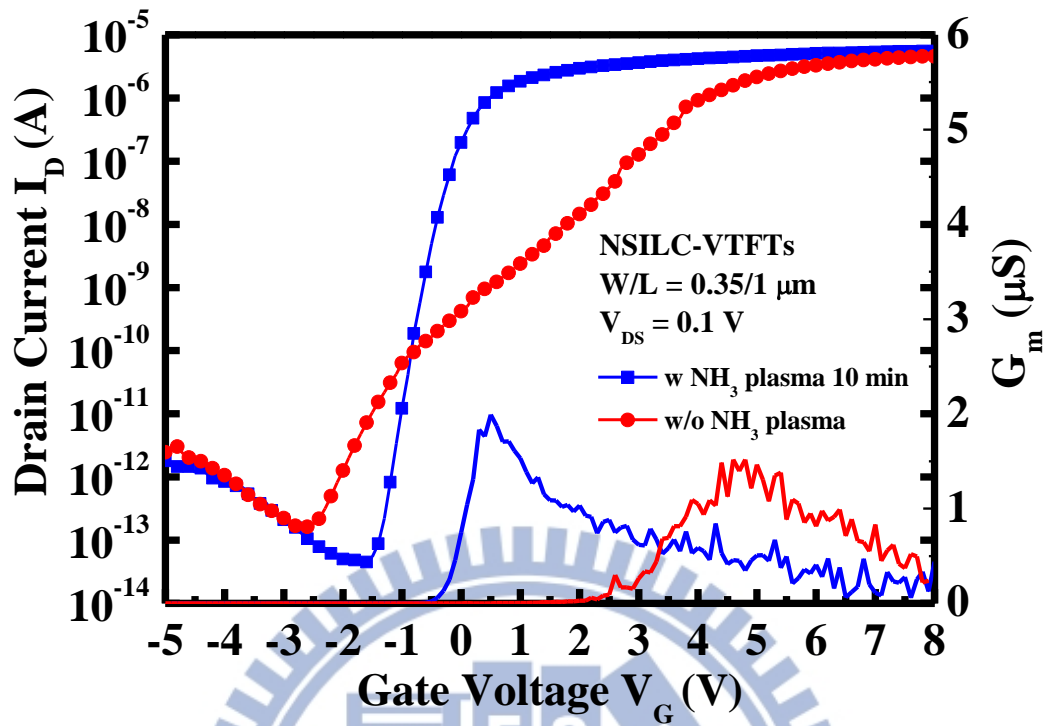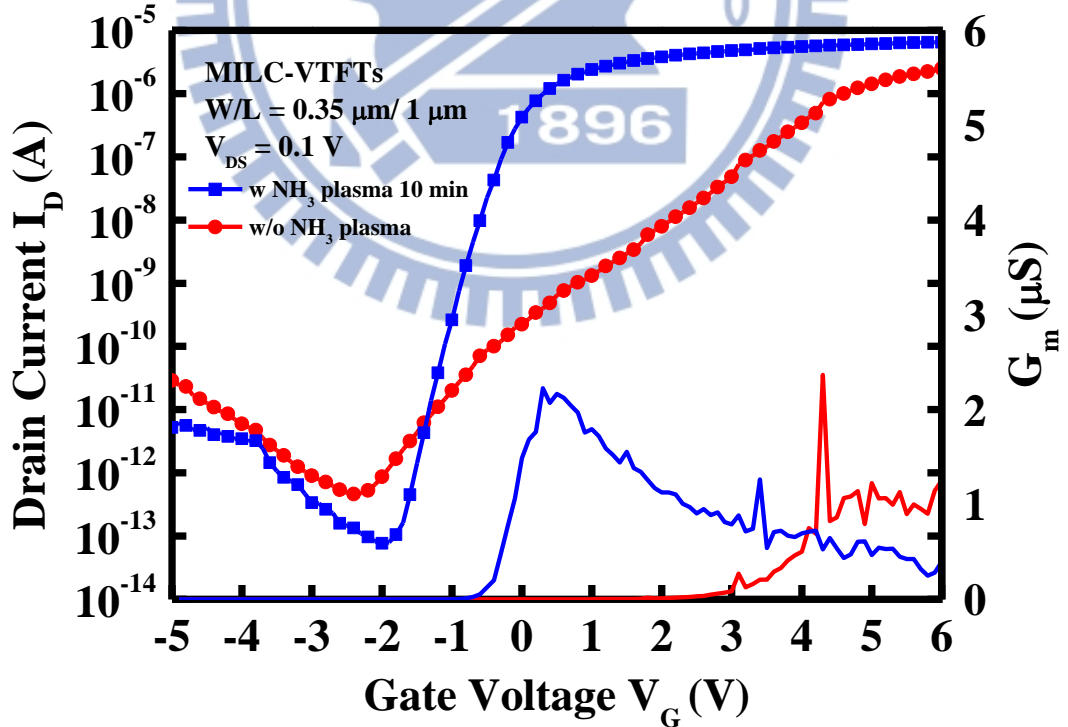
Fig. 3-1 The typical transfer characteristic and the field-effect mobility of (a) NSILC-VTFTs and (b) MILC-VTFTs with and without NH₃ plasma.

Table 3-1 Characteristics of poly-Si TFTs with and without plasma treatment. All parameters are extracted at $V_d = 0.1$ V. W/L = 0.35 μm/ 1 μm

	Condition	S.S. (mV/dec.)	μ_{FE} (cm²/V·s)	N_{it} (10^{12} cm⁻²)	I_{on} (μA)	I_{off} (pA)	I_{on}/I_{off} (×10^7)
NSILC-VTFTs	No-plasma	1206. 9	100.42	20.8	3.30	0.162	2.03
	NH₃ 10 min	224.1	131.87	2.98	5.27	0.041	12.8
MILC-VTFTs	No-plasma	1341.4	75.67	21.0	2.47	0.760	0.295
	NH₃ 10 min	256.8	147.39	3.57	6.49	0.076	8.51

Table 3-2 The width and number of unit channel in the devices.

Group	Device	Unit channel		Total channel width
		width	number	
EW 2	W2C1	2	1	2 μm
	W1C2	1	2	
	W0.5C4	0.5	4	
	W0.4C5	0.4	5	
EW 1	W1C1	1	1	1 μm
	W0.5C2	0.5	2	

(a)

(b)

Fig. 3-2 The top view optical microscope microphotograph of MILC-VTFTs with various widths of crystal filter. (a) Total width = 2 μm (b) Total width =1μm
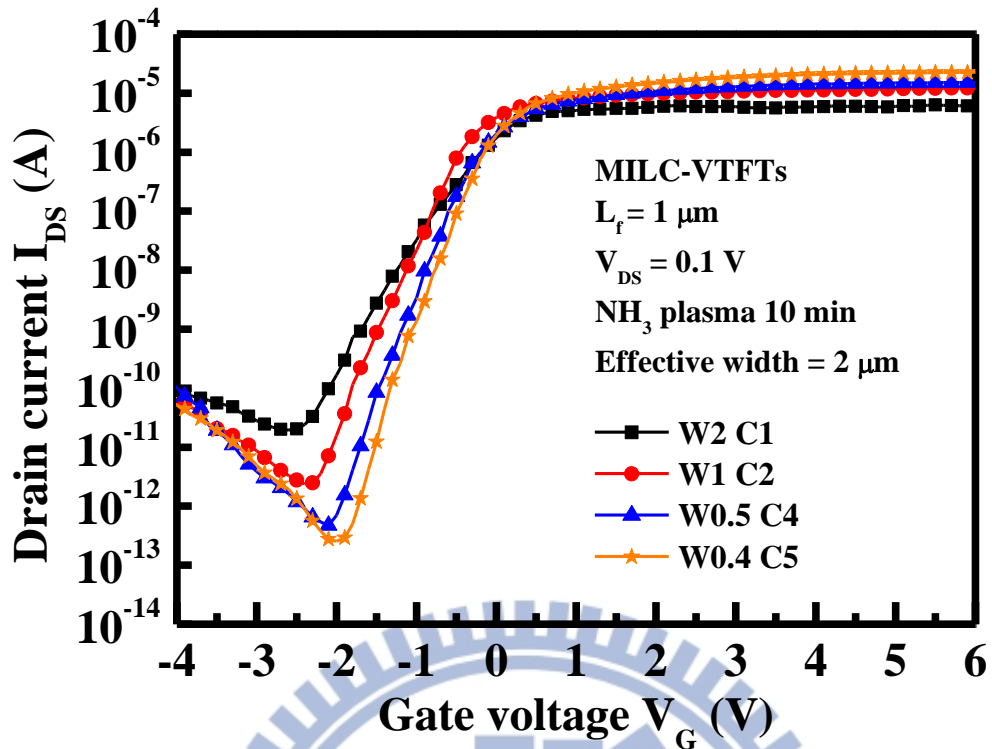
(a) Effective widths = 2 μm
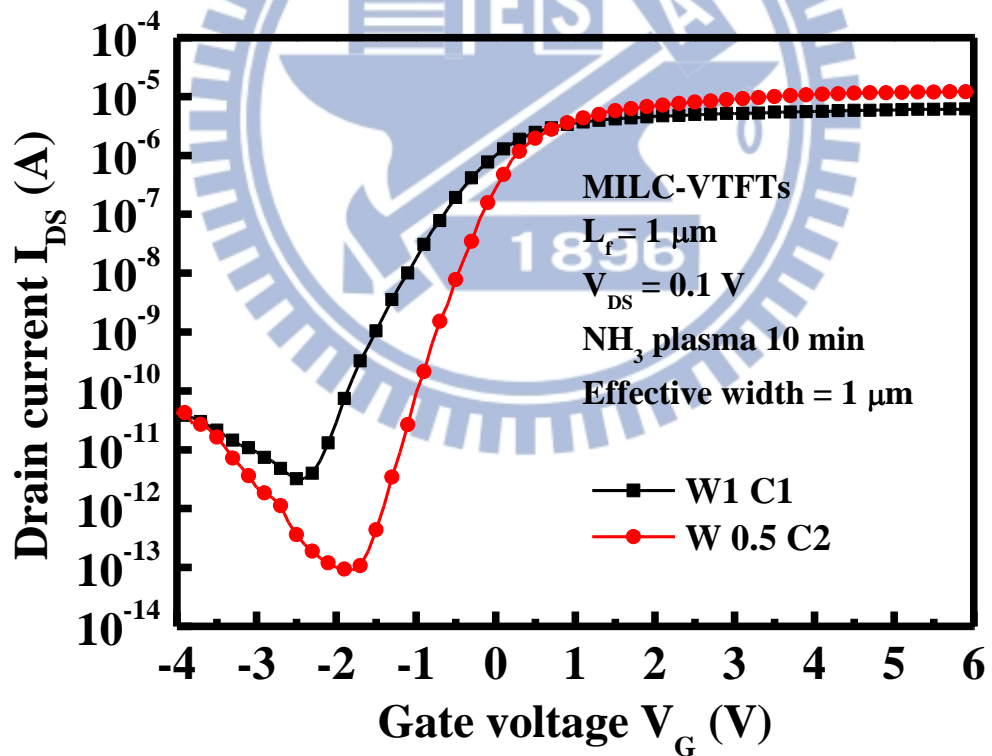
(b) Effective widths = 1 μm

Fig. 3-3 The transfer characteristics of MILC-VTFTs with various widths of crystal filter. (a) Effective widths = 2 μm (b) Effective widths = 1 μm
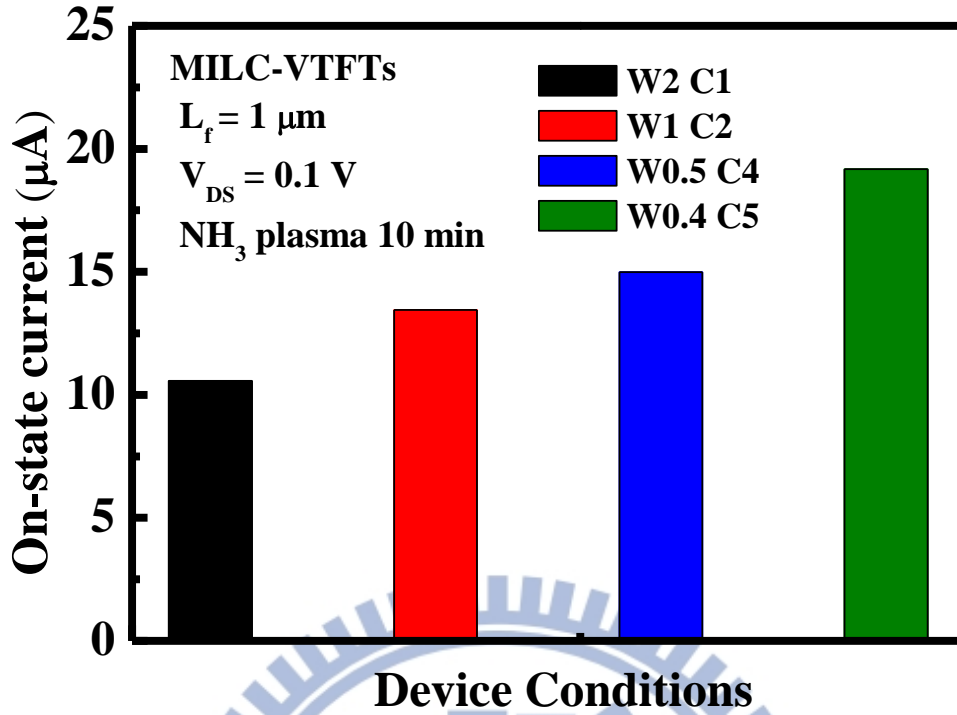
Fig. 3-4 The statistical average values of on-state current of group EW2.
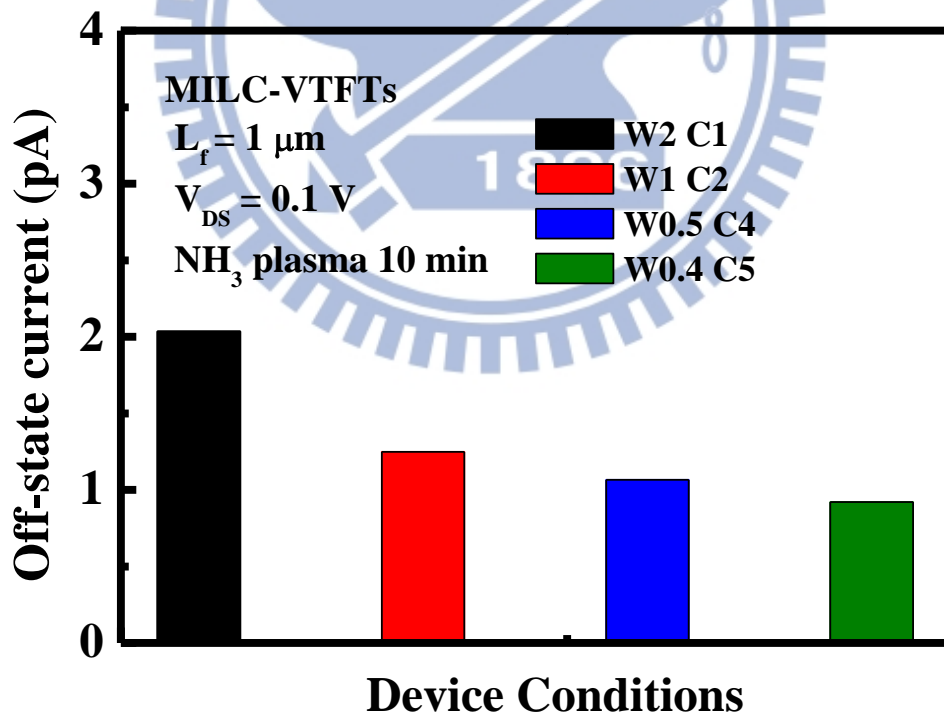
Fig. 3-5 The statistical average values of off-state current of group EW2.
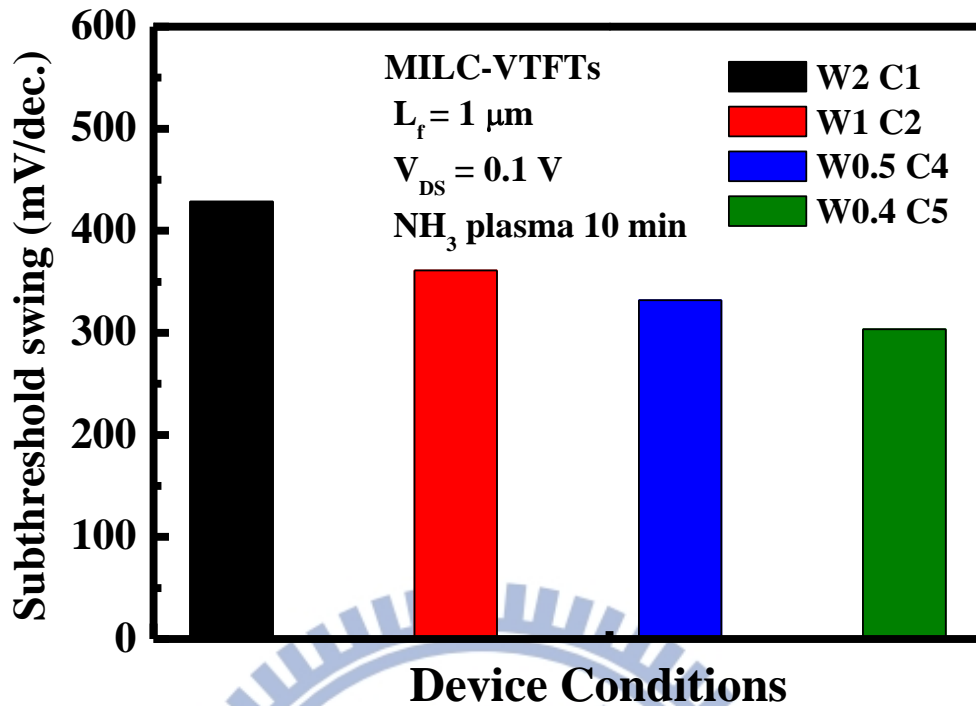
Fig. 3-6 The statistical average values of subthreshold swing of group EW2.
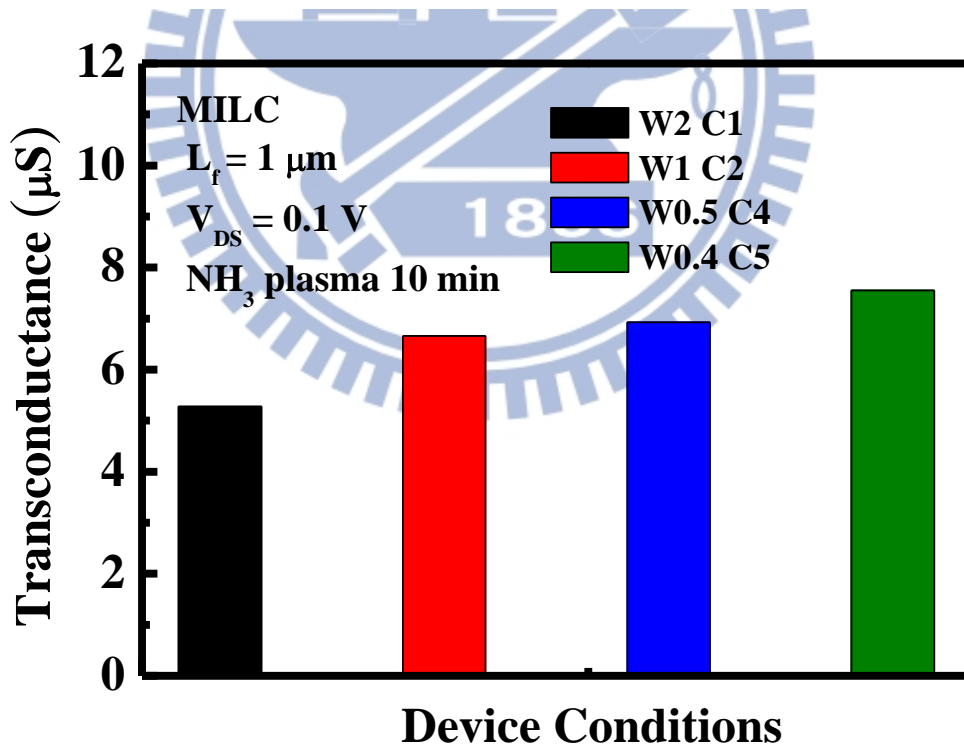
Fig. 3-7 The statistical average values of transconductance of group EW2.
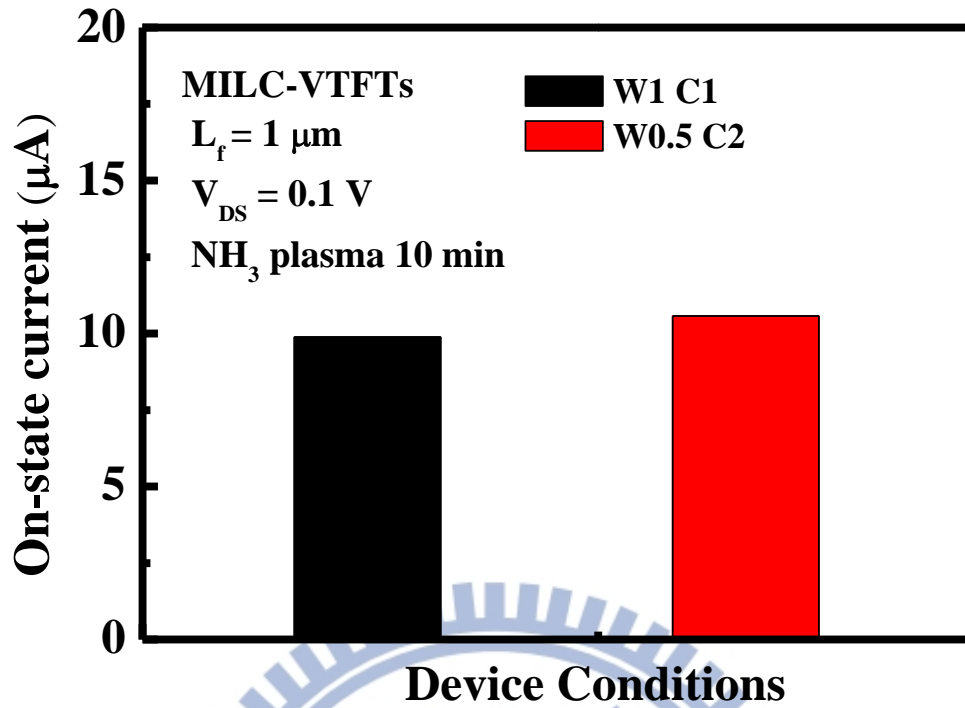
Fig. 3-8 The statistical average values of on-state current of group EW1.
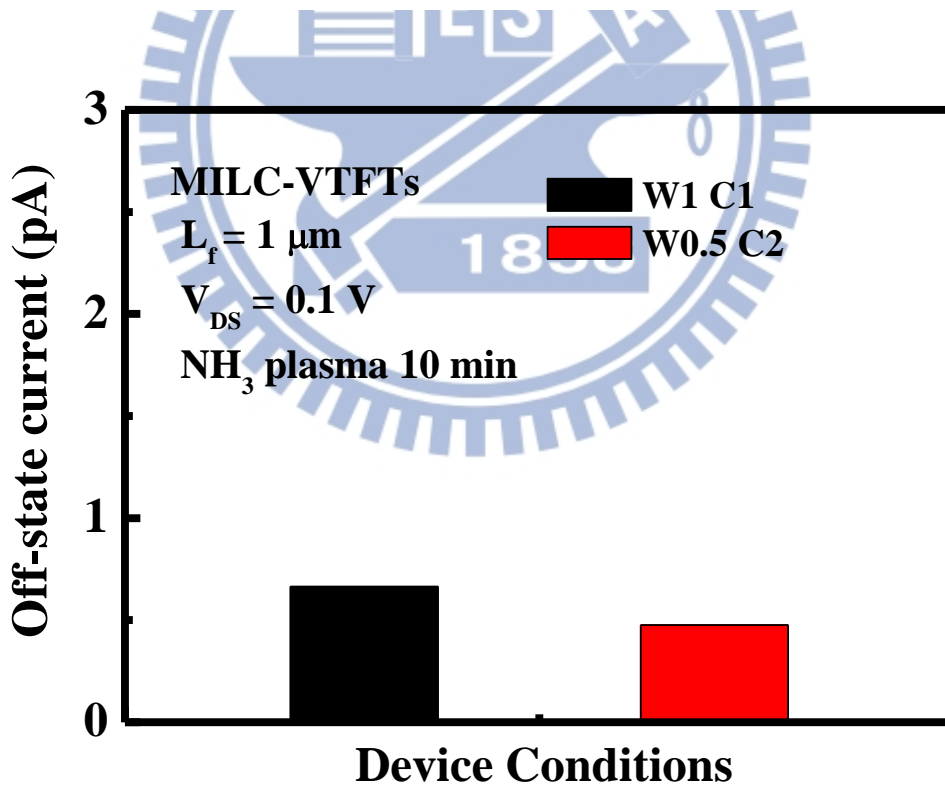
Fig. 3-9 The statistical average values of off-state current of group EW1.
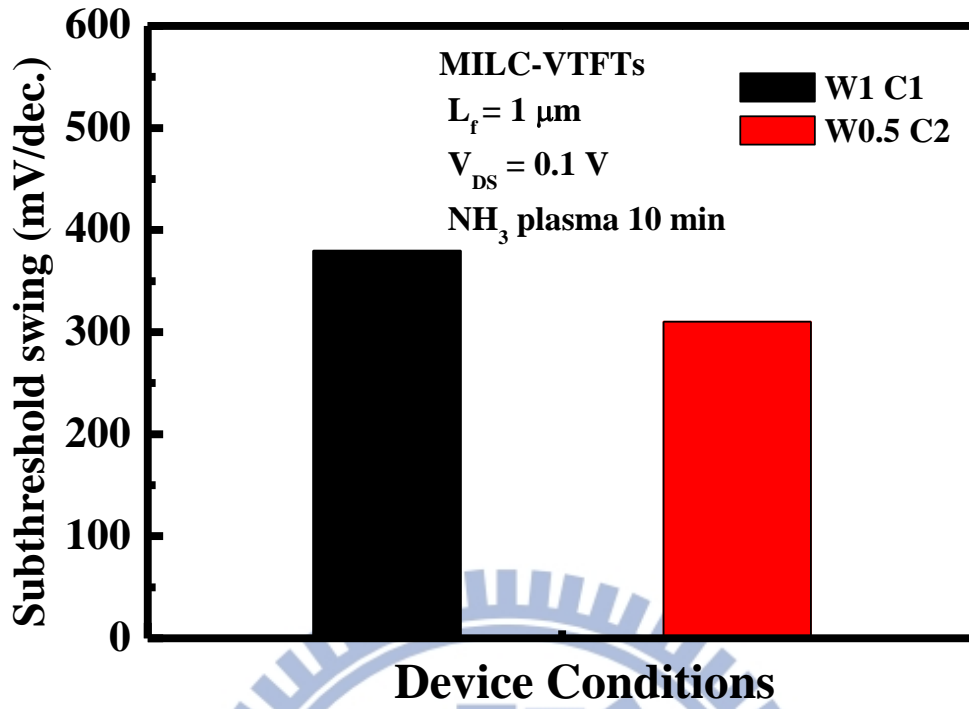
Fig. 3-10 The statistical average values of subthreshold swing of group EW1.
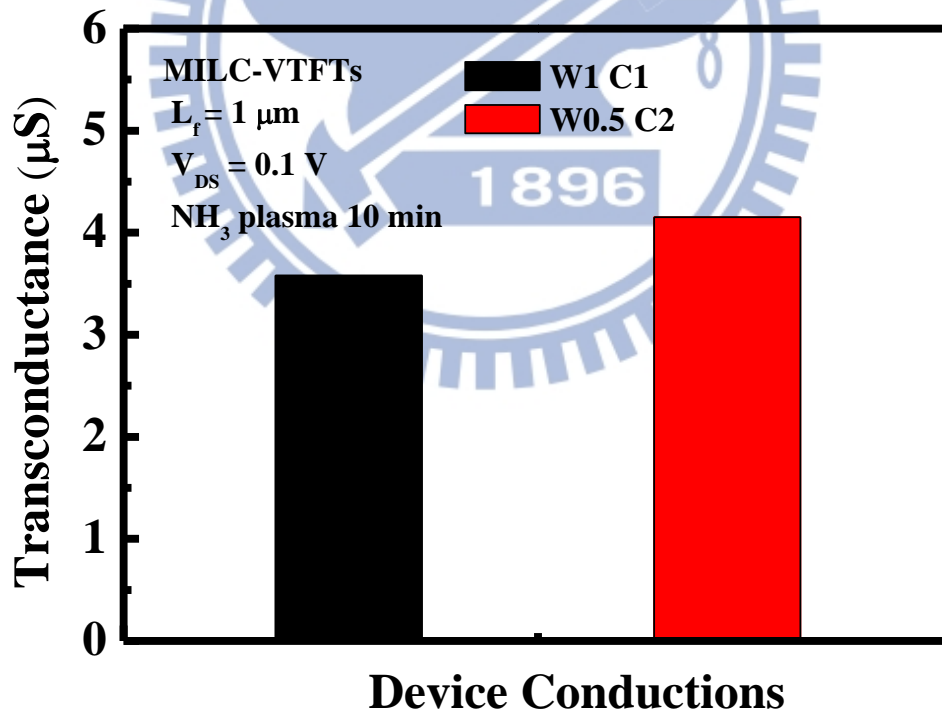
Fig. 3-11 The statistical average values of transconductance of group EW1.

Table 3-3 The statistical average value of some parameters of EW2 and EW1.

MILC-VTFT	W2C1	W1C2	W0.5C4	W0.4C5	W1C1	W0.5C2
S.S. (mV/dec.)	428.67	360.97	331.88	303.66	379.85	310.03
μ_{FE} (cm^2/V-s)	61.1	77.2	80.3	87.5	83.0	96.3
I_{on} (μA)	10.56	13.46	14.98	19.17	9.88	10.57
I_{off} (pA)	2.03	1.25	1.07	0.92	0.66	0.48
I_{on}/I_{off} ($\times 10^7$)	0.52	1.08	1.4	2.08	1.5	2.2
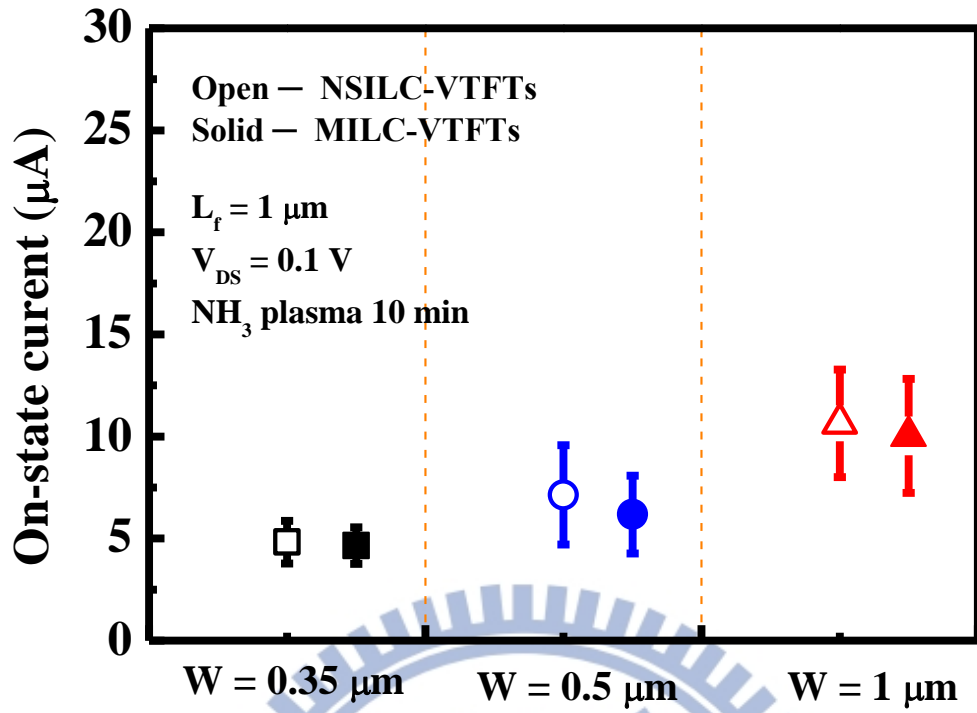
Fig. 3-12 Comparison the on-state current distribution of NSILC-VTFTs and MILC-VTFTs with various channel width.
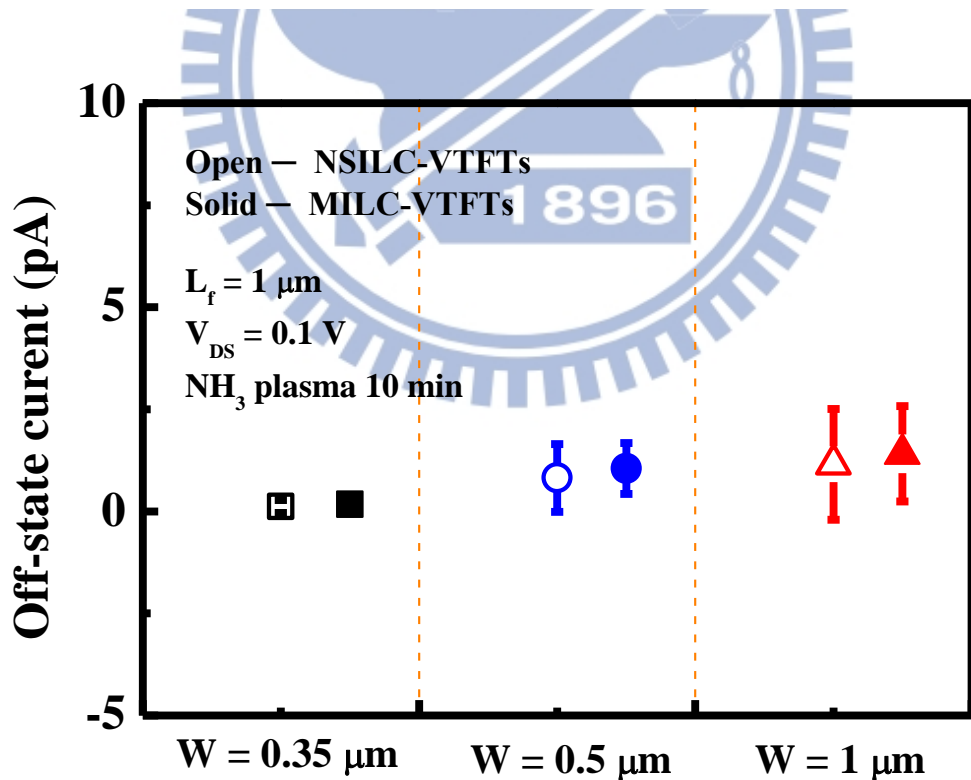
Fig. 3-13 Comparison the off-state current distribution of NSILC-VTFTs and MILC-VTFTs with various channel width.
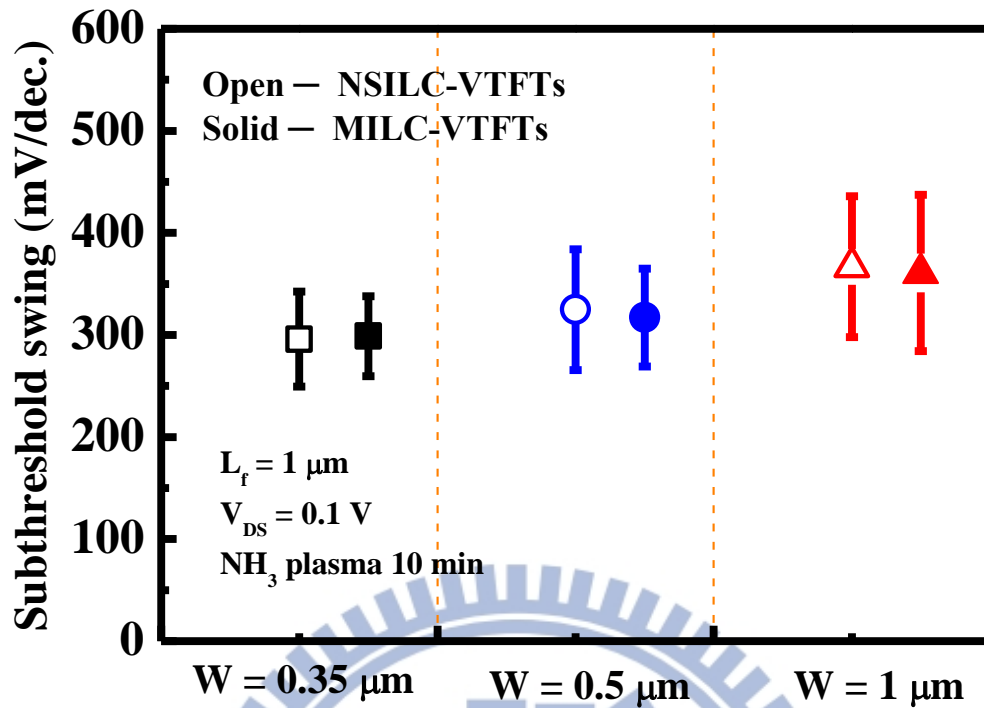
Fig. 3-14 Comparison the subthreshold swing distribution of NSILC-VTFTs and MILC-VTFTs with various channel width.
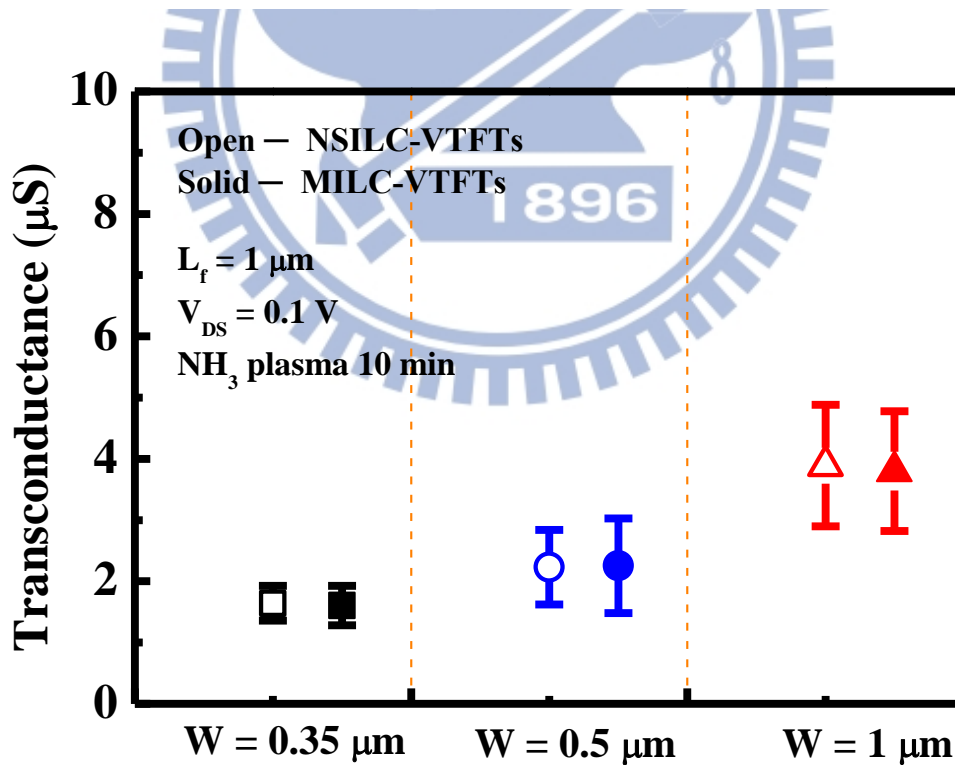
Fig. 3-15 Comparison the transconductance distribution of NSILC-VTFTs and MILC-VTFTs with various channel width.

Table 3-4 Comparison the statistical average value of NSILC-VTFTs and MILC-VTFTs with various channel width.

Condition / Parameter	W = 0.35 μm		W = 0.5 μm		W = 1 μm	
	NSILC-TFTs	MILC-VTFTs	NSILC-TFTs	MILC-VTFTs	NSILC-TFTs	MILC-VTFTs
S.S. (mV/dec.)	295.94	298.81	324.80	317.10	366.92	360.66
μ_{FE} (cm^2/V-s)	108.68	106.16	103.52	104.41	90.11	88.05
I_{on} (μA)	4.83	4.66	7.14	6.18	10.64	10.03
I_{off} (pA)	0.12	0.17	0.82	1.05	1.15	1.41
I_{on}/ I_{off} ($\times 10^7$)	4.03	2.74	0.87	0.59	0.93	0.71
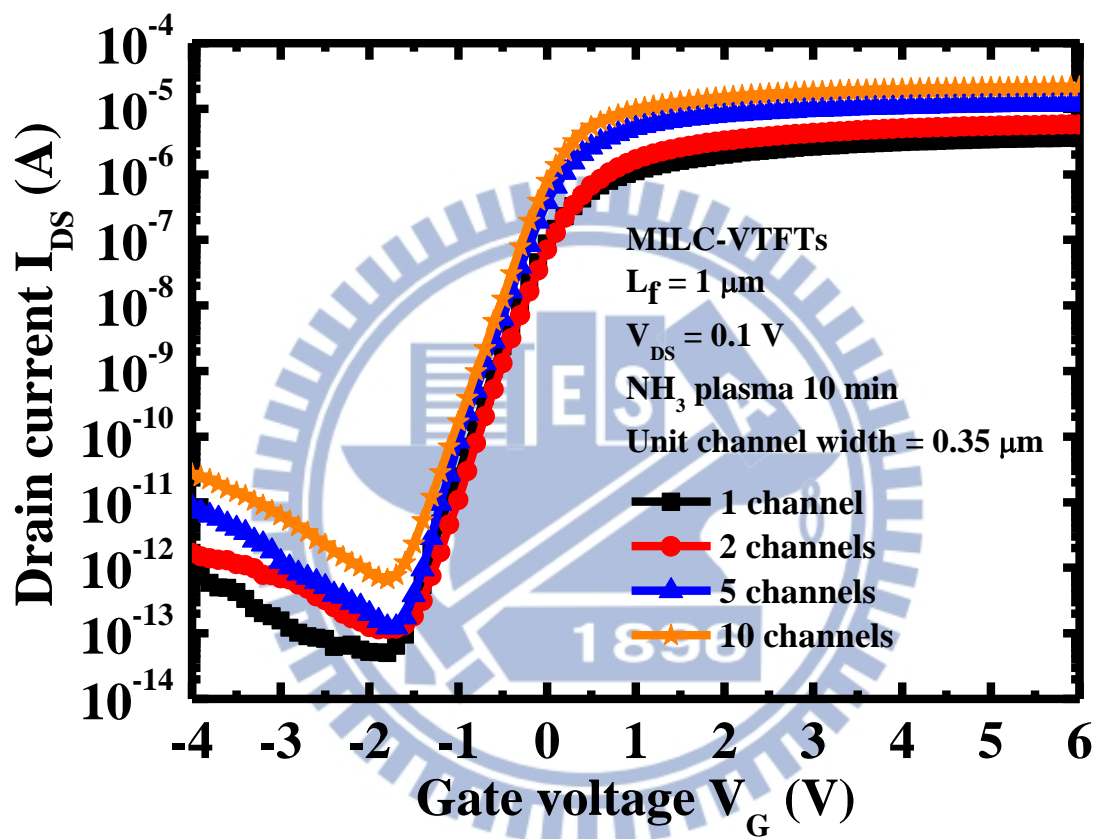
Fig. 3-16 The transfer characteristics of a MILC-VTFT with unit crystal width of 0.35 μm under various channel number.
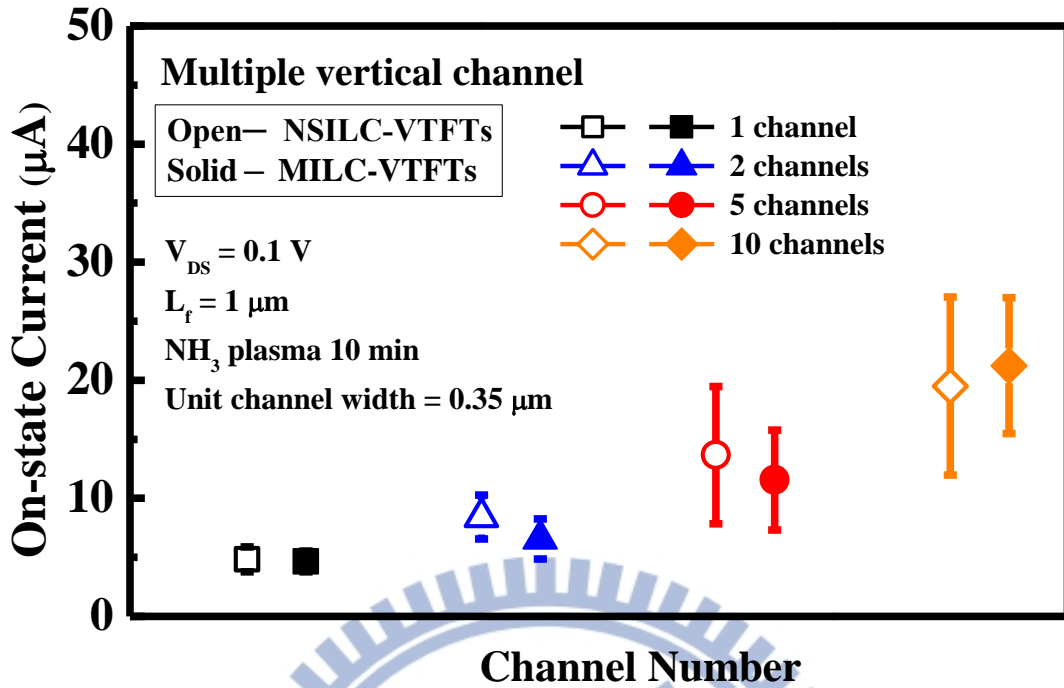
Fig. 3-17 The on-state current distribution of NSILC-VTFTs and MILC-VTFT with unit crystal width of 0.35 μm under various channel number.
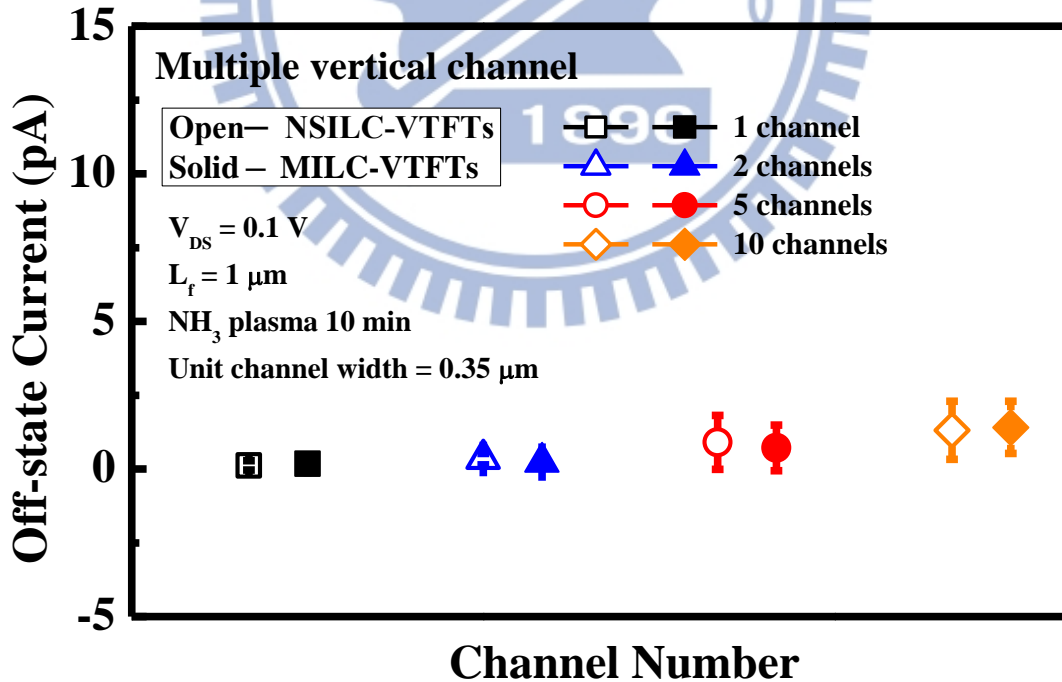
Fig. 3-18 The off-state current distribution of NSILC-VTFTs and MILC-VTFT with unit crystal width of 0.35 μm under various channel number.
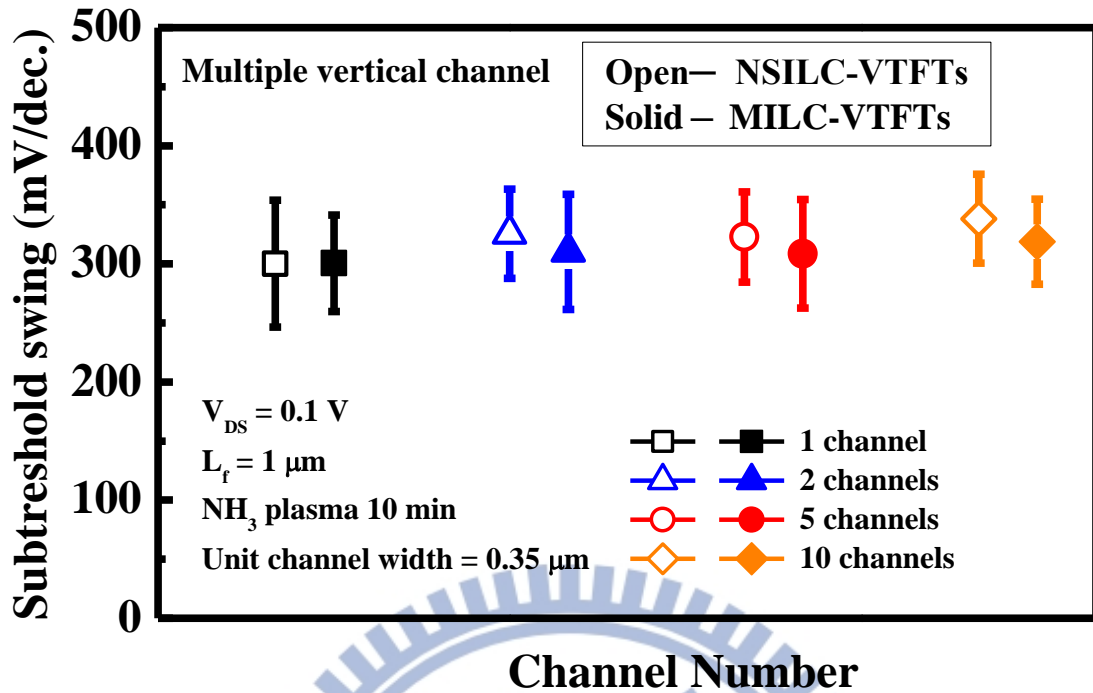
Fig. 3-19 The subthreshold swing distribution of NSILC-VTFTs and MILC-VTFT with unit crystal width of 0.35 μm under various channel number.
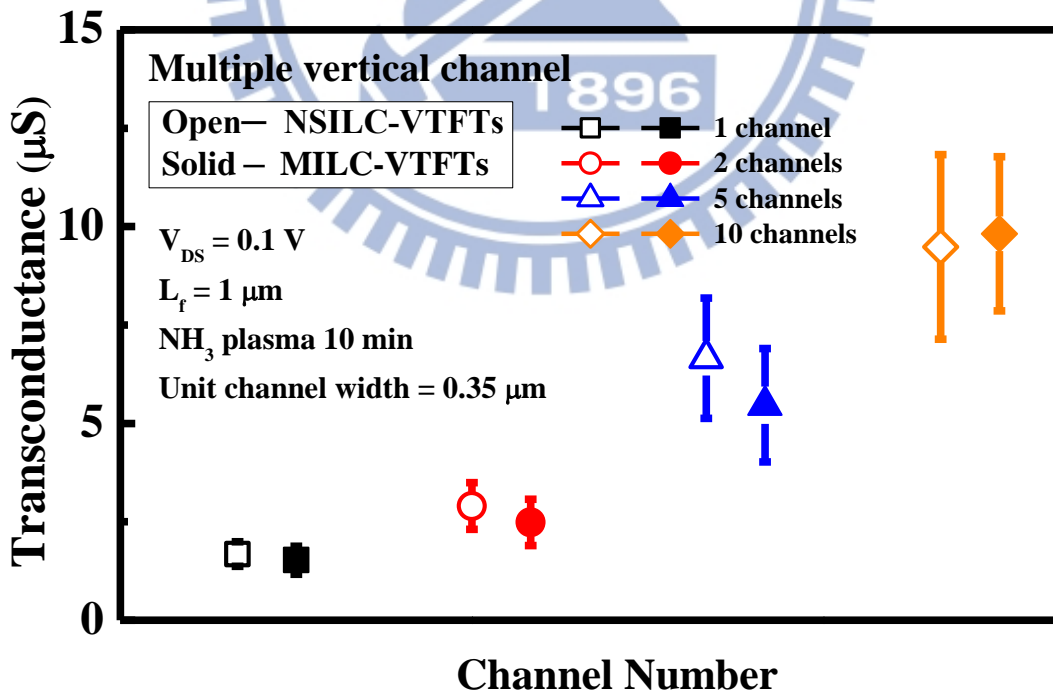
Fig. 3-20 The transconductance distribution of NSILC-VTFTs and MILC-VTFT with unit crystal width of 0.35 μm under various channel number.

Chapter 4

Conclusions and Future Works

4.1 Conclusions

In this thesis, for the first time, we have investigated the characteristic of vertical channel poly-Si thin-film transistors fabricated by MILC with crystal filtering technique. For crystal filtering technique, the narrower crystal filter width has better grain crystallization and less intra-grain, less grain boundaries defects and $NiSi_2$ contaminations in the poly-Si channel. This is attributed to the lower probability of the channel region to cover the grain boundary in narrower width devices and the channel region would have more uniform crystal growth direction than the unfiltered active layer of MILC-VTFT area. The device performance including higher on-state current, steeper subthreshold swing, lower off-state current will be improved by reducing the crystal filter width.

In this thesis, we also observe that the electrical performance of NSILC-VTFTs and MILC-VTFTs seems to be no significantly difference. In this work, we used the unilateral crystallization method to complete the channel crystallized. Therefore, the MILC/MILC grain boundary in the middle of the channel can be eliminated. Once the Ni content is provided by an appropriate amount to complete the channel crystallized, even MILC-VTFTs will be no excess Ni remaining in the channel. Therefore, the NSILC-VTFTs with Ni-silicided seeding window to limited the Ni source is not able to further improve the device characteristics. Besides, the leakage current still can be suppressed by the dual-gate structure and offset region due to reducing the lateral electrical field in the drain depletion region. Thus, the OFF-state current of these device can be reduced below 1 pA/ μm.

4.2 Future works

There are some interesting and important topics that are suggested for the future work. First of all, MILC process is used to crystallize the a-Si layer in this thesis. The on-state current limitation results from the large S/D parasitic series resistance and contact resistance, which remain problems for device scaling and reduce device performance. To decrease the parasitic resistance of the poly-Si TFTs, the fully Ni-salicided S/D and n^+ floating region is a technology to solve this problem.

Second, lower the gate height to achieve the short-channel device, which can overcome the limit of photolithography. Different gate height including 150nm, 100nm can be executed. Thus, the channel length of device can be scaled down below the limitation of I-line stepper. Besides, the lower the gate height, the easier it is to form the spacer and Ni-silicide.

Third, the reliability mechanisms of VTFTs by MILC crystallization method, such as hot carrier stress, NBTI and PBTI can be studied. And we can not only change the material of channel layer to a-Ge or III-V compound material but also change the gate dielectric layer to high-k insulators, such as Al_2O_3, Ta_2O_5 or HfO_2.

Moreover, the vertical channel structure can be applied by as a memory device. This idea is shown in Fig. 4-1. This double-gate SONOS-type TFT memory is suitable for NAND flash memory, due to simple fabrication process, multi-bit per cell and smaller bit size.
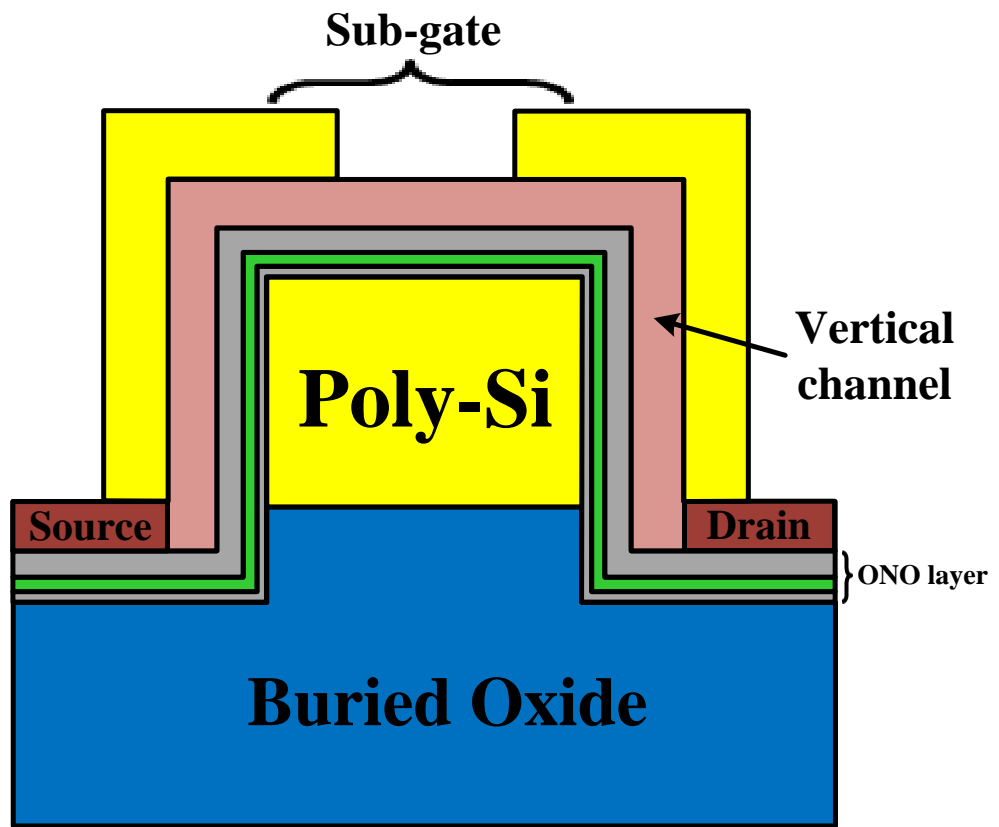
Fig. 4-1 The schematic cross-section of VTFT with O/N/O layer and double-gate.

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鎳金屬誘發側向結晶垂直通道低溫複晶矽薄膜電晶體之研究

The Study of Vertical Channel LTPS TFTs with Metal-Induced Lateral
Crystallization Method