國 立 交 通 大 學

光電工程學系碩士班

碩士論文

高效能矽披覆層非晶銦鎵鋅氧化物薄膜電晶體

High Performance Amorphous In-Ga-Zn-O Thin Film Transistor with Silicon Capping Layer

研究生: 陳良豪

指導教授:冉曉雯 教授

蔡娟娟 教授

中華民國一百零一年七月

High Performance
Amorphous In-Ga-Zn-O Thin Film Transistor
with
Silicon Capping Layer

研究生: 陳良豪　　Student：Liang-Hao Chen

指導教授：冉曉雯　教授　　Advisor：Prof. Hsiao-Wen Zan

蔡娟娟　教授　　Prof. Chuang-Chuang Tsai

A Thesis

Submitted to Electro-Optical Engineering

College of Electrical Engineering and Computer Science

National Chiao Tung University

in partial Fulfillment of Requirements

for the Degree of Master

in

Electro-Optical Engineering

July 2012

Hsinchu, Taiwan, Republic of China

中 華 民 國 一百零一 年 七 月

高效能矽披覆層非晶銦鎵鋅氧化物薄膜電晶體

研究生:陳良豪　　指導教授:冉曉雯 教授

蔡娟娟 教授

國立交通大學

光電工程學系碩士班

中文摘要

非晶氧化金屬半導體比起傳統的非晶矽半導體而言，由於具有高載子移動率(~10 cm^2/Vs)，較低的工作電壓(<5V)，以及極小的次臨界電壓擺幅，近年來被視為深具潛力的半導體材料。其可在低溫(常溫)製程下成膜與高透光的特性，也使得在顯示科技領域上有很好的運用發展性。然而非晶氧化銦鎵鋅薄膜電晶體如果想發展低功率損耗、高頻率操作的電路，則增加其載子移動率，並降低其寄生電容是必要的。

本研究中發現藉由覆蓋層矽的引入會造成載子移動率大幅的提升，推測是a-IGZO主動層中的氧轉移至覆蓋層矽上，使得a-IGZO氧空缺的數目增加，載子濃度大幅提高，導致載子移動率(mobility)變大。因此，我們提出一個加入矽做為覆蓋層的結構來提升元件的特性而不會造成元件效能的折損與漏電，此法可作為一簡單而有效的製程來提升元件效能。另外我們以共濺鍍的方式成長出更高載子移動率的非晶氧化金屬半導體，再搭配上述的覆蓋層矽，並利用改變覆蓋層的覆蓋比例與位置，探討其背後的物理機制。本研究中也試著在不影響電特性的情況下成長保護層，以期能提升元件的穩定度而能實際應用目前的顯示技術上。

High Performance Amorphous In-Ga-Zn-O Thin Film Transistor with Si Capping Layer

Student：Chun-Cheng Yeh　　Advisor: Dr. Hsiao-Wen Zan

Dr. Chuang-Chuang Tsai

Electro-Optical Engineering

National Chiao Tung University

Abstract

With a high mobility (>10 cm^2/Vs) than conventional amorphous silicon semiconductor and a low operating voltage (< 5 V) and small sub-threshold voltage swing, amorphous In-Ga-Zn-O thin-film transistors (a-IGZO TFTs) draw a lot of attentions. Besides, due to a low temperature process and high transparency, a-IGZO TFTs is suitable to develop on flexible displays. However, when a-IGZO TFTs are developed for low-power consumption, high-frequency operating of circuit, improved electron mobility and a low parasitic capacitance are required.

In this study, we found the carrier mobility significantly increase by a silicon capping layer on the back channel. We presume that the oxygen in IGZO films be captured by silicon and transfer to the silicon surface or bulk. Therefore the oxygen vacancy is created to

dramatically increase the carrier concentration and leaded the mobility significantly improved. Hence, we propose a structure with silicon capping layer onto the active layer of bottom-gate a-IGZO TFT to provide a powerful solution of enhancement of device performance that would not cause current leakage and performance degradation. The method of Si capping layer is a simple and effective approach to fabricate a feasible metal oxide transistor. Besides, we also use co-sputtered a-IGZO/IZO to improve the mobility, incorporating with the Si capping layer and changing the capping ratio or position to find the physics behind. Moreover, we try to passivate the device without changing the characteristics to improve the stability so that we could apply to the present display technology.

Acknowledgement

從大學到碩士研究生涯六年，我在交通大學中走過並經歷了人生中最重要的黃金時段。這個學校帶給我的，是充滿知性與感性的。學校的各個人、事、物，從授予我們知識的老師；陪伴著我們歡笑與流淚的同儕；一直給予我們協助的教官與行政人員；有了你們，才能有現在的我。而兩年的碩士期間，更讓我脫離了之前懵懂與不成熟的態度，雖然短暫但卻充實。很感謝冉老師與蔡老師但在這兩年中的指導與照顧，尤其是冉老師在研究上常常會有很前瞻的想法，在遇到瓶頸並與困難時都能給予我許多寶貴的意見，讓我不僅在研究上，更在處理事情的態度上都獲益良多，在此對老師獻上我最誠摯的謝意。

感謝口試委員們不辭辛勞地給予我們研究與論文上的指點與鼓勵，也很感謝研究室的大學長們，不論在生活還是實驗上給我許多寶貴的建議:感謝蔚宗學長、武衛學長、長紘學長、洪正學長、銘志學長、亭州學長、振航學長，你們的經驗與智慧讓我在研究上事半功倍；其中特別感謝長鴻學長在這兩年來實驗的協助與經驗的傳承上都不遺餘力。另外還有已畢業的碩士班學長們不辭辛勞的教導與鼓勵:家新學長、雋正學長、王辰學長、翰政學長，你們辛苦的帶領我們學會大大小小的本領，跟著你們學習的那段時間讓我永生難忘；特別感謝雋正與家新學長，你們對研究上的態度與深厚的功力都深深影響著我，感謝學長們的努力，為我帶來扎實的基礎。感謝實驗室同學們:峻宏、治寬、季遠、凱瑞、建豪，以及其他有機半導體實驗室共同打拼的夥伴，跟你們在一起做實驗

讓無塵室也有了朝氣。另外也感謝蔡娟娟實驗室的辛瑋學長、彥輝、立欣、瓊安同學，李柏璁實驗室的郭光揚學長、品睿學姊、權政同學，陳方中實驗室的亞衛學長與伯丞同學。感謝有大家的陪伴與支持，給我自信與勇氣面對重重困難。也感謝學弟即時的幫助，感謝洪銓、明諺、正強、徐雍，與其他學弟妹們，希望大家在未來的研究上都能順順利利。另外還有兩年來一直在身邊陪伴著我的室友們，明璿、輔仁、智恆、耀嘉，在我沒做研究的時間總能陪著我一起歡笑。

最後要感謝我的父母，給我支持與鼓勵，讓我可以無後顧之憂的完成學業。

陳良豪 2012 於交映樓

Contents

Figure Captions

Table Captions

Chapter 1 Introduction

1-1 Introduction

1-1.1 Advantage of metal oxide transistors

Metal oxide semiconductor was early reported in 1951 by E. E. Hahn [1]. The material of metal oxide composed of heavy metal cations with an electronic configuration $(n - 1)d^{10} ns^{0}$ ($n \geq 4$) are promising candidate for next generation semiconductor. [2] These ns orbitals have large radius, so that there is a large overlap between the adjacent orbitals shows in Fig. 1.1. Over the past few years, several oxide materials are reported to be the channel material in TFTs. The polycrystalline zinc oxide (ZnO) [3], amorphous zinc tin oxide (ZTO) [4], amorphous zinc indium oxide (ZIO) [5], and amorphous indium gallium zinc oxide (IGZO) [6-8] are proposed to be the active layer in transparent TFTs. Among the transparent oxide channel materials, amorphous indium gallium zinc oxide (a-IGZO) applied to thin film transistors (TFTs) has drawn considerable attention due to their high mobility, good transparency, and unique electrical properties. [2] Moreover, the amorphous type of a-IGZO was insensitiveness to the distorted metal–oxygen-metal chemical bonds. [2] Large band gap (>3eV) induces that the a-IGZO material was insensitive to the ambient light and transparent in visible region (400nm~700nm). The carrier contraction (n: 10^{13}~10^{20} cm^{-3}) in the a-IGZO film was tunable by controlling the oxygen pressure during film deposition [9].

When a-IGZO TFTs is applied to temperature limited substrates like flexible substrate, the radio-frequency (rf) sputtering technique is one of a few methods which enables us to deposit thin films of high-melting-temperature materials over large areas at low substrate temperatures. [10] However, H. Hosono et al. proposed that the chemical species and/or a structure in a thin film are naturally unstable when thin films are deposited at low temperatures. [10, 11]

Additionally, they are stable while thin films are deposited at higher temperatures. The chemical species and/or a structure are frozen in the as-deposited thin film which relax to a more stable state and /or give the atoms more energy to rearrange upon thermal annealing, leading to an appreciable change in the electron transport properties. [10, 11] Most oxide TFTs, especially a-IGZO TFTs, are fabricated using physical vapor deposition (PVD) techniques at room temperature and often require a high temperature post-deposition thermal annealing process to get high-performance and high-stability TFTs. [10-16] Among the post-deposition thermal annealing techniques, rapid thermal annealing (RTA) [14, 15] or furnace annealing [16] are usually used to anneal the oxide TFT devices. For the application of a-IGZO TFTs which is fabricated on the temperature limited flexible substrate, high temperature thermal annealing may damage the substrates. Development of the annealing method at low substrate temperature is essential when applying a-IGZO TFTs to flexible and temperature limited substrates

1-1.2 Carrier transmission mechanisms of a-IGZO metal oxide semiconductors

The carrier transport mechanism in amorphous oxide semiconductor, such as a-IGZO, was discussed in this section. Before reporting the a-IGZO mechanism, the transport mechanism of hydrogenated amorphous silicon (a-Si:H) for flexible TFTs will be described briefly. As shown in Fig. 1.2, the carrier transport paths in a-Si:H composed with covalent bonds of sp^3 orbitals was affected obviously by strong spatial directivity and disorder structure. The electronic levels and trap states was influenced by the fluctuation of the bonding angle in the a-Si:H structure. [17] Compare with the a-Si:H, the characteristics in amorphous oxide semiconductors (AOSs) are different from the semiconductors with covalent bonds. The carrier transport path in AOSs was shown in Fig. 1.3. The bottom of the conduction band in the oxide semiconductors that has

large ionicity is primarily composed by spatially spread metal ns (here n is the principal quantum number) orbitals with isotropic shape. [17] Their overlaps with neighboring metal s orbitals are not altered by disordered amorphous structures. Based on these facts, the necessary condition for good conductivity in a-IGZO is that the conduction paths should be composed of the ns orbitals. The principal quantum number is at least 5 [18] and direct overlap among the neighbor metal ns orbitals is possible. The magnitude of this overlap is insensitiveness to distorted metal–oxygen–metal (M–O–M) chemical bonds that intrinsically exist in amorphous materials. [19] The amorphous oxide semiconductors (AOSs) containing post-transition-metal cations was possible to show the degenerate band conduction and high mobility (>10 cm^2/Vs).

The carrier transport mechanism and electronic structure in an amorphous indium gallium zinc oxide semiconductor, from the Fig. 1.4, the Hall mobility of a-IGZO is increased distinctly from ~3 $cm^2 (Vs)^{-1}$ to 13 $cm^2 (Vs)^{-1}$ as carrier concentration increased from 10^{15} cm^{-3} to 10^{19} cm^{-3}. The carrier transport mechanism and electronic structure in an amorphous oxide semiconductor is similar to that of crystalline IGZO, and is explained by percolation conduction through potential barriers in the vicinity of conduction band edge. The potential barriers are thought to originate from random distribution of Ga^{3+} and Zn^{2+} ions in the $GaO^+(ZnO)_5$ layer. The effective mass of a-IGZO was 0.34 m_e, which is almost the same as that of crystalline IGZO. These results imply the electronic structure and carrier transport mechanism in a- IGZO are similar to that in sc-IGZO, which would be associated with the electronic structure of metal-oxide semiconductors in which electron transport paths are made of spherical extended s orbitals and are not largely affected by local distortion of the chemical bonds. [20] We can see that the intermediate region in Fig. 1.5 (10^{14} $cm^{-3}<N_e<N_{th}$), the carriers still need to flow over the potential barriers as E_F is below E_{th}, leading to the thermally activated percolation behaviors in μ and σ. When E_F exceeds E_{th} at $N_e>N_{th}$, the carriers are not affected by potential barriers anymore and exhibit the temperature-independent extended mobility.

Each sub-element in this ternary material of a-IGZO film shows various characteristics to affect the parameters of TFTs. Higher concentration of In atom is expected to generate higher carrier concentration. [21] It is because that the element of In is a big atom and easy to lose electrons, however the oxygen is a small atom and easy to get electrons form In atoms. The released electron from the element of In may move to the conduction band when the composition of a-IGZO lacked for oxygen. [9] Moreover, it will increase the electron concentration of a-IGZO TFTs. On the contrary, the element of Ga was introduced provide high stability in a-IGZO TFTs. [22] Therefore, the element of Ga in the a-IGZO film was reducing the electron concentration and decreasing the carrier mobility. The Ga was chosen because of atomic radius of Ga closed to In. H. Hosono *et al*. reported that the Ga^{3+} in the a-IGZO film attract the oxygen tightly due to the high ionic potential resulted from the small ionic radius and +3 valence. It suppresses the electron injection and induces the oxygen ions escaping from the a-IGZO film. [23] Compare to the carrier concentration in the material of IZO (~10^{21} cm^{-3}), the a-IGZO (~10^{19} cm^{-3}) shows less carrier concentration and is reported in some researches. [23-26] Introducing the element of Ga to the a-IGZO film helps the carrier concentration of the a-IGZO film to be controlled easily. However, the mobility is reduced while the Ga is introduced to the a-IGZO film. H. Hosono *et al.* proposed that when the element of Ga was introduced the a-IGZO film, the carrier concentration and carrier mobility is increased by doping the oxygen molecules. [27] The element of Zn in the a-IGZO film was reported to affect the crystallization of the metal-oxide thin film. When the ratio of the Zn atoms in the a-IGZO film is larger than 65%, the film is became more crystalline structure. [9] The crystalline structure in the a-IGZO film may degrade the electrical characteristic while the uniformity was decreased by the disorder grain boundaries.

1-1.3 Carrier concentration with oxygen vacancy of a-IGZO films

The oxygen vacancy formation process closely relates to the generation of charge carriers, according to Equation (1).

$$O_o^x = \frac{1}{2} O_{2(g)} + V_o^{\bullet\bullet} + 2e^- \quad \text{.....(1)}$$

Here, O_2 is lost from the oxide sublattice (O^x_o) to create a doubly charged oxygen vacancy ($V^{"}_o$) and two free electrons. It can be presumed that IGZO films attain more charge carriers due to thermally enhanced or energy activated oxygen vacancy formation processes. It has been reported that the mobility of amorphous IGZO films depends on the carrier concentration, since the carrier transport is governed by percolation conduction over trap states and is enhanced at high carrier concentrations by filling the trap states.

In order to understand oxygen vacancy in a-IGZO films, the chemical and the oxygen binding energy of O_{1s} were analyzed by X-ray photoelectron spectroscopy (XPS). This analysis method had been used to investigate the origin of carriers in IGZO. The O 1s peak can be fitted to three nearly Voigt functions, centered at 530.15±0.15, 531.25±0.2, and 532.4±0.15 eV, respectively [28]. The highest binding energy (BE) located at 532.4±0.15 eV indicates the presence of loosely bond oxygen on the surface of the metal oxide film. This oxygen belongs to a specific species, $-CO_3$, which is adsorbed H_2O or adsorbed O_2 [28, 29, 30]. The lowest BE, which occurs at 530.15±0.15 eV, is attributed to O^{2-} ions surrounded by In, Ga, or Zn atoms with their full complement of nearest-neighbor O^{2-} ions [28, 30]. The medium BE centered at 531.25±0.2 eV may be associated with O^{2-} ions in the oxygen-deficient regions within the matrix. The variation intensity of the medium BE is connected to the concentration of oxygen vacancies [28, 30]. Generally, metal oxide films with a higher concentration of oxygen vacancies exhibit higher carrier concentration and conductivity.

1-1.4 Back channel effect associated with the electrical performance of oxide transistors

Recently, a few research groups have reported that the adsorbed molecules such as oxygen (O_2)、hydrogen (H_2) and water (H_2O) are strongly associated with the electrical performance of metal-oxide transistors [31]. Gas molecules are well-known to play an important role in carrier transport even at room temperature. The adsorbed oxygen depleted the electron carriers on the *a*-IGZO film, the water molecules induced the formation of an accumulation layer of extra electron carriers. Moreover, severe degradation of the performance of organic transistors has frequently been reported under ambient environments. Ambient conditions may cause the formation of hydrogen-related metastable hole traps in organic semiconductors.

1-2 Motivation

The a-IGZO is promising semiconductor material because of a high mobility (>10 cm^2/Vs) ,a low threshold voltage (< 5 V), and low temperature fabrication processes. The applications on display, a-IGZO TFTs are also promising for the development of RFID tag, smart cards, or other kinds of flexible electronics. However, when a-IGZO TFTs are developed for a low-power high-frequency circuit, improved electron mobility and a low parasitic capacitance are required.

The field effect mobility of a-IGZO TFT influenced by the capping layer is an important topic to investigate. Silicon is a well-used and cheap material, and a simple structure which could highly improve mobility of metal oxide TFT by only introducing a silicon capping layer on the channel region. With the aid of it, we could look forward to a high resolution and small response time flexible display.

1-3 FIGURES OF CHAPTER 1

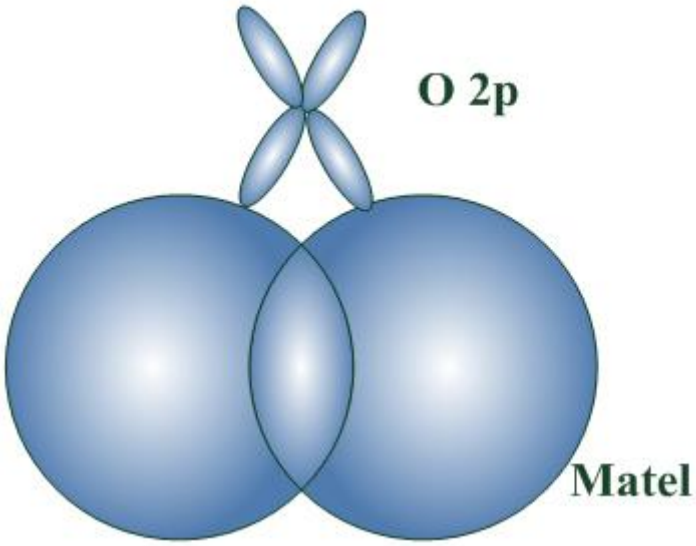


Fig. 1.1 The overlap between the adjacent orbitals [2].

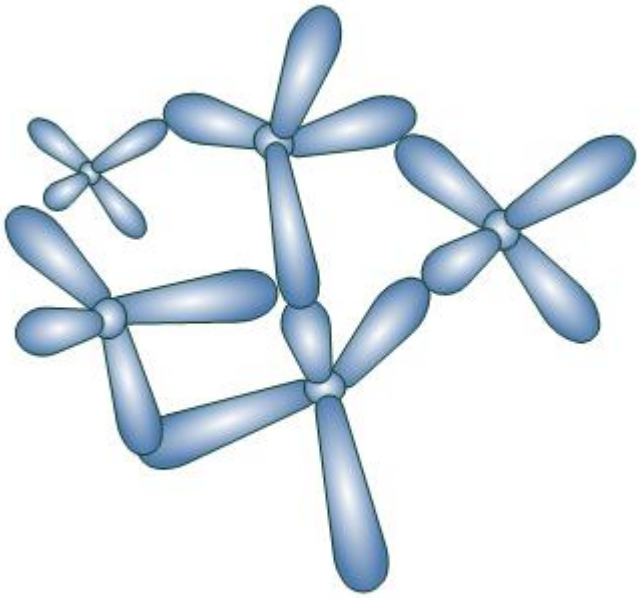


Fig. 1.2 The carrier transport paths in covalent semiconductors [16].

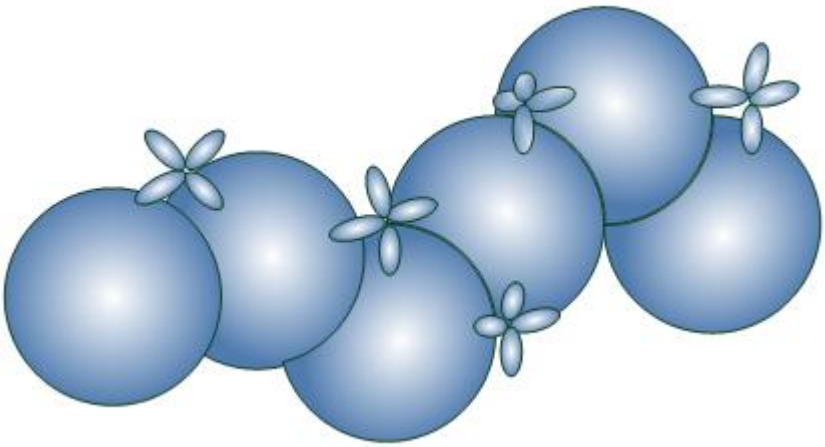


Fig. 1.3 The carrier transport paths in AOSs [16].

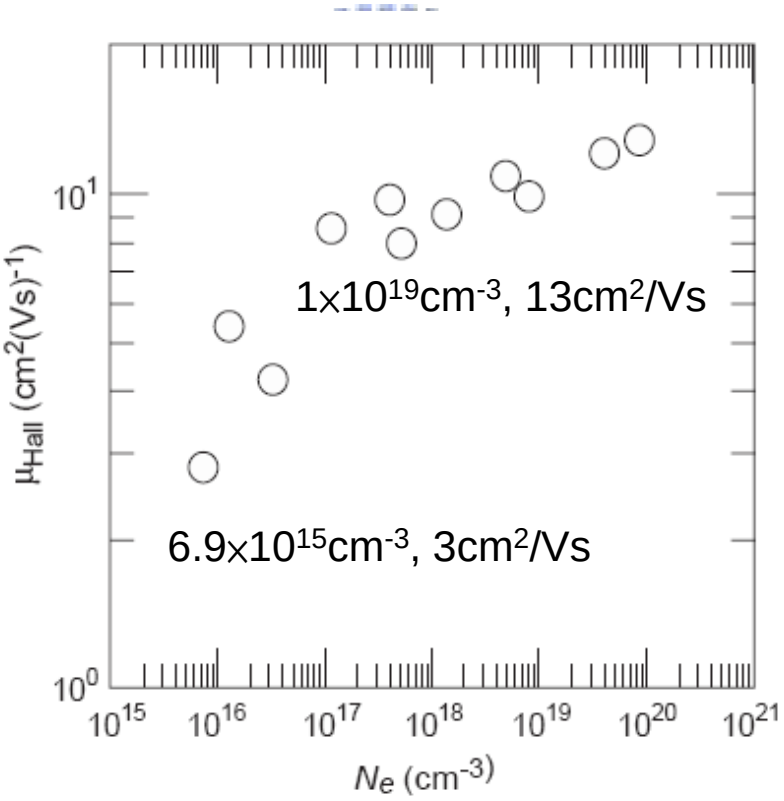


Fig. 1.4 Hall mobility at RT as a function of carrier concentration [19]

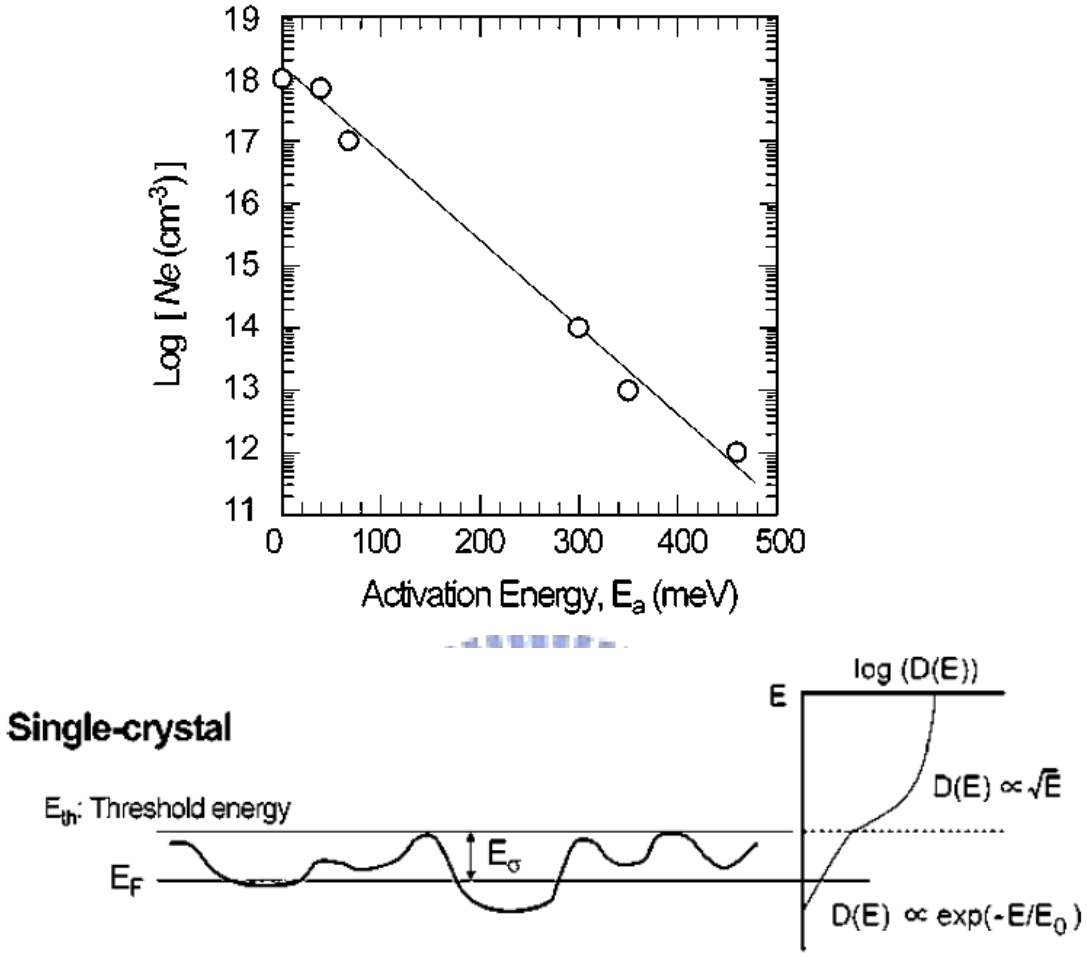


Fig. 1.5 (a) The relationship between log(Ne) and activation energy (Ea). The straight line is the result fitted to the exponential tail density of state model. (b) Schematic energy diagram near the conduction band edge and the density of state for sc-IGZO [20].

Chapter 2 EXPERIMENTAL PROCEDURE

2-1 Device structure and fabrication

Heavily doped p-type Si (100) was used as a substrate and a gate electrode. Figure 2.1 (a) shows a schematic cross-section of the top-contact bottom-gate a-IGZO TFT structure (b) Si-capped top-contact bottom-gate a-IGZO TFT structure are used in this study. The process flow is shown in Fig. 2.2. The detail fabrication process including dielectric deposition, a-IGZO film deposition, source/drain deposition, Si capping layer deposition and passivation layer deposition are described in the following sections.

2-1.1 Dielectric deposition

The dielectric silicon nitride (SiNx) was formed on all samples with 1000 Å using Horizontal Furnace. Before deposition the active layer, the standard clean was carried out to remove the contamination on the dielectric surface. The standard clean is accomplished in two steps, SC1 and SC2. SC1 clean is the first step to remove the particle on the surface. The process was executed with a mixture of ammonium hydroxide, an oxidant hydrogen peroxide, and water in a mixing ratio of 1:4:20.

$$NH_4OH:H_2O_2:H_2O = 1:4:20 \text{ (SC1)}$$

The SC2 clean was used to remove metals from the surface. The cleaning process inSC2 contain three solution of HCl, hydrogen peroxide, and water. The mixture ratio inthe SC2 process was 1:1:6.

$$HCl:H_2O_2:H_2O = 1:1:6 \text{ (SC2)}$$

2-1.2 Substrate clean

Before deposition the active layer, the standard clean was carried out to remove the contamination on the dielectric surface. The standard clean is accomplished in two steps, SC1 and SC2. SC1 clean is the first step to remove the particle on the surface. The process was executed with a mixture of ammonium hydroxide, an oxidant hydrogen peroxide, and water in a mixing ratio of 1:4:20.

$$NH_4OH:H_2O_2:H_2O = 1:4:20 \text{ (SC1)}$$

The SC2 clean was used to remove metals from the surface. The cleaning process in SC2 contain three solution of HCl, hydrogen peroxide, and water. The mixture ratio in the SC2 process was 1:1:6.

$$HCl:H_2O_2:H_2O = 1:1:6 \text{ (SC2)}$$

There are two steps to clean and remove particle and organic pollution on Glass substrate (CORNING EAGLE 2000). The roughness of glass substrate is important for metal deposition and metal adhesion.

The glass cleaning steps are as follow:

Steps:

(1) Glass substrates are place of the DI water current flow for 5 minutes in order to remove the particles.

(2) Put the glass substrates in the acetone with ultrasonic resonance for 5minutes to remove the organic pollution

(3) Put the glass substrates under the DI water current flow for 5 minutes to remove the solvent.

(4) Put the glass substrates in the KG detergent with ultrasonic resonance for 1 minute in order to remove the particles, fingerprint and some metal ionic.

(5) Put the glass substrates under the DI water with ultrasonic resonance for 1 minute twice to remove the residual solvent.

(6) Dry the glass substrates with N_2 flow to blow off the water drop on the substrates

(7) Put the glass substrates on the hot plate at 120℃ for 3 minutes to remove the moisture. Naturally cool down to the room temperature.

2-1.3 a-IGZO film deposition

Generally, pulsed laser deposition (PLD) and ratio frequency (RF) –magnetron sputter were reported to deposit a-IGZO film as channel [33, 34]. In this study, the rf-sputter with 3-in. circular target: In_2O_3:Ga_2O_3:ZnO = 1:1:1 wt.% was used to deposit the a-IGZO film. 30nm a-IGZO channel layer was deposited at room temperature with a power of 100W, a working pressure of 9mTorr, and an Ar/O_2 flow rate of 30/0. The active layer patterning was defined using a shadow mask.

RF sputtering (Fig. 2.3) is a process using radio frequency power supply, operating at 13.56MHz, to generate plasma in which atoms, ions, and clusters are created to sputter the target material. The glow-discharge between a target and a substrate, it's consists of plasma with an equal number of working gas (Ar) and electrons. The ions are accelerated towards to the target by a strong electric field on the target due to the flux of electrons. Consequently, the ions hit the target to eject the target atoms, which are then re-deposited onto the substrate. RF sputtering is performed at low pressure, to increase the mean free path, the distance between collisions, and to improve the quality of the deposited film.

2-1.4 Source/Drain deposition

The metal in source/drain contacts was deposited using thermal evaporator. The base

pressure of the thermal evaporator is 4×10^{-6}torr, and 50nm-thick Aluminum (Al) is deposited through a shadow mask to form the source and drain contacts.

2-1.5 Post-annealing

After deposition of the electrodes, post-annealing is carried out in the furnace. The annealing process at 400℃ in nitrogen (N_2) furnace for 1hr, the base pressure is atmospheric pressure, and the N_2 flow rate is 10 liter per minute (L/min).

2-1.6 Si capping layer deposition

A silicon layer evaporated at the middle of source/drain metal without any contact to source/drain metal at room temperature through a shadow mask. The deposition was started at 5×10^{-6}torr and rate was controlled at 0.25Å /s.

2-1.7 Passivation layer deposition

To reduce the effect of the ambient atmosphere under bias stress, the passivation layer here might play an important role to prevent the adsorption/desorption dynamics of water and oxygen molecules onto the exposed back-channel region of our devices. In many researches, organic materials like photoresists(PR) or PVP and inorganic materials like Al_2O_3 or SiO_2 were widely used [32, 33]. In this work, both STD device and Si-capped device were passivated with photoresist (AZ4620) and SiO_2.

The PR passivation layer was formed in the final step by spin coating and then baking at 120℃ for 15 minutes on the hot plate in the air with its thickness of about 7μm. The device structure is showed in Fig. 2.4.

The SiO_2 passivation was deposited by thermal evaporator with its thickness of about

80nm (in this case the thickness of source and drain were reduced to 40nm). For a better insulator quality of SiO_2 layer, the post annealing step mentioned before was right after this process, and then deposited the Si capping layer (no addition annealing was needed before SiO_2 layer). The devices structures are showed in Fig. 2.5, where the SiO_2 layer covers almost all the a-IGZO film except a channel of 150μm in the middle region.

2-2 Analysis instrument

2-2.1 Current-Voltage measurement instrument

In this study, all electrical characteristics were measured by semiconductor parameter analyzer (Agilent 4156) at room temperature in ambient air.

2-2.2 X-ray photoelectron spectroscopy (XPS) analysis

X-ray photoelectron spectroscopy (XPS) is a quantitative spectroscopic technique that measures the elemental composition, empirical formula, chemical state and electronic state of the elements that exist within a material. XPS spectra are obtained by irradiating a material with a beam of X-rays while simultaneously measuring the kinetic energyand number of electrons that escape from the top 1 to 10 nm of the material being analyzed. XPS requires ultra high vacuum (UHV) conditions. XPS is a surface chemical analysis technique that can be used to analyze the surface chemistry of a material in its "as received" state, or after some treatment, for example: fracturing, cutting or scraping in air or UHV to expose the bulk chemistry, ion beam etching to clean off some of the surface contamination, exposure to heat to study the changes due to heating, exposure to reactive gases or solutions, exposure to ion beam implant, exposure to ultraviolet light.

2-3 Methods of device parameters extraction

In this section, the extractions of the device parameters are discussed in details. The field effect mobility, threshold voltage (V_{TH}), turn on voltage (V_{on}), the on/off current ratio (I_{on}/I_{off}), the sub-threshold swing (S.S) are extracted and assessed, respectively.

2-3.1 Mobility

Mobility is a measurement of the velocity of the carrier move through a Material. A higher mobility allows for higher frequency response such as the time it takes for the device to transfer from off state to on state. In the off state, few current flows through the device. In the on state, large amount of currents flow through the device. A large mobility means the device can conduct more current. The mobility in this study was extracted from the saturation region. The device was operated at drain-voltage of 20V, since the threshold voltage was much lower than 20V. The saturation mobility is determined from the transconductance, define by

$$gm = [\frac{\partial \sqrt{I_D}}{\partial V_G}]_{V_D=const} \quad (2.1)$$

The drift component of drain current is

$$I_D = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS} - V_{TH})^2 \quad (2.2)$$

When the mobility is determined, the transconductance is usually taken to be

$$gm = \sqrt{\frac{W\mu C_{ox}}{2L}} \quad (2.3)$$

When this expression is solved for the mobility, it is known as the saturation mobility

$$\mu_{sat} = [\frac{2g_m^{\ 2}}{\frac{W}{L}C_{OX}}]_{Saturation} \quad (2.4)$$

2-3.2 Turn-on voltage (Von)

Turn-on voltage (V_{on}) is identified as the gate voltage (V_{GS}) at which the drain current begins to increase in a transfer curve. V_{on} can directly characterizes the V_{GS} required to fully“turn off” the transistor in a switching application.

2-3.3 Threshold voltage (Vth)

Threshold voltage is related to the operation voltage and power consumptions of TFTs. We extract the threshold voltage from equation (2.5), the intercept point of the square-root of drain current versus voltage when devices operate in saturation mode.

$$\sqrt{I_D} = \sqrt{\frac{W}{2L}\mu C_{OX}(V_G - V_{TH})} \quad (2.5)$$

2-3.4 Ion/Ioff current ratio

The I_{on}/I_{off} (on/off) ratio represents large turn-on current and small off current. It is an indicator of how well a device will work as a switch. A large on/off current ration means there are enough turn-on current to drive the pixel and low off current to maintain in low consumption.

2-3.5 Sub-threshold swing (S.S)

Another important characteristic for device application is sub-threshold swing. It is a measurement of how rapidly the device switches from off state to on state. Moreover, the sub-threshold swing also represents the interface quality and the defect density.

$$S = [\frac{\partial(\log I_D)}{\partial V_G}]_{V_D=const} \quad (2\text{-}1)$$

If we want to have a better performance TFTs, we need to lower the sub-threshold swing.

2-4 FIGURE OF CHAPTER 2

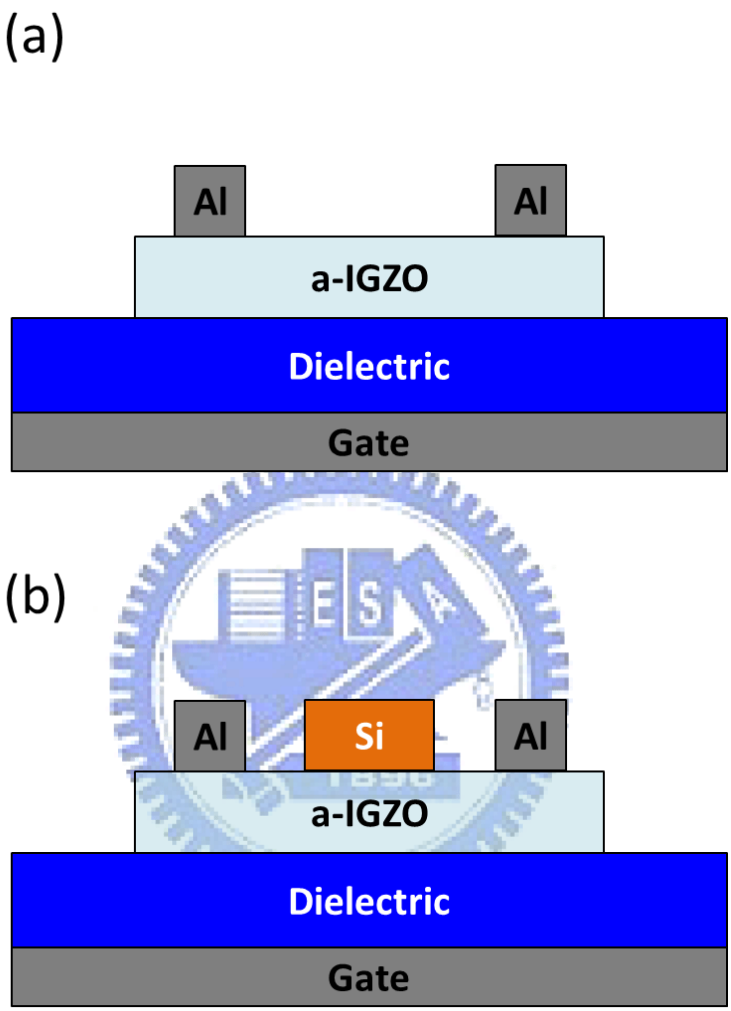


Fig. 2.1 The schematic cross-section of the (a) conventional top-contact bottom-gate a-IGZO TFT. (b) Si-capped the top-contact bottom-gate a-IGZO TFT.

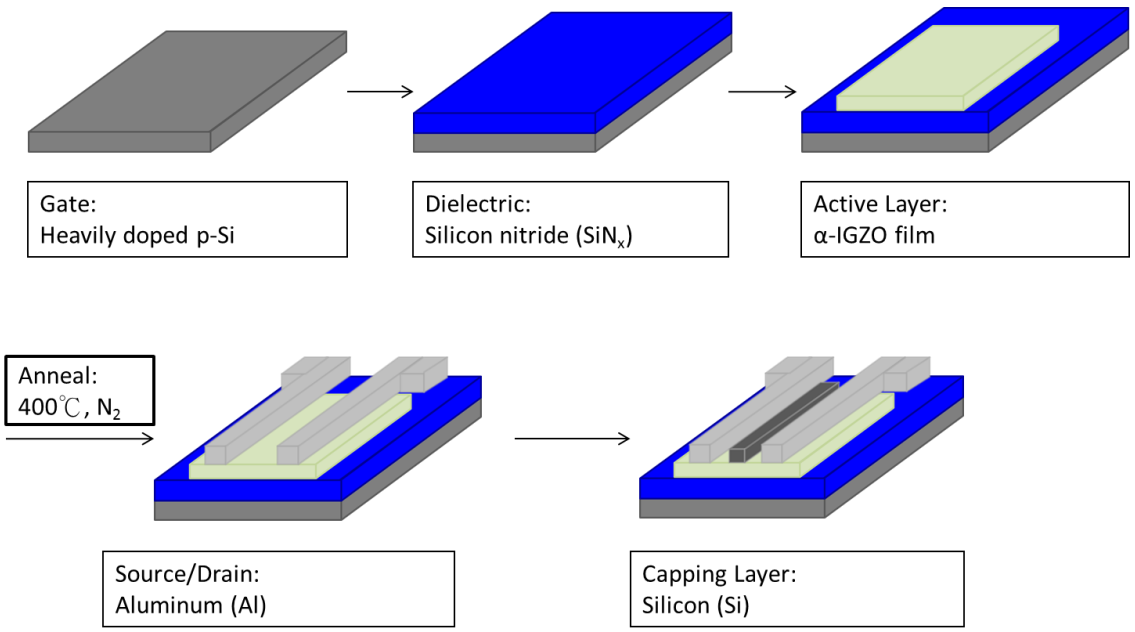


Fig. 2.2 The process flow of conventional top-contact bottom-gate a-IGZO TFT with Si capping layer.

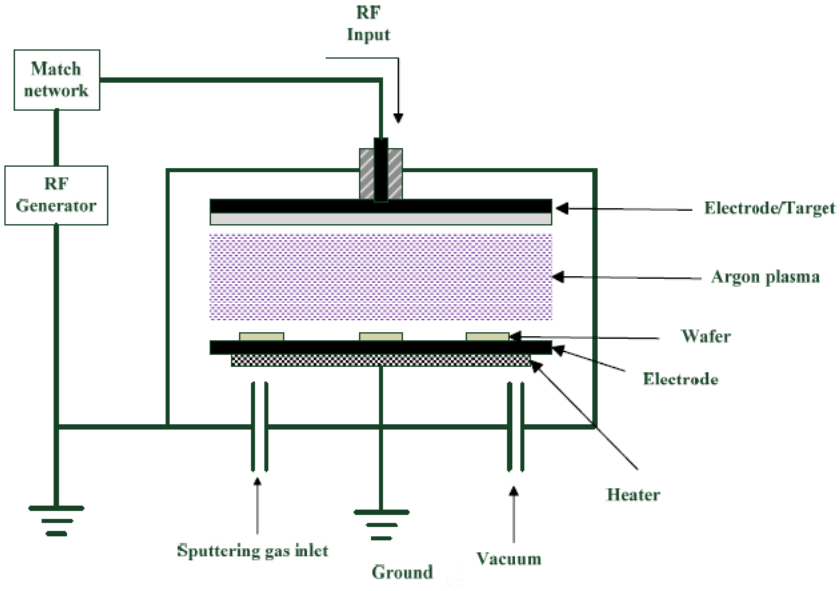


Fig. 2.3 RF-power sputtering deposition system.

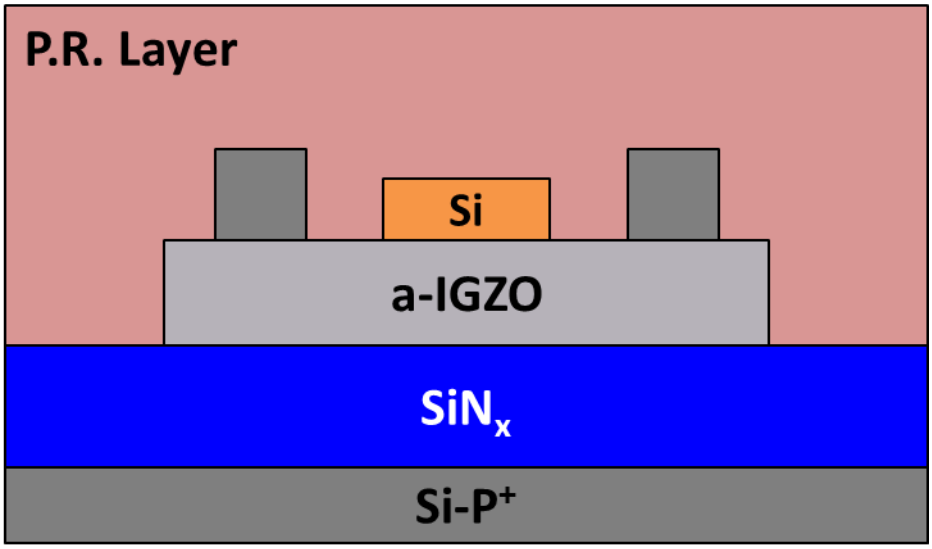


Fig. 2.4 The schematic cross-section of the a-IGZO TFT with Si capping layer and photoresist passivation layer.

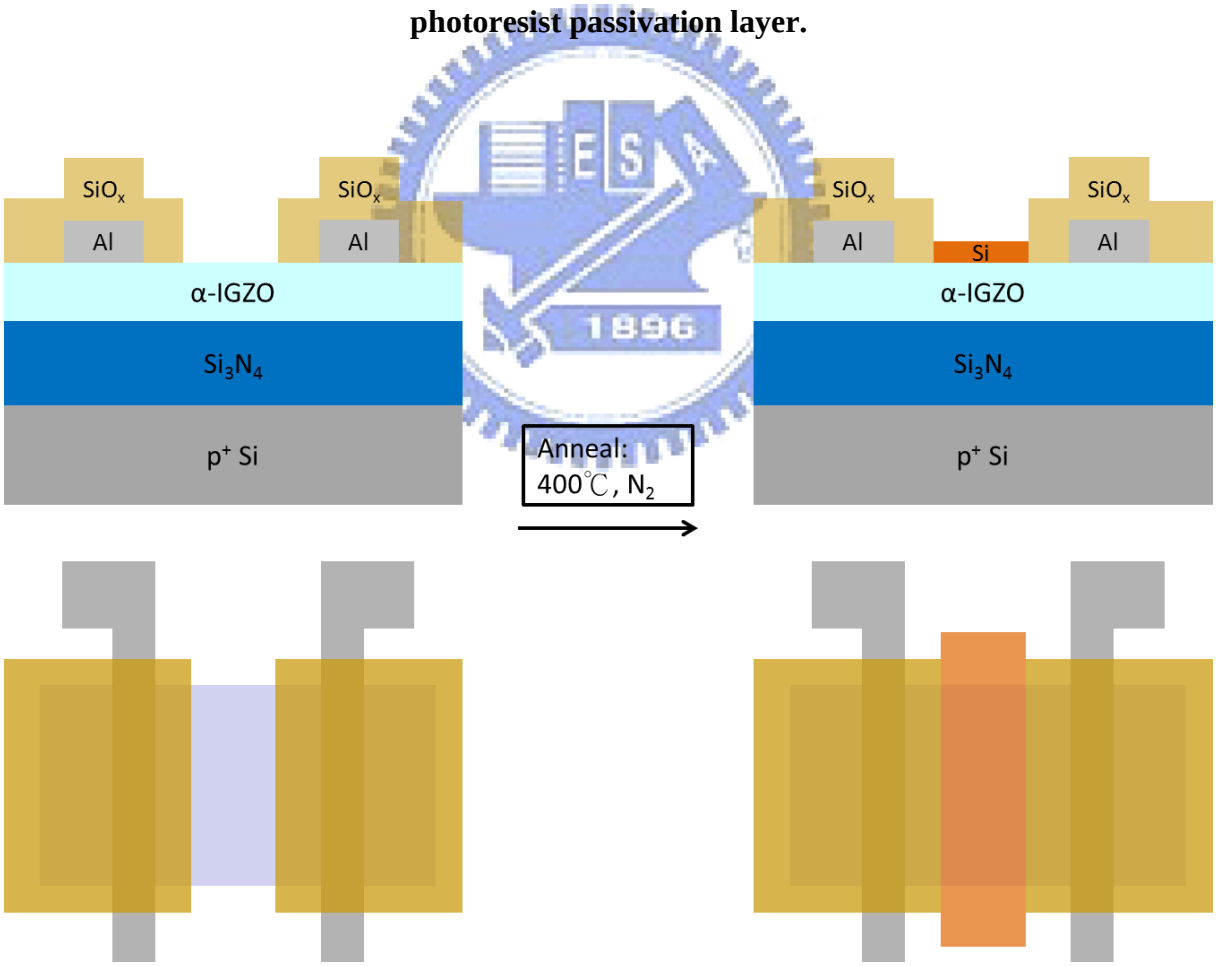


Fig. 2.5 The schematic cross-section and top view of the a-IGZO TFT with Si capping layer and SiO_x passivation layer.

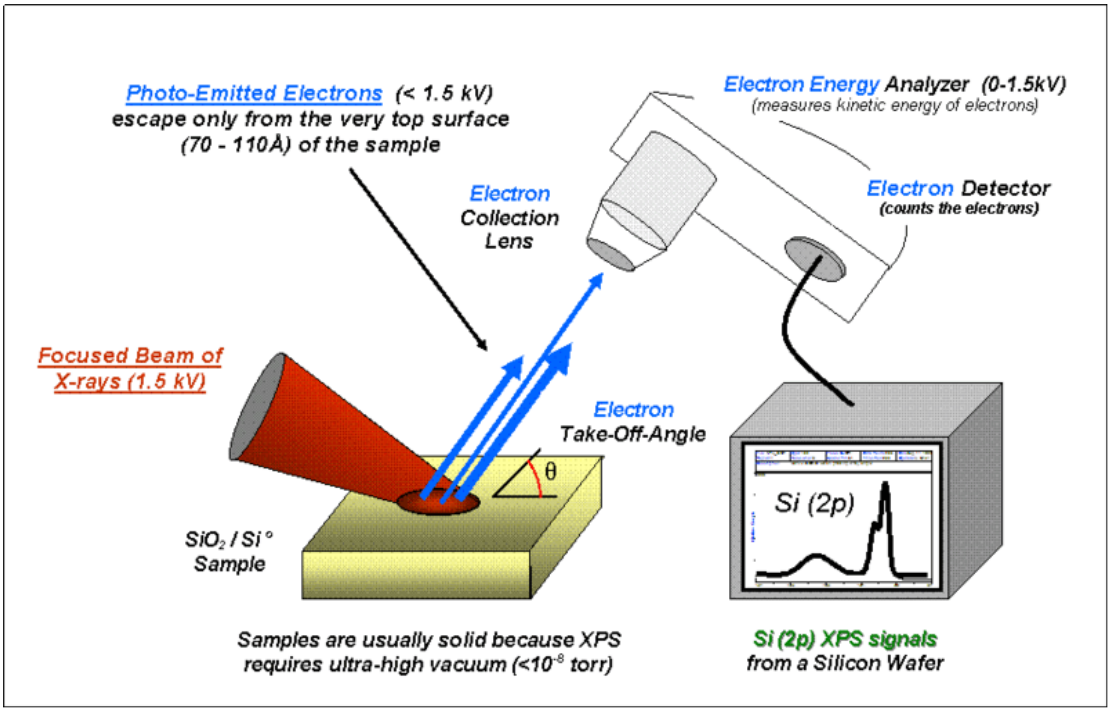


Fig. 2.6 Schematic diagram of XPS system.

Chapter 3 RESULTS AND DISSCUSION

3-1 a-IGZO TFT with Si capping layer

The back channel effect has strong relationship with electrical performance of oxide transistors, we try to apply back channel effect to improve electrical performance through Si capping layer. The silicon capping can induce the formation of a thin accumulation layer of extra electron carriers in back channel. The extra electron carriers can contribute carriers to the front channel and result the mobility significantly increased. In this method, we enhance not only electrical performance but also prevent degradation of the device performance.

In this section, a set of experiments have been demonstrated to investigate the high mobility effect (about than 10 times increment) found in Si-capped a-IGZO TFT.

3-1.1 Motivation

In our groups' previous research, we found that the back interface played an important role in bottom gate a-IGZO TFT. Therefore, the passivation layer became a considerable issue for our device stability. Accidentally, we found that the device was short circuit while capped SiO_x on bottom gate a-IGZO TFT. The cross section and top view of device diagram and its transfer characteristics are shown in Fig. 3.1. We suspected that there were extra electron carriers in back channel to cause short circuit. Taking this phenomenon as an advantage, we reduced the capping area of SiO_x instead of the whole channel part and found that this device exhibited great transfer characteristics.

3-1.2 Transfer characteristics of SiO_x-capped TFT with differnent oxygen ratio

According to the experimental result mentioned above, we reasonably doubt that the extra electron carriers which are created by oxygen vacancy contribute to the large on-current and lead to ultra-high mobility. We co-sputtered Si and SiO_2 to reach different oxygen ratio of SiO_x from x=0 to x=1 on bottom gate a-IGZO TFT to figure out whether different oxygen ratio of SiO_x could create different quantity of oxygen vacancies. In this case, we fixed the capping layer thickness to 20nm, capping length to 300μm and the total channel length to 500μm. In Fig. 3.2, we observed that when the capping layer is lack of oxygen such as Si or SiO, it might be absorb the oxygen from a-IGZO films, and therefore, a-IGZO films can generate extra electron carriers due to oxygen vacancy. The transfer characteristics of SiO_2 capping layer is without different from standard samples. We found that the carrier mobility significantly increase by capping the silicon oxide (SiO_x, x = 0、1) .

3-1.3 Transfer characteristics and time decay of lightly doped and undope Si-capped TFT

From previous section, both silicon and silicon oxide (SiO_x, x = 0、1) could significantly increase the field effect mobility. To simplify the case, from this section we choose only silicon (SiO_x, x = 0) as the capping layer, and the ratio of Si capping length to channel length is 150μm /300μm. In Fig. 3.3, we show the I_D-V_{GS} and $(I_D)^{1/2}$-V_{GS} transfer characteristics of different doped Si-capped devices, where V_{DS} = 20 V. Each device was traced for about 30 days, and the variation of threshold voltage and mobility during 30 days is shown in Fig. 3.4. As we could see, whether doped or undoped Si capping layer would cause threshold voltage

shift to negative right upon deposition, and S.S. as well as μ_{sat} became larger. To explain these, from previous section we know that the extra electron carriers are created by oxygen vacancy. And the increasing oxygen vacancy sites may both contribute to form more donor states and defect states, depending on the local structure [34]. The donor states enhance the electronic conductivity, but the defect states lead to larger S.S. The threshold voltage shift may be caused by the increasing carrier density near back interface of a-IGZO film, which needs negative gate bias to deplete the active layer and to turn off the device.

When devices are exposed to air, the rapid oxidation of Si eliminates the threshold voltage shift, the increased S.S as well as the off current, but decreases the mobility. These all can be explained by the reduction of oxygen vacancies in oxygen rich surrounding. After 30 days, the device has threshold voltage around -1V~-2V and mobility about 50~100cm^2/V_S, the device becomes stable and keeps high mobility. Detail parameters are listed in Table. 3.1.

3-1.4 a-IGZO thickness effect of Si-capped TFT

The a-IGZO thickness effect of Si-capped device is investigated, and the mobility enhancement effect becomes inferior when IGZO thickness increases as shown in Fig. 3.5. Table. 3.2 lists the extracted parameters for standard (in parentheses) and Si-capped devices with various a-IGZO thicknesses. As discussed before, we supposed the threshold voltage shift after Si capping attribute to the creation of oxygen vacancy in a-IGZO film at the interface of Si/a-IGZO. And this effect is supposed to be sensitive to the distance of Si/a-IGZO interface and the front channel of bottom gate a-IGZO TFT. The result indicates that the film becomes harder to deplete when the front channel is far from the Si/a-IGZO interface.

3-1.5 Annealing effect on Si-capped TFT

In previous section we doubt that the decaying characteristics of Si-capped devices are caused by the oxidation. In order to speed up the process, we try annealing the devices. In Fig. 3.6, two experiments are demonstrated. The first device was fabricated with no annealing before capping Si but only one post annealing in the final step; the other one was the same as previous section but added another post annealing in the final step. Both devices show similar results that 400℃ annealing in nitrogen (N_2) furnace for 1hr would eliminate all the effect caused by Si capping.

3-1.6 Passivation layer and stability test of Si-capped a-IGZO TFT

Stability is also an important issue to know if Si capping causes degradation of a-IGZO film, which limits this work in practical application. Here we test only bias stress stability, and both positive bias stress (PBS) and negative bias stress (NBS) are demonstrated. (V_G-V_T=20 for PBS and V_G-V_T=-20 for NBS, and V_D was not supplied during bias stress) Fig. 3.7 shows the transfer characteristics of old standard (old_STD, gas mixing ratio of Ar/O_2 = 25/0.7) and Si-capped device. As we could see, after same bias time both devices exhibit only parallel shifts; i.e. the values of S.S and mobility are not affected, and similar voltage shift is obtained, which indicates Si capping doesn't degrade the stability.

The passivation layer was also used to enhance the stability. Fig. 3.8 shows the bias stress tests of both passivation layers mentioned in Section 2-1.6 on new standard (STD, gas mixing ratio of Ar/O_2 = 30/0) and Si-capped devices. Fig. 3.9 shows the threshold voltage shift versus stress time. The stability under positive bias stress of each device is enhanced as compared with the unpassivated devices, but somehow the negative bias stress becomes a little worse in some cases.

3-2 Co-sputtered a-IGZO/IZO film with Si capping layer

3-2.1 Motivation

The high mobility in the a-IGZO material is attributed to the electron transport by the conduction band, whose minima in a-IGZO are composed of spatially spread nano-second orbitals of post-transition cations (In, Ga, and Zn) without directionality and the fact that their spherical symmetry makes the structural disordering in the amorphous state a rather uncritical issue.

Many groups have reported high performance TFTs with an a-IGZO film co-sputtered using a dual IGZO and indium zinc oxide (IZO) target [35, 36]. The indium content incorporated in the a-IGZO film was varied by controlling the rf power of the IZO target. The effect of the indium content on the performance was significant, and we would combine this with Si capping method to see further improvement.

3-2.2 Film deposition and Transfer characteristics of Co-sputtered a-IGZO/IZO TFT

In this work, we used ratio frequency (RF) –magnetron sputter to deposit our active layer. The co-sputtering was carried out at room temperature with a working pressure of 9mTorr. The input rf power of the $In_2Ga_2ZnO_7$ target was fixed at 100 W, while that of the In_2O_3 –10 wt % ZnO target was varied from 50 to 100 W. The gas mixing ratio was also varied with the In_2O_3 –10 wt % ZnO target. And later the aluminum was deposited as source and drain after a 400℃ post annealing in nitrogen (N_2) furnace for 1hr. We show a great result in Fig. 3.10

and Table. 3.3, where a significant improvement of the device performance was observed for the TFTs with the a-IGZO channel co-sputtered at an IZO rf power of 100 W and 20 volume % of O_2 in Ar/O_2 mixing gas.

3-2.3 Stability test of Co-sputtered a-IGZO/IZO TFT

The bias stress stabilities of co-sputtered device is demonstrated in this section (V_G-V_T=20 for PBS and V_G-V_T=-20 for NBS, and V_D was not supplied during bias stress). Fig. 3.11 shows the transfer characteristics and threshold voltage shift of this device. The instability comparing with the usual a-IGZO TFT is much better in PBS but a little worst in NBS. The higher indium content and higher O_2 gas ratio in the film deposition seem to reduce the defect states, resulting in a much stable device.

3-2.4 Transfer characteristics and time decay of co-sputtered a-IGZO/IZO TFT with Si capping layer

From the result of the above section, we chose a-IGZO channel co-sputtered at IZO rf power of 100 W as our basic device. Then the Si capping layer whose capping length and position were mentioned before was deposited on the co-sputtered a-IGZO/IZO TFT. Fig. 3.12 shows the time decay of I_D-V_{GS} and $(I_D)^{1/2}$-V_{GS} transfer characteristics, where V_{DS} = 20 V. The device was traced for about 30 days, and the variation of threshold voltage and mobility during 30 days is shown in Fig 3.13. When the Si-capped a-IGZO/IZO device is stable, it seems that the threshold voltage becomes more negative than the usual one, but no further improvement of the mobility. All this might attribute to the higher indium content, but we still don't have any proof in this part.

3-3 Mechanism determination and analysis of Si-capped a-IGZO TFT

In the previous experiment, the saturation mobility (μ_{sat}) could rise up to 5~10 times when Si capping half of the channel length on the middle of back interface. If we count the capped part of a-IGZO film as totally conductive, which could be taken as a short channel, the recounted μ_{sat} still reaches to 20~50 cm^2/Vs of the uncapped part. Therefore, it's reasonable to suspect that the Si capping layer has influence on not only the right under part of the film but also the side part. We hence set several experiences to investigate the uncertain affected length of side. And for the possible mechanism of the increasing carrier density, XPS analysis was used to examine whether the main cause is due to excess oxygen vacancy.

3-3.1 Dependency of different Si-capped length and position on a-IGZO TFT

We would separate the experiment into two parts to discus.

In the first part, the Si capping layer was fixed right in the middle of the channel but modulate the total capping length as well as the channel length. In Fig. 3.14, we define a new parameter, μ_{uc}, to represent the recounted mobility for the uncapped part. The shadow mask-designed capping length to channel length (L_{cap}/L) is 150/200, 150/300, 300/400, and 300/500 (μm), respectively. However, with the help of microscope we found that the real length of Si layer was always larger than the defined one. To precisely calculate theμ_{uc}, digital camera is used and the photos of the top view are shown in Fig. 3.15. The transfer characteristics and detail parameters are list in Fig. 3.16 and Table. 3.4. However, in some cases the drain current begins to be suppressed at certain values (ex: 10^{-2} A for channel length

200μm with capping length 150μm). This phenomenon appears only when we get a large drain current (induced by the Si capping layer), and from the I_D-V_{DS} curve in Fig. 3.17 the larger V_{GS} brings to almost total linear region comparing with the smaller drain current one. This could be explained by multi channels. The turn on voltage would be negative when we get a large on current, which indicate that the back channel first appears when the device starts to turn on. With increasing V_{GS}, the drain current increases rapidly attribute to both front and back channel until reaching certain values (V_C). Then the carriers wouldn't increase anymore in the back channel but only in the front channel which contributes to the drain current. The band diagram in Fig. 3.18 could make a clear illustration.

The second part we placed the Si capping layer right at the side of the channel. Here we added more conditions of the length varieties. The shadow mask-designed capping length to channel length (L_{cap}/L) is (100, 125, 150, 175)/200, (100, 150, 200, 250)/300, (200, 250, 300, 350)/400, and (300, 350, 400 ,450)/500 (μm), respectively. Fig. 3.19 shows the top view diagram, and in this plot the drain is on the left hand side. Here we also take the real photos of the top view in Fig. 3.20, and the transfer characteristics and detail parameters are list in Fig. 3.21 and Table. 3.5, where μ_{uc} is obtained using the real length. From the experiment data above, the influence of Si capping layer could expand to within 100μm to the side. When the Si was capped on the source side, the transfer characteristics presented to a quit different behavior. We could see from Fig. 3.22 and Table. 3.6, the on current of large V_{DS} is much larger with no differences between two threshold voltage values when Si capping layer leans against drain side. But when we apply smaller V_{DS} like 0.1 V or 1 V, the on current and the calculated field effect mobility are almost the same of these two. From the standard field effect transistor theory, the higher V_{DS} would form stronger depletion, but the excess carriers near drain side make it hard to deplete. Therefore, at the same V_{GS} the drain current could reach higher until pinch-off, which means the saturation current would also be higher at the

same V_{DS}. It is matched with the I_D-V_{DS} curve in Fig. 3.23, and the diagrams in Fig. 3.24 could help to understand.

3-3.2 XPS analysis of Si-capped device

Finally, XPS analysis is used to survey the variation of oxygen vacancy caused by Si capping. Fig. 3.25 (a) shows the depth profile diagram of XPS. There are three phases in our definition which based on the atomic concentration variation of O_{1s}、Zn_{2p3}、Ga_{2p3} and In_{3d5} as a function of sputtering time, and all is shown in Fig. 3.25 (b). The XPS spectrum of O_{1s} with different depth is shown in Fig. 3.26. The Si capping layer region is from 0 to 1.6 min and the Si/IGZO interface region is from 1.6 to 2.3 min. After the etching time over 2.3min is the IGZO bulk layer.

The O_{1s} XPS spectrum can be fitted by three peaks. For adjustment, the C 1s at 284.6eV is used as the reference to calibrate the energy positions of all detected peaks. The peak with the lower energy value of 530.30 eV, represents O^{2-} ions combined with Zn, Ga, and In ions, in the IGZO compound system. The medium binding energy value at 531.15 eV, is associated with O^{2-} ions which are in oxygen vacancy regions within the IGZO films. The higher binding energy value of 532.40 eV, is related to loosely bonded oxygen on the IGZO surface, including absorbed H_2O, CO_3, or O_2. Analysis for bottom gate a-IGZO with Si capping layer with etching time 1.6, 1.8, 2, 2.3 and 3.5 min and without Si capping layer (STD) are shown in Fig. 3.27 (a), (b), (c), (d), (e), and (f), respectively. The peak fitting function is Voigt area, and a linear base line is used. We observed the content of oxygen vacancy of IGZO without any treatment is almost the same with Si capping layer of IGZO films at 3.5-min etching time from O_{1s} XPS spectra analysis. Hence, we can make sure the criteria of IGZO films are identical. Therefore, the oxygen vacancy becomes richer at the IGZO surface due to Si capping layer from a series of

O_{1s} XPS spectra. The area ratio of O_M 1s peak, O_L 1s peak, and O_M 1s peak to O_L 1s peak and O_M 1s peak (O_M / (O_L +O_M)), is shown in Table 3.6.

In addition, Fig. 3.28 shows the XPS spectra of In_{3d5} with etching time 1.6, 1.8, 2, 2.3, 2.6, 3.5 min and STD. The lower binding energy corresponds to the In^0 bonding state of In-In Bonds, and the higher binding energy corresponds to the In^{3+} bonding state of In_2O_3. Hence, near the Si/IGZO interface the In shifts to lower binding energy, which indicates the higher conductivity within this region.

3-4 FIGURE OF CHAPTER 3

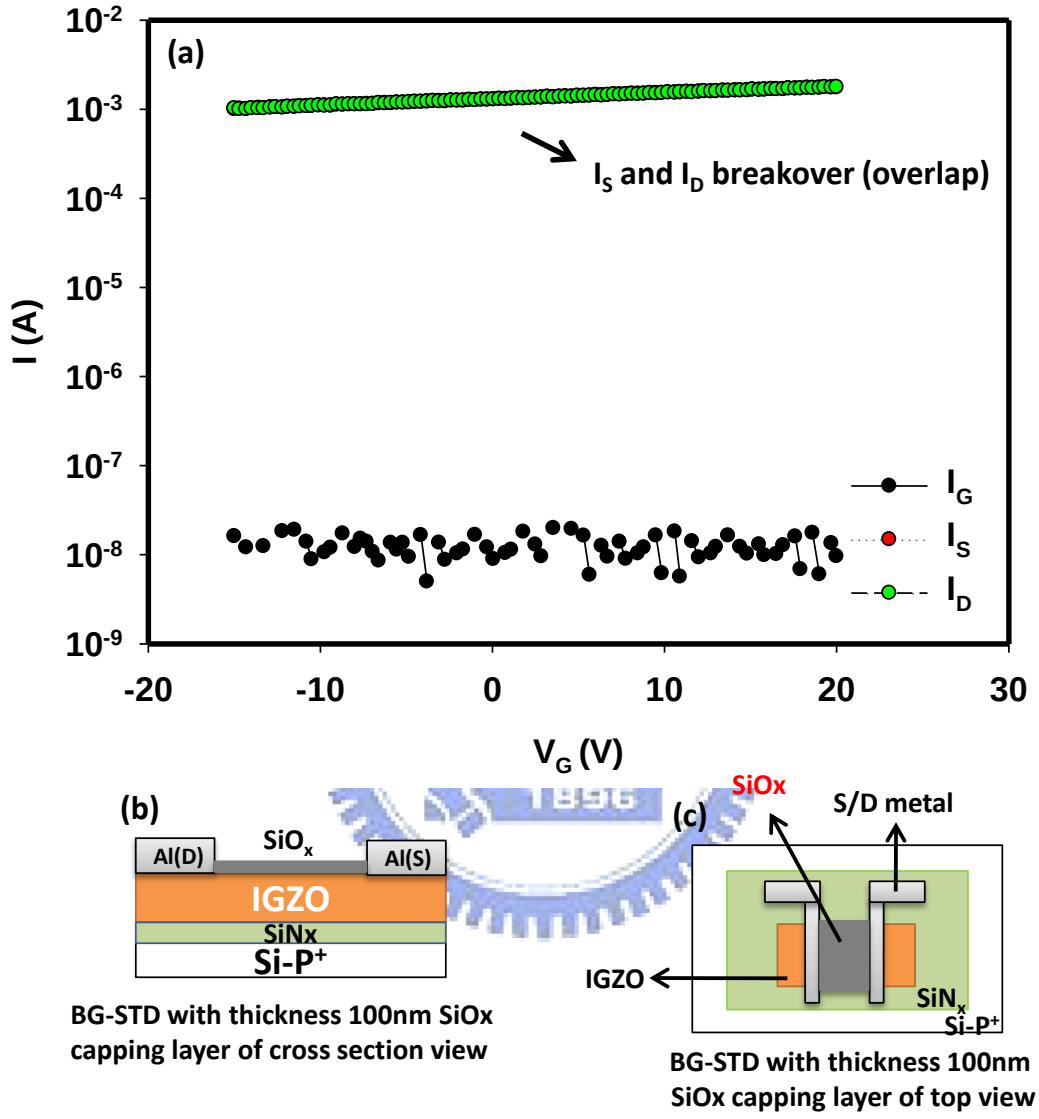
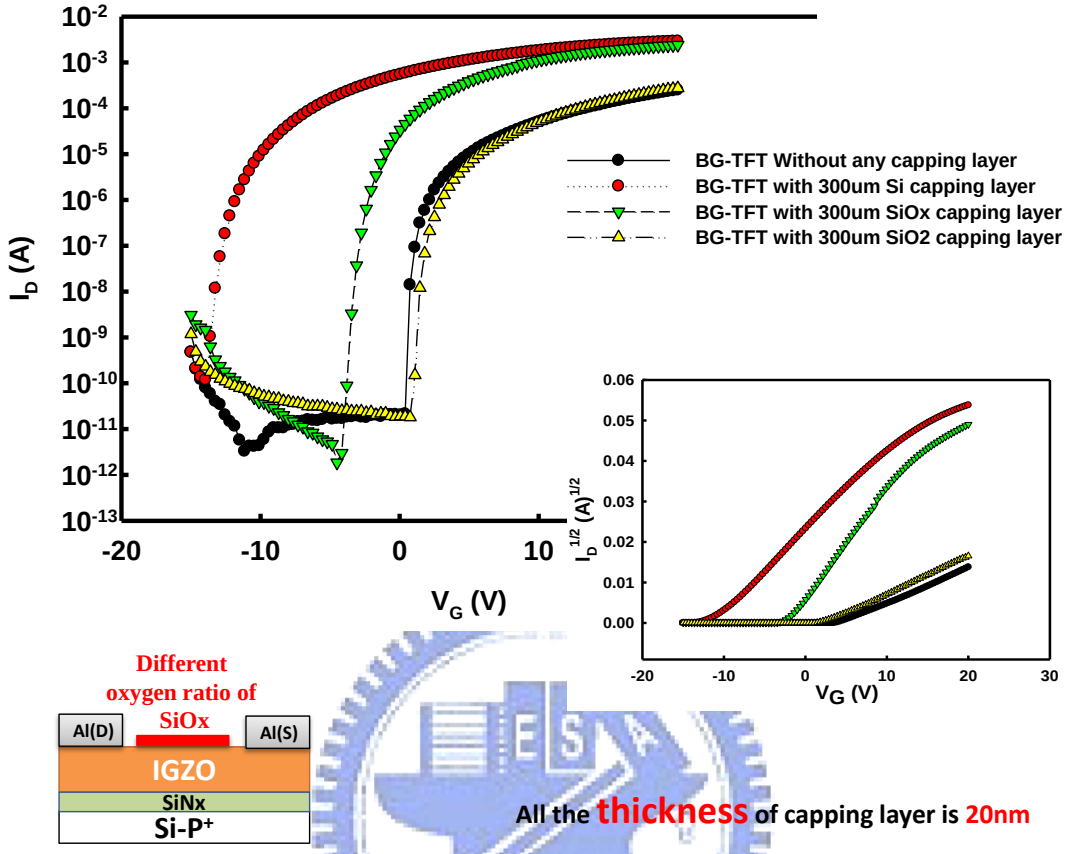


Fig. 3.1 (a) The transfer characteristics of capping SiO_x BG-STD TFTs. (b) and (c) is cross section and top view of device diagram.



Capped Area Ratio	Different oxygen ratio of SiOx	*VT (V)*	*μ (cm2/Vs)*	*μ max (cm2/Vs)*	*S.S. (dec./V)*	*On/Off*
0/500	None	3.91	11.66	17.26	0.22	1.10E+08
300/500	X=0	-10.78	88.2	136.14	0.35	2.40E+07
300/500	X=1	-1.93	151.82	165.52	0.24	8.00E+08
300/500	X=2	2.17	14.67	18.68	0.25	1.50E+07

Fig. 3.2 The transfer characteristics and cross section of device diagram of BG-STD TFT with capping different oxygen ratio layer, and typical parameters of TFT with capping different oxygen ratio layer.

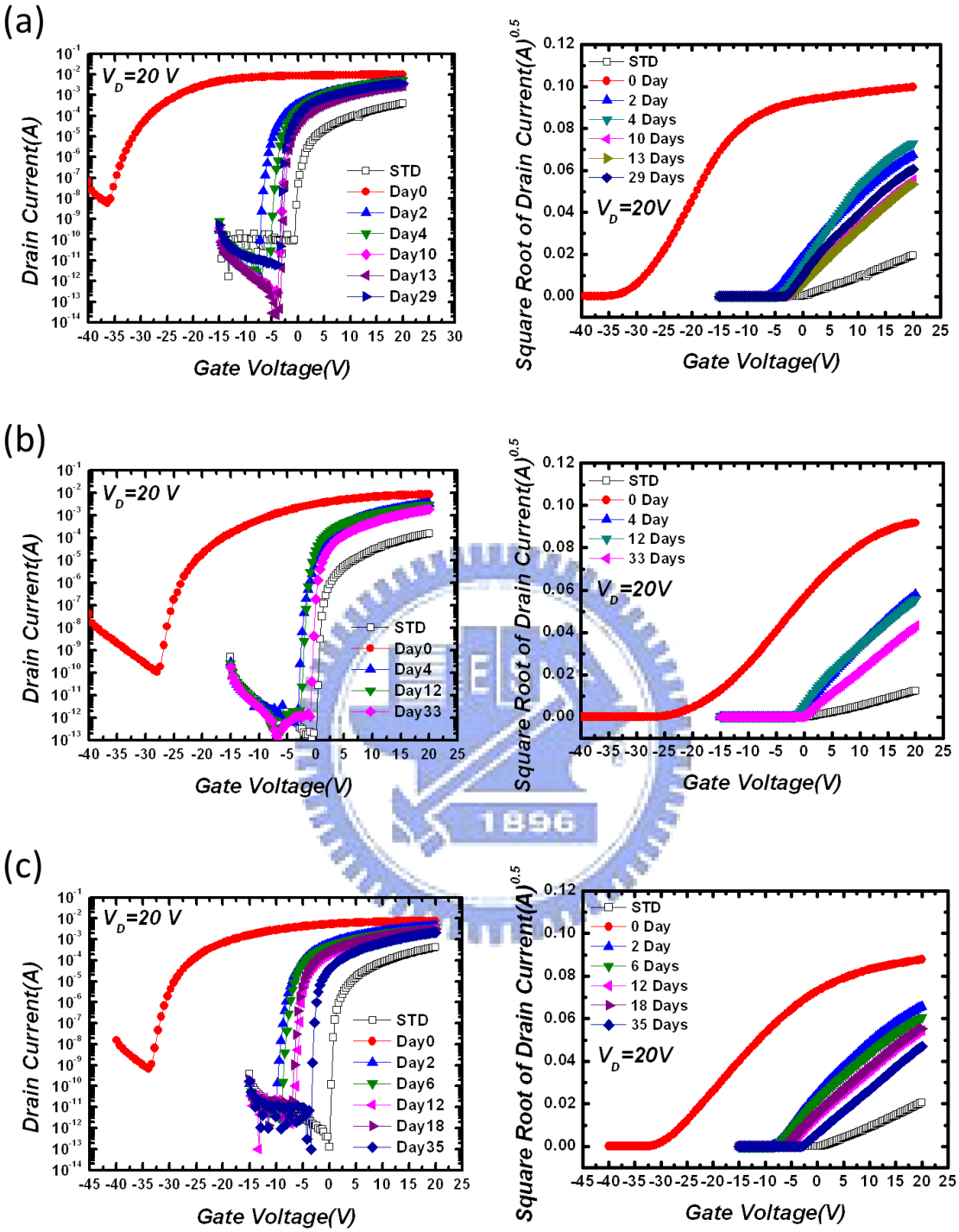


Fig. 3.3 The transfer characteristics of (a) undoped, (b) p-doped and (c) n-doped Si-capped device.

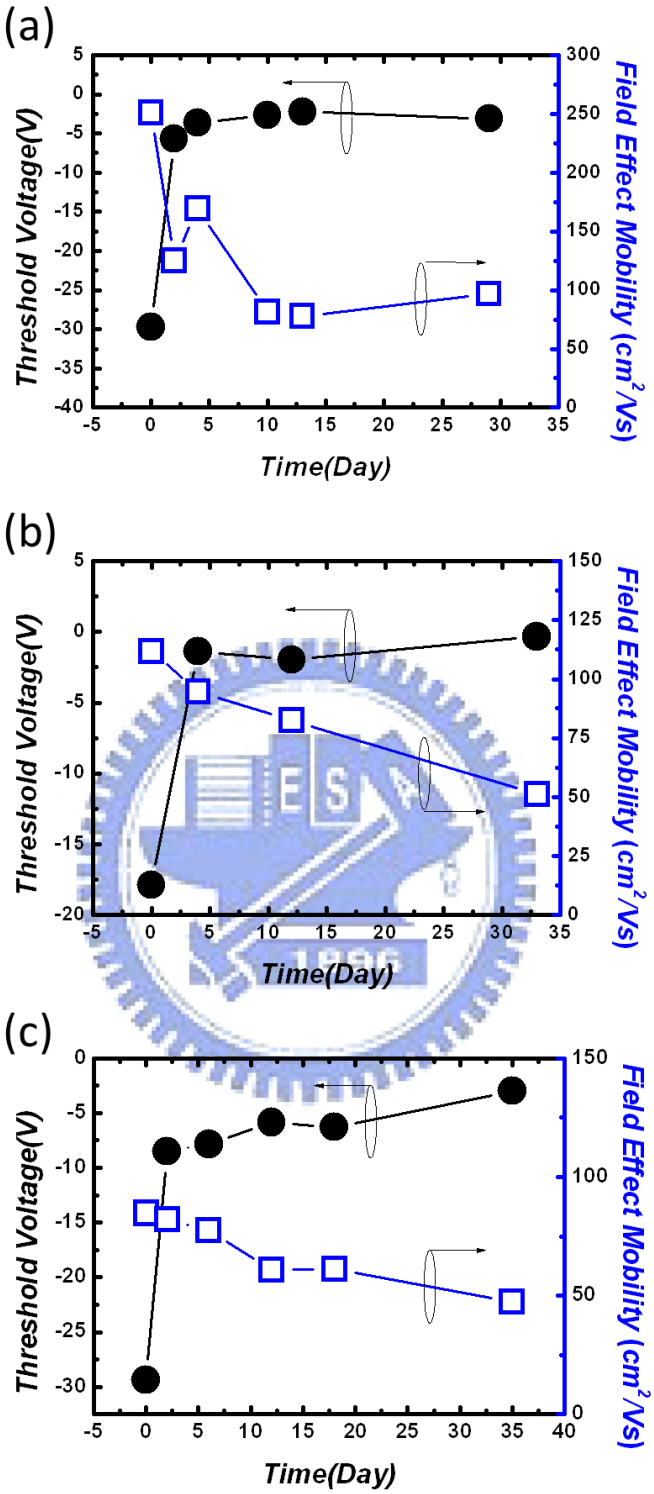


Fig. 3.4 The variation of threshold voltage and mobility of (a) undoped, (b) p-doped and (c) n-doped Si-capped device during 30 days.

Sample	Sequence	V_T (V)	V_{on}(V)	μ (cm2/Vs)	S.S. (V/dec.)	On/Off
Un-doped Si	Day 0	-29.7	-36.4	250.98	1.35	3.10E+07
	Day29	-3.12	-3.8	96.67	0.20	1.50E+08
p-doped Si	Day 0	-17.88	-28	111.93	0.93	3.20E+08
	Day33	-0.34	-1.18	66.65	0.2	1.70E+08
n-doped Si	Day 0	-29.37	-34	84.73	0.99	1.10E+08
	Day 35	-3.01	-3.45	47.56	0.08	2.20E+10
STD	-	0.26	-0.65	10.32	0.26	3.80+06

Table. 3.1 The extracted parameters of a-IGZO TFTs with different Si capping layers.

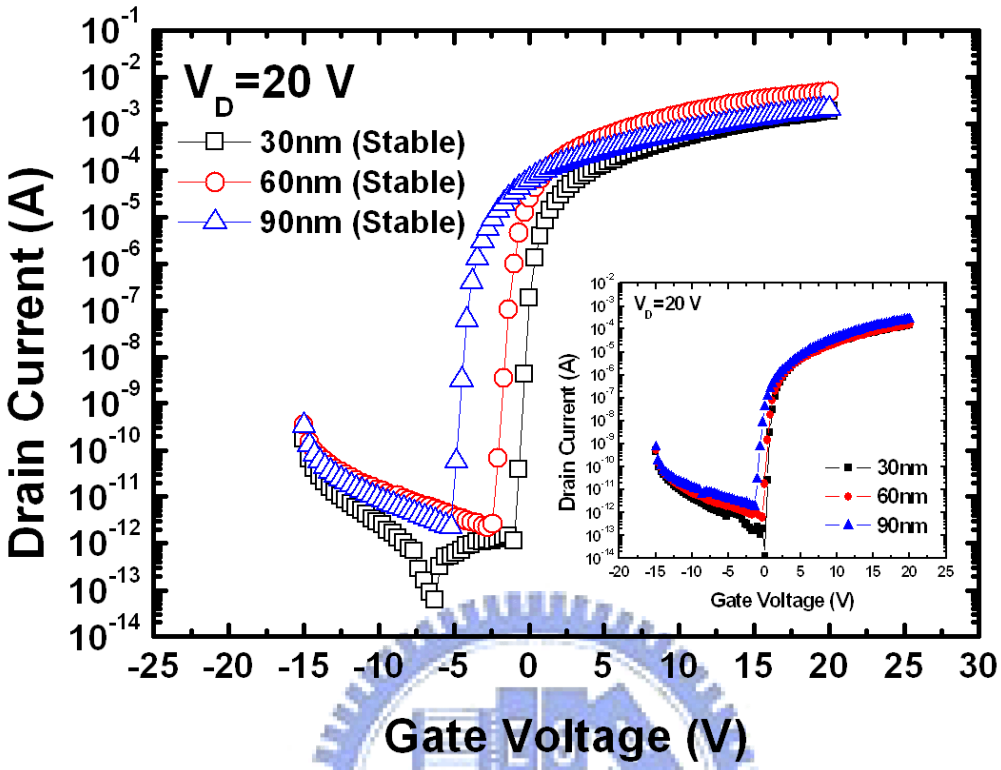


Fig. 3.5 Transfer characteristics of Si capped devices with various a-IGZO thicknesses. The inset shows the initial transfer characteristics of uncapped devices with various a-IGZO thicknesses.

Thickness	V_T (V)	V_{on}(V)	μ (cm2/Vs)	S.S. (V/dec.)	On/Off
30nm	-0.34(1.61)	-1	51.18(4.54)	0.2	1.60E+09
60nm	-1.41(1.84)	-2.75	134.53(4.74)	0.33	2.10E+09
90nm	-4.08(2.06)	-5.2	37.2(8.13)	0.24	8.80E+08

Table. 3.2 Extracted parameters for standard (in parentheses) and Si-capped devices with various a-IGZO thicknesses.

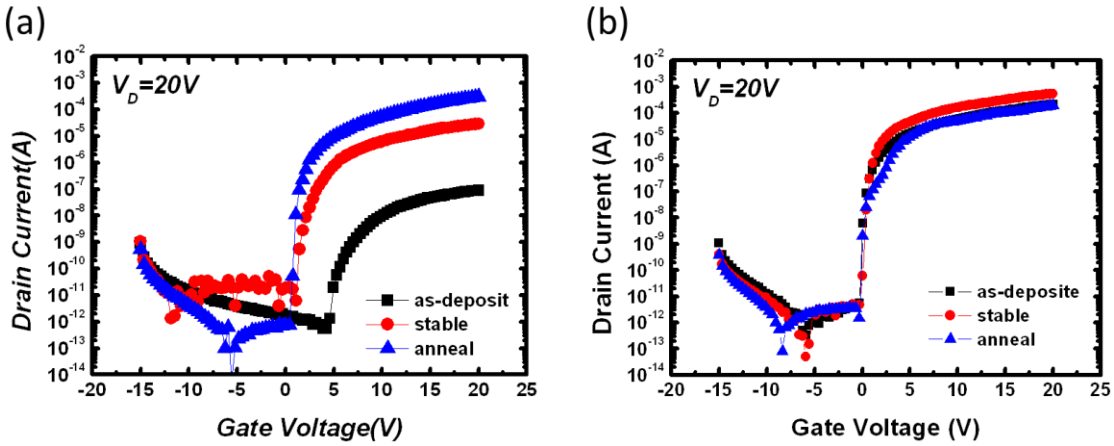


Fig. 3.6 Transfer characteristics of (a) STD without annealing before capping Si and (b) STD with annealing before capping Si. Both Si-capped devices are treated with post annealing when stable.

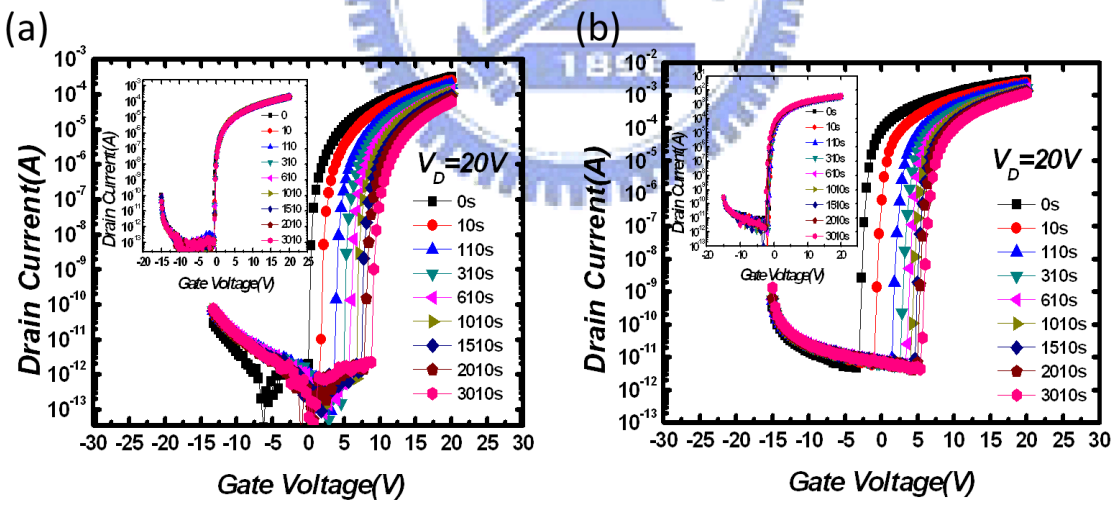


Fig. 3.7 Transfer characteristics of (a) old_STD and (b) Si-capped device during positive bias stress. The inset shows the negative bias stress.

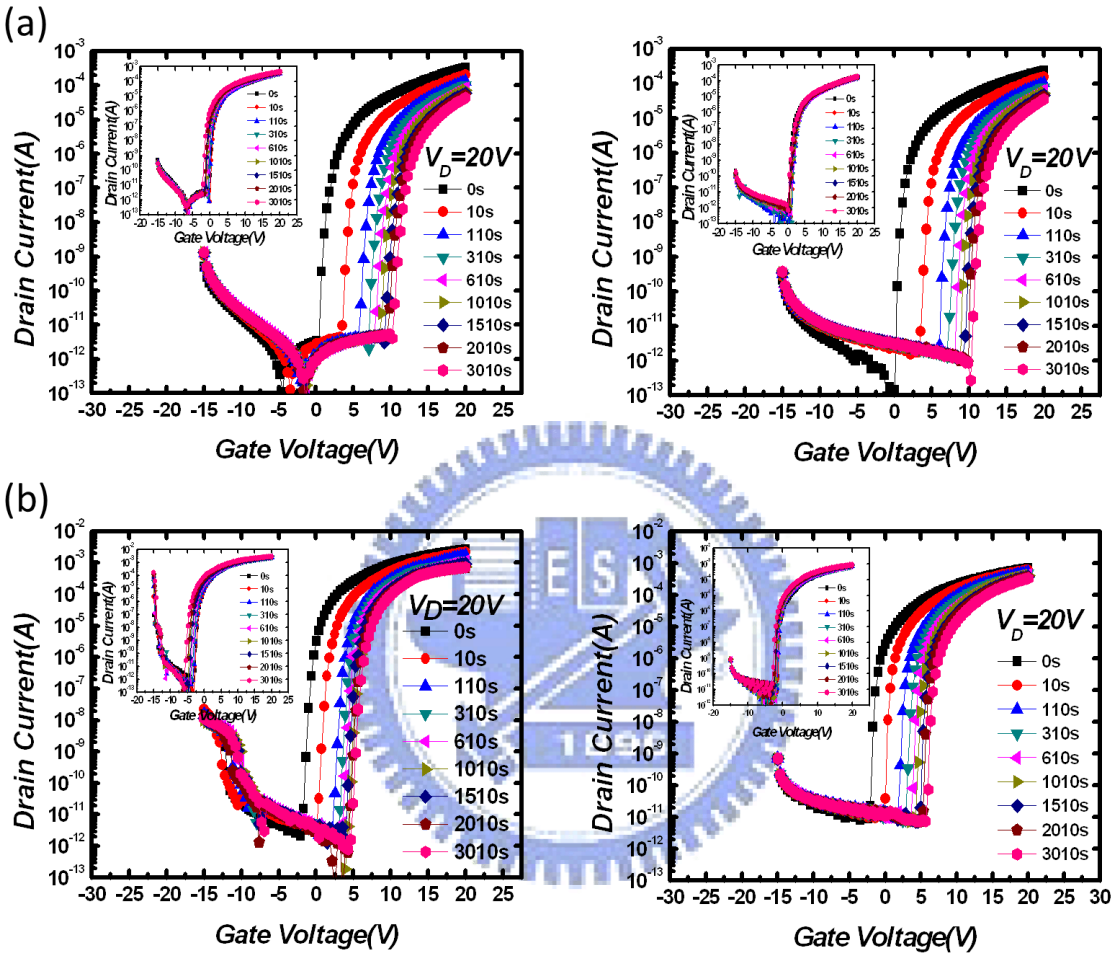


Fig. 3.8 Transfer characteristics with photoresist (left) and SiO_x (right) passivation layer of (a) STD and (b) Si-capped device during positive bias stress. The inset shows the negative bias stress.

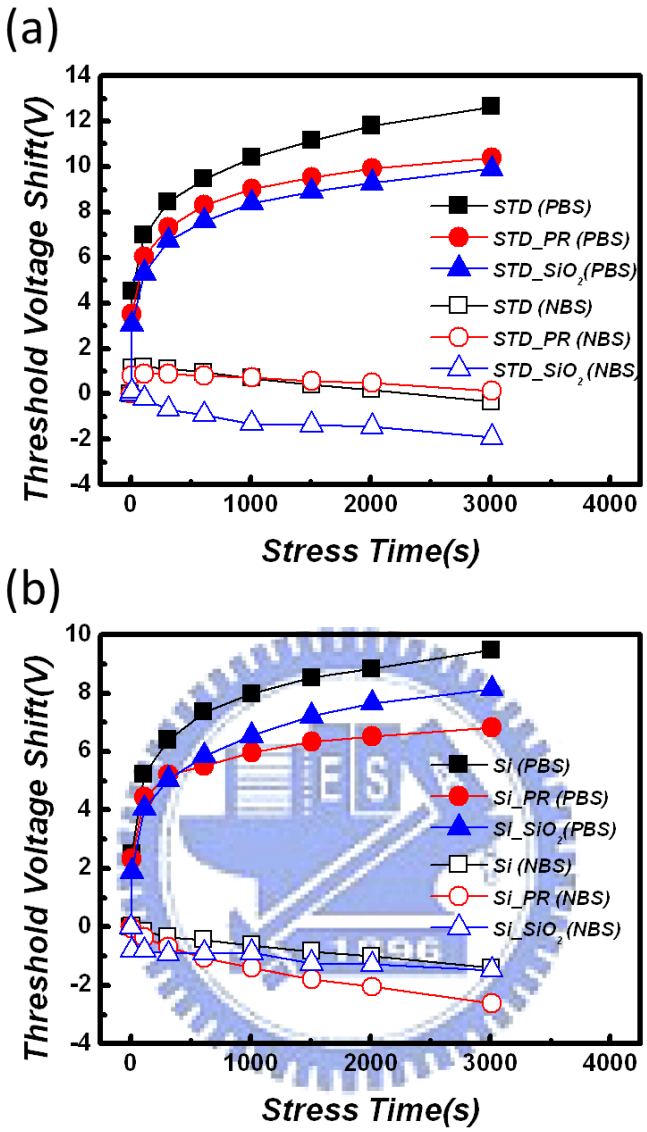


Fig. 3.9 Threshold voltage shift of (a) STD and (b) Si-capped device with and without passivation layer during bias stress.

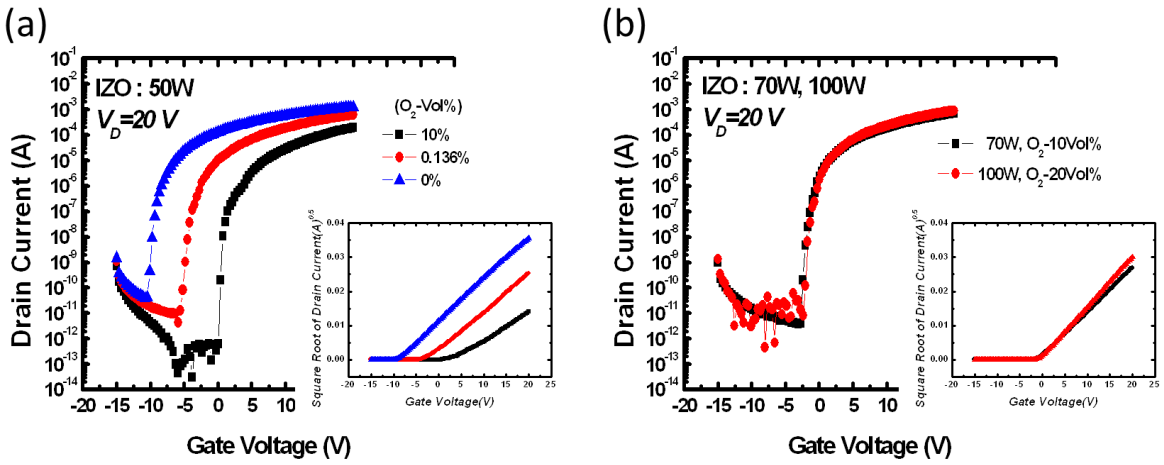


Fig. 3.10 Transfer characteristics of a-IGZO/IZO co-sputtered film with IGZO fixed 100W and IZO (a) 50W and (b) 70W and 100W with different oxygen gas ratios.

Sample	V_T (V)	V_{on}(V)	μ (cm2/Vs)	S.S. (V/dec.)	On/Off
50W_0%	-8.74	-10.45	18.95	0.33	3.10E+07
50W_0.136%	-2.61	-5.9	13.46	0.44	1.50E+08
50W_10%	3.92	0.05	8.56	0.14	3.20E+08
70W_10%	-0.95	-2.75	18.3	0.23	1.70E+08
100W_20%	-0.54	-2.4	24.14	0.29	1.10E+08

Table. 3.3 Extracted parameters for a-IGZO/IZO co-sputtered devices with various powers and oxygen gas ratios.

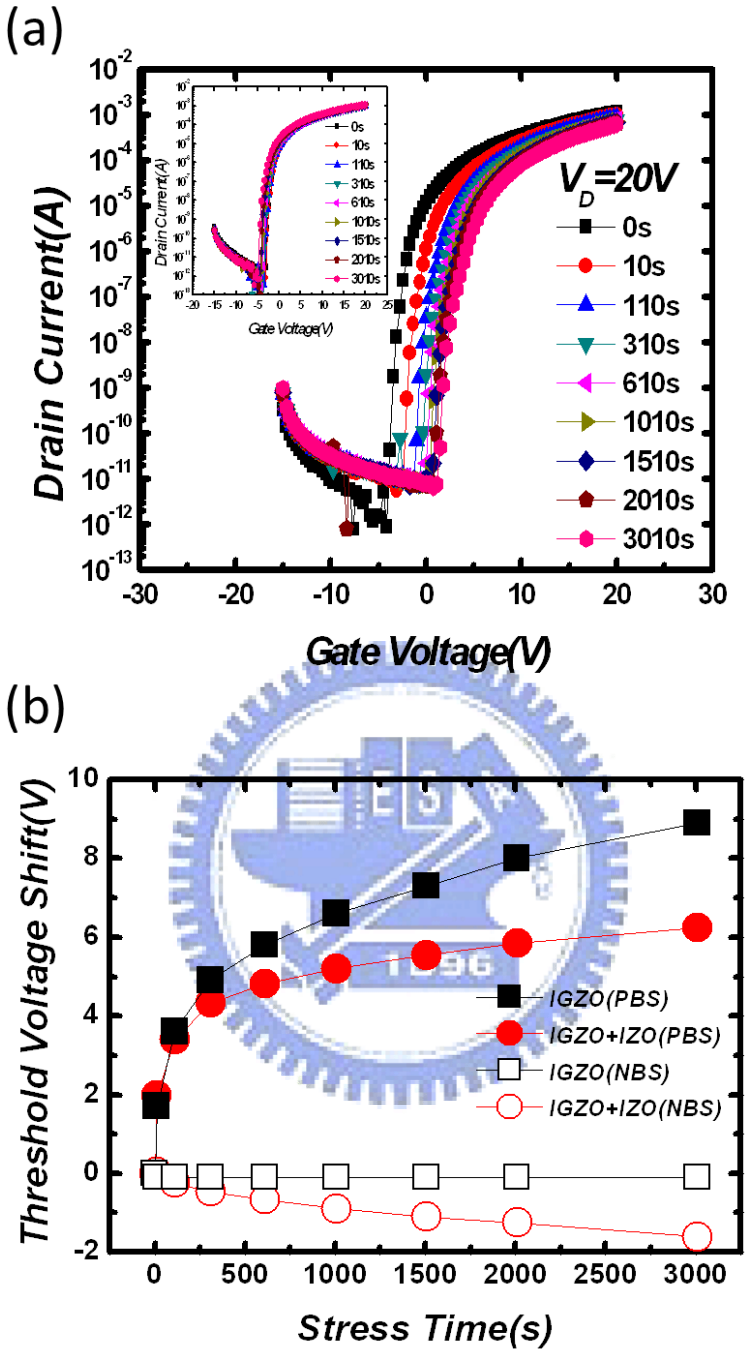


Fig. 3.11 (a) Transfer characteristics and (b) threshold voltage shift of a-IGZO/IZO co-sputtered device during positive bias stress and negative bias stress.

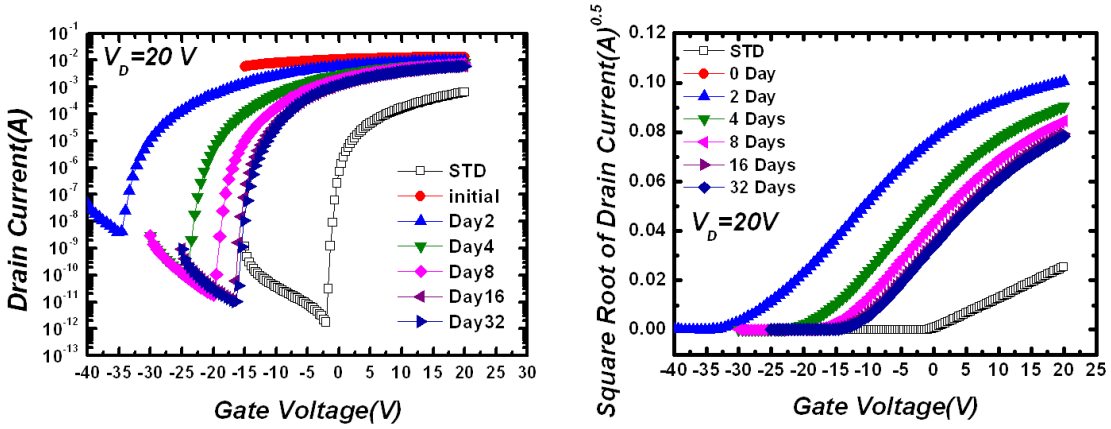


Fig. 3.12 The transfer characteristics of a-IGZO/IZO co-sputtered device with Si capping layer.

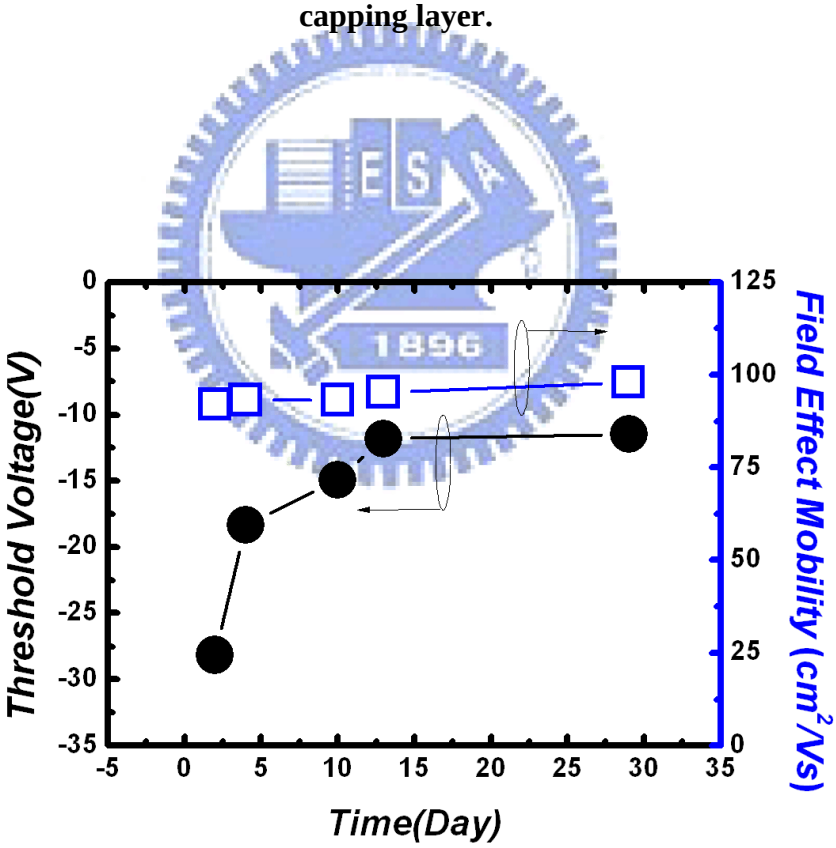


Fig. 3.13 The variation of threshold voltage and mobility of a-IGZO/IZO co-sputtered device with Si capping layer during about 30 days

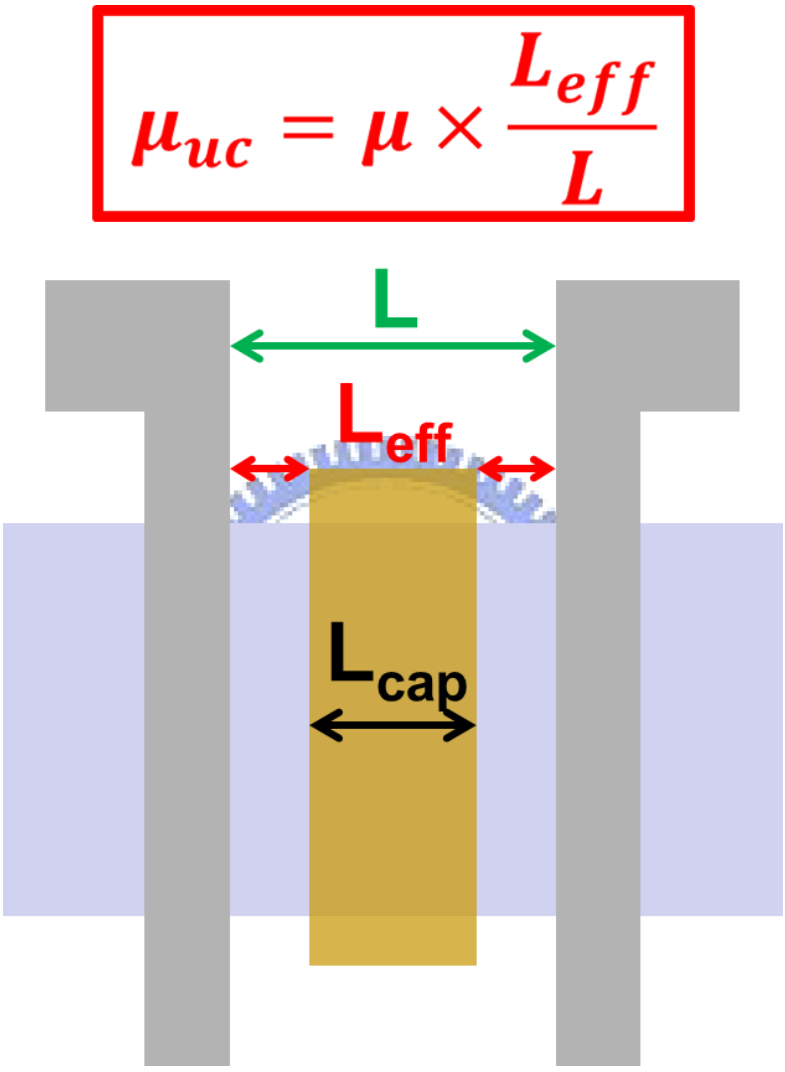


Fig. 3.14 Top view and definition of μ_{uc} and other parameters with Si capping layer in the middle.

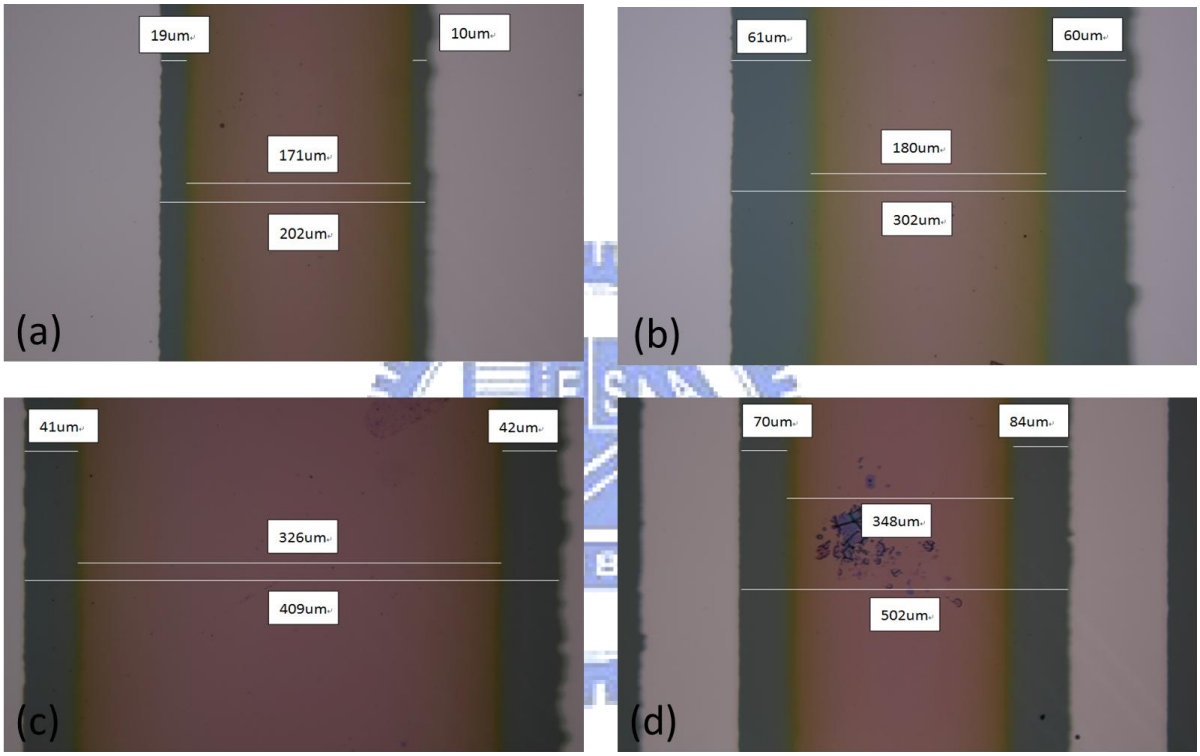


Fig. 3.15 Top view in real photos and measured length of all parameters. The ratio of uncapped length to channel length (a) 29/202 (b) 121/302 (c) 83/326 and (d) 154/502.

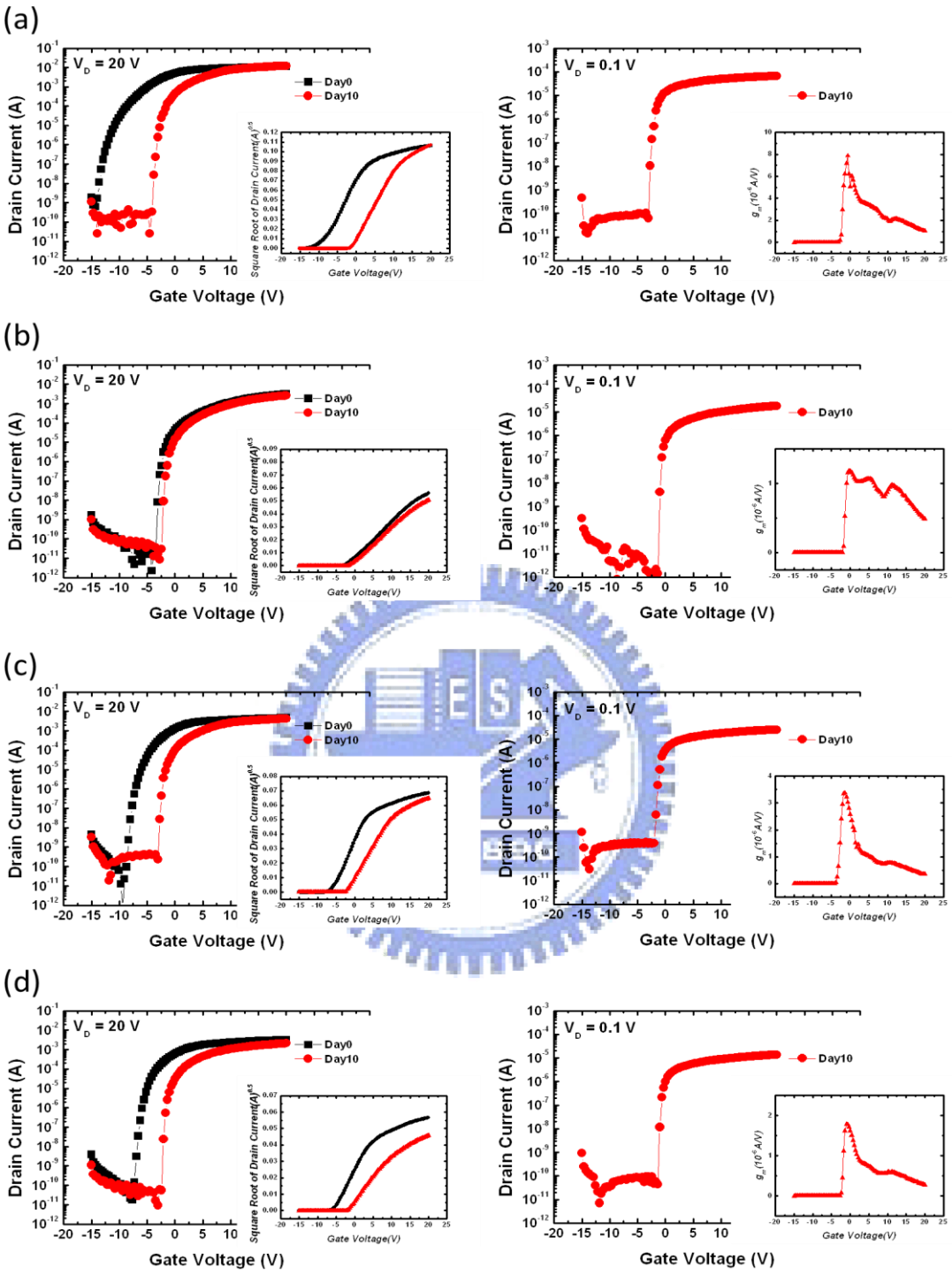


Fig. 3.16 The transfer characteristics of different ratios of uncapped length to channel length with Si capping layer in the middle (a) 29/202 (b) 121/302 (c) 83/326 and (d) 154/502. The inset is $(I_D)^{0.5}$ on the left side for saturation region and g_m on the right side for linear region.

L(L_{eff})	V_D_Sequence	V_T (V)	V_{on}(V)	μ (cm2/Vs)	μ_{uc} (cm2/Vs)	S.S. (V/dec.)	On/Off
202(29)	Day 0	-9.09	-14.3	451.36	64.80	0.54	1.80E+07
	Day 10	-2.94	-4.5	361.63	51.92	0.26	4.90E+08
	0.1V_Day 10	-2.12	-3.1	228.31	32.78	0.16	1.00E+06
302(121)	Day 0	-2.28	-3.45	86.03	34.47	0.14	1.50E+08
	Day 10	-1.11	-2.75	82.2	32.93	0.23	3.00E+08
	0.1V_Day 10	-0.7	-1.35	55.11	22.08	0.1	1.30E+07
409(89)	Day 0	-6.05	-9.4	523.45	106.23	0.3	7.20E+09
	Day 10	-2.23	-3.1	294.39	59.74	0.17	1.80E+07
	0.1V_Day 10	-1.45	-2.05	184.92	37.53	0.28	6.60E+04
502(154)	Day 0	-5.55	-7.65	363.8	111.60	0.34	1.80E+08
	Day 10	-1.79	-2.4	174.21	53.44	0.13	3.80E+07
	0.1V_Day 10	-0.88	-1.35	115.85	35.54	0.14	3.10E+05

Table. 3.4 Extracted parameters for different ratios of uncapped length to channel length of a-IGZO devices with Si capping layer in the middle.

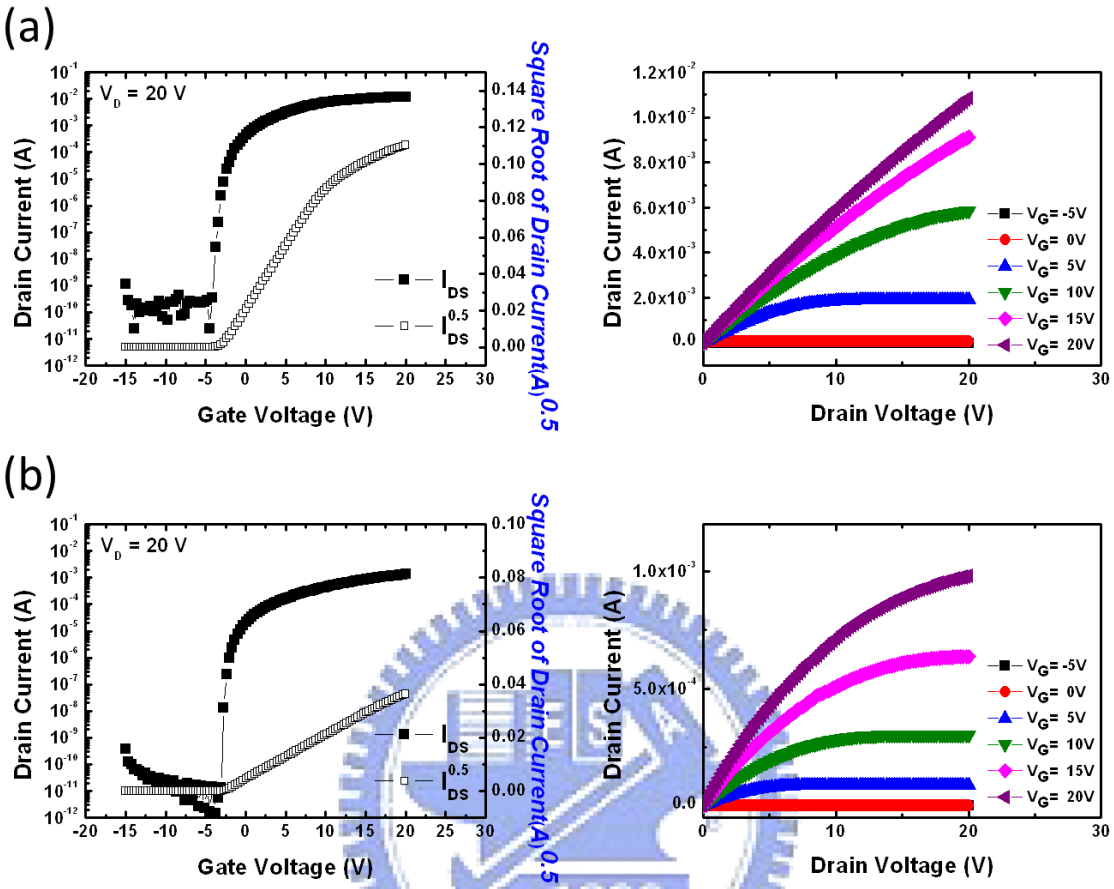


Fig. 3.17 The transfer characteristics and I_D-V_D curves of (a) high on current (b) normal on current Si capped devices.

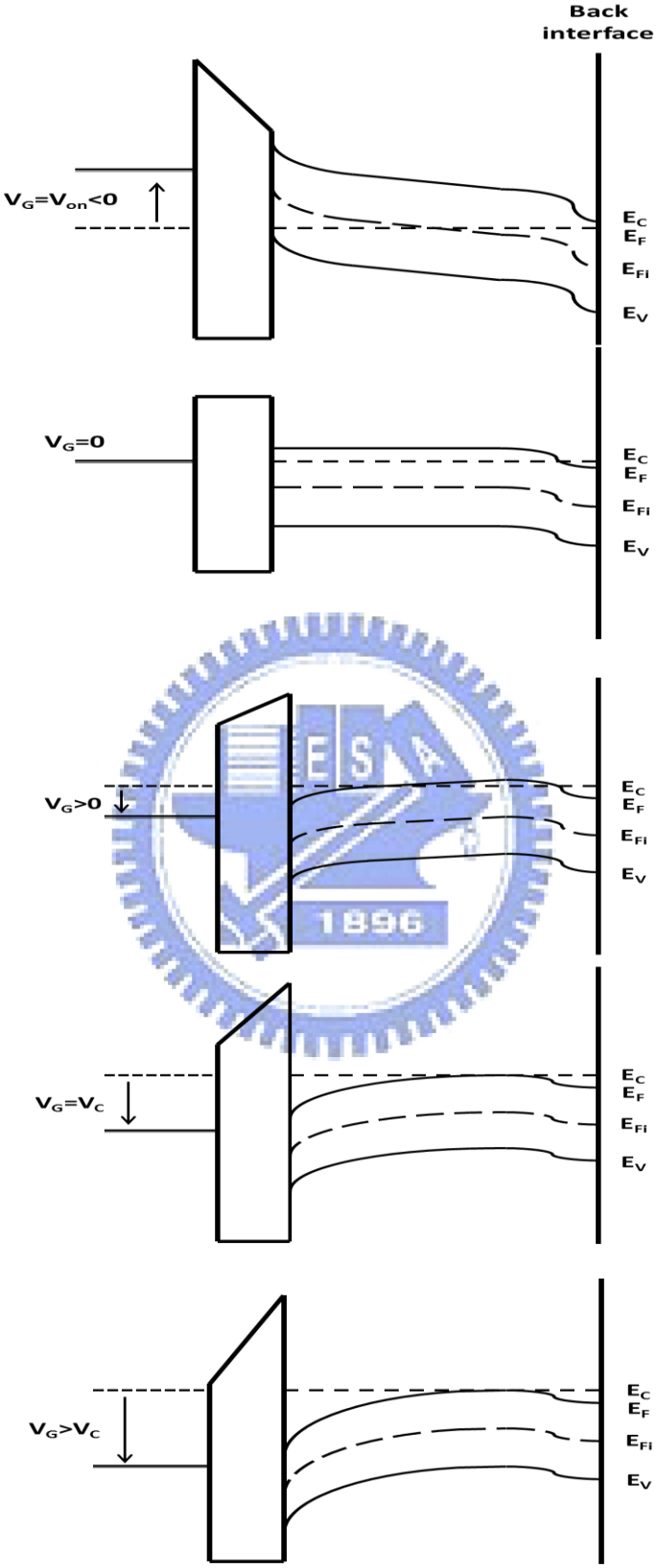


Fig. 3.18 The band diagram to explain the suppressed on current at high gate voltage.

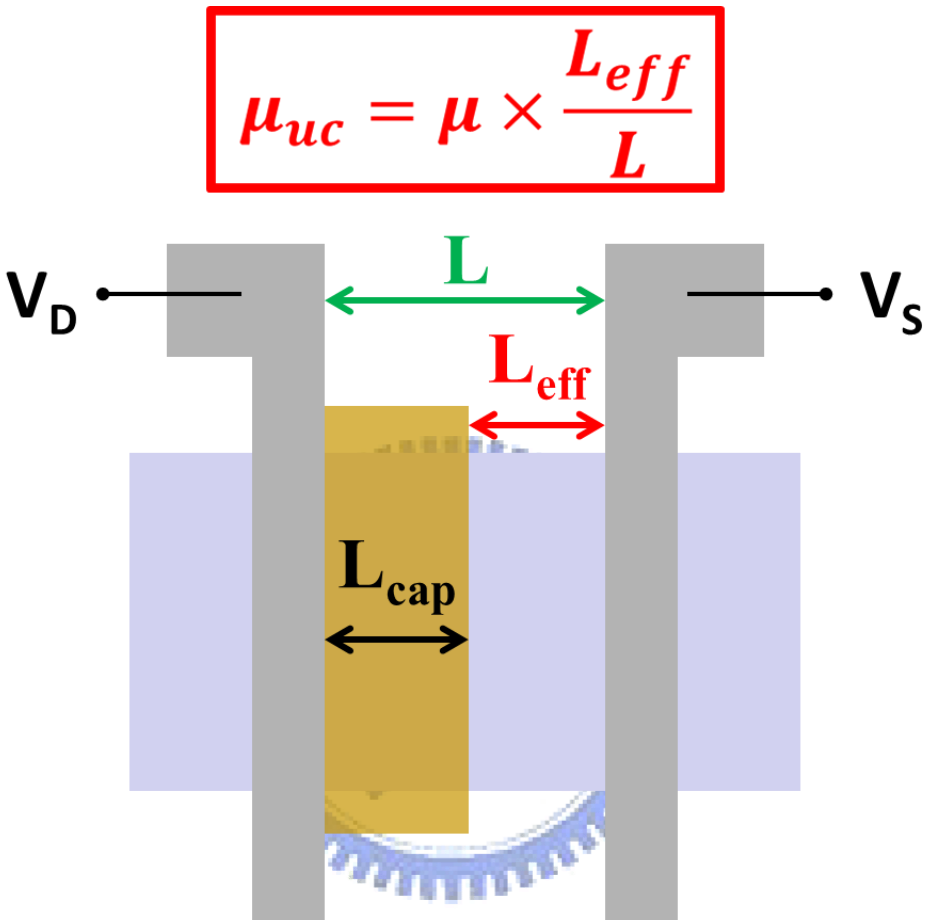
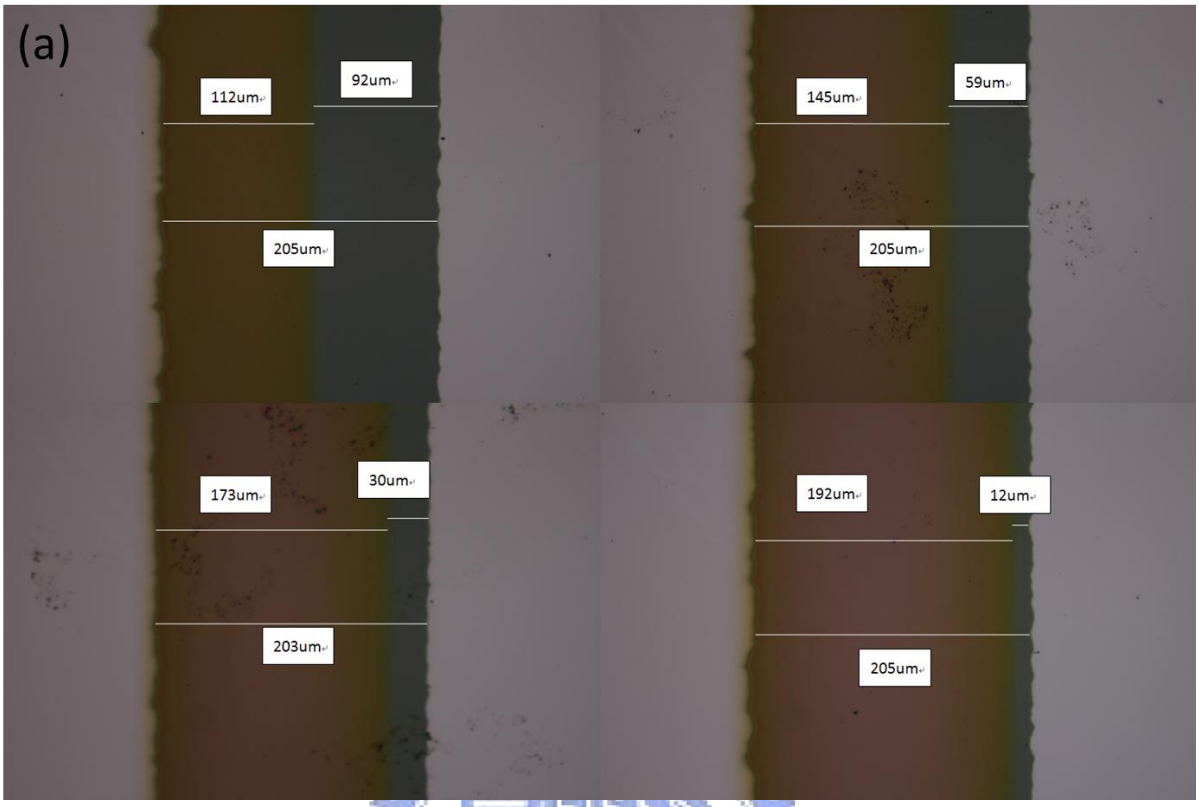
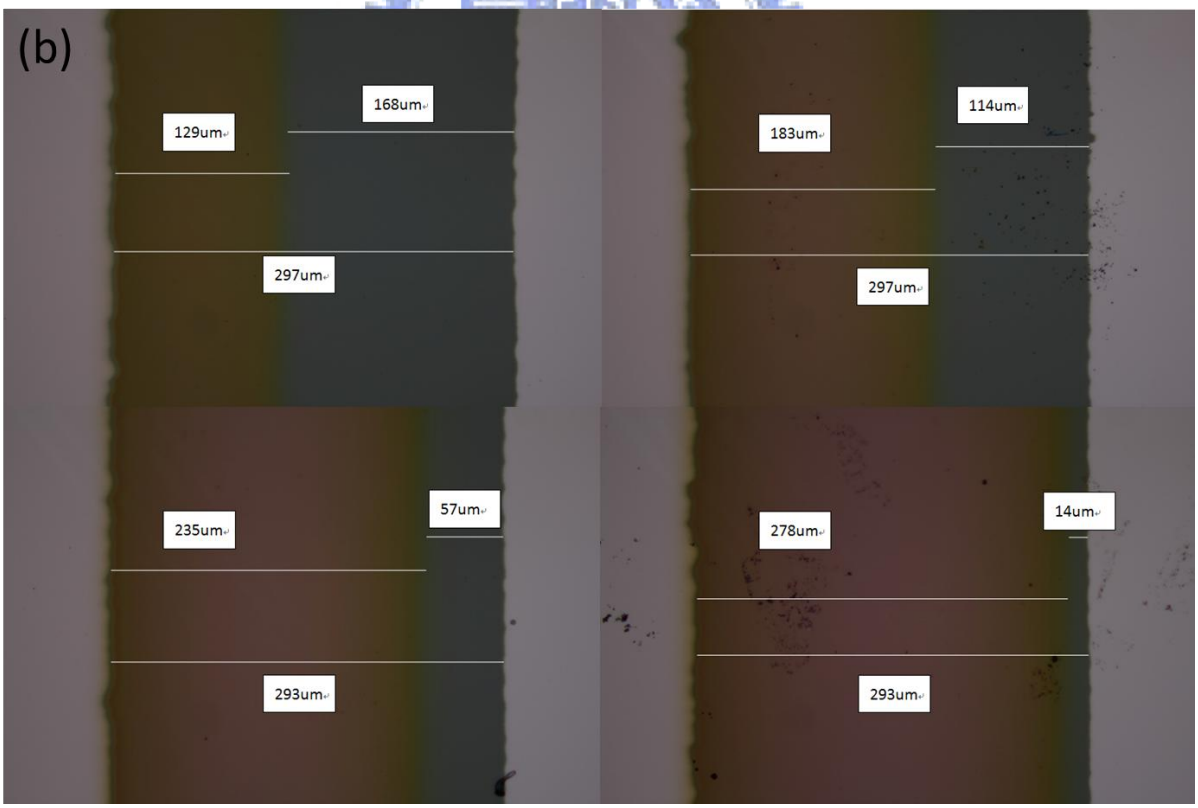


Fig. 3.19 Top view and definition of μ_{uc} and other parameters with Si capping layer closed to drain.


(a)
112um
92um
205um
145um
59um
205um
173um
30um
203um
192um
12um
205um


(b)
129um
168um
297um
183um
114um
297um
235um
57um
293um
278um
14um
293um

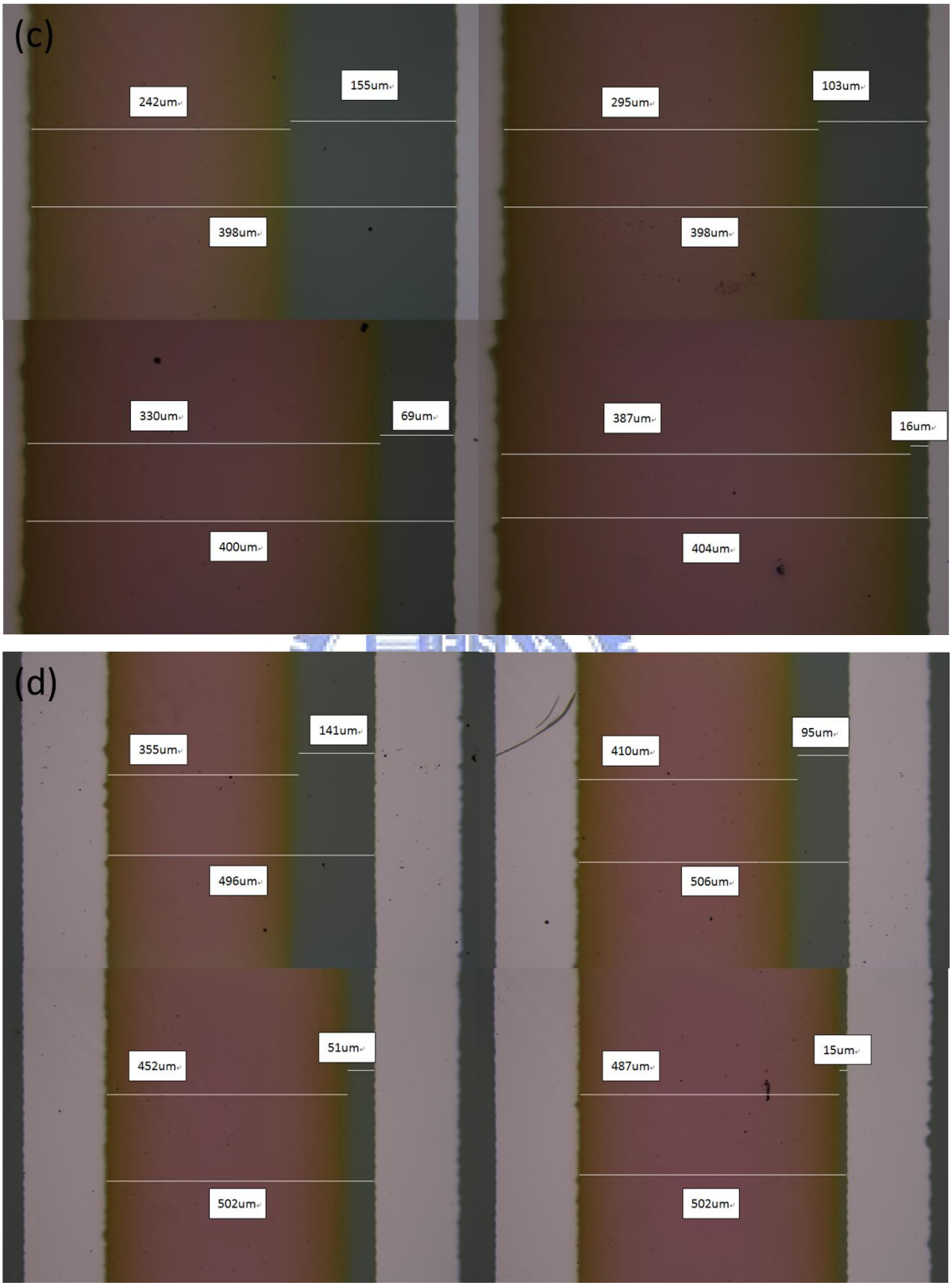


Fig. 3.20 Top view in real photos and measured length of all parameters with Si capping layer closed to drain.

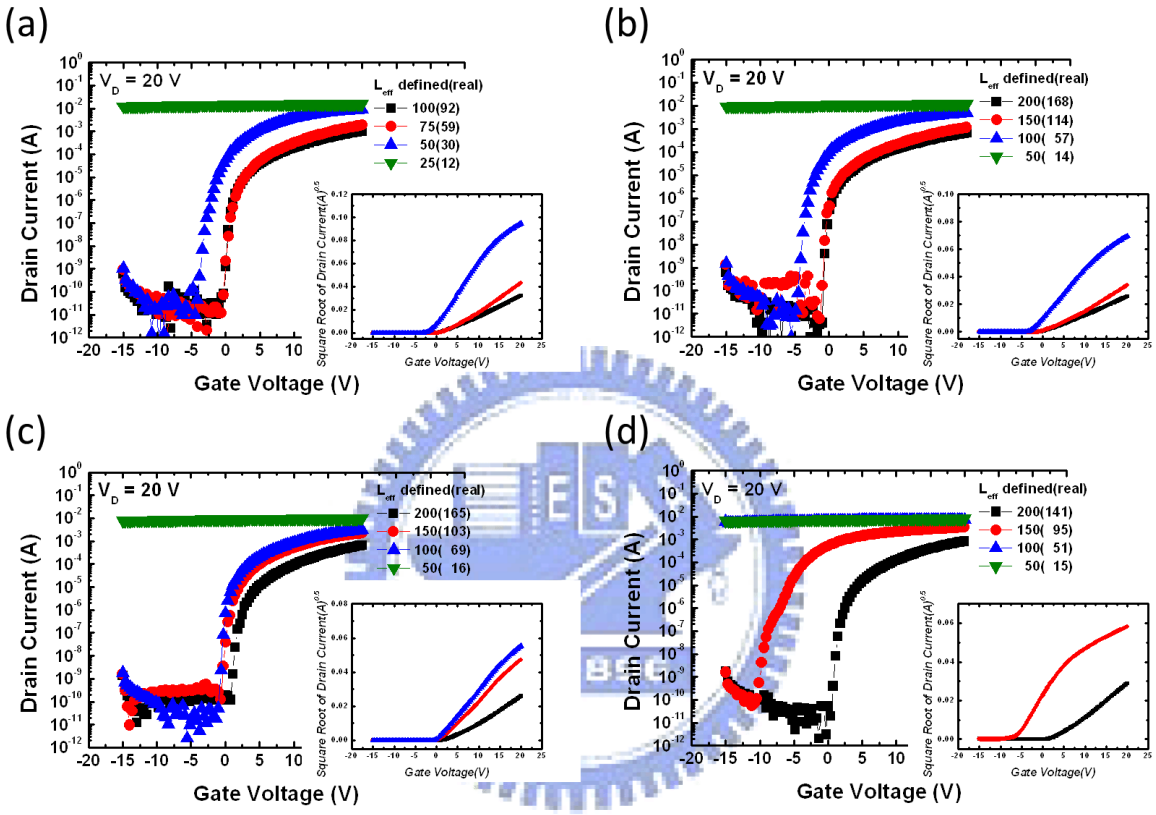


Fig. 3.21 The transfer characteristics of different ratios of uncapped length to channel length with Si capping layer closed to drain. The inset shows the $(I_D)^{0.5}$ for saturation region.

$L(L_{eff})$	V_T (V)	V_{on}(V)	μ (cm2/Vs)	μ_{uc} (cm2/Vs)	S.S. (V/dec.)	On/Off
205(92)	0.75	-0.3	18.97	8.73	0.25	1.30E+07
205(59)	1.3	-0.65	32.47	9.58	0.38	1.60E+08
203(30)	-1.36	-4.5	223.33	33.50	0.37	9.00E+08
205(12)						
297(168)	-0.08	-1	15.83	8.86	0.12	1.70E+08
297(114)	0.35	-1.35	30.01	11.40	0.21	1.90E+08
293(57)	-2.71	-5.2	146.68	27.87	0.38	7.00E+08
293(14)						
398(155)	2.9	0.75	30.28	11.73	0.34	5.50E+06
398(103)	1.41	-0.65	106.93	27.53	0.31	1.70E+07
400(69)	0.31	-1.35	138.99	23.98	0.29	1.70E+08
404(16)						
496(141)	3.49	0.4	56.78	16.01	0.27	4.40E+07
506(95)	-6.4	-11.15	230.95	43.88	0.74	6.50E+07
502(51)						
502(15)						

Table. 3.5 Extracted parameters for different ratios of uncapped length to channel length of a-IGZO devices with Si capping layer closed to the drain side.

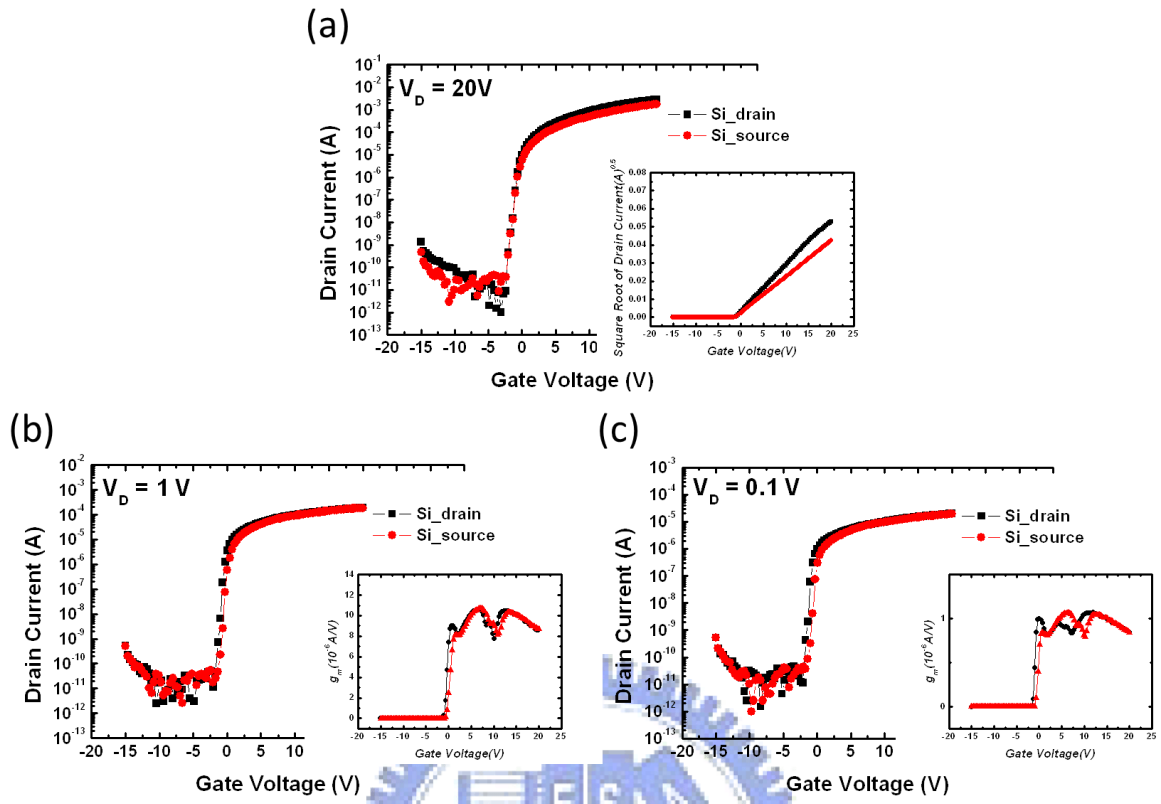


Fig. 3.22 The transfer characteristics of Si-capped devices with different positions (close to drain or source) and applied drain voltages for (a) V_D = 20 V (b) V_D = 1V and (c) V_D = 0.1 V. The inset is $(I_D)^{0.5}$ for saturation region and g_m for linear region.

V_{DS}	Si capping side	V_T (V)	V_{on}(V)	μ (cm2/Vs)	μ_{uc} (cm2/Vs)	S.S. (V/dec.)	On/Off
20V	Drain	-1.23	-2.4	100.45	25.11	0.32	3.10E+08
	Source	-1.21	-2.4	59.46	14.87	0.41	4.70E+07
1V	Drain	-0.41	-2.05	74	18.5	0.38	1.70E+07
	Source	0.29	-1.35	73.82	18.46	0.4	4.00E+06
0.1V	Drain	-0.73	-2.05	73.26	18.32	0.31	1.70E+06
	Source	0.18	-1.7	74.33	18.58	0.51	5.30E+05

Table. 3.6 Extracted parameters of Si-capped devices with different positions (close to drain or source) and applied drain voltages.

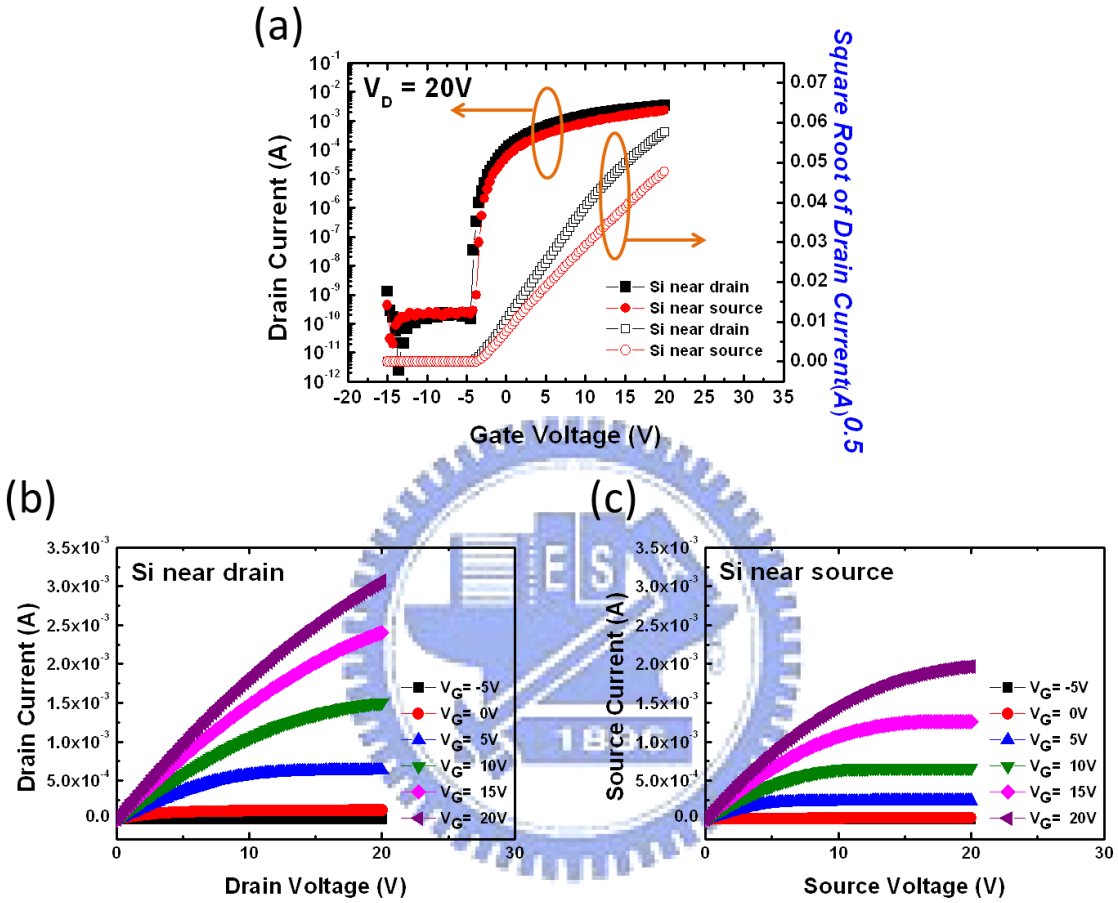


Fig. 3.23 (a) The transfer characteristics and (b), (c) the I_D-V_D curves of Si-capped devices with different positions (close to drain or source).

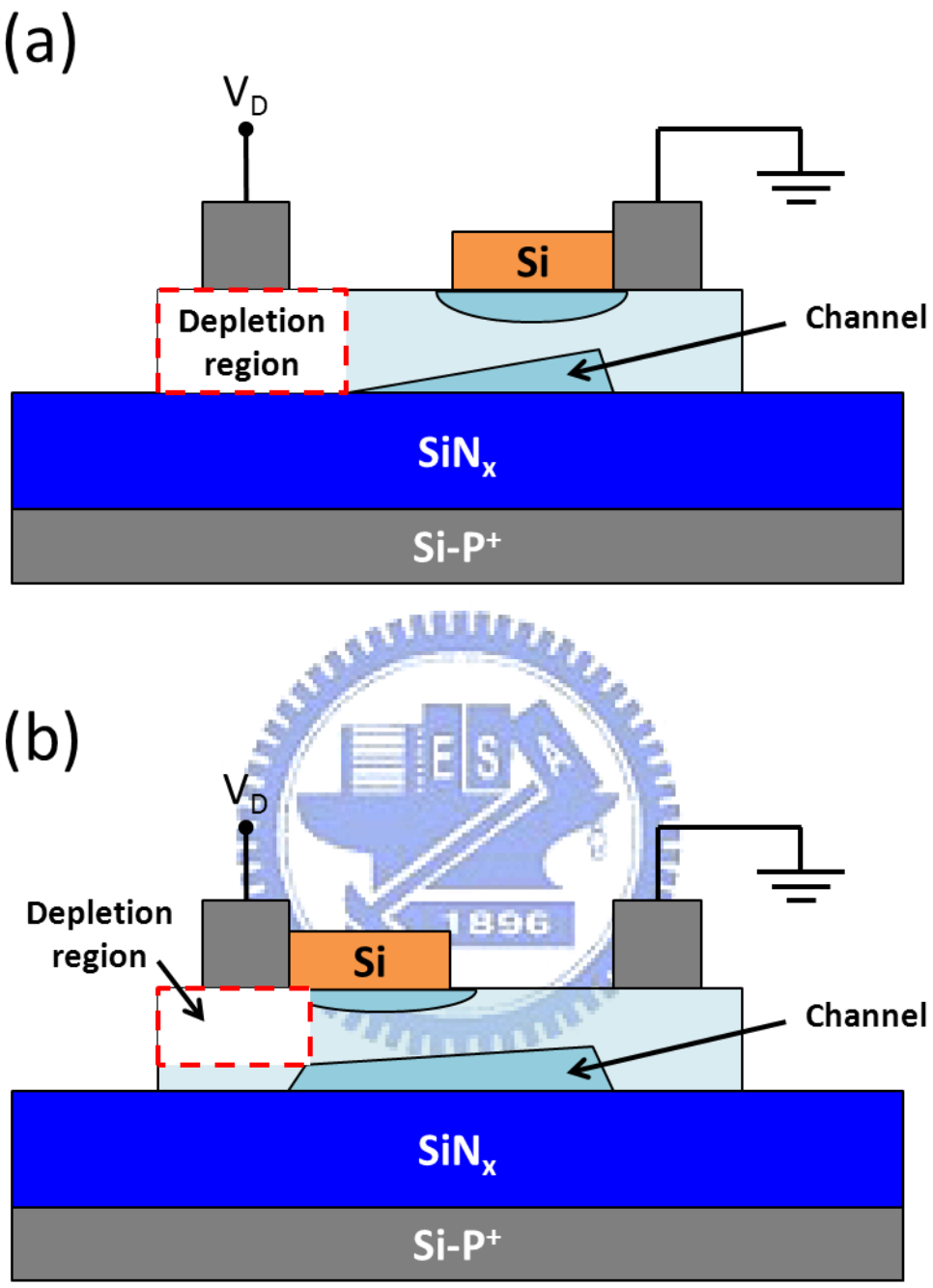


Fig. 3.24 The schematic cross-section and mechanism of the a-IGZO TFT with Si capping layer (a) close to source and (b) close to drain side.

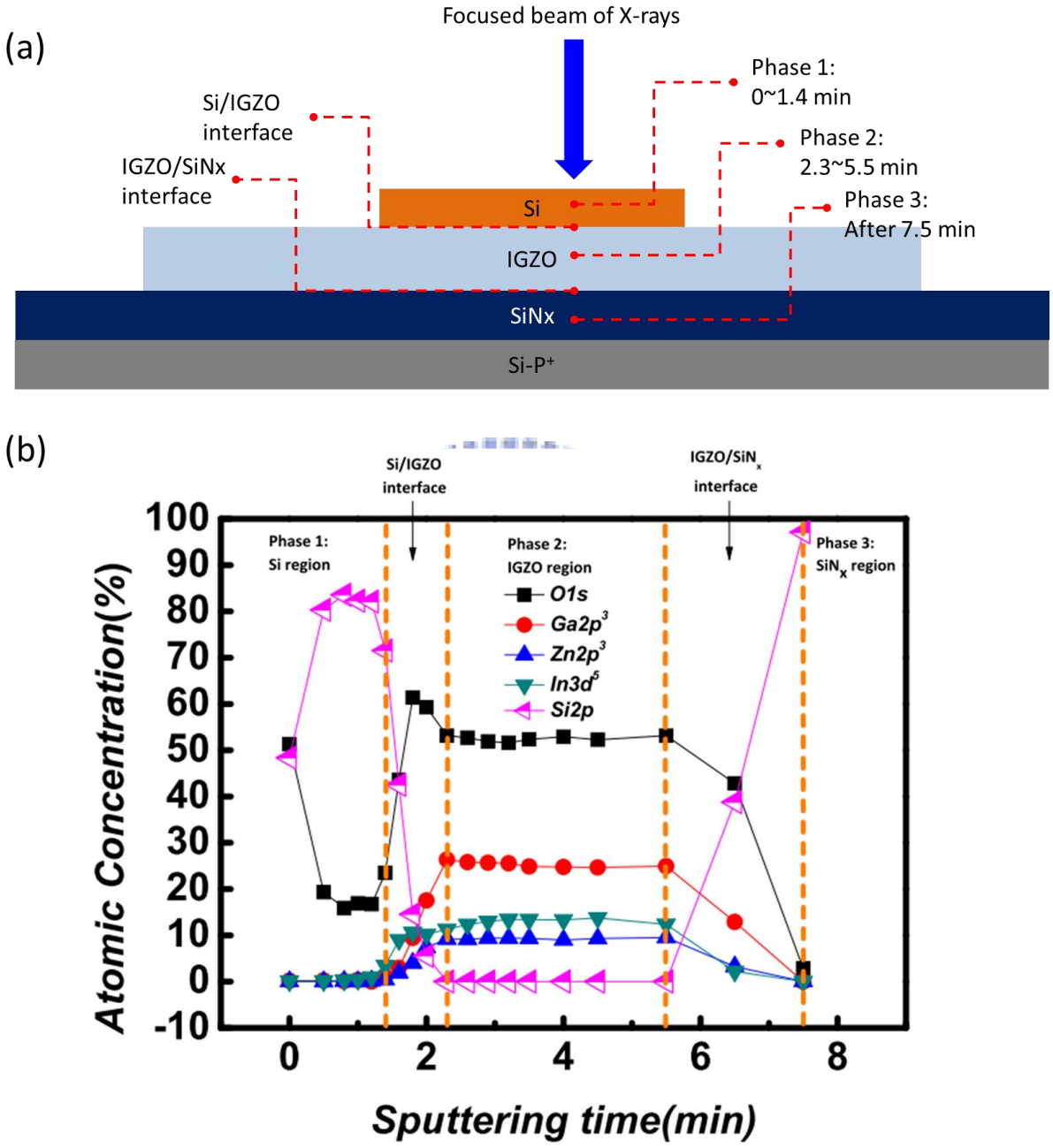


Fig. 3.25 (a) Depth profile diagram with etching position variation to etching time and (b) the atomic concentration variation of O_{1s}、Zn_{2p3}、Ga_{2p3} and In_{3d5} of depth profile with sputtering time.

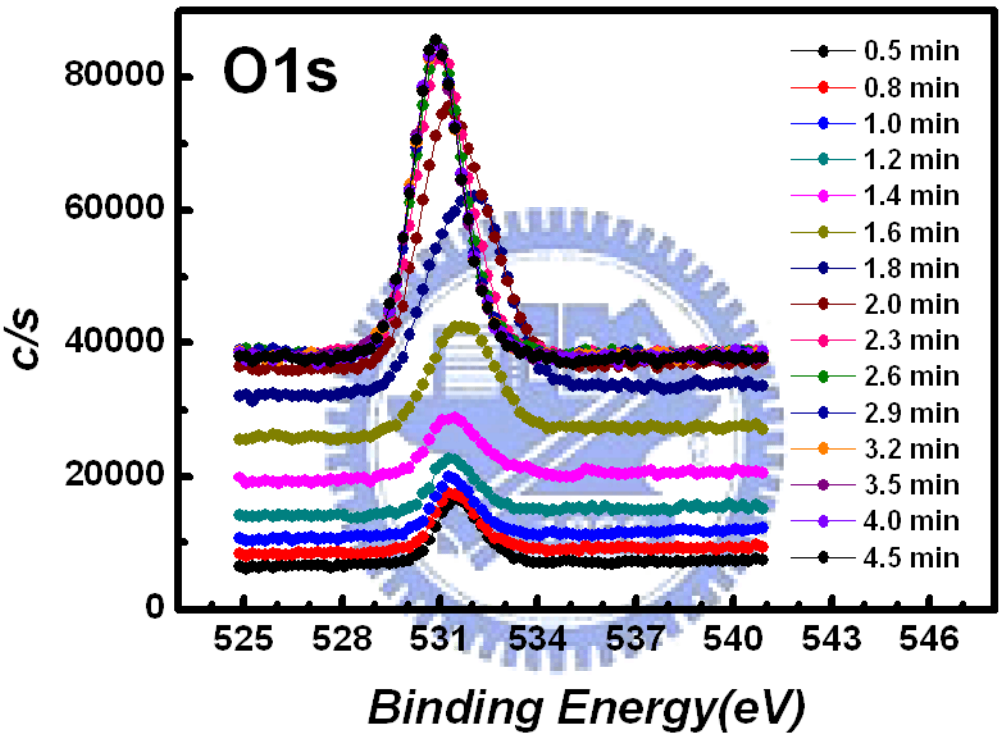
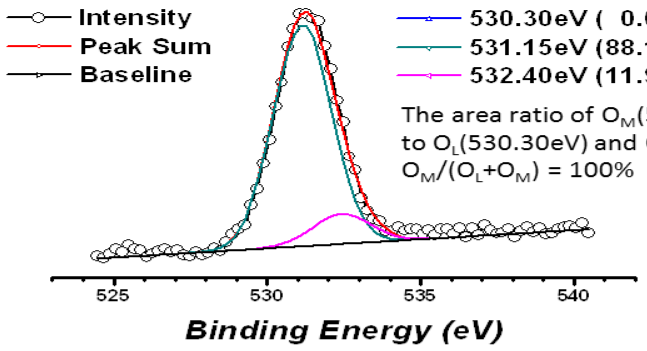
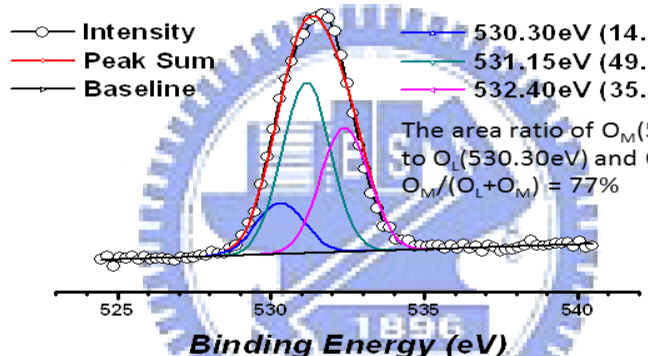


Fig. 3.26 O_{1s} XPS spectra for bottom gate a-IGZO capping SiOx layer with etching time.

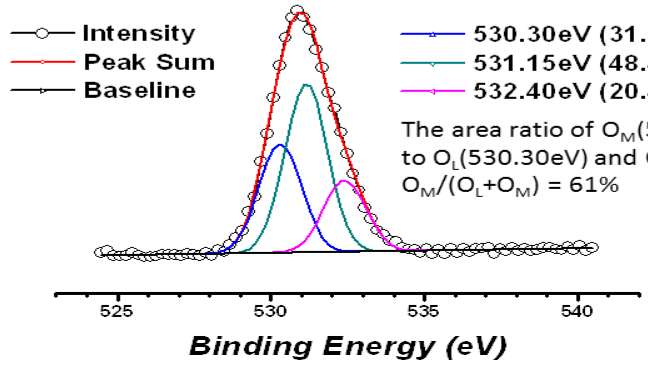
(a) Etching time 1.6 min
(Si/IGZO interface)



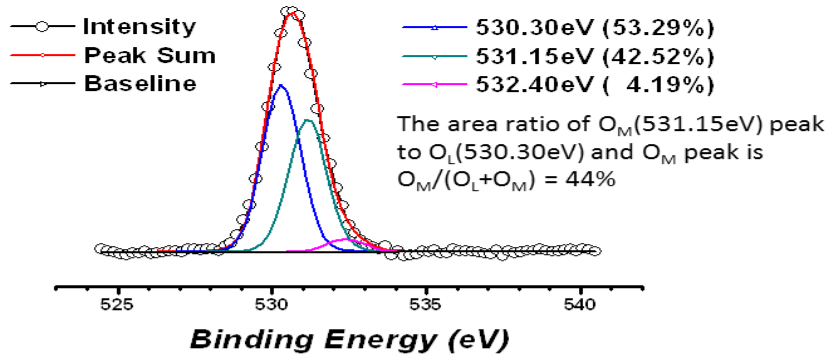
(b) Etching time 1.8 min
(Si/IGZO interface)



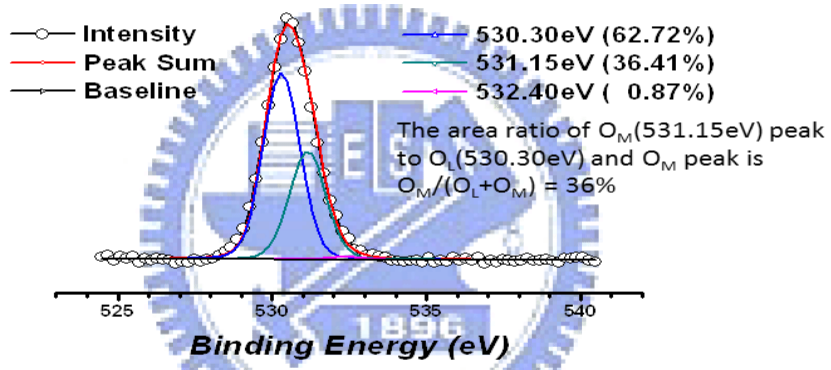
(c) Etching time 2.0 min
(Si/IGZO interface)



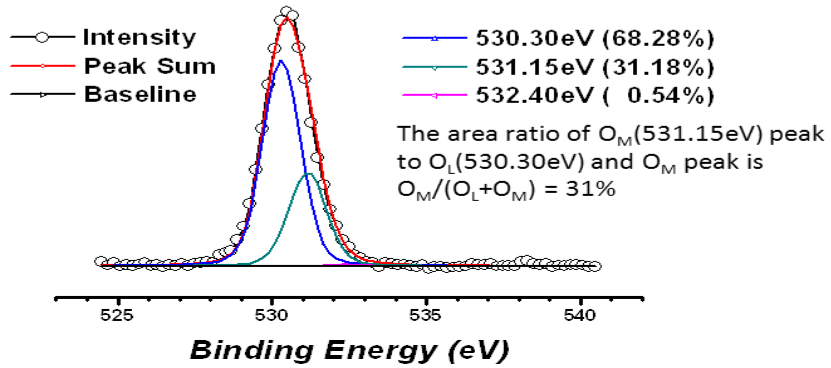
(d) Etching time 2.3 min
(at IGZO back surface)



(e) Etching time 2.6 min
(below IGZO back surface)



(f) Etching time 3.5 min
(in IGZO bulk)



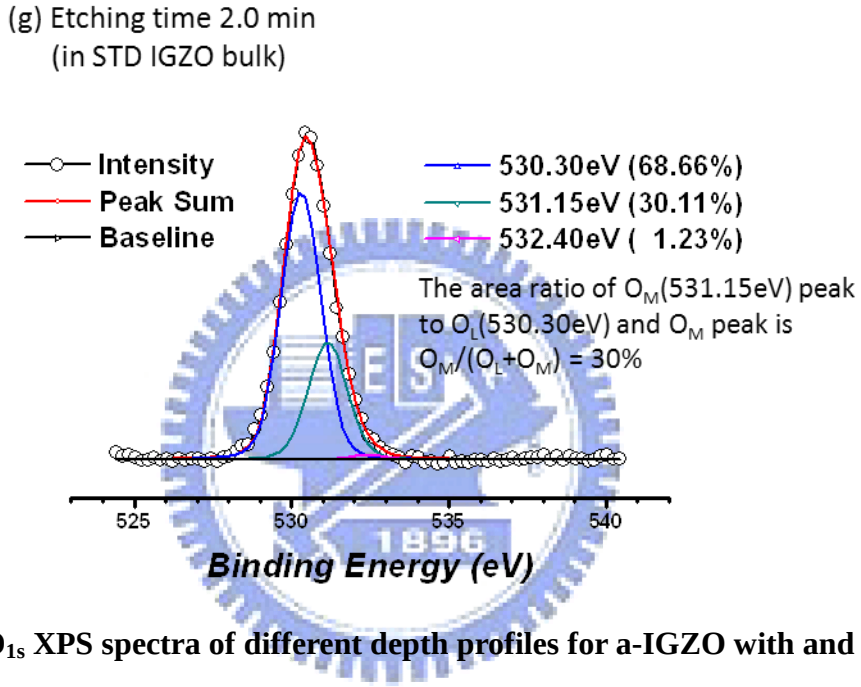


Fig. 3.27 The O_{1s} XPS spectra of different depth profiles for a-IGZO with and without Si capping layer; (a), (b), (c), (d), (e) and (f) for Si-capped a-IGZO with etching time 1.6, 1.8, 2.0, 2.3, 2.6, and 3.5 min, respectively. (g) for STD a-IGZO in the bulk.

	Area ratio of O_L(530.30eV) peak (%)	Area ratio of O_M(531.15eV) peak (%)	$O_M/(O_L+O_M)$ (%)
Etching 1.6 min (Si/IGZO)	0.00	88.10	100
Etching 1.8 min (Si/IGZO)	14.82	49.27	77
Etching 2.0 min (Si/IGZO)	31.17	48.42	61
Etching 2.3 min (at IGZO back surface)	53.29	42.59	44
Etching 2.6 min (below IGZO back surface)	62.72	36.41	36
Etching 3.5 min (in IGZO bulk)	68.28	31.18	31
Etching 2.0 min (STD IGZO bulk)	68.66	30.11	30

Table. 3.7 The area ratio of O_L(530.30eV) 1s peak, O_M(531.15eV) 1s peak and $O_M/(O_L+O_M$)with different etching time.

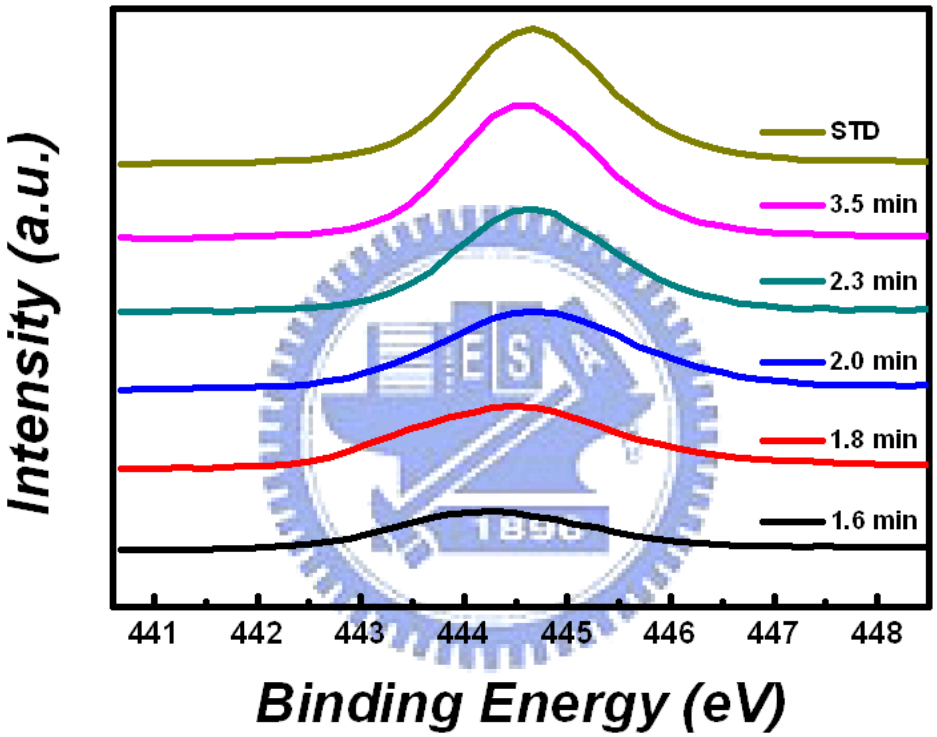


Fig. 3.28 The In_{3d5} XPS spectra of different depth profiles for a-IGZO with and without Si capping layer; the lines from the bottom are Si-capped a-IGZO with etching time 1.6, 1.8, 2.0, 2.3 and 3.5 min, repectively. The top line is for STD a-IGZO in the bulk.

Chapter 4 CONCLUSIONS AND FUTURE WORK

4-1 Conclusions

In this thesis, a-IGZO thin film transistor with a Si capping layer was fabricate, and we discussed some interesting mechanism of the device in detail. The oxygen ratio of Si resource were first found to related with the characteristics, and we observed that when the capping layer is lack of oxygen such as Si or SiO, it might be absorb the oxygen from a-IGZO films, and therefore, a-IGZO films can generate extra electron carriers due to oxygen vacancy. This simple structure could provide a powerful solution of enhancement of device performance. However, the Si-capped device would decay with time, which indicates that it was sensitive to the environment, and high temperature annealing could eliminate all the effect and return to its original state. Therefore, the passivation layer was needed to isolate with the environment, and also could improve the stability. The deposition method and material of passivation layer were great issues, and in this study we still couldn't find a better way to protect the device without changing the characteristics and enhance the stability.

Secondly, the high performance co-sputtered a-IGZO/IZO was developed. But combined with Si capping layer, the threshold voltage would be too negative to increase the power consumption when stable.

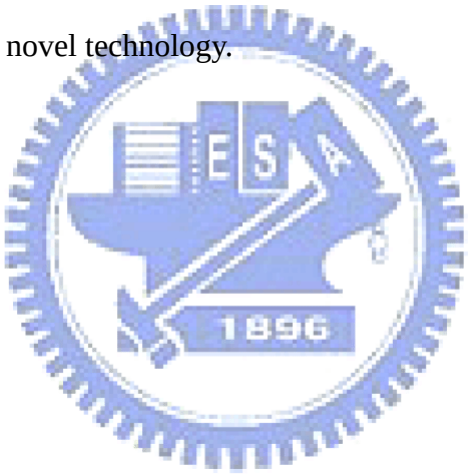
In the end, a set of experiments were designed to investigate some mechanism of Si capping layer on a-IGZO. We changed the capping length and position, took the real photos and realized the effect would be not only right beneath the capping area but expand to the side within 100 μm. The XPS analysis helped us to prove that the oxygen vacancies really increased near back interface with the Si capping layer.

In summary, the method of capping Si layer is a simple and effective approach to fabricate

a feasible metal oxide transistor. But we have still a lot of works to discover the whole mechanism and more applocations.

4-2 Future Work

Although high mobility is obtained by capping Si as a reduction layer, the detail mechanism is still unclear. According to experiment results, it is sure that oxygen vacancy increase near the interface region, which cause higher carrier concentration and conductivity, but how far and deep the effect would take place is a uncontrollable thing. Moreover, the stability is really a big issue in practical use. We hope that a suitable passivation layer could well satisfy and apply to the novel technology.



Reference

[1] E. E. Hahn, *J. Appl. Phys.*, **22** (1951) 855.

[2] M. Orita, H. Ohta, M. H irano, S. Narushima and H. Hosono, *Philosophical magazine B* , **81** (2001) 501.

[3] S. Masuda, K. Kitamura, Y. Okumura, S. Miyatake, H. Tabata, and T. Kawai, *J. Appl. Phys.*, **93** (2003) 1624.

[4] W. B. Jackson, R. L. Hoffman, and G. S. Herman, *Appl. Phys. Lett.*, **87** (2005) 193503.

[5] N. L. Dehuff, E. S. Kettenring, D. Hong, H. Q. Chiang, J. F. W ager, R. L. Hoffman, C. –H. Park, and D. A. Keszler, *J. Appl. Phys.*, **97** (2005) 064505.

[6] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, *Nature*, **432** (2004) 488.

[7] K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano, and H. Hosono, *Microelectronic Engineering*, **72** (2004) 294.

[8] H. Yabuta, M. Sano, K. Abe, T. Aiba, T. Den, H. Kumomi, K. Nomura, T. Kamiya, and H. Hosono, *Appl. Phys. Lett.*, **89** (2006) 112123.

[9] P. Barquinha, L. Pereira, G. Gonçalves, R. Martins, and E. Fortunato, *J. Electrochem. Soc.*, **156** (2009) H161.

[10] H. Kumomi, K. Nomura, T. Kamiya, and H. Hosono, *Thin Solid Films*, **516** (2008) 1516.

[11] H. Hosono, K. Nomura, Y. Ogo, T. Uruga, and T. Kamiya, *J. Non-Cryst. Solids*, **354** (2008) 2796.

[12] H. Q. Chiang, B. R. McFarlane, D. Hong, R. E. Presley, and J. F. Wager, *J. Non-Cryst. Solids*, **354** (2008) 2826.

[13] P. Görrn, M. Sander, J. Meyer, M. Kröger, E. Becker, H.-H. Johannes, W. Kowalsky, and T. Riedl, *Adv. Mater.*, **18** (2006) 738.

[14] W. Lim, D.P. Norton, J.H. Jang, V. Craciun, S.J. Pearton, and F. Ren, *Appl. Phys. Lett.*, **92** (2008) 122102.

[15] R. L. Hoffman, B. J. Norris, and J. F. Wager., *Appl. Phys. Lett.*, **82** (2003) 733.

[16] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano and H. Hosono, *Nature*, **432** (2004) 488.

[17] N. F. Nott, *Adv. Phys.*, **26** (1977) 363.

[18] S. Narushima, M. Orita, M. Hirano, and H. Hosono, *Phys. Rev. B*, **66** (2002) 035203.

[19] A. Takagi, K. Nomura, H. Ohta, H. Yanagia, T. Kamiya, M. Hirano, and H. Hosono, *Thin Solid Films*, **486** (2005) 38.

[20] K. Nomura, T. Kamiya, H. Ohta, K. Ueda, M. Hirano, and H. Hosono, *Appl. Phys. Lett.*, **85** (2004) 1993.

[21] T. Iwasaki, N. Itagaki, T. Den, H. Kumomi, K. Nomura, T. Kamiya, and H. Hosono, *Appl. Phys. Lett.*, **90** (2007) 242114.

[22] T. Kamiya, H. Hiramatsu, K. Nomura, and H. Hosono, *J. Electroceram.*, **17** (2006) 267.

[23] H. Hosono, *J. Non-Cryst. Solids*, **352** (2006) 851.

[24] H. C. Pan, M. H. Shiao, C. Y. Su, and C. N. Hsiao, *J. Vac. Sci. Technol. A*, **23** (2005) 1187.

[25] R. Martins, P. Barquinha, I. Ferreira, L. Pereira, G. Goncalves, and E. Fortunato, *J. Appl. Phys.*, **101** (2007) 044505.

[26] B. S. Jeong, Y. G. Ha, J. Moon, A. Facchetti, and T. J. Marks, *Adv. Mater.*, **22** (2010) 1346.

[27] K. Nomura, A. Takagi, T. Kamiya, H. Ohta, M. Hirano and H. Hosono, *Jpn. J. Appl. Phys.*, **45** (2006) 4303.

[28] M. Chen, X. Wang, Y. H. Yu, Z. L. Pei, X. D. Bai, C. Sun, R. F. Huang, and L. S. Wen, *Appl. Surf. Sci.*, **158** (2000) 134.

[29] R. Sanjinés, C. Coluzza, D. Rosenfeld, F. Gozzo, Ph. Alméras, F. Lévy, and G. Margaritondo, *J. Appl. Phys.*, **73** (1993) 3997.

[30] T. Szörényi, L. D. Laude, I. Bertóti, Z. Kántor, and Zs. Geretovszky, *J. Appl. Phys.*, **78** (1995) 6211.

[31] J. S. Park, J. K. Jeong, H. J. Chung, Y. G. Mo, and H. D. Kim, *Appl. Phys. Lett.*, **92** (2008) 072104.

[32] J. K. Jeong, H. W. Yang, J. H. Jeong, Y. G. Mo, and H. D. Kim, *Appl. Phys. Lett.*, **93** (2008) 123508.

[33] D. H. Cho ,S. H. Yang , J.-H. Shin , C. W. Byun , M. K. Ryu , J. I. Lee , C. S. Hwang and H. Y. Chu, *J. Korean Phys. Soc.*, **54** (2009) 531.

[34] T. Kamiya, K. Nomura, M. Hirano and H. Hosono, *Phys. Stat. Sol. (c)*, **5** (2008) 3098.

[35] J. K. Jeong, H. W. Yang, J. H. Jeong, Y. G. Mo, and H. D. Kim, *Appl. Phys. Lett.*, **91** (2007) 113505.

[36] H. J. Chang, K. M. Huang, C. H. Chu, S. F. Chen, T. H. Huang, and M. C. Wu, *ECS Trans.*, **28** (2010) 137.