國 立 交 通 大 學

光電工程學系碩士班

碩士論文

具有奈米點摻雜之
高效能雙閘極非晶銦鎵鋅氧薄膜電晶體

High Performance Dual Gate Amorphous Indium-Gallium-Zinc-Oxide Thin Film Transistor With Nanometer Dot-like Doping

研 究 生: 廖峻宏

指導教授：蔡娟娟 教授

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中文摘要

近年來非晶氧化銦鎵鋅用作薄膜電晶體的主動層上被視為深具潛力的材料。此材料比起傳統非晶矽半導體具有高載子遷移率(~10 cm^2/Vs),較低的工作電壓(<5V)，以及其小的次臨界電壓擺幅。當要應用 a-IGZO 薄膜電晶體於電子元件上，需要發展低損耗、高操作頻率以及良好的電特性，也就是朝高載子遷移率和低次臨界擺幅作為目標。許多技術可以提升電子特性，藉由連結上閘極與下閘極的雙閘極操控電晶體通道為其中一種技術。先前的研究中，利用一個新穎的製程結構-奈米點摻雜於通道上來有效提高 a-IGZO TFTs 的載子遷移率。我們提出在 a-IGZO 通道上形成許多鄰近高導電的奈米點狀摻雜可以降低位障，藉此新的製程結構可以使上閘極電晶體的載子遷移率從 4 $cm^2V^{-1}s^{-1}$ 大幅提升至 79$cm^2V^{-1}s^{-1}$。而在本文中，結合雙閘極操作電晶體與奈米點摻雜的技術，期望能在 a-IGZO 中降低垂直電場的影響進而提高效能。最後，我們在雙閘極操作下相比較上閘極與下閘極的電流合成功提升了 1.5 倍的電流，而使用上絕緣層的介電常數來萃取等效的載子遷移率，此雙閘極奈米孔洞結構 a-IGZO 薄膜電晶體可達到 272 $cm^2V^{-1}s^{-1}$　上閘極奈米孔洞結構也可以達到 102 $cm^2V^{-1}s^{-1}$。

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High Performance Dual Gate Amorphous Indium-Gallium-Zinc-Oxide Thin Film Transistor
With
Nanometer Dot-like Doping

Student: Chun-Hung Liao Advisor: Prof. Chuang-Chuang Tsai

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Abstract

Recently, a-IGZO is the high-potential material for active layer of thin film transistor. With a high mobility (>10 cm^2/Vs) than conventional amorphous silicon semiconductor and a low operating voltage (< 5 V) and small sub-threshold voltage swing, amorphous In-Ga-Zn-O thin-film transistors (a-IGZO TFTs) draw a lot of attentions. When a-IGZO TFTs are developed for a low-power high-frequency circuit, good electron performances, such as high field-effect mobility (μ_{FE}) and low sub-threshold swing (S.S.) are required. Dual gate (DG) is one of the techniques to enhance the performance of a-IGZO TFTs by connecting top gate (TG) and bottom gate (BG) together to enhance the channel accumulation. In our previous work, we have demonstrated that the effective mobility of a-IGZO TFT can be greatly improved by utilizing nano-meter dot-like doping (NDD) in a-IGZO channel region. We

proposed that the NDD structure lowers the potential barrier in the intrinsic a-IGZO by the neighboring high conductive regions and hence increase the field-effect mobility of TG a-IGZO TFTs from 4 to 79 $cm^2V^{-1}s^{-1}$. In this work, we employ NDD in DG a-IGZO TFTs. By connecting TG and BG together, we expect to reduce the vertical field in a-IGZO film and to further enhance the mobility. We successfully obtain a 1.5-times enhanced output current in DG NDD a-IGZO TFT. Taking the gate capacitance of TG NDD as the reference, the effective mobility for TG NDD a-IGZO TFT and for DG NDD IGZO TFT are 102 $cm^2V^{-1}s^{-1}$ and 272 $cm^2V^{-1}s^{-1}$, respectively.

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兩年，轉眼之間就過去。當初跨科系考進交大光電所，懵懂的我對一切都很陌生，當時看著學長們彼此討論著實驗的數據，疑問多到無所適從，那時總是聽到一句，”以後你就懂了”。到今天，雖然還是對許多地方不懂，但是能順利完成這篇論文。首先感謝指導教授冉曉雯老師和蔡娟娟老師的指導。其中，冉老師在研究上教導我積極與嚴謹的態度，並且講求實驗的效率，有許多前瞻的概念讓我在這兩年對不同的製程作研究，也藉此能接觸到更寬廣的領域。蔡老師則是讓我能提前見識公司的專業，與學校的不同讓眼界更為寬廣。在此對老師們致上最深的敬意。

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Chapter 1

Introduction

1-1 Introduction

1-1.1 The advantage of metal-oxide transistors

Metal-oxide semiconductor was first reported in 1964 by H. A. Klasens *et.al.* [1] The material of metal oxide composed of heavy metal cations with an electronic configuration $(n-1)d^{10}ns^{0}$ ($n \geq 4$) are promising candidate for next generation semiconductor. [2] There is a large overlap between the adjacent orbitals which have large radius, show in Fig. 1.1. In the past few years, there are some metal-oxide materials have been reported as the channel materials in TFTs, such as the polycrystalline zinc oxide (ZnO) [3], amorphous zinc tin oxide (ZTO) [4], amorphous zinc indium oxide (ZIO)[5], and amorphous indium gallium zinc oxide (IGZO).[6-8] Among the transparent metal-oxide channel materials, amorphous indium gallium zinc oxide (a-IGZO) is promising as active layer of thin film transistors (TFTs) due to their good transparency, high mobility, and unique electrical properties.[2] Furthermore, the amorphous IGZO was insensitiveness to the distorted metal–oxygen-metal chemical bonds.[2] Large band gap (>3eV) induces that the a-IGZO material is transparent in visible region (400nm~700nm) and is insensitive to

the ambient light. The carrier concentration (n: 10^{13}~10^{20} cm^{-3}) in the a-IGZO film can be tunable by controlling the oxygen pressure or the composition of IGZO target during film deposition.[9]

a-IGZO TFTs is applied in temperature limited substrates like glass or flexible substrate, so that the radio-frequency (rf) sputtering technique is one of a few methods which enables us to deposit thin films of high-melting-temperature materials over large areas at low substrate temperatures.[10] However, H. Hosono *et al.* proposed that the chemical species and/or a structure in a thin film are naturally unstable, when the thin films are deposited at low temperatures. [10,11] On the contrary, they are stable while the thin films are deposited at higher temperatures. The chemical species and/or a structure are frozen in the as-deposited thin film which relax to a more stable state and /or give the atoms more energy to rearrange upon thermal annealing, leading to an appreciable change in the electron transport properties. [10,11] Most metal-oxide TFTs are fabricated by physical vapor deposition (PVD) techniques at room temperature and often require a high temperature post-deposition thermal annealing process to obtain high-performance and high-stability TFTs, especially in a-IGZO TFTs. [10-16] Among the post-deposition thermal annealing techniques, rapid thermal annealing (RTA) [14,15] or furnace annealing [16] are usually utilized to anneal the metal-oxide TFT devices. For the application of a-IGZO TFTs which is

fabricated on the flexible substrate, high temperature thermal annealing may damage the substrates. Development of the low annealing temperature method is necessary when the a-IGZO thin film is deposited on flexible or others temperature limited substrates.

1-1.2 Carrier transport mechanism of metal-oxide semiconductors

The mechanism of carrier transport in amorphous oxide semiconductor, a-IGZO, was discussed in this section. The transport mechanism of hydrogenated amorphous silicon for flexible TFTs will be described briefly before reporting the a-IGZO mechanism. As shown in Fig. 1.2, the paths of carrier transport in a-Si:H composed with covalent bonds of sp^3 orbitals was affected obviously by strong spatial directivity and disorder structure. The electronic levels and trap states were influenced by the fluctuation of the bonding angle in the a-Si:H structure. [17] Compare with the a-Si:H, the characteristics in amorphous oxide semiconductors (AOSs) are different from the semiconductors with covalent bonds. The carrier transport path in AOSs was shown in Fig. 1.3. The bottom of the conduction band in the oxide semiconductors that has large ionicity is primarily composed by spatially spread metal ns (here n is the principal quantum number) orbitals with isotropic shape. [17] There were no

conduction paths formed by the 4s orbitals had been obtain so far in any amorphous oxide. Based on these facts, the necessary condition for good conductivity in a-IGZO is that the conduction paths should be composed of the ns orbitals. The principal quantum number is at least 5 [18] and direct overlap among the neighbor metal ns orbitals is possible. The magnitude of this overlap is insensitiveness to distorted metal–oxygen–metal (M–O–M) chemical bonds that intrinsically exist in amorphous materials.[19,20] The amorphous oxide semiconductors (AOSs) containing post-transition-metal cations was possible to show the degenerate band conduction and high mobility (>10 cm^2/Vs). [18,21]

The carrier transport mechanism and electronic structure in an amorphous indium gallium zinc oxide semiconductor, from the Fig. 1.4, the Hall mobility of a-IGZO is increased distinctly from ~3 cm^2 $(Vs)^{-1}$ to 13 cm^2 $(Vs)^{-1}$ as carrier concentration increased from 10^{15} cm^{-3} to 10^{19} cm^{-3}. The carrier transport mechanism and electronic structure in an amorphous oxide semiconductor is similar to that of crystalline IGZO, and is explained by percolation conduction through potential barriers in the vicinity of conduction band edge. The potential barriers are thought to originate from random distribution of Ga^{3+} and Zn^{2+} ions in the $GaO^{+}(ZnO)_5$ layer. The effective mass of a-IGZO was 0.34 m_e, which is almost the same as that of crystalline IGZO. These results imply the electronic structure and carrier transport

mechanism in a- IGZO are similar to that in sc-IGZO, which would be associated with the electronic structure of metal-oxide semiconductors in which electron transport paths are made of spherical extended s orbitals and are not largely affected by local distortion of the chemical bonds.[22] We can see that the intermediate region in Fig. 1.5 (10^{14} cm^{-3}<N_e<N_{th}), the carriers still need to flow over the potential barriers as E_F is below E_{th}, leading to the thermally activated percolation behaviors in μ and σ. When E_F exceeds E_{th} at N_e>N_{th}, the carriers are not affected by potential barriers anymore and exhibit the temperature-independent extended mobility.[23]

Each sub-element in this ternary material of a-IGZO film shows various characteristics to affect the parameters of TFTs. A higher concentration of In atom is expected to generate higher carrier concentration. [24] The element of In is a big atom and easy to lose electrons while the oxygen is a small atom and easy to get electrons form In atoms. The released electron from the element of In may move to the conduction band when the composition of a-IGZO is lacked for oxygen. [25] Furthermore, it will enhance the carrier transport during the operation in IGZO TFTs. The element of Ga was introduced provide high stability in a-IGZO TFTs. [26] Therefore, the element of Ga in the a-IGZO film was reducing the electron concentration and decreasing the carrier mobility. The Ga was chosen because of atomic radius of Ga closed to In. H. Hosono *et al.* reported that the Ga^{3+} in the

a-IGZO film attract the oxygen tightly due to the high ionic potential resulted from the small ionic radius and +3 valence. It suppresses the electron injection and induces the oxygen ions escaping from the a-IGZO film, providing relative high stability to the device. [27] Compare to the carrier concentration in the material of IZO (~10^{21} cm^{-3}), the a-IGZO (~10^{19} cm^{-3}) shows less carrier concentration and is reported in some researches. [20, 27-29] Introducing the element of Ga to the a-IGZO film helps the carrier concentration of the a-IGZO film to be controlled easily. However, the mobility is reduced while the Ga is introduced to the a-IGZO film. H. Hosono *et al.* proposed that doping the oxygen molecules to increasing the carrier concentration and the carrier mobility when the element if Ga was introduced the a-IGZO film.[30] The element of Zn in the a-IGZO film was reported to affect the crystallization of the metal-oxide thin film. When the ratio of the Zn atoms in the a-IGZO film is larger than 65%, the crystalline structure was reported.[25] The crystalline structure in the a-IGZO film may degrade the electrical characteristic while the uniformity was decreased by the disorder grain boundaries.

1-1.3 Carrier concentration with oxygen vacancy of a-IGZO films

The oxygen vacancy formation process closely relates to the generation of

charge carriers, according to Equation (1).

$$O_o^x = \frac{1}{2} O_{2(g)} + V_o^{\bullet\bullet} + 2e^- \quad \text{.....………..(1)}$$

O_2 is lost from the oxide sublattice ($O^x{}_o$) to create a doubly charged oxygen vacancy ($V^{''}{}_o$) and two free electrons. It can be presumed that IGZO films attain more charge carriers due to thermally enhanced or energy activated oxygen vacancy formation processes. It has been reported that the mobility of amorphous IGZO films depends on the carrier concentration, since the carrier transport is governed by percolation conduction over trap states and is enhanced at high carrier concentrations by filling the trap states.[31]

In order to understand oxygen vacancy in a-IGZO films, the chemical and the oxygen binding energy of O_{1s} were analyzed by X-ray photoelectron spectroscopy (XPS). This analysis method had been used to investigate the origin of carriers in IGZO. By Gaussian fitting, these O_{1s} peaks could be consistently divided into three peaks, approximately centered at 530.5, 531.5, and 532.5 eV. The peak with the lower energy value of 530.5 eV, represents O^{2-} ions combined with Zn, Ga, and In ions, in the IGZO compound system. This indicates the stochiometric ratio between the metal cations and oxygen anions. The medium binding energy value at 531.5 eV, is associated with O^{2-} ions which are in oxygen vacancy regions within the IGZO films.

Therefore, the change in the intensity of this peak may be largely connected to a variation in the concentration of oxygen vacancy. The higher binding energy value of 532.5 eV, is related to loosely bonded oxygen on the IGZO surface, including absorbed H_2O, CO_3, or O_2. The peak could be completely eliminated when the film is annealed or slightly etched by a plasma treatment, and is therefore considered inconsequential.[32]

1-1.4 Introduction the relationship between Argon plasma treatment and a-IGZO films

Recently, we have more requirements about technology products. Moreover, a-IGZO TFTs are promising for developed a low-power high-frequency circuit because of their high mobility. The effect of Ar plasma treatment on amorphous indium gallium zinc oxide thin films was investigated. The net electron carrier concentration (10^{20}–10^{21} cm^{-3}) of the *a*-IGZO thin films dramatically increased upon their exposure to the Ar plasma compared to that (10^{14} cm^{-3}) of the as-deposited thin film. Furthermore, the sheet resistivity dramatically decreased after Ar plasma treated 60 seconds. Above results we mentioned were shown in Fig. 1.6. Energetic Ar ion bombardment during plasma treatment is known to induce the preferential sputtering of the relatively light atoms from the surfaces of II-VI or III-V group semiconductors

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as a result of the physical momentum transfer between the ions in the plasma and the atoms on the material surface. Therefore, it is believed that the dramatic change of the electron concentration upon the exposure to the Ar plasma comes from the oxygen deficiency on the *a*-IGZO film surface. [33]

1-2 Motivation

Metal oxide semiconductor usually possess direct band gap and transparent characteristic. There are many advantages of a-IGZO such like high mobility (>10 cm^2/Vs), large band gap (>3eV), and low temperature fabrication processes. The applications on display, a-IGZO TFTs are also promising for the development of RFID tag, smart cards, and other types of flexible electronics. When a-IGZO TFTs are developed for a low-power high-frequency circuit, good electron performances, such as high field-effect mobility (μ_{FE}) and low subthreshold swing (S.S.) are required. Dual gate (DG) is one of the techniques to enhance the performance of a-IGZO TFTs by connecting top gate (TG) and bottom gate (BG) together to enhance the channel accumulation. We combine the dual gate structure in TFT and the technique of enhancement device performance. Trying to find out what is the most effective technique to realize a high performance TFT with high electron mobility.

1-3 Thesis outline

In chapter 1, we introduced briefly the background of amorphous metal-oxide TFTs and the mechanism of carrier transport . Moreover, the Argon plasma treatment can increase the carrier concentration of a-IGZO films.

In chapter 2, we introduced the experiment setup such as device fabrication, plasma system, and how to extract the characteristics parameters. Then overview experiment equipment such as radio frequency (RF) sputter, thermal evaporator, and HP 5210A electric transfer characteristic measurement.

In chapter 3, extracted the capacitance of top gate insulator and bottom gate insulator. the variation of resistivity of a-IGZO thin film formed a function of Ar treatment time were discussed and improved past research combined the method of nano dot-like doping method and dual gate structure demonstrated the drain current obtain 1.5times enhanced output current in DG NDD a-IGZO TFT.

In chapter 4, the results in our research are concluded. Suggestions for future work are also provided for further studies on a-IGZO TFTs.

Figure in Chapter 1

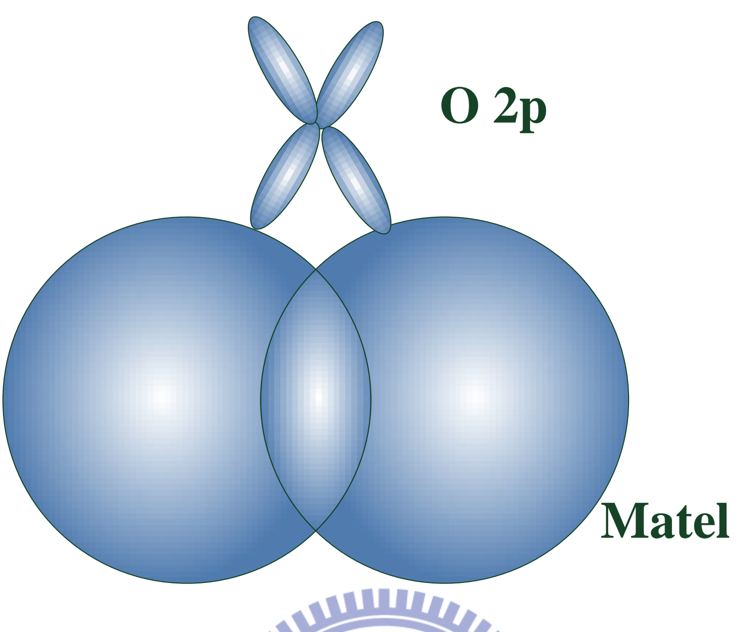

Fig. 1.1 The overlap between the adjacent orbitals [2].

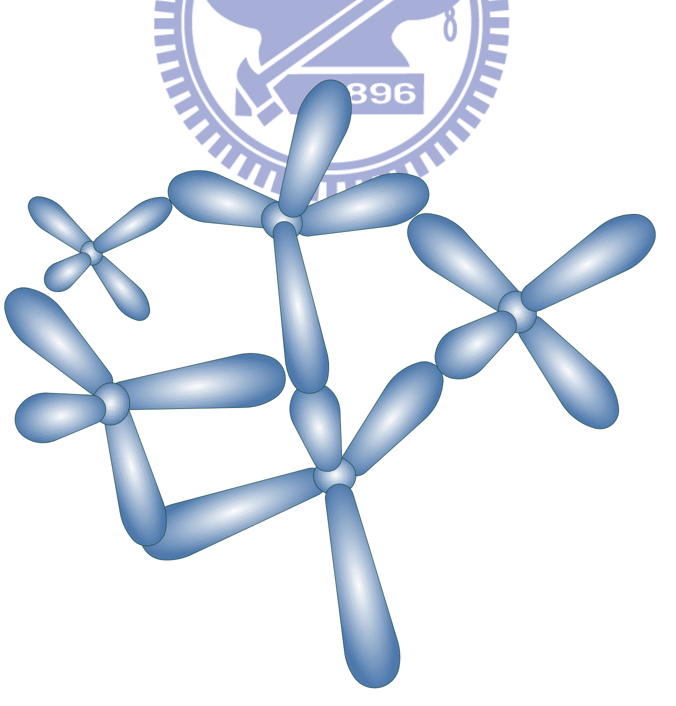

Fig. 1.2 The carrier transport paths in covalent semiconductors [2].

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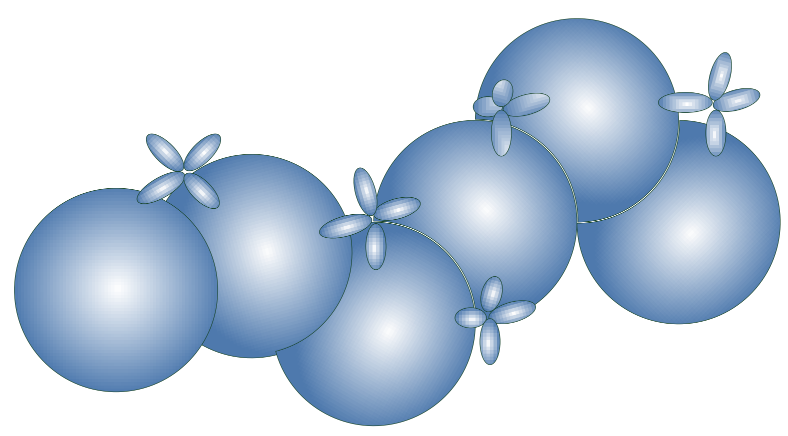


Fig. 1.3 The carrier transport paths in AOSs [2].

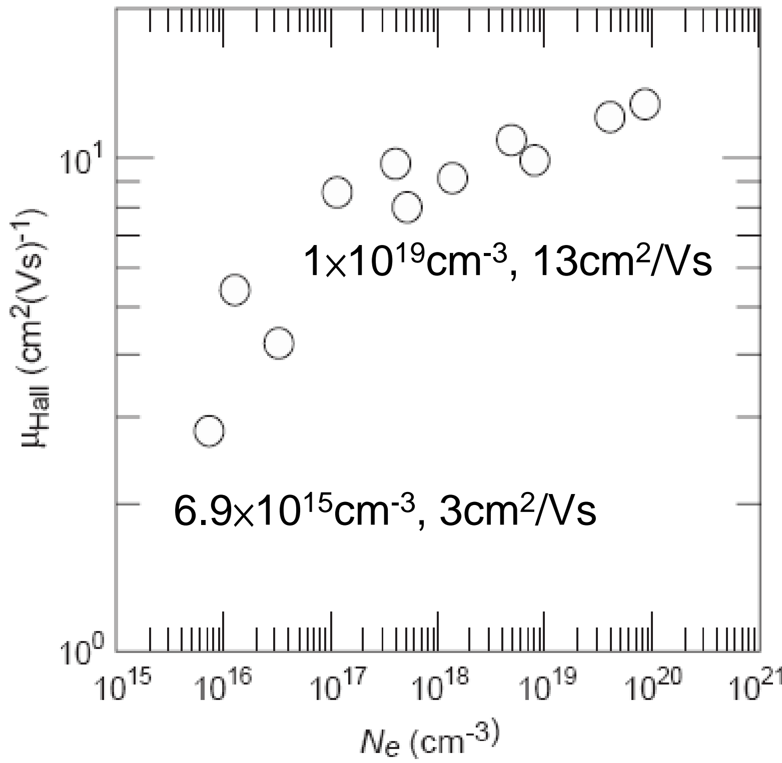


Fig. 1.4 Hall mobility at RT as a function of carrier concentration [22].

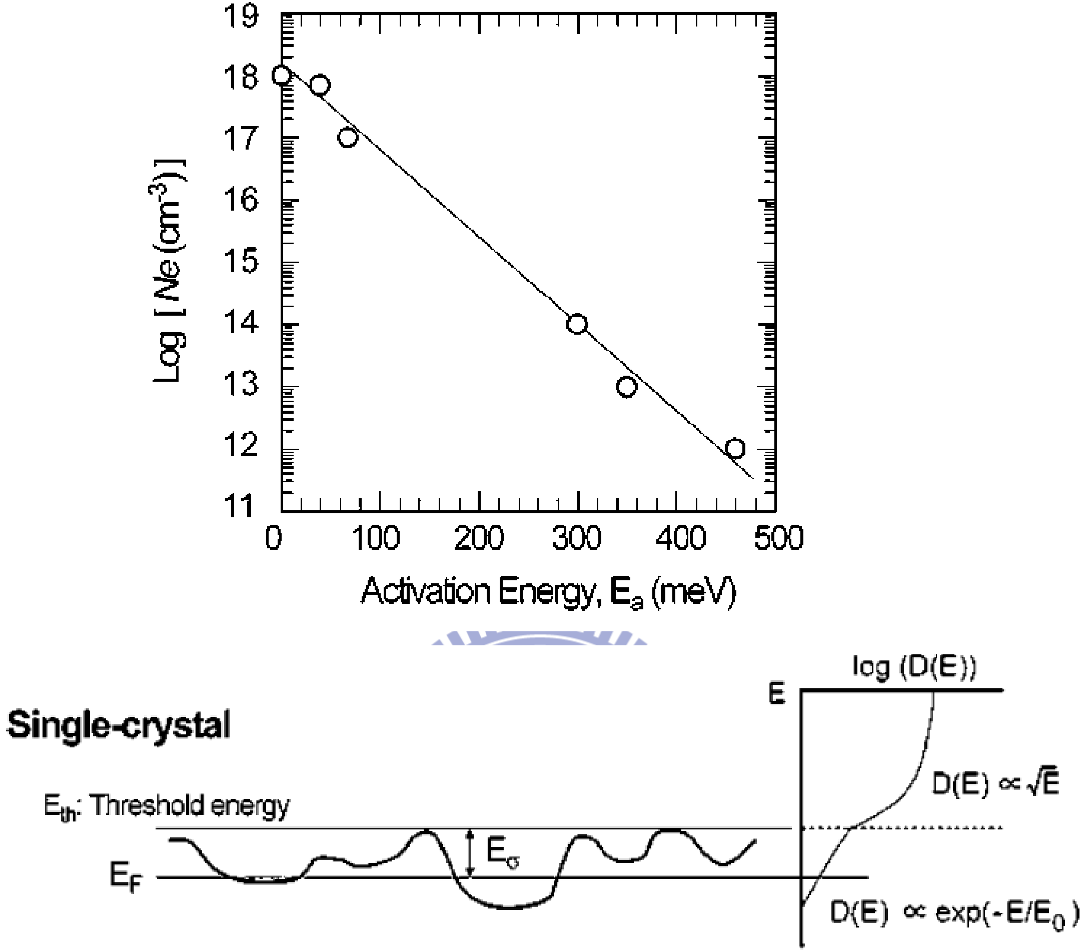


Fig. 1.5 (a) The relationship between log(Ne) and activation energy (Ea). The straight line is the result fitted to the exponential tail density of state model. (b) Schematic energy diagram near the conduction band edge and the density of state for sc-IGZO [23].

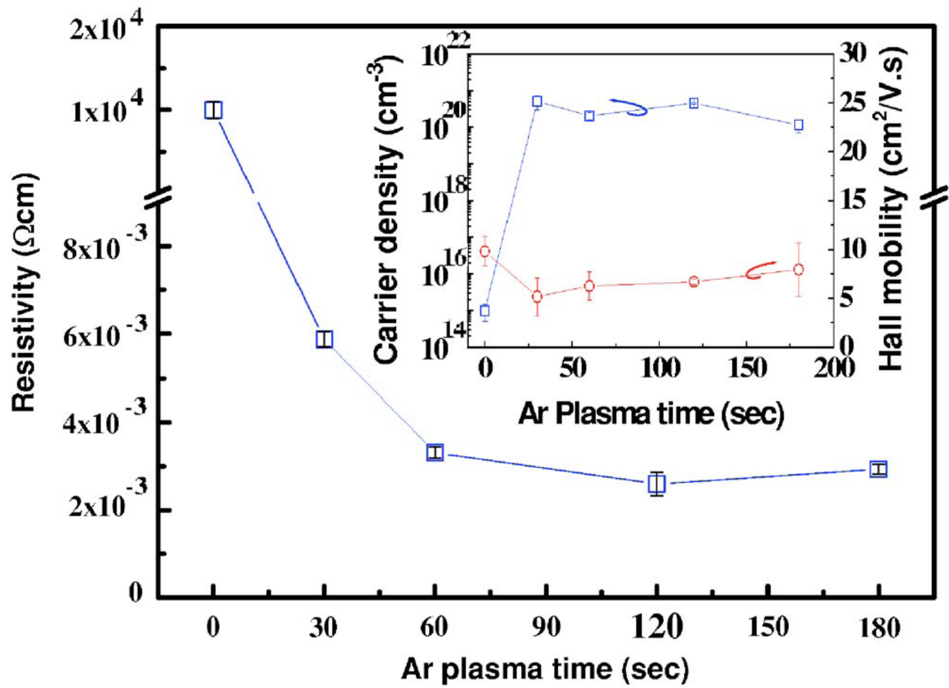


Fig. 1.6 (Color online) Resistivity of *a*-IGZO thin films as a function of an Ar plasma exposure time. The net electron carrier concentration and the Hall mobility of *a*-IGZO thin films were shown in the inset [33].

Chapter 2

Experimental Procedure

2-1 Device structure and fabrication

The process flow of DG a-IGZO TFT with or without nano-dot structure is shown in Fig. 2.1. and Fig 2.2 . The p-type heavy doped Si wafer was prepared as the bottom gate and the 100-nm-thick SiN_x as the bottom gate insulator. A 50-nm-thick IGZO was deposited on SiN_x by RF sputter. Then the substrate was annealed at 400°C for 1 hour in N_2 environment. A 2000 Å cross-linkable poly(4-vinyl phenol) (PVP) was spin-coated on the a-IGZO surface as the top gate insulator. Nanometer dot-like structure was fabricated by using positively charged polystyrene (PS) spheres (Merck, K6–020) as the shadow mask. A 1000 Å Al was then evaporated as top metal gate electrode. After removing the PS spheres using an adhesive tape (Scotch, 3M), the PVP at sites without Al coverage was removed by 50w O_2 plasma treatment for 13 min. Then, 50w Ar plasma was applied onto the bare IGZO channel region for 1 min. Aside of the gate region, high-conductivity IGZO areas serve as the self-aligned source and drain electrodes. Figure 2.3 (a) shows a schematic cross-section of the top-contact Dual-gate a-IGZO TFT without NDD structure (b) top-contact Dual-gate a-IGZO TFT with NDD structure .

2-1.1 Silicon nitride (SiNx) deposition

The dielectric silicon nitride (SiNx) was formed on all samples with 1000 Å using Horizontal Furnace. 1000 Å silicon nitride (SiN_x) developed dielectric layer to fabricate a-IGZO TFT devices. Its backside silicon nitride on the silicon wafer, was etched by reactive ion etching (RIE).To remove SiN_x layer on the back electrode of substrate, gases including Oxygen (O2) 5sccm and Tetrafluoromethane (CF4) 80sccm were induced. The process pressure and RF power were controlled about 15.0 Pa and 100W respectively.

2-1.2 Substrate clean

Before deposition the active layer, the standard clean was carried out to remove the contamination on the dielectric surface. The standard clean is accomplished in two steps, SC1 and SC2. SC1 clean is the first step to remove the particle on the surface. The process was executed with a mixture of ammonium hydroxide, an oxidant hydrogen peroxide, and water in a mixing ratio of 1:4:20.

$$NH_4OH:H_2O_2:H_2O = 1:4:20 \text{ (SC1)}$$

The SC2 clean was used to remove metals from the surface. The cleaning process in SC2 contain three solution of HCl, hydrogen peroxide, and water. The mixture ratio in the SC2 process was 1:1:6.

$$HCl:H_2O_2:H_2O = 1:1:6 \text{ (SC2)}$$

By these two steps , Particle and organic pollution were cleaned and removed on dielectric surface. The roughness of substrate is important for metal deposition and metal adhesion.

2-1.3 a-IGZO film deposition

Recently , there are many researchs reported by using pulsed laser deposition (PLD) and ratio frequency (RF) magnetron sputter to deposit a-IGZO film as active layer . In this study, the RF-sputter with 3-in. circular target: In_2O_3:Ga_2O_3:ZnO = 1:1:1 at.% was used to deposit the a-IGZO film. 50nm a-IGZO channel layer was deposited at room temperature with a power of 100W, a working pressure of 9mTorr, and an Ar/O_2 flow rate of 30/0. The active layer patterning was defined using a shadow mask.

RF sputtering (Fig. 2.4) is a process using radio frequency power supply, operating at 13.56MHz, to generate plasma in which atoms, ions, and clusters are created to sputter the target material. The glow-discharge between a target and a substrate, it's consists of plasma with an equal number of working gas (Ar) and electrons. The ions are accelerated towards to the target by a strong electric field on the target due to the flux of electrons. Consequently, the ions hit the target to eject the target atoms, which are then re-deposited onto the substrate. RF sputtering is performed at low pressure, to increase the mean free path, the distance between

collisions, and to improve the quality of the deposited film.

2-1.4 Post-annealing

After deposition of a-IGZO film as active layer , post-annealing was carried out in the furnace. The annealing process at 400℃ with N_2 flow ratio 10L/min was about one hours after the furnace temperature stabilizing .

2-1.5 Poly (4-vinyl phenol) (PVP) spin coating

In this thesis, PVP is utilized not only as a dielectric layer but also Positively charged polystyrene particles (Merck, K6-020) adherent layer .

The PVP molecular weight was about 20000 from Aldrich. PVP have OH function groups on its molecule structure, poly(melamine-co-formaldehyde) (PMF) was used to be cross-linking agent for PVP, and propylene glycol monomethyl ether acetate (PGMEA) as the solvent. Their chemical structures of PVP and PMF are schematically shown in Fig. 2.5. First, we dissolved PVP and PMF in the PGMEA solvent with a magnetic stirrer for overnight. A 420 nm cross-linkable poly(4-vinyl phenol) (PVP) was 8wt% in the solution, and fixed PVP and PMF weight ratio was 11:4. We then filtered mixed solution through a syringe filter with 0.2μm PTFE membrane and spun coating on the substrate at 6000 rpm for 40sec. To avoid unnecessary leakage current through the PVP, we removed additional solution on the

substrate by the cotton swabs with PGMEA. Put the substrates on the hot plate and cured at 200℃ for 1 hour in the ambient air. The cross-link reaction was more completed at high temperature and for a long time, let OH functional groups on the PVP can be cross-linked by PMF as more as possible.

2-1.6 Nano-dot pattern structure

The surface of PVP was made hydrophilic by exposure to UV-Ozone for 1 min before submerging the substrate into positively charged polystyrene (PS) spheres (Merck, K6–020) diluted in an ethanol solution . The diameter of polystyrene spheres was 200 nm . Particles concentration was diluted with ethanol to 1.2 wt%. Submersion time was 3 minutes to allow the adsorption to reach saturation. Excess particles were rinsed off in a beaker with ethanol and then transferred to a beaker with boiling Isopropanol (IPA) solution for ten seconds. The key procedure in this fabrication is that the substrate is then transferred to a beaker with boiling Isopropanol solution for ten seconds. The substrate is finally blown dry immediately in an unidirectional nitrogen flow. The benefit of this method is the possibility to process large areas in a short processing time without photolithography.

Under high vacuum (5×10^{-6}torr) deposit 100nm Aluminum (99.999%) thin film as gate electrode and defined by shadow mask. After removing the polystyrene spheres

by using an adhesive tape (Scotch, 3M), the nano-dot structure was almost completed.

After removing the polystyrene spheres by using an adhesive tape (Scotch, 3M), the PVP at sites without Al coverage was etched by 50 W O_2 plasma for 13 min. Then, the source/drain region and the bare channel region (without PVP coverage) was treated with Ar plasma to increase the conductivity. After Ar treatment for 1 min. , a self-aligned structure was formed. The channel width and length of the top gate devices are 1000 μm and 300 μm, respectively. For DG-STD, the process flow is similar to that depicted in Fig. 2.2 except that the PS sphere absorption process is removed.

2-1.7 Source and drain electrodes deposition

We deposited 100-nm-Al (99.999%) through shadow mask as source and drain electrodes of dual-gate TFTs. The deposition was started at 5×10-6torr and rate was controlled at 2Å /s. The device channel width and length was 1000μm and 300μm.

2-2 Analysis instruments

2-2.1 Current-Voltage measurement instrument

All devices were measured by semiconductor parameter analyzer (Agilent E5270B) at room temperature in ambient air.

2-2.2 Four-point probe resistivity measurement

The four-pint probe configuration is usually used to measure the sheet resistance of semiconductor. Four identical probes are placed in a linear configuration, equally spaced, along the sample. Current is forced through the outer probes, while the voltage is measured across the inner probes. The voltage is measured using a high impedance meter, which minimizes the current flow, thereby minimizing the contact resistance to a negligible value.

2-2.3 Spin coater

Spin coating process is used to dissolvent materials. The top gate dielectric layer can be fabricated by spin coating. The initial spin speed determined the thickness of thin film, and the final spin speed determined the uniformity of the film. After spinning for 6000 rpm 40sec. , the baking process is proceeded to evaporate the solvent of the solution to form the passivation layer.

2.2.4 X-ray photoelectron spectroscopy (XPS) analysis

X-ray photoelectron spectroscopy (XPS) is used to measure the elemental composition, empirical formula, chemical state and electronic state of the elements

that exist within a material. XPS spectra are obtained by irradiating a material with a beam of X-rays while simultaneously measuring the kinetic energyand number of electrons that escape from the top 1 to 10 nm of the material being analyzed in ultra high vacuum (UHV) conditions. XPS is a surface chemical analysis technique that can be used to analyze the surface chemistry of a material in its "as received" state, or after some treatment, for example: fracturing, cutting or scraping in air or UHV to expose the bulk chemistry, ion beam etching to clean off some of the surface contamination, exposure to heat to study the changes due to heating, exposure to reactive gases or solutions, exposure to ion beam implant, exposure to ultraviolet light. Fig. 2.6 is schematic diagram of XPS.

2-2.5 Scanning electron microscopy (SEM)

The principle of SEM imaging is due to using the electron beam emitted by heating tungsten wire. Then, the electron beam focused together to form a small electron beam by the anode of the accelerating voltage after two to three electromagnetic lens composed of electro-optical system. Finally, the beam focused on the specimen for two-dimensional scanning. When the electron beam scans the specimen, high-energy electron beam interact with matter. Electronic elastic collision and inelastic collision effects result a secondary electron and backscatter electron etc. Signal amplified after the specimen's surface

morphology, will be able to simultaneously screen imaging. Fig. 2.7 is schematic diagram of SEM.

2-3 Methods of device parameters extraction

In this section, the extractions of the device parameters are discussed in details. Turn on voltage (V_{on}), threshold voltage(V_{th}),the field effect mobility, the sub-threshold swing (S.S), and the on/off current ratio (I_{on}/I_{off}) are extracted and assessed, respectively.

2-3.1 Turn-on voltage (V_{on})

Von can directly characterizes the gate voltage required to fully "turn on" the transistor in a switching application. Turn-on voltage (V_{on}) is identified as the gate voltage at which the drain current begins to increase in a transfer curve.

2-3.2 Threshold voltage (V_{th})

Threshold voltage is related to the operation voltage and power consumptions of TFTs. We extract the threshold voltage from equation (2.1), the intercept point of the square-root of drain current versus voltage when devices operate in saturation mode

$$\sqrt{I_D} = \sqrt{\frac{W}{2L}\mu C_{OX}}(V_G - V_{TH}) \tag{2.1}$$

2-3.3 Mobility

Mobility is a parameter of how fast carriers can move in material. A higher magnitude of mobility allows for a faster switching time, i.e., the time it takes for the device switching from the off state to on state. In the off state, few current flows through the device. In the on state, large amount of currents flow through the device. A large mobility means the device can conduct more current. The mobility in this study was extracted from the saturation region. The device was operated at drain-voltage of 20V, since the threshold voltage was much lower than 20V. The saturation mobility is determined from the transconductance, define by

$$g_m = \left[\frac{\partial\sqrt{I_D}}{\partial V_G}\right]_{V_D=const} \tag{2.2}$$

The drift component of drain current is

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{2.3}$$

When the mobility is determined, the transconductance is usually taken to be

$$g_m = \sqrt{\frac{W\mu C_{ox}}{2L}} \tag{2.4}$$

When this expression is solved for the mobility, it is known as the saturation mobility

$$\mu_{sat} = \left[\frac{2{g_m}^2}{\frac{W}{L}C_{ox}}\right]_{saturation} \tag{2.5}$$

2-3.4 I_{on}/I_{off} current ratio

The I_{on}/I_{off} (on/off) ratio represents large turn-on current and small off current. It is an indicator of how well a device will work as a switch. A large on/off current ration means there are enough turn-on current to drive the pixel and low off current to maintain in low consumption.

2-3.5 Sub-threshold swing (S.S)

It is a measurement of how rapidly the device switches from off state to on state. Moreover, the sub-threshold swing also represents the interface quality and the defect density.

$$S = \left[\frac{\partial V_G}{\partial(\log I_D)}\right]_{V_D=const} \tag{2.6}$$

If we want to have a better performance TFTs, we need to lower the sub-threshold swing.

Figure in Chapter 2

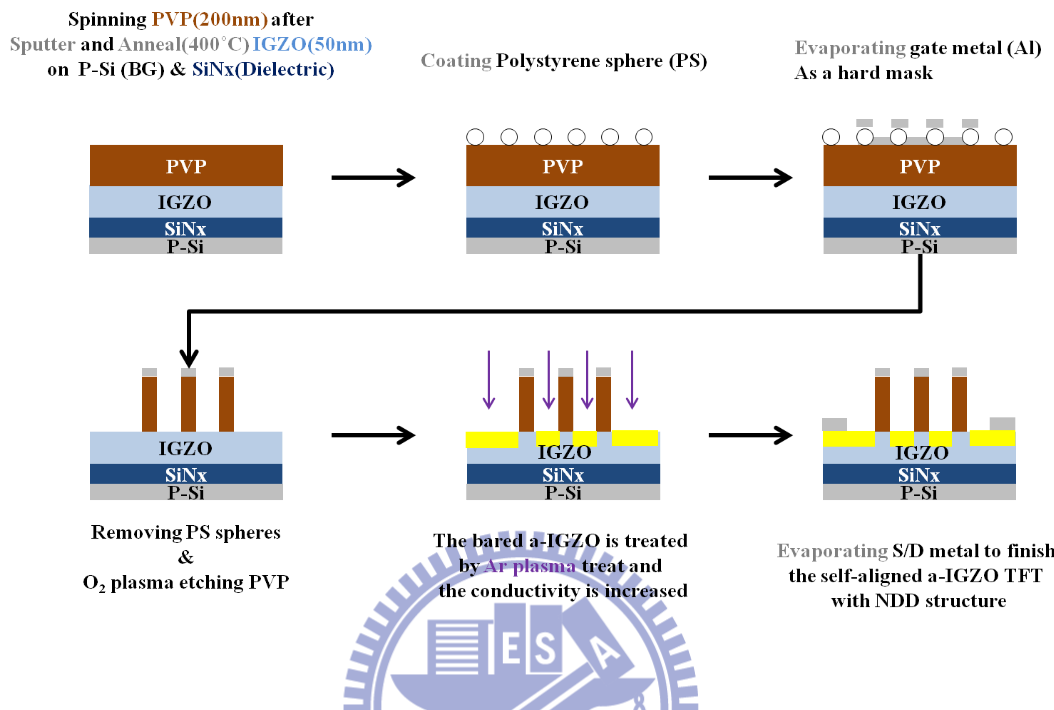


Fig. 2.1 The process flow of the DG- (Dual-gate with nano-dot structure by Ar plasma treatment) a-IGZO TFT.

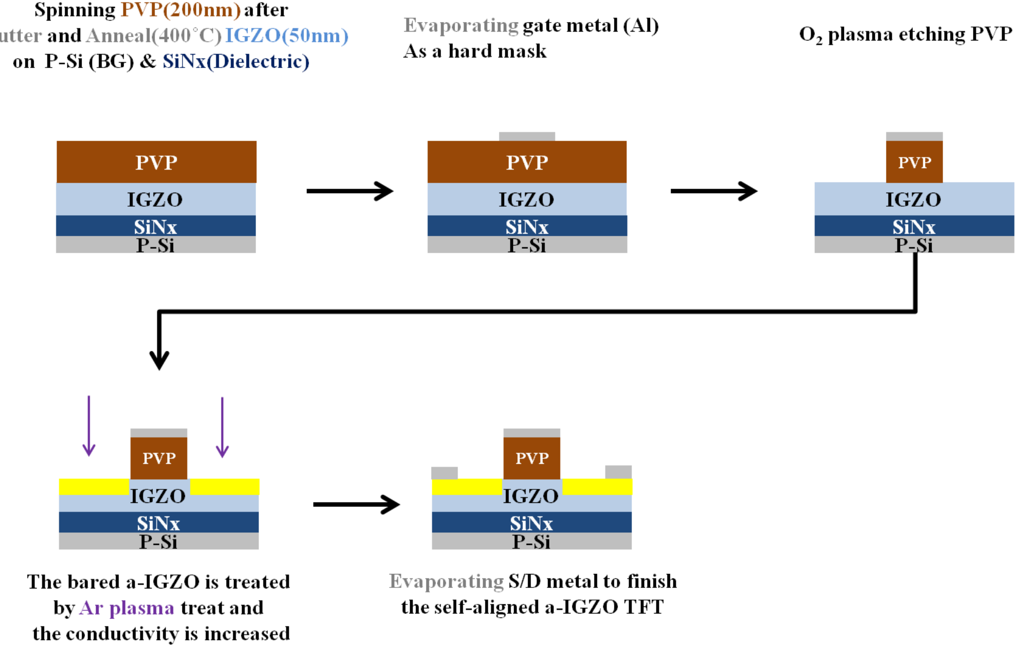


Fig. 2.2 The process flow of the standard DG- (Dual-gate without nano-dot structure by Ar plasma treatment) a-IGZO TFT.

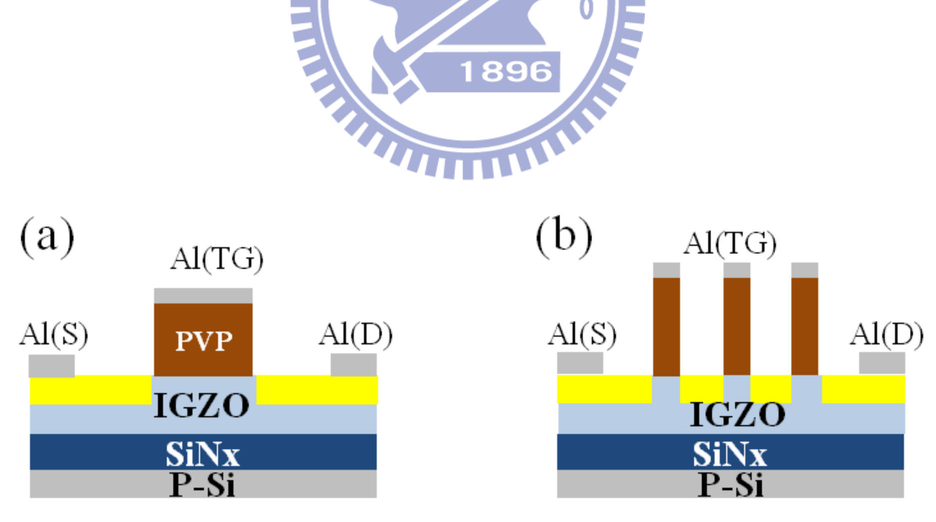


Fig. 2.3 Schematic device structures. (a) and (b)is dual-gate (DG) of a-IGZO TFTs without and with NDD by Ar plasma treatment.

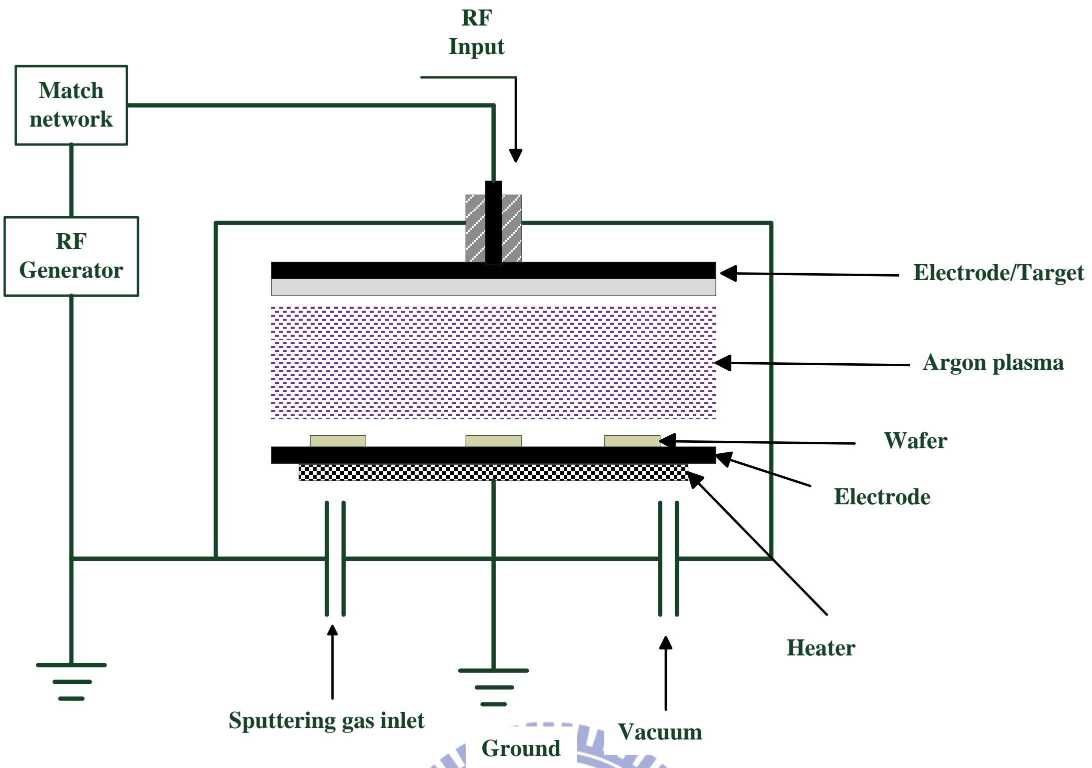


Fig. 2.4 RF-power sputtering deposition system.

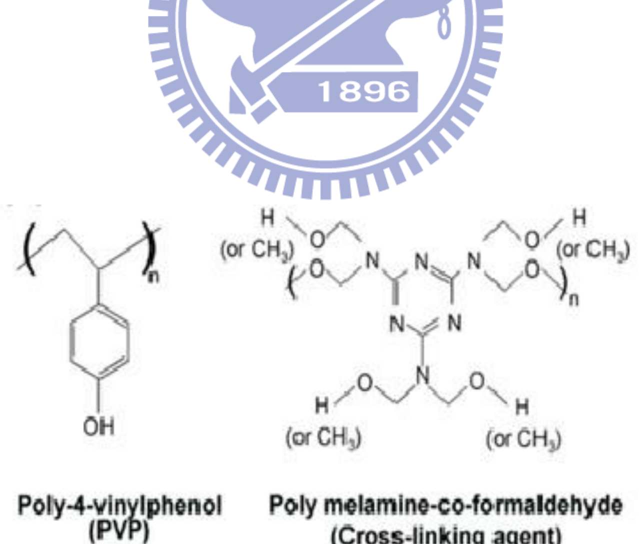


Fig. 2.5 The molecular structure of PVP and PMF

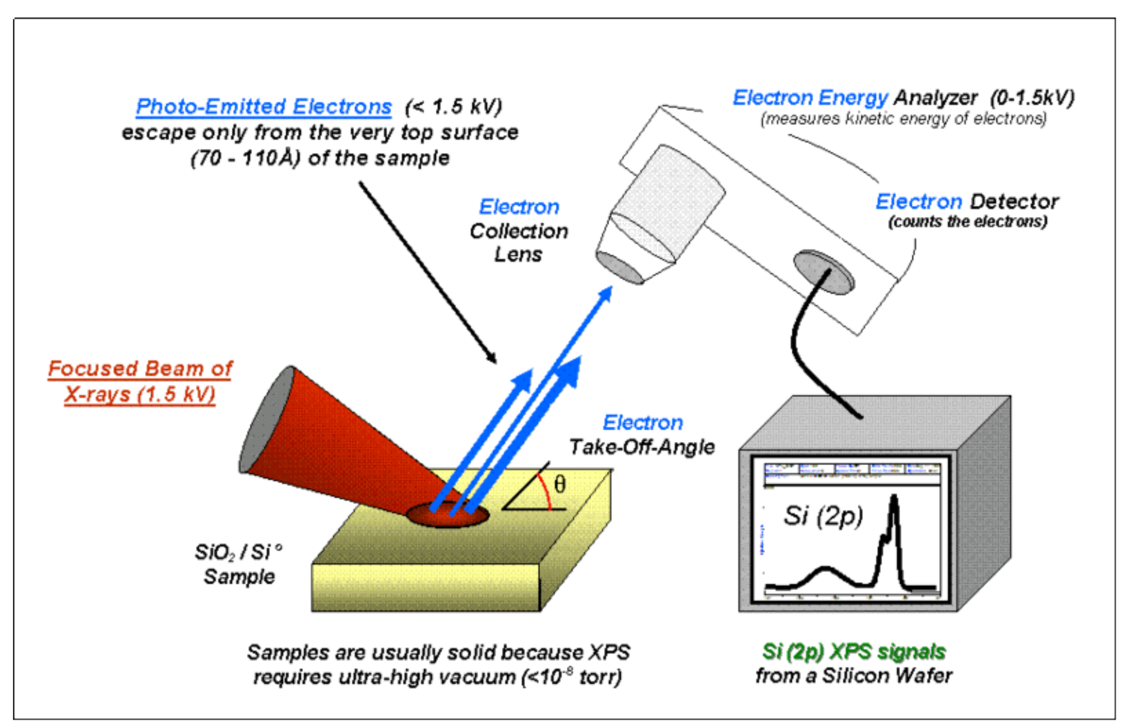


Fig. 2.6 Schematic diagram of XPS system.

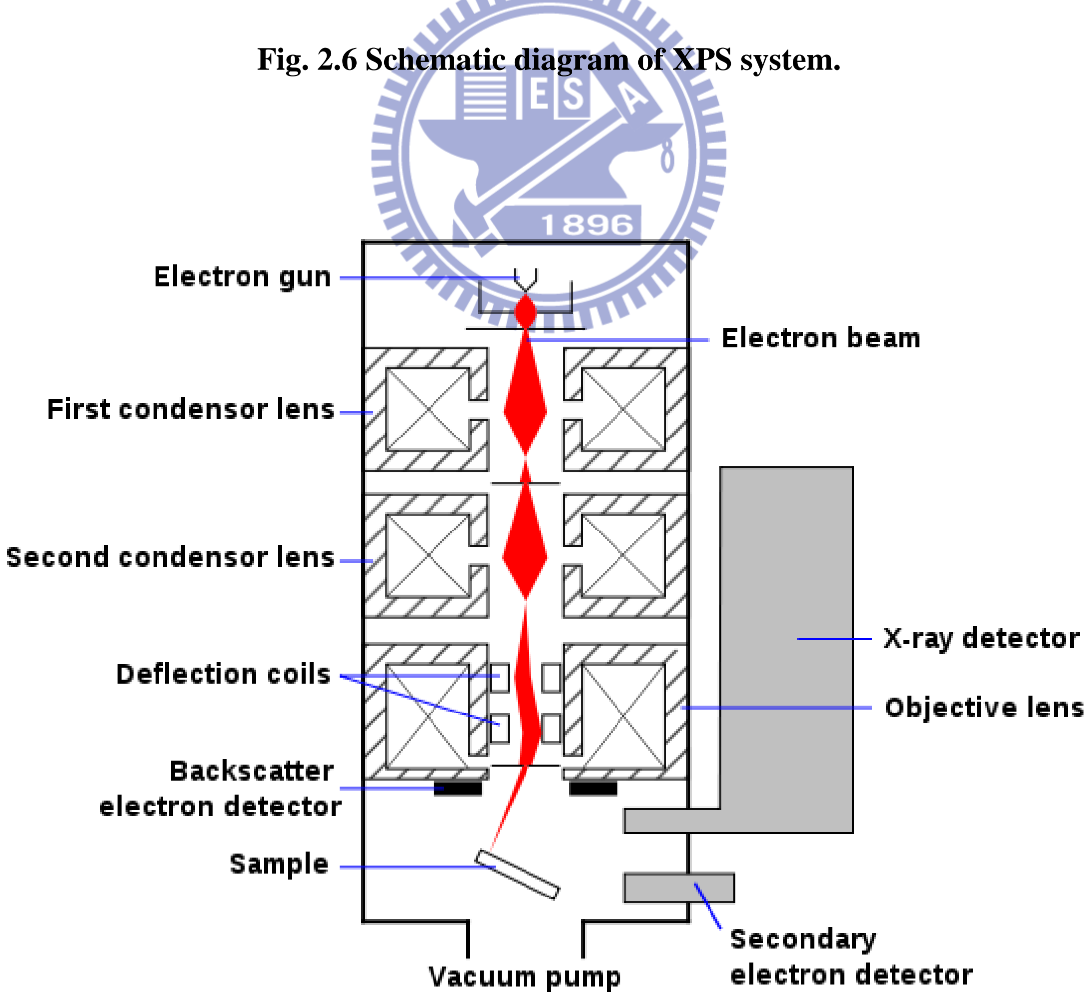


Fig. 2.7 Schematic diagram of SEM system.

Chapter 3

Results and Discussions

With a high mobility (>10 cm^2/Vs) and a low threshold voltage (< 5 V) under low temperature process, amorphous In-Ga-Zn-O thin-film transistors (a-IGZO TFTs) draw a lot of attentions. However, when a-IGZO TFTs are developed for a low-power high-frequency circuit, improved electron mobility and a low parasitic capacitance are required. In this section, we measure the capacitance of PVP and SiN_x as top gate insulator and bottom gate insulator, discuss the influence of a-IGZO film under Ar plasma treatment and the influence of drain current enhancement in dual gate measurement . In this study, we used a novel, simple process to improve the mobility of the a-IGZO TFTs to obtain a high carrier mobility of a-IGZO TFTs, and proposed a efficient manufacturing method, called "nano-dot doping". And Fig. 3.1 is Schematic device structures. (a) is standard(STD) dual gate a-IGZO TFT and (b) is dual gate (DG) of a-IGZO TFTs with NDD by Ar plasma treatment.

3.1 The capacitances of top gate insulator and bottom gate insulator

The gate insulator capacitance per unit area is an important factor of device parameters extraction. It can use C-V measurement to find out the capacitance of dielectric layer. We spin coating PVP on ITO substrate, and then evaporate Al through shadow mask as metal pad. The top insulator capacitance per unit area is 16.1 (nF/cm^2) by measuring this Metal-Insulator-Metal structure. On the other hand, The bottom insulator capacitance per unit area is 53.1 (nF/cm^2) . Fig 3.2 is Schematic metal-insulator-metal (M-I-M) device structures of (a) bottom gate insulator, (b) top gate insulator.

3.2 The resistivity of a-IGZO Thin Film as a function of Ar Plasma treatment time

We can use four-point probe to measure sheet resistance . Fig. 3.3 shows the sheet resistance of the *a*-IGZO thin film as a function of the Ar plasma treatment time. As-deposited *a*-IGZO thin film usually had a high resistivity ($>10^5$ Ω*cm) upon its treat to the Ar plasma 60s, the resistivity of the *a*-IGZO film dramatically decreased by approximately several orders of magnitude from 10^5 Ω*cm to 0.04 Ω*cm. The resistivity became saturated over that. Moreover, the saturation of resistivity was

observed above the treatment time of 60 s can be tentatively speculated as follows: As a consequence of preferential sputtering of oxygen, the enrichment of cations including In, Ga, and Zn on the surface would balances out the preferential sputtering of oxygen, which makes the steady-state condition (i.e., saturation behavior) achieved.[34]

3.3 Previous researches of a-IGZO top gate thin film transistor with Nano-dots structure

In this section, we briefly introduced previous researches of top gate thin film transistor with nano-dots doping structure. Discuss in two parts: The influence of Ar plasma treatment time on Top-Gate TFT and the influence of dot concentration on Top-Gate a-IGZO TFT.

Fig. 3.4 the transfer characteristics of different Ar plasma treatment time on TG-NDD 0.8 wt% TFTs. For 1 min. Ar treatment, the source/drain resistance was too high that devices can't turn on totally. And then, increasing Ar plasma treatment time to 3 min., the mobility is 79 cm^2/V-sec, and the S.S. is 1.2 V/dec. and the threshold voltage is 0.75V. As treatment time increasing to 5 min., the leakage current was raised.

Fig. 3.5 The transfer characteristics of different dots concentration on TG-STD,

TG-NDD (PS 0.2 wt %), and TG-NDD (PS 0.8 wt %). It was obviously increased the field-effect mobility when the dots concentration increased. Table I.

Based on above two researches and different RIE system, we chose new produce condition, Ar treatment time was 1 min. and PS sphere concentration was 1.2wt%. Fig.3.6 showed the SEM images of cross sectional view of the a-IGZO TFTs and top view of 1.2wt% dots-like structure on the substrate.

3.4 The effect of nano-dots dopping by the Ar plasma treatment on the Dual-Gate a-IGZO TFT

The transfer characteristics of NDD a-IGZO TFT are shown in Fig. 3.5, TG represents that the gate bias is applied only on top gate electrode while the bottom gate is floated. BG represents bottom gate measurement with a floated top gate. DG represents that the gate bias is applied onto top gate and bottom gate simultaneously. All electron characteristics of devices were measured by Agilent E5270B parameter analyzer in the dark. In this dual-gate device, the Ar plasma treatment produces the source and drain regions with high electron concentration. The channel length defined by without the Ar treatment region is 300 μm. The capacitances of top insulator and bottom insulator are 16.1 and 53.1 (nF/cm^2), respectively. For simplicity, we demonstrate the effective mobilities calculated by using top insulator capacitance as

μ_{eff}(TI) and using bottom insulator capacitance as μ_{eff}(BI) . Typical parameters such as threshold voltage (V_{TH}), effective mobility (μ_{eff}), subthreshold swing (S.S.), and on/off current ratio of TG, BG, and DG a-IGZO TFTs are listed in Table II.

In order to compare the influence of nano-dots structures, we fabricate the Dual gate a-IGZO TFT without nano-dot structure as standard devices. Fig. 3.1(a) is Schematic device structure. The transfer characteristics of STD a-IGZO TFT are shown in Fig. 3.8. The channel length defined by without the Ar treatment region is 300 μm. All typical parameters are listed in Table III.

To investigate the current of the three operation modes (TG, BG, and DG), we extract the current amount at a fixed bias condition (V_{DS}=20 V, V_{GS}-V_{TH}=10 V) in Fig. 3.9. The current comparison at low lateral field (bias condition: V_{DS}= 0.1 V, V_{GS}-V_{TH}=10 V) is shown in the inset of Fig. 3.9. For STD device, DG operation is almost the same as BG operation. TG operation gives smaller current due to the smaller capacitance in top gate insulator. Specifically, the capacitances of top insulator and bottom insulator are 16.1 and 53.1 nF/cm^2 respectively. For NDD device, TG operation and BG operation deliver similar output current, indicating that the effective mobility in TG operation is higher. The DG operation with high lateral field (V_{DS}=20 V, V_{GS}-V_{TH}=10 V) delivers a 4-times larger current than BG or TG operation. The result reveals that DG operation not only open both top and bottom

channels, but also produce higher effective mobility. If the lateral field is small, as shown by the inset of Fig. 3.9, DG-mode current almost equals to the summary of TG-mode current and BG-mode current. No mobility enhancement can be observed.

3.5 Barrier Lowering and electric field

We separate two parts to discuss the enhanced effective mobility in NDD devices with Ar treatment and the mechanism of additional drain current enhancement of dual gate measurement.

Firstly, there are some reasons to explain the enhanced effective mobility in NDD devices. The effective channel length is reduced due to the conductive dots regions in the channel. In previous researches, we estimate the intrinsic channel length as the effective channel length. The effective channel length of 0.2wt% and 0.8 wt% PS sphere density is reduced from 1000μm to 684μm and 500μm, Fig 3.11.When we use new effective channel length to modify the mobility extraction, the mobility of top gate measurement are 32.5 cm^2/Vs and 39.6 cm^2/Vs respectively, which is 8-10 times bigger than the STD top gate devices. It is not sufficient to explain the enhanced mobility in TG-NDD devices.

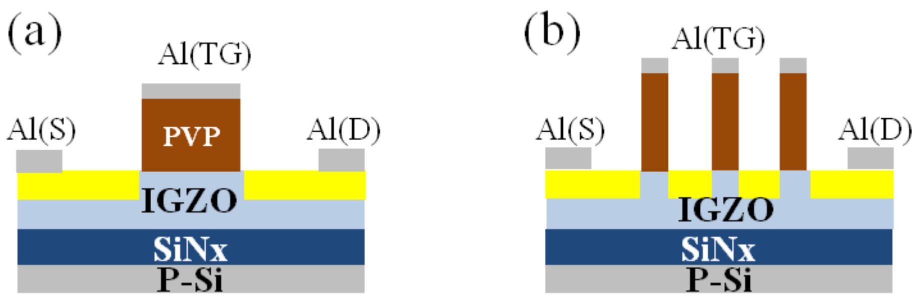
As we know, the electron transport in a-IGZO is governed by the percolation transport. The reduction electron mobility is formed by potential barriers which is caused by the random distribution of Ga^{3+} and Zn^{2+} ions in the network structure.

When high density conductive dots-like regions in device transport channel, the potential barrier is lower. As a result, the electron mobility of top gate measurement is larger than bottom gate measurement.

The barrier lowering effect is observed in many semiconductor devices. The Schottky barrier at the metal-organic interface shows a Schottky-barrier lowering effect when increasing the doping level of organic semiconductor. [35]. For short-channel MOSFETs, the built-in potential barrier between the heavily-doped source and the bulk suffers from the drain-induced-barrier-lowering effect [36-38]. For poly-Si TFTs, the grain boundary barrier is also lowered by the drain-to-source electric field [39].

Secondly, the barrier lowering effect is presumed to be strongly dependent on lateral electric field. the reduced vertical field in DG mode may enhance the barrier lowering effect and increase the mobility. As a result, When drain bias (V_{DS}) is 0.1V , RI is around 1, representing that the dual gate operation simply turns on top channel and bottom channel simultaneously. When V_{DS} = 20 V, however, RI increases to be 1.5, revealing that increasing lateral electric field the electric mobility and the drain current of dual gate mode are increasing. In contrast with NDD structure, STD device which without nano-dots structure does not show the drain current of dual gate mode is bigger than the sum of the other mode.

Figure in Chapter 3



Dual-Gate devices

Fig. 3.1 Schematic device structures. (a) and (b) is Dual gate (DG) of a-IGZO TFTs without and with NDD.

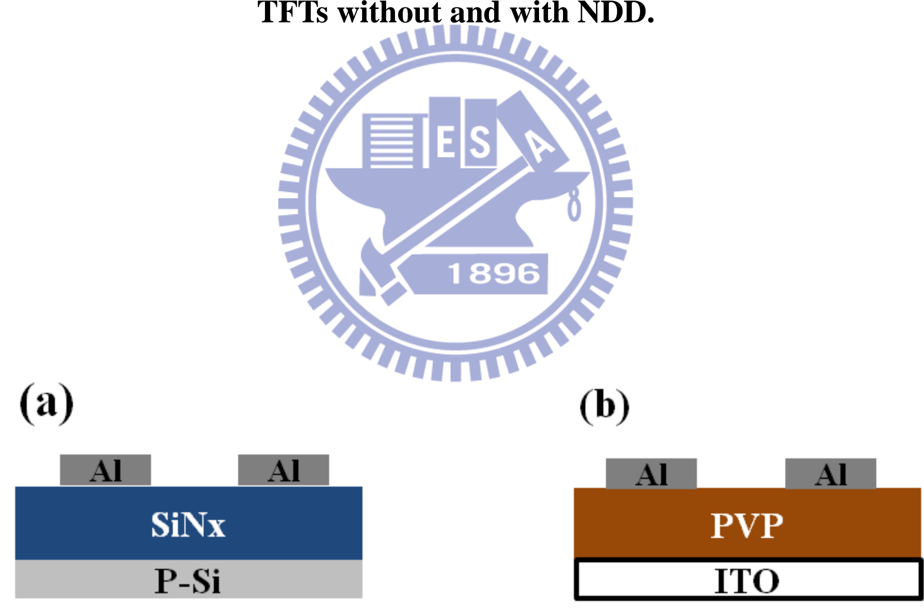


Fig. 3.2 Schematic metal-insulator-metal (M-I-M) device structures of (a) bottom gate insulator, (b) bottom gate insulator.

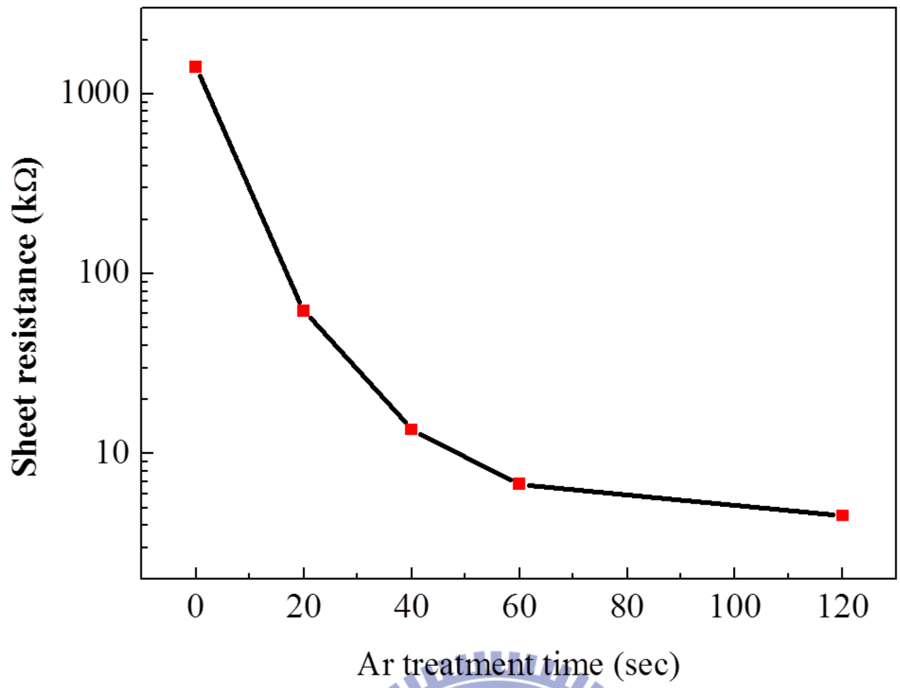
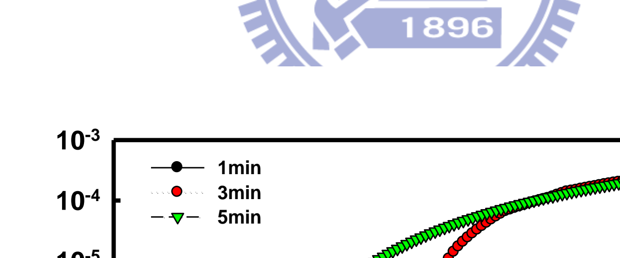


Fig. 3.3 The sheet resistance of a-IGZO thin films as a function of an Ar plasma treatment time.



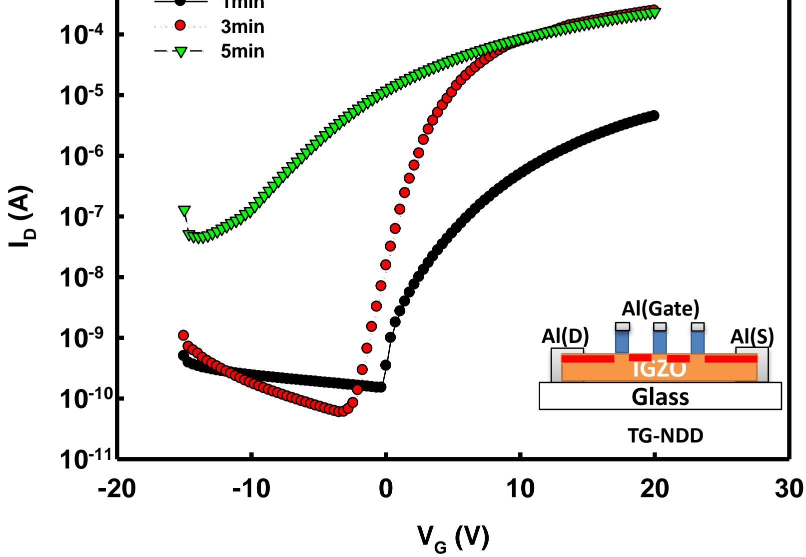


Fig. 3.4 The transfer characteristics of different Ar plasma treatment time on TG-NDD 0.8 wt% TFTs.

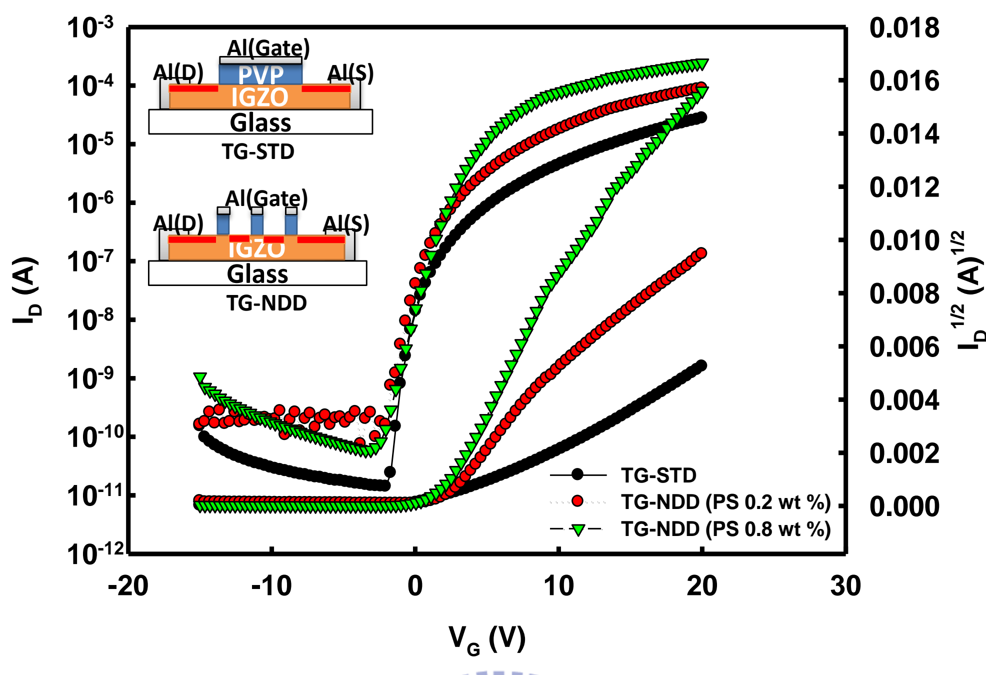


Fig. 3.5 The transfer characteristics of TG-NDD TFTs without and with different dot concentration doping.

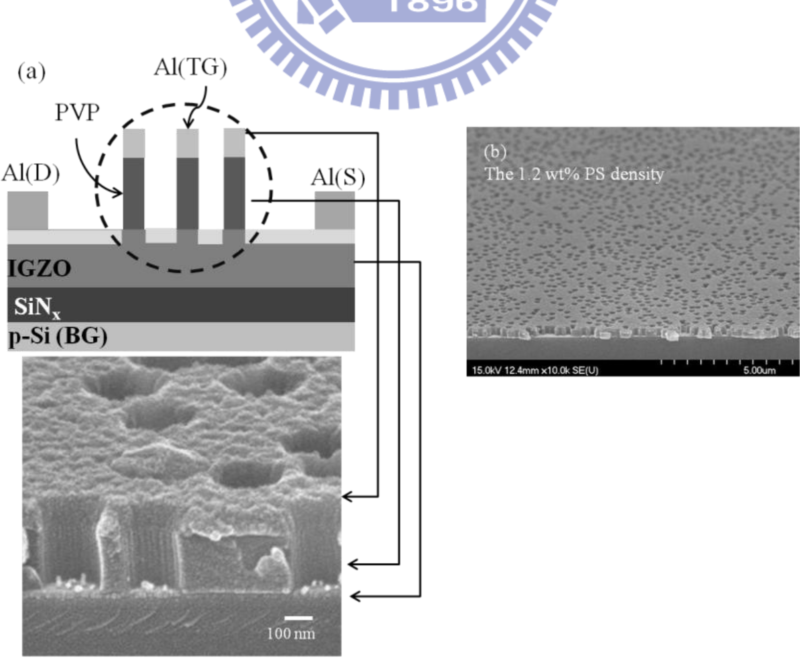


Fig. 3.6 SEM images. (a) Cross sectional view of the a-IGZO TFTs. (b) 1.2 wt% of polystyrene spheres with diameters of 200nm on the substrate.

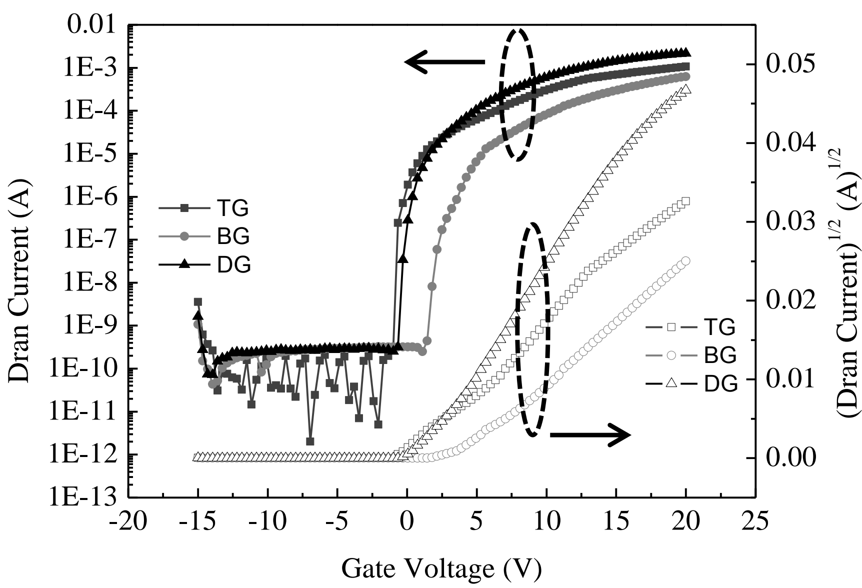


Fig. 3.7 The transfer characteristics of NDD a-IGZO TFT operated in top gate, bottom gate and dual gate modes.

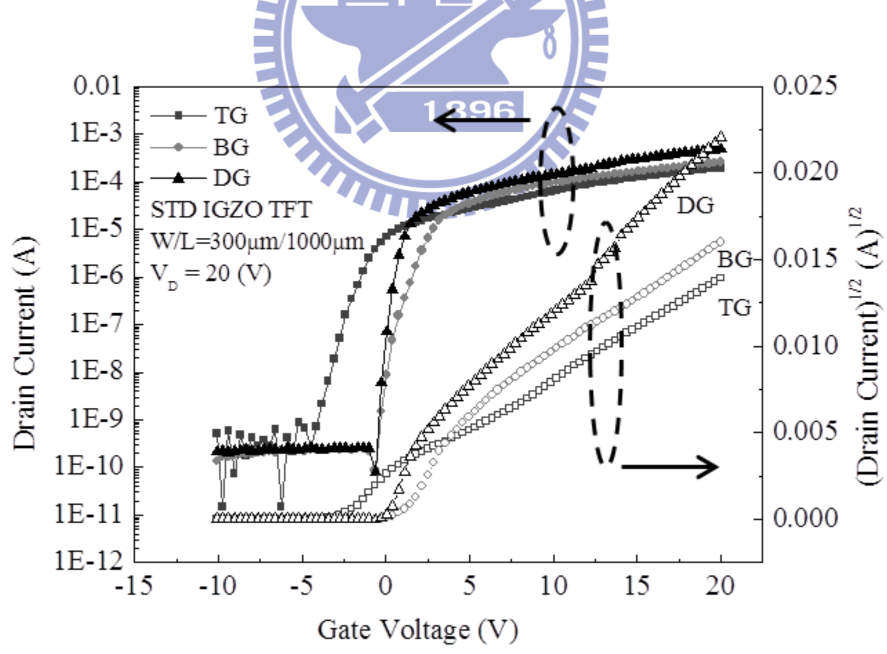


Fig. 3.8 The transfer characteristics of STD a-IGZO TFT operated in top gate, bottom gate and dual gate modes.

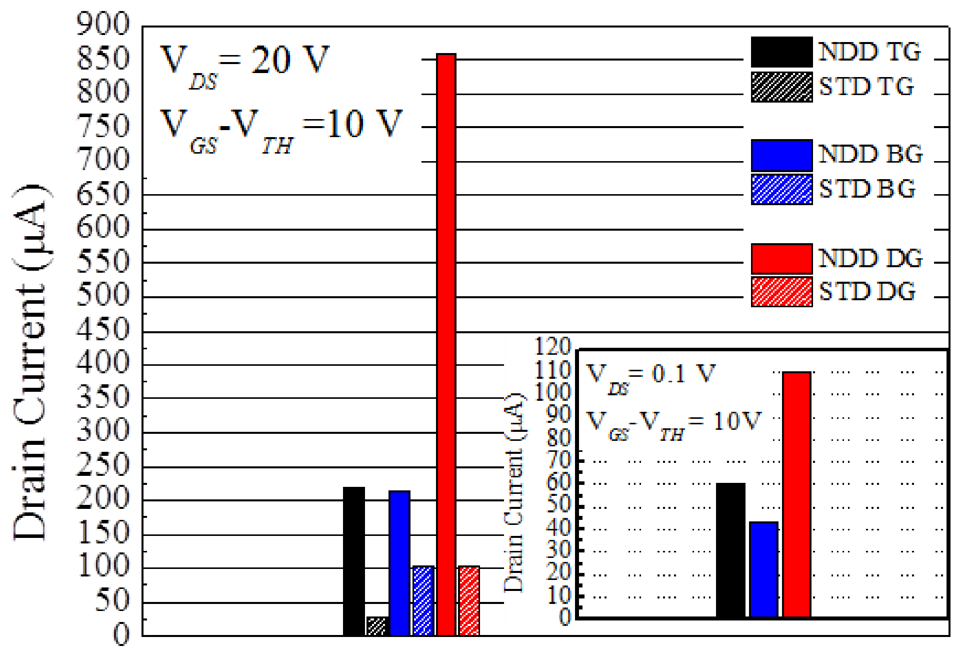


Fig. 3.9 The current amount bars under TG, BG and DG operation modes at the fixed bias V_{DS} = 20 V and V_{DS} -V_{TH}= 10 V, and V_{DS} = 0.1 V as shown in inset chart.

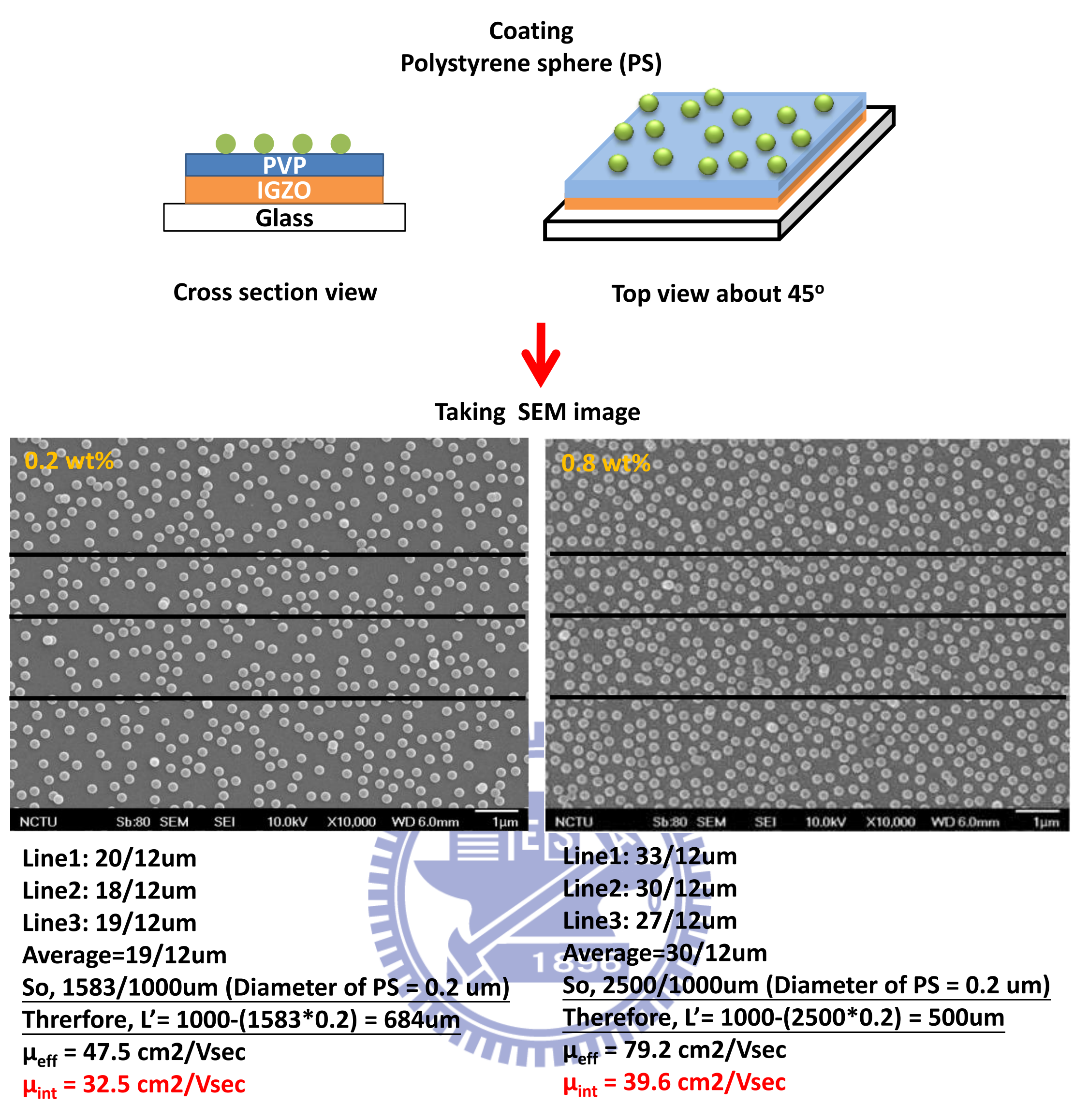


Fig. 3.10 The new method of mobility calculation process and schematic diagram

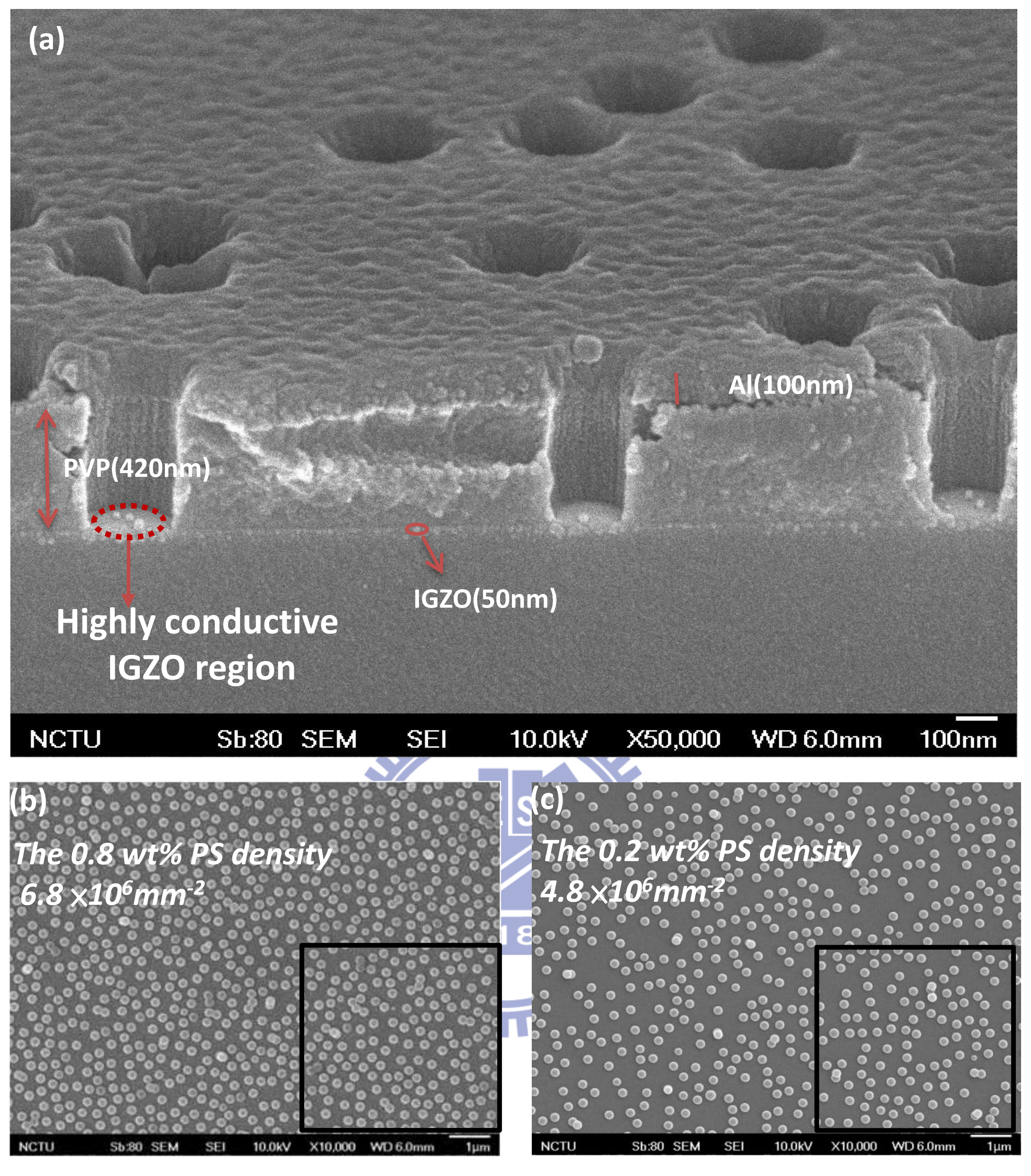
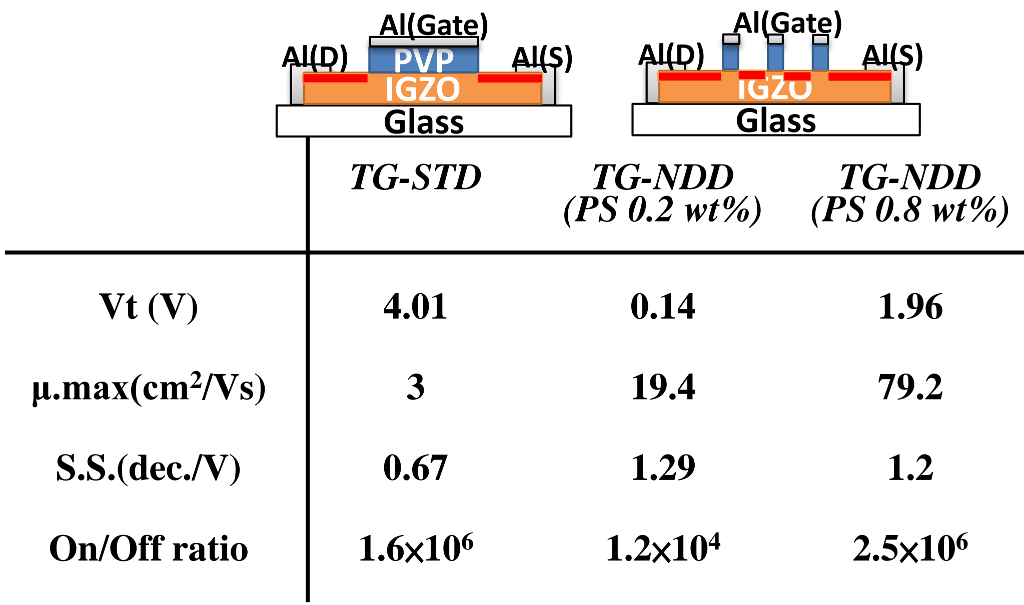


Fig. 3.11 SEM images. (a) Cross sectional view of the a-IGZO TFTs. (b) 0.8 wt% and (c) 0.2 wt% of polystyrene spheres with diameters of 200nm on the substrate. The average of 0.8 wt% and 0.2 wt% PS density calculated in the 5um^2 square are 6.8*10^6 mm^{-2} and 4.8*10^6 mm^{-2}, respectively.



	TG-STD	*TG-NDD (PS 0.2 wt%)*	*TG-NDD (PS 0.8 wt%)*
Vt (V)	**4.01**	**0.14**	**1.96**
μ.max(cm^2/Vs)	**3**	**19.4**	**79.2**
S.S.(dec./V)	**0.67**	**1.29**	**1.2**
On/Off ratio	**1.6×10^6**	**1.2×10^4**	**2.5×10^6**

Table 1. Typical parameters of TG-NDD TFTs with and without nano-dot doping.

	MODE	V_{TH} (V)	μ_{eff}(TI) (cm^2/Vs)	μ_{eff}(BI) (cm^2/Vs)	S.S. (V/dec.)	I_{on}/I_{off}
NDD	TOP GATE	-0.52	102.23	N/A	0.23	5.4×10^6
	BOTTOM GATE	3.25	N/A	24.84	0.33	1.4×10^6
	DUAL GATE	1.10	272.29	90.76	0.34	8.7×10^6

TABLE II. Typical parameters of TG, BG, and DG a-IGZO TFTs with NDD structure.

	MODE	V_{TH} (V)	μ_{eff}(TI) (cm^2/Vs)	μ_{eff}(BI) (cm^2/Vs)	S.S. (V/dec.)	I_{on}/I_{off}
STD	TOP GATE	-4.98	11.58	N/A	0.82	7.5×10^5
	BOTTOM GATE	0.45	N/A	8.57	0.43	3.0×10^6
	DUAL GATE	-2.16	38.25	11.53	0.27	6.0×10^6

TABLE III. Typical parameters of TG, BG, and DG STD a-IGZO TFTs .

Chapter 4

Conclusions and Future Work

4-1 Conclusions

We demonstrate that the NDD a-IGZO TFT exhibits a 1.5 times current increase and a corresponding high effective mobility as 272 $cm^2V^{-1}s^{-1}$ by connecting the top-gate and bottom-gate together to form a dual-gate (DG) NDD a-IGZO TFT. The dual-gate enhancement effect is strongly dependent on drain bias, indicating that the enhancement effect is pronounced when lateral electric field plays an important role. For NDD a-IGZO TFT, it has been proposed that the high effective mobility (100 $cm^2V\text{-}^1s^{-1}$) is due to the suppressed potential barrier in intrinsic a-IGZO. In this work, the DG operation reduces the vertical electric field, enhances the lateral field induced barrier lowering effect and hence enlarges the effective mobility of NDD a-IGZO TFT.

4-2 Future Work

We propose the high mobility, low operating voltage and small sub-threshold swing of dual gate a-IGZO TFTs with nano dot-like doping . But, we still have some problem to solve. The Ar treatment a-IGZO film decline in ambient environment, maybe we could apply passivation layer on the NDD devices to maintain its reliability and stability. The distribution of PS spheres are random, we could replace

nano-imprint technique by present method.

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