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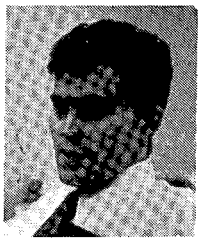

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The New General Realization Theory of FET-Like Integrated Voltage-Controlled Negative Differential Resistance Devices

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***Abstract*—A new general realization theory of FET-like voltage-controlled negative differential resistance device is presented. A feedback-transfer model (FTM) of the FET, which contains four different kinds of feedback connections and their own mathematical conditions, is set up. Based on this model, a general simple realization technique is explored. Using this technique many negative differential resistance FET-like integrated devices either new or published are generated, and their integrated circuit configurations and basic properties are studied and discussed. Application example for a specific device is demonstrated, which substantiates the exactness of the proposed theory.**

List of Symbols

C_0	Gate oxide capacitance per unit area.
G_0	Drain-to-source conductance with zero drain voltage.
G_{OB}	G_0 of the basic EMOSFET in the Lambda MOSFET.
G_{OF}	G_0 of the feedback EMOSFET in the Lambda MOSFET.
G_{OL}	G_0 of the load EMOSFET in the Lambda MOSFET.
I_{DS}	Drain current in the CS-EMOSFET.
$I_{i(o)}$	Input (output) current of the integrated device.
$I_{ib(f)}$	Input current of the basic (feedback) device.
$I_{ob(f)}$	Output current of the basic (feedback) device.
I_p	Peak current.
I_V	Valley current.
K	Modifying substrate factor.
L	Channel length.
N_A	Doping concentration of p-type substrate.
q	Electron charge.
R_I	External input resistance.
R_N	Differential negative resistance.
$V_{DS(GS)}$	Drain (gate)-to-source voltage of the CS-EMOSFET.
V_{FB}	Flat band voltage of MOS capacitor.
V_I	Input fixed voltage bias.
$V_{i(o)}$	Input (output) voltage of the in-

Manuscript received July 24, 1979; revised December 3, 1980. This work was supported by the National Science Council, Republic of China, under Contract NSC-68E-0404(02).

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0098-4094/81/0500-0382$00.75

tegrated device.

$V_{ib(f)}$ Input voltage of the basic (feedback) device.

$V_{ob(f)}$ Output voltage of the basic (feedback) device.

V_p Peak voltage.

V_V Valley voltage.

Z Channel width.

ϕ_{fp} The potential difference between the Fermi potential and the intrinsic potential of p-type substrate at flat band condition.

ϵ_s Dielectric permittivity of silicon substrate.

μ_n surface mobility of electrons.

BJT Bipolar Junction Transistor.

CB Common-Base.

CC Common-Collector.

CD Common-Drain.

CE Common-Emitter.

CG Common-Gate.

CS Common-Source.

n-(p-) DMOSFET n-channel (p-channel) Depletion-mode Metal-Oxide-Semiconductor Field-Effect Transistor.

n-(p-) EMOSFET n-channel (p-channel) Enhancement-mode MOSFET.

n-(p-) JFET n-channel (p-channel) Junction Field-Effect Transistor.

I. Introduction

INTEGRATED voltage-controlled negative differential resistance devices which consist of two feedback-connected basic active devices and at most one passive element, may offer many advantages over the more complicated negative resistance circuits. The integrated devices constructed around a field-effect transistor (FET) are called FET-like devices. So far, many devices of this kind have been explored [1]–[7]. Several attempts [8]–[10] have been made to construct a general realization theory which is far more necessary and useful. Although some of them [8], [9] may generate few devices, they have been unable to characterize the devices in detail at the same time. The deficiency of the previous theories is mainly due to emphasizing circuits rather than devices. Others [9], [10] have shown to be still not general enough when applied to practical design situations. More recently, another realization theory [11] which has generated several integrated voltage-controlled negative differential resistance devices through simple feedback connection around a MOSFET is shown to be more advantageous than those mentioned above, although it has been applied to one basic active device and one feedback connection type only.

In this paper, a general realization theory which is based upon a new feedback-transfer model (FTM) and is constructed both from mathematical and structural view points, is presented in Section II. The characteristics, realization procedures, and devices based on the developed theory are given in Section III, where the primary properties of the generated devices are tabulated and discussed. In Section IV, the integrated structure and properties of the tabulated devices are compared and discussed. Moreover, a specific application example based on the developed theory is calculated in detail in this section. In the last section conclusion and discussion are given.

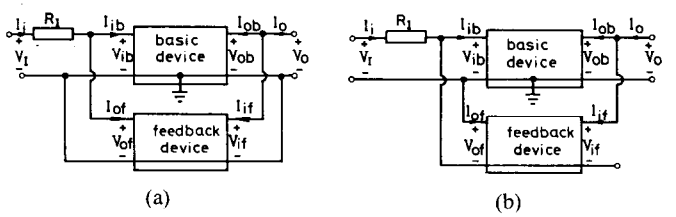


Fig. 1. Configurations of two voltage-shunt feedback connections of the integrated voltage-controlled negative resistance devices. (a) Class IAR. (b) Class IBR.

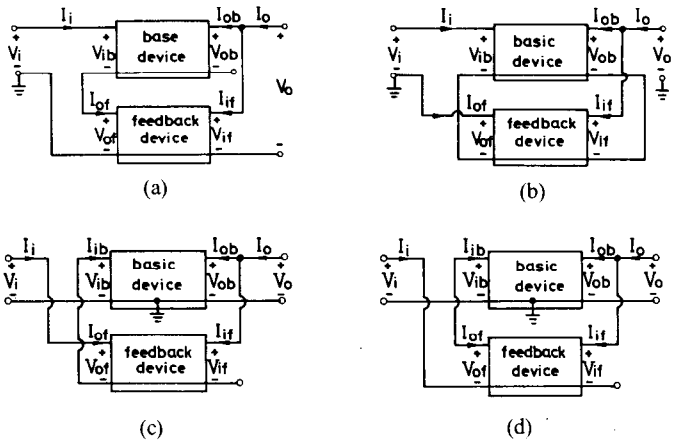


Fig. 2. Configurations of four voltage-series feedback connections of the integrated voltage-controlled negative resistance devices. (a) Class IIA. (b) Class IIB. (c) Class IIC. (d) Class IID.

II Feedback-Transfer Model of FET

There are two biasing modes for the FET. For a nongain mode such as common gate (CG), the biasing mode is of constant current drive. For gain modes such as common source (CS) and common drain (CD), the biasing mode is of constant voltage drive with zero input current. We consider here only gain modes.

The general structure of voltage-controlled negative differential resistance devices is a constant voltage drive field-effect basic device feedback-connected by a properly chosen feedback device. Since output current is not a multivalue function of output voltage in either N- or Λ-type [2] negative resistance, only voltage-series and voltage-shunt feedback connections are possible to generate it. Under short-circuit consideration and feedback device input or output terminal transformation defined as the interchange of position and bias between two input terminals or output terminals which will transform one operating mode into another (e.g., CS into CD), some redundant connections can be eliminated and only two in voltage-shunt feedback and four in voltage-series feedback are left, as shown in Figs. 1 and 2, respectively, where both three terminal basic and feedback devices are represented by two-port block diagrams. In these figures two voltage-shunt connections are called class IAR and class IBR, while four voltage-series

TABLE I
THE CONSTRAINTS ASSOCIATED WITH THE TERMINAL VOLTAGE POLARITIES, THE TERMINAL CURRENT DIRECTIONS, AND THE DEVICE MODES OF THE FOUR FEEDBACK CONNECTIONS CLASS IAR, CLASS IBR, CLASS IIA, AND CLASS IIB

parameter / class	V_{if} =	I_{if} =	V_{of} =	I_{of} =	properties of feedback devices	mode of basic devices
IAR	V_{ob}		V_{ib}		R_I	gain mode
IBR	$V_{ob}-V_{ib}$	$I_i-I_{ib}-I_{of}$	$-V_{ib}$		R_I non-gain mode	gain mode
IIA	$V_{ob}+V_{of}$	$I_{ib}+I_{ob}$		I_i+I_{ob}		gain mode
IIB	V_{ob}			$-I_{ib}-I_{ob}-I_{if}$	non-gain mode	gain mode

connections are called class IIA, class IIB, class IIC, and class IID. Note that only nongain mode feedback devices need to be considered in class IBR, IIB, and IID.

Since input current I_{ib} of the basic device must exist in class IIC and class IID, these two kinds of connections are not suitable for gain mode field-effect basic devices. Further inspecting class I connections, it is shown that for gain mode field-effect basic devices, input resistance R_I must be used, as shown in Fig. 1. All the constraints mentioned above, together with terminal voltage and current constraints obtained from structures shown in Figs. 1 and 2, are listed in Table I.

Refering to the feedback connection structures of the integrated negative differential resistance devices shown in Figs. 1 and 2, we choose two adequate terminal variables from the four in each of the integrated device, its feedback device and voltage driven basic device. In terms of the chosen variables, the other two can be expressed to appropriately describe the characteristics of the integrated device or its constituent devices. For class I connections with $I_{ib}=0$, the characteristics may be expressed by

$$I_0=I_0(V_0,V_I) \tag{1}$$

$$I_i=I_i(V_0,V_I) \tag{2}$$

$$I_{ob}=I_{ob}(V_{ob},V_{ib}) \tag{3}$$

$$V_{of}=V_{of}(I_{of},V_{if}) \tag{4}$$

$$I_{if}=I_{if}(I_{of},V_{if}). \tag{5}$$

For class II, those of the basic device and feedback device are changed to

$$V_{ob}=V_{ob}(I_{ob},V_{ib}) \tag{6}$$

$$I_{of}=I_{of}(V_{of},V_{if}) \tag{7}$$

$$I_{if}=I_{if}(V_{of},V_{if}). \tag{8}$$

It can be easily seen that the output characteristics of voltage-controlled negative resistance devices must always satisfy the condition

$$R_N^{-1}=\left.\frac{\partial I_0}{\partial V_0}\right|_{\text{fixed drive}}<0 \quad \text{(in negative differential resistance region).} \tag{9}$$

From this point of view we construct mathematically the sufficient and necessary condition for a feedback device to generate a negative differential resistance device.

For a voltage drive class IAR, the input circuit has the following relation:

$$V_I=R_I I_{of}+V_{of} \tag{10}$$

where V_I is constant. To be more general we still consider R_I being dependent on $V_{ob}(V_{if})$, $V_{ib}(V_{of})$, I_{of}, and V_I. But V_{of}, I_{of}, and V_I are also related as indicated in (10), so we may write

$$R_I=R_I(V_I,V_{of},V_{ob}). \tag{11}$$

By making use of partial derivative theory and equations from (1)–(5) and (11), we have

$$\left.\frac{\partial I_0}{\partial V_o}\right|_{V_I}=\left(\frac{\partial I_{ob}}{\partial V_{ib}}-\frac{1}{R_I}\frac{\partial I_{if}}{\partial I_{of}}-\frac{V_I-V_{of}}{R_I^2}\frac{\partial I_{if}}{\partial I_{of}}\frac{\partial R_I}{\partial V_{of}}\right)\left.\frac{\partial V_{of}}{\partial V_0}\right|_{V_I}-\frac{V_I-V_{of}}{R_I^2}\frac{\partial I_{if}}{\partial I_{of}}\frac{\partial R_I}{\partial V_{ob}}<0 \tag{12}$$

where $\partial V_{of}/\partial V_0|_{V_I}$ can be rewritten as

$$\left.\frac{\partial V_{of}}{\partial V_0}\right|_{V_I}=\left[\frac{\partial V_{of}}{\partial V_{if}}-\frac{V_I-V_{of}}{R_I^2}\frac{\partial V_{of}}{\partial I_{of}}\frac{\partial R_I}{\partial V_{ob}}\right]\cdot\left[1+\frac{1}{R_I}\frac{\partial V_{of}}{\partial I_{of}}+\frac{V_I-V_{of}}{R_I^2}\frac{\partial V_{of}}{\partial I_{of}}\frac{\partial R_I}{\partial V_{of}}\right]^{-1}. \tag{13}$$

Substituting (13) into (12), we obtain the desired condition

$$\left[\left(\frac{\partial I_{ob}}{\partial V_{ib}}-\frac{1}{R_I}\frac{\partial I_{if}}{\partial I_{of}}-\frac{V_I-V_{of}}{R_I^2}\frac{\partial I_{if}}{\partial I_{of}}\frac{\partial R_I}{\partial V_{of}}\right)\frac{\partial V_{of}}{\partial V_{if}}-\frac{V_I-V_{of}}{R_I^2}\frac{\partial R_I}{\partial V_{ob}}\left(\frac{\partial I_{ob}}{\partial V_{ib}}\frac{\partial V_{of}}{\partial I_{of}}+\frac{\partial I_{if}}{\partial I_{of}}\right)\right]\cdot\left[1+\frac{1}{R_I}\frac{\partial V_{of}}{\partial I_{of}}+\frac{V_I-V_{of}}{R_I^2}\frac{\partial V_{of}}{\partial I_{of}}\frac{\partial R_I}{\partial V_{of}}\right]^{-1}+\frac{\partial I_{ob}}{\partial V_{ob}}+\frac{\partial I_{if}}{\partial V_{if}}<0. \tag{14}$$

Similarly we can derive the condition for a voltage drive class IBR with nongain mode feedback device. The condition is

$$-\left\{\frac{\partial V_{of}}{\partial V_{if}}\left[\frac{\partial I_{ob}}{\partial V_{ib}}\left(1+\frac{\partial I_{if}}{\partial I_{of}}\right)+\frac{1}{R_I}\frac{\partial I_{if}}{\partial I_{of}}-\frac{V_I+V_{of}}{R_I^2}\frac{\partial I_{if}}{\partial I_{of}}\frac{\partial R_I}{\partial V_{of}}\right]+\frac{V_I+V_{of}}{R_I^2}\frac{\partial R_I}{\partial V_{ob}}\cdot\left(\frac{\partial V_{of}}{\partial I_{of}}\frac{\partial I_{ob}}{\partial V_{ib}}-\frac{\partial I_{if}}{\partial I_{of}}\right)-\frac{\partial I_{if}}{\partial V_{if}}\left(\frac{\partial I_{ob}}{\partial V_{ib}}\frac{\partial V_{of}}{\partial I_{of}}+1+\frac{1}{R_I}\frac{\partial V_{of}}{\partial I_{of}}-\frac{V_I+V_{of}}{R_I^2}\frac{\partial R_I}{\partial V_{of}}\frac{\partial V_{of}}{\partial I_{of}}\right)\right\}\cdot\left[1+\frac{\partial I_{if}}{\partial I_{of}}+\frac{1}{R_I}\frac{\partial V_{of}}{\partial I_{of}}-\frac{V_I+V_{of}}{R_I^2}\frac{\partial V_{of}}{\partial I_{of}}\frac{\partial R_I}{\partial V_{of}}\right]^{-1}+\frac{\partial I_{ob}}{\partial V_{ob}}<0. \tag{15}$$

For a voltage drive class IIA, the condition is

$$\left[\frac{\partial I_{of}}{\partial V_{of}}+\frac{\partial I_{if}}{\partial V_{of}}+\frac{\partial I_{of}}{\partial V_{if}}-\frac{\partial V_{ob}}{\partial I_{ob}}\frac{\partial I_{of}}{\partial V_{if}}\frac{\partial I_{of}}{\partial V_{of}}-\frac{\partial V_{ob}}{\partial V_{ib}}\frac{\partial I_{of}}{\partial V_{if}}\right]$$

$$\cdot\left[1+\frac{\partial V_{ob}}{\partial I_{ob}}\frac{\partial I_{of}}{\partial V_{of}}-\frac{\partial V_{ob}}{\partial V_{ib}}\right]^{-1}+\frac{\partial I_{if}}{\partial V_{if}}<0. \quad (16)$$

For a voltage drive class IIB, the condition is

$$-\left\{\left(\frac{\partial I_{of}}{\partial V_{of}}+\frac{\partial I_{of}}{\partial V_{if}}\right)\left[\frac{\partial V_{ob}}{\partial I_{ob}}\left(\frac{\partial I_{of}}{\partial V_{of}}+\frac{\partial I_{if}}{\partial V_{of}}\right)-\frac{\partial V_{ob}}{\partial V_{ib}}\right]\right\}$$

$$\cdot\left[1+\frac{\partial V_{ob}}{\partial I_{ob}}\left(\frac{\partial I_{of}}{\partial V_{of}}+\frac{\partial I_{if}}{\partial V_{of}}\right.\right.$$

$$\left.\left.+\frac{\partial I_{of}}{\partial V_{if}}+\frac{\partial I_{if}}{\partial V_{if}}\right)-\frac{\partial V_{ob}}{\partial V_{ib}}\right]^{-1}+\frac{\partial I_{of}}{\partial V_{of}}<0. \quad (17)$$

The general guide-line in the above calculations is to express negative resistance in (9) in terms of the characteristics of the basic and the feedback devices, rather than the composite characteristics of the integrated device. Thus the conditions derived may serve as a design rule for the integrated negative differential resistance devices. Further simplications of these conditions will be performed in Section III.

Both the structural feedback connections shown in Figs. 1 and 2, and the mathematical conditions in (14)–(17) form the essential model of our general realization theory. Since this model concerns mainly with feedback and transfer characteristics, we refer it as FTM.

III. Characteristics and Realization Techniques

A. Characteristics of Basic Active Devices

Two kinds of characteristics for the associated basic active devices are required in the FTM of the FET. One is the terminal voltage polarities and current directions in all three operating configurations of both complementary conduction carrier types of the basic active devices. These are needed to satisfy the constraints listed in Table I. The other is the forward transfer, reverse transfer, input, and output characteristics. These are needed in the mathematical conditions of the FTM. As a first step these two kinds of characteristics must be provided for the generation of negative differential resistance devices.

By investigating and comparing all the partial derivatives contained in the conditions of the FTM, it is found that only ten different kinds of characteristics for both basic and feedback devices are required. They are selected from:

forward transfer characteristics

$$\left(\left.\frac{\partial V_o}{\partial V_i}\right|_{I_o},\left.\frac{\partial I_o}{\partial I_i}\right|_{V_o},\left.\frac{\partial I_o}{\partial V_i}\right|_{V_o}\right)$$

reverse transfer characteristics

$$\left(\left.\frac{\partial V_i}{\partial V_o}\right|_{I_i},\left.\frac{\partial I_i}{\partial I_o}\right|_{V_i},\left.\frac{\partial I_i}{\partial V_o}\right|_{V_i}\right)$$

input characteristics

$$\left(\left.\frac{\partial I_i}{\partial V_i}\right|_{V_o},\left.\frac{\partial V_i}{\partial I_i}\right|_{V_o},\left.\frac{\partial I_i}{\partial V_i}\right|_{I_o},\left.\frac{\partial V_i}{\partial I_i}\right|_{I_o}\right)$$

and output characteristics

$$\left(\left.\frac{\partial I_o}{\partial V_o}\right|_{V_i},\left.\frac{\partial V_o}{\partial I_o}\right|_{V_i},\left.\frac{\partial I_o}{\partial V_o}\right|_{I_i},\left.\frac{\partial V_o}{\partial I_o}\right|_{I_i}\right).$$

Moreover, the characteristics of R_I, $\partial R_I/\partial V_{ob}$, and $\partial R_I/\partial V_{of}$, are needed in a voltage drive class I. The desired ten kinds of characteristics may be calculated from dc characteristics of the device, while $\partial R_I/\partial V_{ob}$ and $\partial R_I/\partial V_{of}$ may be determined as long as R_I is realized.

B. Realization Procedures and Generated Devices

The general realization procedures which use the derived prior theory to generate negative resistance devices are:

(1) Using the characteristics in the specified type of basic device and feedback device, simplify the general conditions in the FTM.

(2) Subjecting to the simplified condition and corresponding constraints of terminal voltages and currents, choose suitable feedback devices for one basic device to form the integrated device.

(3) Using the equivalent circuit of the device, design the integrated structure as compactly as possible.

(4) Using the device physics or terminal characteristics, characterize the dc characteristics of the integrated voltage-controlled negative differential resistance device, such as negative resistance, peak voltage, valley voltage, etc.

B-1. Class IAR Device:

First consider a CS n-channel EMOSFET in the saturation region, we have $\partial I_{ob}/\partial V_{ib}>0$, $\partial I_{ob}/\partial V_{ob}=0$. For a feedback device with $I_{if}=0$ and suitable R_I with $\partial R_I/\partial V_{of}\geqslant 0$, the condition of (14) may be simplified to be

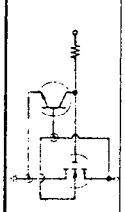
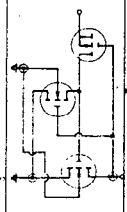
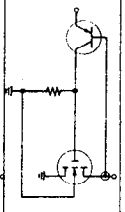
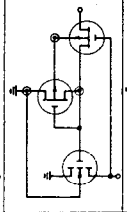
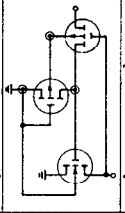
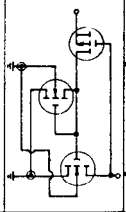
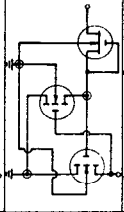
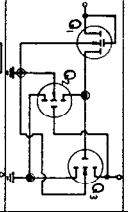
$$\frac{\partial V_{of}}{\partial V_{if}}<\frac{V_I-V_{of}}{R_I^2}\frac{\partial R_I}{\partial V_{ob}}\frac{\partial V_{of}}{\partial I_{of}} \quad (18)$$

with negative differential resistance R_N being

$$R_N^{-1}=\frac{\dfrac{\partial I_{ob}}{\partial V_{ib}}\dfrac{\partial V_{of}}{\partial V_{if}}-\dfrac{V_I-V_{of}}{R_I^2}\dfrac{\partial R_I}{\partial V_{ob}}\dfrac{\partial I_{ob}}{\partial V_{ib}}\dfrac{\partial V_{of}}{\partial I_{of}}}{1+\dfrac{1}{R_I}\dfrac{\partial V_{of}}{\partial I_{of}}+\dfrac{V_I-V_{of}}{R_I^2}\dfrac{\partial V_{of}}{\partial I_{of}}\dfrac{\partial R_I}{\partial V_{of}}}. \quad (19)$$

Two special features corresponding to $\partial R_I/\partial V_{ob}=0$ and $\partial V_{of}/\partial V_{if}=0$ in (18) are considered. The former leads to the generation of Λ-MOSFET [6], [7] or its similarities [5], [11], while the latter generates some new devices. All are shown in the first six rows of Table II. The combination of these two features also leads to the new device shown in the seventh row of Table. II. The negative resistance types of these devices may be determined from (19). In Λ-type

TABLE II
THE GENERATED VOLTAGE-CONTROLLED NEGATIVE RESISTANCE DEVICES OF CLASS IAR, USING CS AND CD n-CHANNEL EMOSFET AS BASIC DEVICES

CS n-EMOSFET								basic device
CE npn BJT	CS n-EMOSFET	CC pnp BJT	CD p-DMOSFET	CD p-EMOSFET	CD p-EMOSFET	CS n-EMOSFET	CS n-EMOSFET	feedback device
								equivalent circuit
2 (substrate bias, isolation)	2 (substrate bias)	1 (isolation)	3 (substrate bias)	3 (substrate bias)	2	3	3 (load device with substrate bias)	number of MPs
same	complementary	complementary	complementary	complementary	complementary	same	same	type of conduction carriers
N	λ	λ	λ	λ	λ	λ	λ	type of negative resistnace
3	3	3	3	3	3	3	3	number of operating terminals
const. voltage	const. voltage	const. voltage	const. voltage	const. voltage	const. voltage	const. voltage	const. voltage	biasing mode
published [3], [11]	published [11]	new	new	new	new	published [11]	published [6] - [7]	new or published

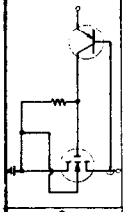
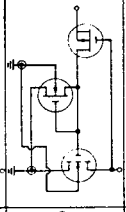
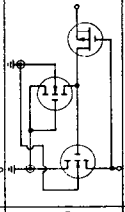
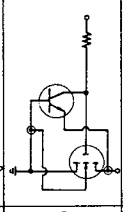
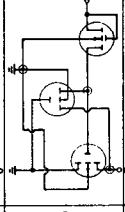
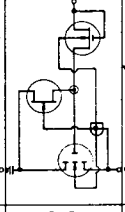
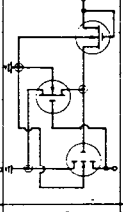
normal CD n-EMOSFET							basic device
CC pnp BJT	CD p-DMOSFET	CS p-DMOSFET	abnormal CB npn BJT	abnormal CG n-EMOSFET	CD n-JFET	CD n-DMOSFET	feedback device
							equivalent circuit
2 (substrate bias, isolation)	2 (substrate bias)	2 (substrate bias)	2 (substrate bias, isolation)	3 (substrate bias)	1.5 (substrate bias)	3 (substrate bias)	number of MPs
same	complementary	complementary	same	same	same	same	type of conduction carriers
λ	λ	λ	N	N	λ	λ	type of negative resistance
3	3	3	3	3	3	3	number of operating terminals
const. voltage	const. voltage	const. voltage	const. voltage	const. voltage	const. voltage	const. voltage	biasing mode
new	new	new	new	new	new	new	new or published

TABLE III
THE GENERATED VOLTAGE-CONTROLLED NEGATIVE RESISTANCE DEVICES OF CLASS IAR, USING JFET AND DMOSFET AS BASIC DEVICES

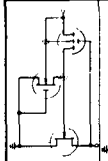
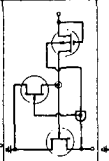
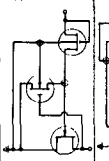
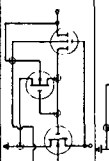
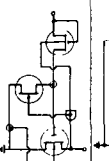
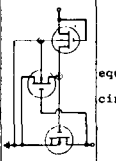
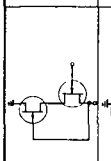
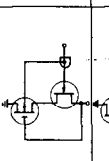
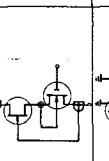
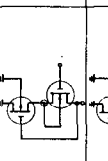
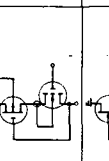
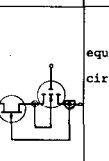
CS n-JFET			CS n-DMOSFET			basic device
CD n-EMOSFET	CS p-JFET	CS p-DMOSFET	CD n-EMOSFET	CS p-JFET	CS p-DMOSFET	feedback device
						equivalent circuit
2 (substrate bias)	1.5 (substrate bias and isolation)	2 (substrate bias)	4 (substrate bias)	2.5 (substrate bias)	2 (substrate bias)	number of MPs
same	complementary	complementary	same	complementary	complementary	type of conduction carriers
λ	λ	λ	λ	λ	λ	type of negative resistance
3	3	3	3	3	3	number of operating terminals
const. voltage	const. voltage	const. voltage	const. voltage	const. voltage	const. voltage	biasing mode
new	new	new	new	new	new	new or published

TABLE IV
THE GENERATED VOLTAGE-CONTROLLED NEGATIVE RESISTANCE DEVICES OF CLASS IIA

CS n-JFET		CS n-DMOSFET		CS n-EMOSFET		basic device
CS p-JFET	CS p-DMOSFET	CS p-JFET	CS p-DMOSFET	CD p-DMOSFET	CD p-JFET	feedback device
						equivalent circuit
0 (isolation)	0.5 (substrate bias)	1.5	1 (substrate bias)	1 (substrate bias)	1.5	number of MPs
complementary	complementary	complementary	complementary	complementary	complementary	type of conduction carriers
λ	λ	λ	λ	λ	λ	type of negative resistance
3 or 2	3 or 2	3 or 2	3 or 2	3	3	number of operating terminals
const. voltage or no bias	const. voltage or no bias	const. voltage or no bias	const. voltage or no bias	const. voltage	const. voltage	biasing mode
published [4],[9],[10]	published [2],[10]	published [2],[10]	published [2],[10]	new	published [1]	new or published

R_N^{-1} is zero in larger voltage range, while in N-type R_N^{-1} is positive.

For feedback device with $I_{if} \neq 0$ and R_I = constant, the simplified condition is

$$\frac{\partial V_{of}}{\partial V_{if}} < -\frac{\dfrac{\partial I_{if}}{\partial V_{if}}\left(1+\dfrac{1}{R_I}\dfrac{\partial V_{of}}{\partial I_{of}}\right)}{\dfrac{\partial I_{ob}}{\partial V_{ib}}-\dfrac{1}{R_I}\dfrac{\partial I_{if}}{\partial I_{of}}} \tag{20}$$

which generates the device in the eighth row of Table II.

In Table II we also list those of CD n-channel EMOSFET, while in Table III we list those of JFET and DMOSFET. The duals of these integrated devices are not indicated.

B-2. Class IBR Device:

Using the relations $\partial I_{if}/\partial I_{of} \simeq -1$ and $\partial R_I/\partial V_{of} \leqslant 0$, the condition of (15) is simplified. From the simplified condition it can be seen that no devices exist.

B-3. Class IIA Device:

For a CS n-EMOSFET in the saturation region, we have $\partial V_{ob}/\partial V_{ib} \to -\infty$, $\partial I_{ob}/\partial V_{ob} = 0$. The simplified condition is

$$R_N^{-1} = \frac{\partial I_{of}}{\partial V_{if}}\left(\left.\frac{\partial I_{ob}}{\partial V_{ib}}\right|_{V_{ob}} - \frac{\partial I_{if}}{\partial V_{of}}\right) \cdot \left[\left.\frac{\partial I_{ob}}{\partial V_{ib}}\right|_{V_{ob}} + \frac{\partial I_{of}}{\partial V_{of}}\right]^{-1} + \frac{\partial I_{if}}{\partial V_{if}} < 0. \tag{21}$$

The generated devices are shown in Table IV. Also listed are those of CS n-channel DMOSFET and JFET. In case of $I_{if} = 0$ in (21), we have $\partial I_{of}/\partial V_{if} < 0$ whenever the saturation region of FET is reached. This in turn hints that it is impossible to have flat saturation region shown in the characteristics of these devices. Such property has been confirmed in the literature [1], [2].

B-4. Class IIB Device:

No devices exist.

V. APPLICATION EXAMPLE

For all the FET-like devices generated and tabulated in Table II–IV, their biasing modes are the constant-voltage modes. However, some devices which may conduct even without bias are denoted by the no-bias mode. The number of operating terminals in these special devices may be three or two as indicated in the tables. If the major conduction carrier in each constituent device of the generated devices is electron (or hole), the generated device is denoted as the same carrier type; otherwise, the complementary type is denoted in the tables. Since the linear region of a CG-EMOSFET and the saturation region of a CB-BJT are not normally used in the conventional circuit applications, we denote them using an extra word "abnormal" as listed in Table II.

Although the compactness in the integrated structure realized from the equivalent circuit of the generated device is dependent upon many foctors such as fabrication technology, layout rule, etc., one of the determining guide-lines is to find the connection points that may be merged into the common IC regions. Such a connection point is defined as the merged point (MP) and is indicated by a small circle, as shown in the tables. For the generated devices with the same type of the constituent devices, more MP's in general may have smaller chip size. If the two gate regions of an integrated structure in a JFET can not be merged together in a MP, the number of such a MP is counted to be 0.5 and is denoted by a semicircle. Note that if the source and the substrate electrodes of the constituent FET's in a negative resistance device are not at the same poten-

tial, the substrate bias or back-gate bias effect must be considered. Moreover, some constituent devices must be isolated in the integrated structure of a generated device, then extra area must be paid for such isolations. Both the substrate bias and the isolation are also listed in the tables.

In the case of applying these generated devices to digital IC's, three important factors, namely, the density performance and compatibility with the well-developed fabrication technology, should be considered to determine their advantages. Due to the negligible valley current for the Λ-type negative resistance and the promising high-speed operation for the same type of conduction carrier (electron), only five devices listed in Table II and two devices listed in Table III are further compared. If we exclude the devices involving isolation and the devices involving the fabrication of JFET or p-DMOSFET which is not yet well-developed in digital IC's, only two published devices listed in the first two rows of Table II and two new devices listed in the ninth row of Table II and the third row of Table III are considered to be advantageous.

In order to demonstrate the capability of our general realization theory, the Lambda MOSFET [11] in the first row of Table II is characterized directly by using the developed theory.

Under the gradual channel approximation with negligible channel-length modulation effect, the current equation for a CS n-EMOSFET are

$$I_{DS}=G_0\left\{\left(V_{GS}-V_{FB}-2\phi_{fp}-\frac{V_{DS}}{2}\right)V_{DS}-\frac{2}{3}K\left[\left(V_{DS}+2\phi_{fp}\right)^{3/2}-\left(2\phi_{fp}\right)^{3/2}\right]\right\} \quad \text{(linear region)} \quad (22)$$

$$I_{DS}=\frac{G_0}{2}\left\{\left(V_{GS}-V_{FB}-2\phi_{fp}\right)^2-g^2(K,V_{GS})-\frac{4}{3}K\left\{\left[V_{GS}-V_{FB}+g(K,V_{GS})\right]^{3/2}-\left(2\phi_{fp}\right)^{3/2}\right\}\right\} \quad \text{(saturation region)} \quad (23)$$

where

$$G_0=\frac{\mu_n ZC_0}{L}$$

$$K=\frac{(2\epsilon_s qN_A)^{1/2}}{C_0}$$

$$g(K,V_{GS})=\frac{K^2}{2}-K\left(V_{GS}-V_{FB}+\frac{K^2}{4}\right)^{1/2}.$$

If the substrate-bias effect in the load EMOSFET which is always operated in the saturation region, is considered, R_I in (11) may be written as

$$R_I(V_I,V_{of})\equiv\frac{\partial I_{of}}{\partial(V_I-V_{of})}$$

$$=G_{\mathrm{OL}}^{-1}\left[\left(V_I-V_{of}-V_{\mathrm{FB}}-2\phi_{fp}\right)+K\left(2\phi_{fp}+V_{of}\right)^{1/2}\right]^{-1}. \quad (24)$$

Consider only the case that the basic device is operated in the saturation region. The feedback device may be operated in the saturation region when the output voltage V_0 is small and in the linear region as V_0 is large. For the feedback device in the saturation region, we have

$$\left.\frac{\partial V_{of}}{\partial V_{if}}\right|_{I_{of}}\to-\infty,\quad \left.\frac{\partial V_{of}}{\partial I_{of}}\right|_{V_{if}}\to\infty,$$

and

$$\left.\frac{\partial V_{of}}{\partial V_{if}}\right|_{I_{of}}\Big/\left.\frac{\partial V_{of}}{\partial I_{of}}\right|_{V_{if}}=-\left.\frac{\partial I_{of}}{\partial V_{if}}\right|_{V_{of}}$$

which can be calculated from (23). Further using (24), the differential negative resistance R_N may be calculated from (19) and expressed as

$$R_N=-\left\{\frac{1}{R_I}+(V_I-V_{of})G_{\mathrm{OL}}\left[1-K\left(2\phi_{fp}+V_{of}\right)^{-1/2}\right]\right\}\cdot(G_{\mathrm{OB}}G_{\mathrm{OF}})^{-1}\left\{\left(V_{of}-V_{\mathrm{FB}}-2\phi_{fp}\right)-g(K,V_{of})g'(K,V_{of})-K\left[V_{of}-V_{\mathrm{FB}}+g(K,V_{of})\right]^{1/2}\left[1+g'(K,V_{of})\right]\right\}\cdot\left\{\left(V_0-V_{\mathrm{FB}}-2\phi_{fp}\right)-g(K,V_0)g'(K,V_0)-K\left[V_0-V_{\mathrm{FB}}+g(K,V_0)\right]^{1/2}\left[1+g'(K,V_0)\right]\right\}^{-1} \quad (25)$$

where $g'(K,V_{of})$ is the first-order derivative of $g(K,V_{of})$ with respect to V_{of}. The voltage V_{of} may be expressed in terms of V_0 and V_I using the relation $V_I=I_{of}R_I+V_{of}$, and is written as

$$V_I=R_I(V_{of})\frac{G_{\mathrm{OF}}}{2}\left\{\left(V_0-V_{\mathrm{FB}}-2\phi_{fp}\right)^2-g^2(K,V_0)-\frac{4}{3}K\left\{\left[V_0-V_{\mathrm{FB}}+g(K,V_0)\right]^{3/2}-\left(2\phi_{fp}\right)^{3/2}\right\}\right\}+V_{of}. \quad (26)$$

Using (25) and (26) R_N may be expressed as a function of V_0 and V_I. Integrating R_N^{-1} relative to the variable V_0, the I_0–V_0 characteristic of the Lambda MOSFET in the negative resistance region may be obtained with an arbitrary constant C.

Using (25) the peak point of the device is determined by setting $R_N^{-1}=0$. The peak voltage V_p is the voltage V_{if} such that

$$\left.\frac{\partial I_{of}}{\partial V_{if}}\right|_{V_{of}}=0$$

whereas the peak current I_p is the current I_{ob} of the basic device when $V_{ob}=V_p$. Both V_p and I_p are expressed in terms of V_I. Using the boundary condition $I_0(V_p)=I_p$, the constant C in the expression is determined.

For the feedback device being operated in the linear

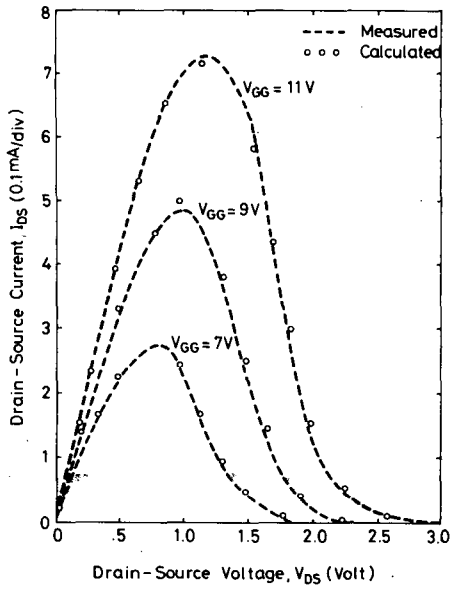


Fig. 3. Comparisons between the output characteristic of the fabricated Lambda MOSFET (dots) and the computer simulated results (line).

region, the negative resistance R_N is

$$R_N = -\left\{1+G_{OF}^{-1}\left[V_0 - V_{FB} - 2\phi_{fp} - K\left(V_{of}+2\phi_{fp}\right)^{1/2}\right]^{-1} \cdot\left\{\frac{1}{R_I}+\left(V_I - V_{of}\right)G_{OL}\left[1-K\left(2\phi_{fp}+V_{of}\right)^{-1/2}\right]\right\}\right\} \cdot\left(G_{OB}V_{of}\right)^{-1}\left\{\left(V_0 - V_{FB} - 2\phi_{fp}\right) - g(K,V_0)g'(K,V_0) - K\left[V_0 - V_{FB} + g(K,V_0)\right]^{1/2}\left[1+g'(K,V_0)\right]\right\}^{-1} \cdot\left[V_0 - V_{FB} - 2\phi_{fp} - V_{of} - K\left(V_{of}+2\phi_{fp}\right)^{1/2}\right]. \quad (27)$$

Using the relation

$$V_I = R_I(V_{of})G_{OF}\left\{\left(V_0 - V_{FB} - 2\phi_{fp} - \frac{V_{of}}{2}\right)V_{of} - \frac{2}{3}K\left[\left(V_{of}+2\phi_{fp}\right)^{3/2} - \left(2\phi_{fp}\right)^{3/2}\right]\right\} + V_{of} \quad (28)$$

V_{of} may be solved in terms of V_0 and V_I. Thus the negative resistance R_N as well as the output current I_0 of the Lambda MOSFET may be obtained with the similar procedures cited above.

The valley point is determined by using

$$\left.\frac{\partial I_{ob}}{\partial V_{ib}}\right|_{V_{ob}} = 0$$

which is the second condition of $R_N^{-1}=0$. The valley voltage V_V is obtained by first solving $V_{ib}(=V_{of})$ from

$$\left.\frac{\partial I_{ob}}{\partial V_{ib}}\right|_{V_{ob}} = 0$$

and then substituting V_{ib} into (28) to obtain V_0. The calculated V_V is then substituted into the expression $I_0(V_0, V_I)$ to obtain the valley current I_V for a given V_I. Since $R_N^{-1}=0$ for $V_0 > V_I$, the negative resistance is of Λ-type.

TABLE V
MOS TESTING DESIGN PARAMETERS OF THE FABRICATED LAMBDA MOSFET

Parameters \ Transistor	Q_1	Q_2	Q_3
Geometrical channel width (μm)	20	75	200
Geometrical channel length (μm)	75	15	15
Effective channel width (μm)	20	75	200
Effective channel length (μm)	69.6	9.6	9.6

Nsub = $5 \times 10^{15}/cm^3$, tox = 1000 Å

The integrated structure of the Lambda MOSFET had been realized and fabricated by using the conventional Al-gate technology. Based upon the developed theory, the simulation of the Lambda MOSFET is made for the output characteristic and is compared to the experimental data, as shown in Fig. 3, where the electron surface mobility is assumed to be 500 $cm^2/V \cdot s$ and the dimensions and parameters of the fabricated device are listed in Table V. It is clearly seen that the general agreements between the experimental data and the theoretical computations are obtained, which substantiate the exactness of the theory. Similar procedures can be done for other devices.

V. CONCLUSION AND DISCUSSION

In this paper we have presented a new general realization theory of FET-like voltage-controlled negative differential resistance devices in an unified manner. Using the developed theory and technique, many negative differential resistance devices either new or published are generated. Some primary properties of the generated devices are exactly predicted and partly confirmed by the published literatures; moreover, their integrated circuit capabilities are initially investigated through counting the number of merged points on the basis of the existing IC planar technology. In order to demonstrate the capability of the proposed model, the Lambda MOSFET using three enhancement-mode n-MOSFET's is analyzed and modeled in detail. Good agreements between the experimental data of the fabricated device and the computer simulation are obtained. Hence, it is not difficult to perform a thorough search for all the FET-like devices using the proposed realization techniques.

Since the feedback circuits are realizable from the FTM, once a basic circuit is chosen, the generation of more complex negative differential resistance circuits may be easily extended. Thus the capability of the proposed model is great. As regard to other applications of the developed model and simulation technique, we will present elsewhere.

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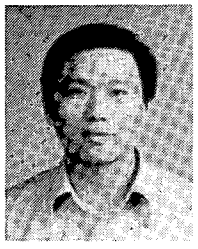

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Minimal Cascade Factorization of Real and Complex Rational Transfer Matrices

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Abstract—**A cascade factorization $R(\lambda)=R_1(\lambda)\cdot R_2(\lambda)\cdots R_k(\lambda)$ of an $n\times n$ nonsingular rational matrix $R(\lambda)$ is said to be minimal when the McMillan degrees of the factors add up to the McMillan degree of the original matrix. In this paper we give necessary and sufficient conditions for such a factorization to exist in terms of a state-space realization for $R(\lambda)$. Next, we focus on numerical and algorithmic aspects. We discuss the numerical conditioning of the problem and we give algorithms to compute degree one factorizations and real degree two factorizations. Finally, we discuss the special case where $R(\lambda)$ is a para J-unitary matrix.**

Manuscript received June 2, 1980; revised October 26, 1980. This work was supported in part by the National Science Foundation under Contracts MCS78-11985 and ENG78-10003, and by the U.S. Army Research Office under Contract DAAG29-79-C-0215.

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I. INTRODUCTION

The problem of factorization of an $n\times n$ rational matrix $R(\lambda)$ into two factors $R(\lambda)=R_1(\lambda)\cdot R_2(\lambda)$ has recently received a lot of attention. In [10] sufficient conditions for the factorization to exist are given and it is shown by example that, in general, nontrivial factorizations (i.e., where the factors are not constant) may not exist. Independently, Van Dooren [25] and Bart *et al.* [2] gave necessary and sufficient conditions in terms of a state-space realization for $R(\lambda)$ [3]. The mathematical factorization theory is further elaborated in [2]. The work of Vandewalle [24] also deserves attention. There necessary and sufficient conditions are derived for a matrix $R_1(\lambda)$ to be a minimal factor of $R(\lambda)$ in terms of the parameters of the matrix itself.

0098-4094/81/0500-0390$00.75