Modeling and Optimization of Monolithic Polycrystalline Silicon Resistors

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Abstract—The processing parameters of monolithic polycrystalline silicon resistors are examined, and the effect of grain size on the sensitivity of polysilicon resistivity versus doping concentration is studied theoretically and experimentally. Because existing models for polysilicon do not accurately predict resistivity dependence on doping concentration as grain size increases above 600 Å, a modified trapping model for polysilicon with different grain sizes and under various applied biases is introduced. Good agreement between theory and experiments demonstrates that an increase in grain size from 230 to 1220 Å drastically reduces the sensitivity of polysilicon resistivity to doping levels by two orders of magnitude. Such an increase is achieved by modifications of the integrated-circuit processes. Design criteria for the optimization of monolithic polysilicon resistors have also been established based on resistivity control, thermal properties, and device geometry.

Symbols

A Cross-section area of resistor (cm^2).
E_A Impurity (acceptor) level (eV).
E_a Activation energy of resistivity to $1/kT$ (eV).
E_F Fermi energy level (eV).
E_g Energy band gap (eV).
E_i Intrinsic Fermi level referred to E_{i0} (eV).
E_{i0} Intrinsic Fermi level at center of the grain (eV).
E_T Grain-boundary trapping state energy referred to E_{i0} (eV).
e_T Trapping state energy referred to E_i at grain boundary (eV).
h Planck's constant.
I Current (A).
I_s Saturation current (A).
J Current density (A/cm^2).
k Boltzmann's constant.
L Grain size (cm).
l half-width of crystallite neutral region (cm).
m_e^* Electron effective mass (kg).
m_h^* Hole effective mass (kg).
N Doping concentration (cm^{-3}).
N^+ Ionized impurity concentration (cm^{-3}).
N^* Doping concentration below which grains are completely depleted (cm^{-3}).
N_g Number of grains between resistor contacts.
n_i Intrinsic carrier concentration (cm^{-3}).
p Hole concentration (cm^{-3}).
$p(0)$ Hole concentration in neutral region or at center of the grain (cm^{-3}).
$\bar{p}$ Average carrier (hole) concentration (cm^{-3}).
q Elementary charge.
Q_T Grain-boundary trapping state density (cm^{-2}).
Q_T^+ Effective (or ionized) trapping state density (cm^{-2}).
R Resistance (Ω).
T Absolute temperature (K).
V_a Applied voltage between resistor contacts (V).
V_B Built-in potential barrier height (V).
V_{ba} Applied voltage across grain-boundary barriers (V).
V_c Applied voltage across crystallite neutral region (V).
V_g Applied voltage across each grain (V).
W Width of depletion region (cm).
δ Grain-boundary thickness (cm).
ϵ Single-crystal silicon permittivity.
ρ Polysilicon resistivity ($\Omega \cdot cm$).
ρ_B Barrier resistivity ($\Omega \cdot cm$).
ρ_C Crystallite bulk resistivity ($\Omega \cdot cm$).
ρ_{GB} Grain-boundary resistivity ($\Omega \cdot cm$).
μ_{eff} Polysilicon effective mobility [$cm^2/(V \cdot s)$].
μ_n Electron mobility of single-crystal silicon [$cm^2/(V \cdot s)$].
μ_p Hole mobility of single-crystal silicon [$cm^2/(V \cdot s)$].

I. Introduction

POLYCRYSTALLINE silicon (polysilicon) has been studied for many years and has found an increasing number of recent applications [1] in solar cells, integrated-circuit elements such as silicon-gate MOS devices, interconnections, passivation or isolation layers, monolithic distributed *RC* filters, and high-value resistors. Polysilicon resistors are important for integrated circuits for the following reasons:

They are compatible with such monolithic silicon technologies as MOS or bipolar (BJT) processes [2].

Resistance can be adjusted through several decades by ion implantation where the lightly doped material has a sheet resistance as high as that of pure intrinsic single-crystal silicon especially required in low-power circuits.

Resistors top-deposited on the field oxide of MOS IC's or on

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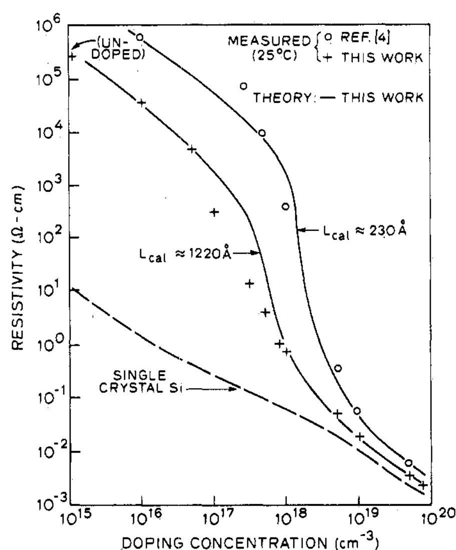


Fig. 1. Measured and theoretical resistivities versus doping concentrations at room temperature for polysilicon with various grain sizes and for single-crystal silicon.

the isolation region of bipolar transistors require no extra area compared to the large space occupied by diffused or ion-implanted resistors.

Because they are isolated by a thick oxide, resistance is much less dependent on substrate bias, and parasitic capacitance is smaller than that resulting from junction isolation in diffused or implanted resistors.

Their negative temperature coefficient can compensate for the temperature dependence of leakage or subthreshold current in active devices [3].

Their linearity is good for a common electric field where sheet resistance ranges as high as gigaohm per square; this is in contrast to the much lower linearity and less controllability of all other monolithic resistors [2].

The following problems are encountered when employing polysilicon for monolithic resistors.

The sensitivity of polysilicon resistivity to doping concentration is very large, especially in the high-resistivity range; for example, over the doping level of 5×10^{17} to 5×10^{18} cm^{-3}, a resistivity change of approximately five decades has been observed (Fig. 1) [4].

The structure of polysilicon and grain size are sensitive to thermal processing steps; in addition, implanted arsenic dopants segregate to the grain boundaries in quantities that are dependent on annealing temperatures [5]. These cause poor resistivity control and instability in doped polysilicon [2], [6].

Polysilicon shows a very large temperature coefficient, especially in lightly doped samples. For example, a sheet resistance of 1 GΩ/□ at 25°C drops three decades when the temperature is elevated to 160°C [4].

To resolve these problems, this paper introduces a new modified trapping model for monolithic polysilicon resistors with small and large grain sizes and applies it to device analysis and optimization. Processing parameters are selected to ensure good control and reproducibility of the material properties. Experimental procedures are described. Theoretical and experimental results are compared, and the validity of this quantitative model is demonstrated. Based on this model, design criteria (such as resistivity control, thermal properties, and device geometry) are established for monolithic polysilicon resistors.

A. Processing Parameters

By comparing the sharp change in resistivity versus doping concentration (ρ versus N) in polysilicon to the gradual change in single-crystal silicon, resistivity dependence on the doping level in polysilicon is expected to approach that of single-crystal silicon and thereby demonstrate lower sensitivity [2], [7] as grain size increases. High deposition temperature or the deposition of thick film can result in a large grain size; however, acceptable surface roughness, lithography resolution, and smaller device geometry limit the maximum size. Other device-processing constraints dictate the highest deposition temperature. This paper investigates the effect of grain size on the ρ versus N curve based on published data [4], [8] for 1.0- and 0.67-μm-thick polysilicon layers with grain sizes of 230 and 420 Å and deposition temperatures of 750° and 960°C, respectively, and on data obtained from this work for 1.0- and 5.0-μm-thick films deposited at 1050°C and with grain sizes from 0.1 to 1.0 μm.

The columnar structure of polysilicon increases the diffusivity of dopants to a much higher degree than does single-crystal silicon [9]. Because the diffusion process strongly depends on grain structure and deposition temperature, doping polysilicon with a diffusion source is difficult to control. Better control is achieved by dopant ion implantation [4] through an oxide layer on top of the polysilicon to avoid loss of dopants during subsequent thermal steps; high-temperature postimplantation annealing was used to activate and redistribute them uniformly throughout the film immediately after implantation. It was also observed that the sensitivity of grain size to annealing temperature is reduced substantially at 1000°C or higher [10]. Grain growth is also related to deposition temperature; the initial size of polysilicon deposited at 600° to 900°C is small, and significant changes in structure and dimensions occur during subsequent higher thermal steps [8]. On the other hand, a high deposition temperature produces relatively large grains that are unlikely to change during subsequent thermal anneals and, therefore, achieves better stability and control [2].

Dopant segregation at grain boundaries is undesirable for good resistivity control. Implanted arsenic segregates at annealing temperatures of 800° to 900°C [5]; in contrast, phosphorus- and boron-doped polysilicon deposited at 1225°C demonstrated no segregation [11]. This behavior is explained as follows. At a low annealing temperature of 750°C for 40 min, the diffusion distance of dopants is small and segregation could be minimum [12]. At an annealing temperature of 800° to 900°C, this distance becomes larger and, because diffusion along grain boundaries is higher than in single-crystal silicon, segregation may occur. At higher temperatures, the difference in diffusivities along the boundaries and in single crystals is less pronounced [13] and, as a result, segregation is minimized.

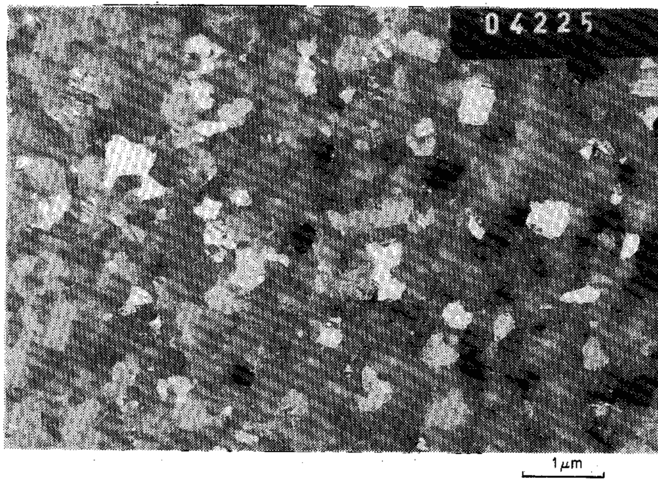


Fig. 2. Dark-field TEM of a 1-μm polysilicon film. The grain configuration in certain crystal orientations is well defined.

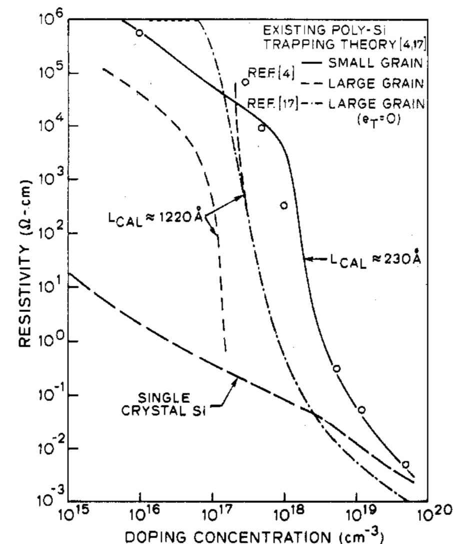


Fig. 3. Theoretical room-temperature resistivity versus doping concentration of a grain size of 1220 Å based on [4] and [17].

At all annealing temperatures, however, segregation of the boron dopants is least significant compared to phosphorus and arsenic [5], and grain growth is found much less enhanced in this work [14].

Based on these observations, it is expected [2] that high-temperature deposition and ion implantation with boron through an oxide cap followed by a high-temperature anneal will result in more controllable and reproducible resistivity in polysilicon.

B. Existing Models

Polysilicon material is composed of crystallites joined together by grain boundaries (Fig. 2). Inside each crystallite, atoms are arranged in such a way that it can be considered a small single crystal. The grain boundary consists of layers of disordered atoms that represent a transitional region between different orientations of neighboring crystallites.

Two models have been proposed to explain the effect of a grain boundary on the electrical properties of doped polysilicon. The first is a dopant-segregation model wherein the grain boundary serves as a sink for the preferential segregation of impurity atoms that become inactive at the boundary [15]. This model, however, cannot explain the mobility minimum at the critical doping level and the temperature dependence of resistivity. The second is a carrier-trapping model [4], [16], [17] wherein the grain boundary contains trapping states caused by defects resulting from disordered or incomplete atomic bonding; these states trap part of the carriers from the ionized and uniformly distributed dopants. This process not only reduces the number of carriers but also creates a potential barrier from the electrically charged traps and impedes the motion of carriers from one crystallite to another. This model better explains the sharp change in resistivity versus doping level, mobility minimum, and temperature dependence. Even if the dopants do segregate, the trapping model can still be applied, based on an active-dopant concentration that can be obtained by subtracting the inactive-dopant concentration from the implanted concentration [5]. In our work, the validity of carrier trapping is maintained by using boron as the dopant and selecting optimal processing conditions to minimize dopant segregation.

Kamins [16] applied carrier trapping qualitatively to explain the mobility behavior in polysilicon. Seto [4] developed the first quantitative derivations to demonstrate the validity of the trapping model. These derivations, however, cannot be applied to a grain larger than 600 Å because they predict a discontinuity near the critical doping concentration (Fig. 3) as the result of an incomplete treatment of the effective trapping state density when the depletion region is only partially extended into the grain. Baccarani [17] modified Seto's work to include the possibility that traps may be only partly filled when grains are partially depleted; however, this modification should be further extended to agree with the experimental data in the ρ versus N (Fig. 3) and mobility versus doping concentration (μ versus N) curves [4]. All of these works consider the barrier in polysilicon as a metal–semiconductor Schottky barrier, which does not explain the hyperbolic-sine I-V characteristic observed by Korsh [18] in lightly phosphorus-doped polysilicon and by Tarng [19] in oxygen-rich polysilicon films. Korsh and Tarng proposed a symmetrical semiconductor-to-semiconductor junction to explain this large-signal I-V behavior. Seager *et al.* [12], [20] studied the properties of a neutron-transmutation doped bulk-polysilicon ingot with a grain size of 100 μm, and similar results were obtained in their only partially depleted samples.

Because the ρ versus N and μ versus N behavior of large-grain polysilicon cannot be explained by existing models, a new modified trapping model is introduced in this paper; its preliminary results have been published [7]. Its demonstrated agreement with experimental data stems from its inclusion of the crystallite bulk effect, impurity level in the neutral region of the crystallite, and effective trapping state density instead of metallurgical traps. Correlation between small-signal resistivity and the large-signal I–V characteristic is observed at all doping levels, and the average carrier-concentration concept is used in interpreting Hall-measurement data. The modeling

parameters for a large-grain material have been determined from experiments, and their effect on the ρ versus N curve has been studied.

II. Experiment

A. Sample Preparation and Measurements

To measure resistivity and mobility accurately, ring-and-dot resistors, rectangular resistors, four-point probe pads, and Van der Pauw structures [2], [21] were used. Undoped 1.0- and 5.0-μm polysilicon films were deposited onto a 5000-Å SiO_2 layer thermally grown on p-type 10-Ω · cm ⟨100⟩-oriented silicon wafers. The deposition was done in an atmospheric-pressure CVD epitaxial reactor by H_2 ambient pyrolysis of silane at 1050°C with a deposition rate of 2700 Å/min. A 2000-Å layer of SiO_2 was thermally grown over the undoped polysilicon at 1050°C in a dry-wet-dry cycle. Boron doses ranging from 1×10^{12} to 8×10^{15} cm^{-2} were implanted with an energy of 135 keV through the oxide. Highly doped contacts spaced 5 to 550 μm apart were formed by implanting a 5×10^{14} cm^{-2} boron dose at 25 keV through windows opened in the SiO_2 layer. The wafers were then heated at 1100°C for 30 min in N_2 to anneal implantation damage and to ensure uniform dopant distribution. A 1.5-μm aluminum layer was deposited in an electron-beam system and defined over contact areas by etching. The contacts were alloyed at 450°C for 30 min in N_2.

Six runs were performed. The first included wafers with ring-and-dot resistors, four-point probe pads, and Van der Pauw structures which were cut into pieces for isolation and with no need to etch the polysilicon. Wafers for the next three runs had various dimensions of isolated rectangular resistors in addition to the above structures and required polysilicon etch for device isolation. The SiO_2 layer over polysilicon film was applied as a mask for etching and then was stripped off, and a new layer of oxide was grown at 1050°C for isolation and smooth step coverage. The second and third runs were the same and were used to check process tolerances. The third and fourth runs differed in that polysilicon was implanted with dopants after the polysilicon etch in the third but before the etch in the fourth, and the wafers oxidized after implantation in the fourth run were more resistive because of loss of dopants. The fifth run included polysilicon resistors in a bipolar process [22]; the resistor p^+ contacts were formed by following the boron predeposition and drive-in schedules. The 1-μm polysilicon film was used in these first five runs. The sixth was the same as the first except that the films were 5 μm thick. Each run had six to ten different implant doses, with one to three wafers per dose. The results reported here represent an average of measurements obtained from these samples, and more than 30 dies on each wafer were used. Data from the first run were compared to the theoretical calculations because possible leaching of dopants was minimum.

The thickness of the polysilicon film measured by the α-step profiler ranged from 0.96 to 1.10 μm for the first five runs and from 4.6 to 5.4 μm for the sixth run. The silicon consumed in the oxidation steps was estimated and checked during the process, and the final thickness of the sample was used in the calculations of doping concentration. In the 1-μm layers, this concentration was determined from the implant dose by assuming a uniform dopant distribution. In the 5-μm films, the thickness of the doped layer was measured by the spreading-resistance technique. The grain size was measured from transmission electron microscopy (TEM). The distributions of grain size for various doses were studied in detail via both the dark-field and bright-field methods [14]. Dark-field microscopy revealed a diffraction pattern only in certain crystal orientations from which the grain configuration can be well defined (Fig. 2). Grain area and size were determined, assuming cubic structures. Fig. 4 is an example of the results obtained. The average grains were approximately 2400 and 5000 Å in the 1- and 5-μm films, respectively; however, they were most frequently observed to be smaller than this average and, in the 1-μm film, they were approximately 1700 Å.

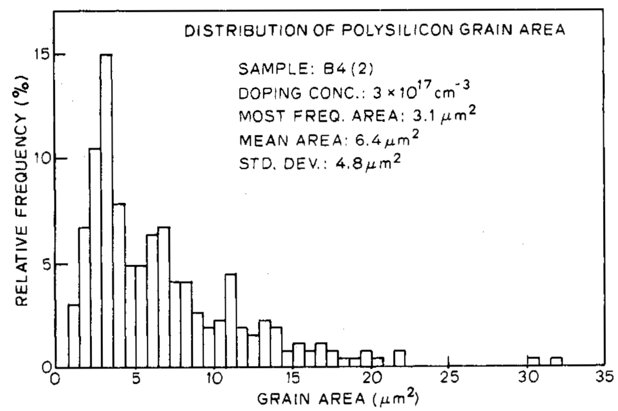


Fig. 4. Statistical distribution of the grain area of a 1-μm polysilicon film. 269 grains were used in this sample.

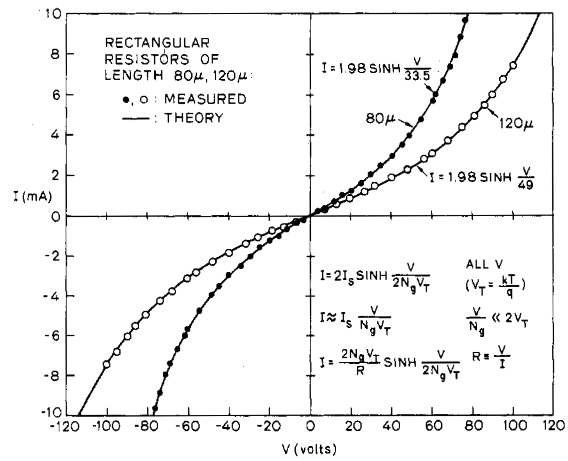


Fig. 5. Theoretical and experimental I–V characteristics of polysilicon resistors. The I–V function for the 80-μm resistor can be obtained from that of a 120-μm device by proper scaling.

Electrical measurements included the I–V characteristic, resistivity, and Hall voltage. The I–V data were obtained by means of a measurement system having a current sensitivity of better than 10 pA over a voltage range from −100 to 100 V. A hyperbolic-sine I–V characteristic (Fig. 5) was observed in all doping ranges for both ring-and-dot and rectangular resis-

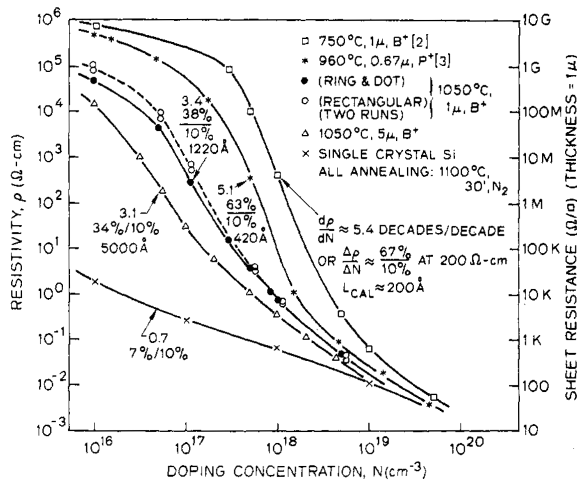


Fig. 6. Measured room-temperature resistivity versus doping concentration of polysilicon films with various grain sizes. The slope at 200 Ω · cm in each curve is expressed by both decades/decades and percentage change versus 10-percent variation in doping concentration. The calculated grain size L_{cal} is shown for comparison.

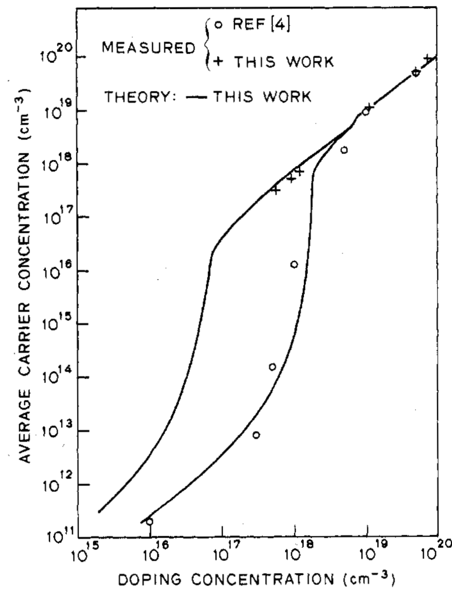


Fig. 7. Measured and theoretical average carrier concentration versus doping concentration of polysilicon films with different grain sizes.

tors of various dimensions [23]. Resistivity was always measured over the linear *I-V* range with small applied bias. Sheet resistance, especially for the high-value resistor, is difficult to obtain from our Hall setup and was calculated, therefore, from measured resistance and device geometry [21]. Contact resistance, lateral diffusion of contact dopants, and actual width were determined using resistors with different dimensions [21]. All measurements were performed over a temperature range of 25° to 144°C.

Hall measurements of Van der Pauw structures were obtained at room temperature in a standard ASTM setup [24]. A permanent magnet with a magnetic field of 1 kG was used. For each measurement, the polarities of the injected current and magnetic field were reversed, and the value of the Hall voltage was averaged over four readings. *I-V* linearity was verified frequently. The highly doped edges ensured good ohmic contact between the probes and sample; however, in samples with a doping concentration of less than 5×10^{17} cm^{-3}, the resistance across them was too high and degraded measurement accuracy below acceptable levels in our Hall setup. In the basic equations [24], [25] required to calculate the mobility and carrier concentration from Hall measurements, the constant $3\pi/8$ [16], [25] was used for the nondegenerate samples (low or medium doping concentrations at medium or high temperatures, such as $<6.5 \times 10^{18}$ cm^{-3} for boron at room temperature) and a unity was used in the degenerate samples (low temperature and very high doping concentrations, such as $>6.5 \times 10^{18}$ cm^{-3} for boron in single-crystal silicon) [25].

B. Results

Measured room-temperature ρ versus N curves and the data obtained for polysilicon deposited at lower temperatures [4], [8] are presented in Fig. 6. The ρ versus N curve corresponding to the smallest grain is on the right and shifts to the left as size slightly increases. For the smallest grain at a resistivity of 200 Ω · cm, a resistivity change of approximately 67 percent is observed for a 10-percent variation in doping concentration which, on a logarithmic scale, corresponds to a change of 5.4 decades in resistivity for only a 1-decade variation in doping concentration. A more moderate 38-percent change in resistivity for a 10-percent deviation in dose (3.4 decades/decade) is achieved with larger grain polysilicon films formed by a higher deposition temperature. Resistors fabricated in a bipolar process (the sixth run) indicated that more than 85 percent of devices across a 2-in wafer had a sheet-resistance spread of ±8 percent at a value of 2.6 MΩ/□. Preliminary results showed less than ±30-percent variations in absolute sheet resistance between wafers and demonstrated that greater reproducibility can be obtained under tighter process control.

Fig. 7 is a plot of average carrier concentration $\bar{p}$ versus doping concentration N obtained from the data of this work and by Seto [4]. In lightly doped samples $\bar{p} \ll N$ because most carriers are trapped. As N increases, the traps are filled and $\bar{p}$ approaches the ionized doping concentration N^+. At higher doping, it is interesting to compare the ratio of $\bar{p}$ to N (Table I) to that of single-crystal silicon [25]. The same tendency is observed that demonstrates the partial-ionization effect of dopants as a result of the existence of an impurity level, which is more important than the trapping effects in highly doped material. For $N > 5 \times 10^{18}$ cm^{-3}, $\bar{p}$ is roughly equal to N and resistivity is almost independent of temperature, which support the predictions of degeneracy.

Hole mobility is plotted in Fig. 8. For large grains, the mobility minimum occurs at less than 5×10^{17} cm^{-3} which is lower than that in small grains [4].

Fig. 9 is a plot of the linear least mean square approximation to the resistivity data normalized by the resistivity at 144°C versus $1/kT$. The slope of the approximation increases as the doping concentration is reduced [4]. Data for ρ versus N at 25°, 71°, and 144°C are plotted in Fig. 10. The slope of this curve becomes smaller at higher temperatures and moves toward the single-crystal curve.

III. Theory

Polysilicon material is a three-dimensional substance with grains having a distribution of sizes and irregular shapes (Fig.

TABLE I
ROOM-TEMPERATURE CARRIER CONCENTRATIONS FOR SIX SAMPLES WITH DIFFERENT DOPING CONCENTRATIONS
(Unit: cm^{-3})

Doping Concentration	Measured p	Calculated N^+	Calculated p
5×10^{17}	3.0×10^{17}	4.4×10^{17}	3.6×10^{17}
8×10^{17}	5.1×10^{17}	6.8×10^{17}	6.1×10^{17}
1×10^{18}	7.1×10^{17}	8.4×10^{17}	7.8×10^{17}
5×10^{18}	4.1×10^{18}	3.96×10^{18}	3.9×10^{18}
1×10^{19}	9.9×10^{18}	1.0×10^{19}	9.99×10^{18}
5×10^{19}	6.0×10^{19}	5.0×10^{19}	5.0×10^{19}

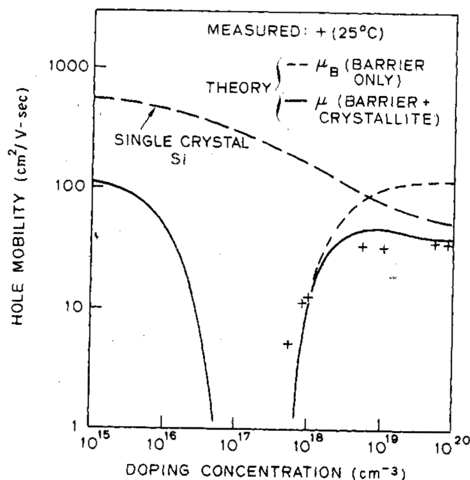


Fig. 8. Measured and theoretical hole mobility versus doping concentration of a polysilicon film with a grain size of 1220 Å. The dashed line indicates the calculation without including crystallite bulk mobility.

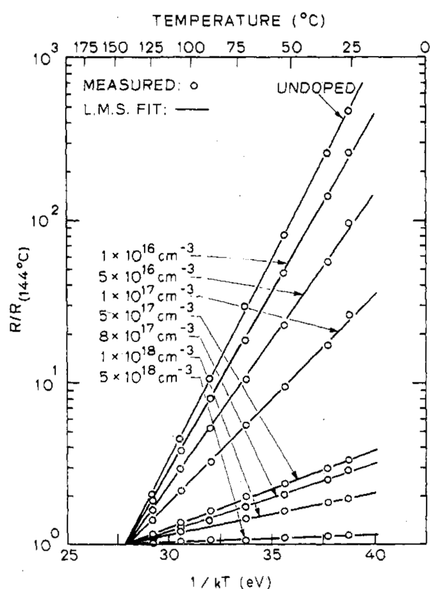
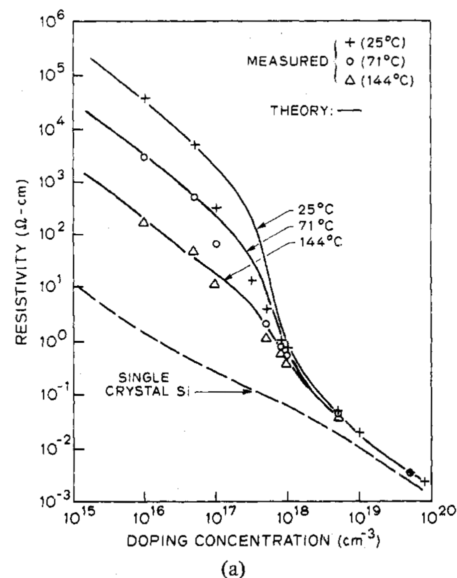
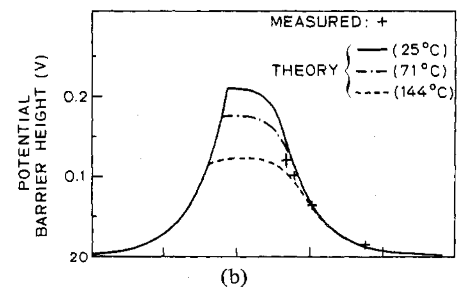


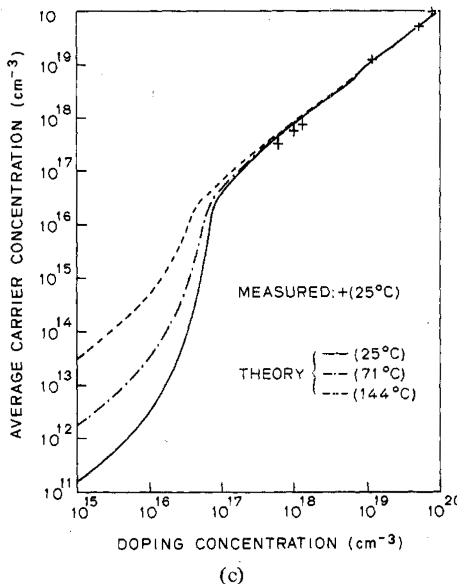
Fig. 9. Measured resistivity versus $1/kT$ for samples with different doping concentrations over a temperature range from 25° to 144°C. The solid lines denote the linear least mean square approximations to the data.



(a)



(b)



(c)

Fig. 10. The model applied to different temperatures. (a) Measured and theoretical resistivity versus doping concentration. (b) Corresponding potential barrier versus doping concentration. (c) Average carrier concentration versus doping concentration.

2). For simplicity, we assume that polysilicon is composed of identical cubic grains with a grain size L and that its transport properties are one-dimensional (Fig. 11). The applied voltage V_a over all N_g grains between two resistor contacts is assumed to be equally dropped across all grains (grain voltage is $V_g = V_a/N_g$). The single-crystal silicon energy-band structure is applicable inside the crystallites. For convenience, the intrinsic Fermi level E_{i0} at the center of the grain is chosen to be a

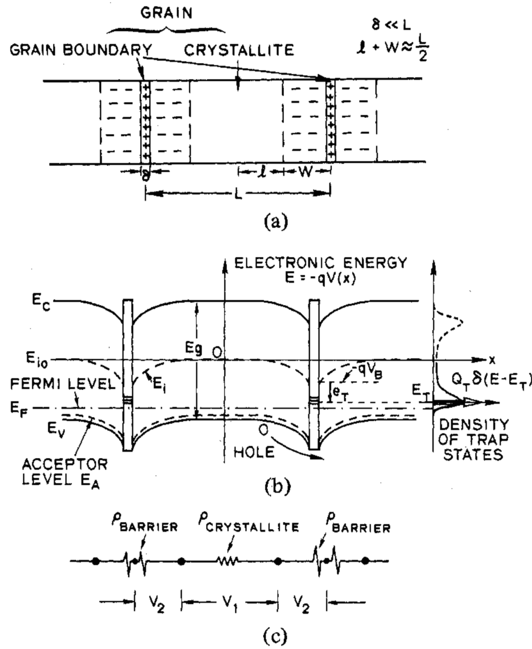


Fig. 11. The modified polysilicon trapping model. (a) One-dimensional grain structure. (b) Energy-band diagram for p-type dopants. (c) Grain boundary and crystallite circuit. Only the partially depleted grain is shown. When completely depleted, there is no neutral region and the depleted region extends throughout the grain. When undoped, there is no depleted region and the Fermi level is believed to lie near the middle of the band gap.

zero electronic energy; the energy is positive for upward and negative for downward direction. The grain boundary is of thickness δ which is much smaller than L and contains Q_T traps that are initially neutral and become charged at a certain monoenergetic level E_T referred to E_{i0} after trapping the carriers.

A. Undoped (Nearly Intrinsic) Material

It is generally believed [12], [16], [19] that the chemical potential of polysilicon grain boundaries lies somewhere near the middle of the forbidden band gap. If no intentional dopant impurities are added into the deposited polysilicon film, the energy band is relatively uniform throughout the film; therefore, other than grain-boundary effects, its behavior is similar to that of a uniform intrinsic single-crystal silicon. The resistivity of polysilicon ρ, therefore, is

$$\rho = \rho_C \left(1 - \frac{\delta}{L}\right) + \rho_{GB} \left(\frac{\delta}{L}\right) \tag{1}$$

where ρ_{GB} is resistivity as a result of the grain boundary, and ρ_C is the single-crystal resistivity described by [26]

$$\rho_C = \frac{1}{qn_i(\mu_n + \mu_p)} \tag{2}$$

where μ_n and μ_p are electron and hole mobilities, and the intrinsic carrier concentration n_i is [26]

$$n_i = 2\left(\frac{2\pi kT}{h^2}\right)^{3/2} (m_e^* m_h^*)^{3/4} \exp(-E_g/2kT) \tag{3}$$

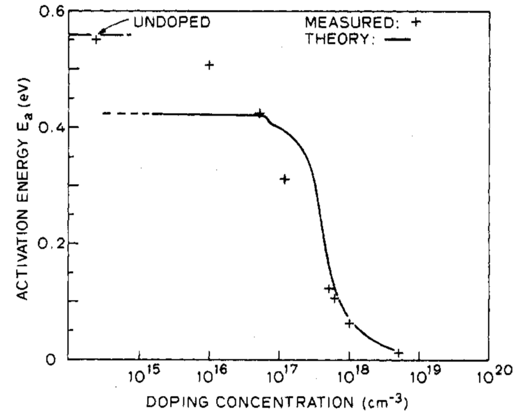


Fig. 12. Experimental and theoretical activation energy versus doping concentration.

where the forbidden band gap of silicon E_g is [26]

$$E_g = 1.16 - \frac{7.02 \times 10^{-4} T^2}{T + 1108}. \tag{4}$$

B. Doped Material

When polysilicon film is doped with one type of impurity, most dopants enter the crystallite lattice substitutionally and are assumed to be uniformly distributed throughout the film after subsequent thermal treatment. An impurity level is formed inside the crystallites, and impurity atoms are ionized to create majority mobile carriers [25]. The traps in the grain boundary charged by trapping mobile carriers deplete the regions in the crystallites, and potential barriers are thereby formed on both sides of the grain boundary (Fig. 11(b)). For simplicity, the depletion approximation, which assumes that mobile carriers are neglected and that impurity atoms are totally ionized in the depleted region, is used to calculate the energy-band diagram. Poisson's equation becomes [4]

$$\frac{d^2 V}{dx^2} = \frac{qN}{\epsilon}, \quad l \leqslant |x| \leqslant \frac{L}{2}. \tag{5}$$

By integrating this equation twice and using the boundary conditions that $V(x)$ is continuous and that $dV/dx = 0$ at $x = l$, the potential $V(x)$ is

$$V(x) = \pm \frac{qN(x - l)^2}{2\epsilon}, \quad l \leqslant x \leqslant \frac{L}{2}. \tag{6}$$

The potential barrier height V_B is the difference between $V(L/2)$ and $V(0)$; that is

$$V_B = \pm \frac{qNW^2}{2\epsilon} \tag{7}$$

where + denotes p-type dopants and - indicates the n-type, and W is the depletion-region width $(L/2 - l)$. The following sections focus on p-type dopants; however, similar results can be derived for n-types.

1) Resistivity and Mobility: polysilicon resistivity is composed of three serial components; one is the result of the potential barrier, and the second is the bulk resistivity of the

crystallite. The third component represents the actual grain boundary and is negligible because of the very narrow boundary width [4], [27]. Barrier conductivity is the consequence of two components—thermionic emission and field emission across the barrier. Thermionic emission results from those carriers with an energy high enough to surmount the potential barrier; field emission stems from carriers with less energy than the barrier but capable of tunneling quantum mechanically through the barrier. For simplicity, only the barrier conductivity from thermionic emission is derived. The study of field emission is described in [28]. The bulk resistivity of the crystallite neutral region, resulting from lattice and impurity scatterings, is equal to the resistivity of single-crystal silicon [29], [30].

Thermionic-emission theory for metal-semiconductor Schottky barriers demonstrates [26] that

$$J = qp(0)\left(\frac{kT}{2\pi m_h^*}\right)^{1/2} \exp(-qV_B/kT) \cdot [\exp(qV/kT) - 1] \tag{8}$$

where $p(0)$ is the hole concentration in the equilibrium neutral region [17] expressed [26] as

$$p(0) = n_i \exp(-E_F/kT) \tag{9}$$

where E_F is the Fermi level with respect to E_{i0}. In polysilicon, however, semiconductor material exists on both sides of the barrier. Rather than the metal-semiconductor junction used in some earlier models [4], [17], therefore, grain-boundary barriers are considered in these derivations as a symmetrical semiconductor-to-semiconductor junction [18], [19]. The grain voltage is dropped on both the barriers and crystallite bulk. The voltage across the barrier V_{ba} is assumed to be equally divided on each side of the junction, and the transport equation, therefore, becomes [18], [19]

$$J = 2qp(0)\left(\frac{kT}{2\pi m_h^*}\right)^{1/2} \exp(-qV_B/kT) \sinh\left(\frac{qV_{ba}}{2kT}\right) \tag{10}$$

where $p(0)$ is the hole concentration at the center of the grain, as defined in (9). If $V_{ba} \ll 2kT/q$, then

$$J \approx q^2 p(0)\left(\frac{1}{2\pi m_h^* kT}\right)^{1/2} \exp(-qV_B/kT) V_{ba}. \tag{11}$$

Over this linear J-V range, barrier resistivity ρ_B (defined as the electric field divided by current density) is

$$\rho_B = \frac{V_{ba}}{J(2W)} = \frac{1}{2Wq^2 p(0)} (2\pi m_h^* kT)^{1/2} \exp(qV_B/kT). \tag{12}$$

Similarly, crystallite bulk resistivity is

$$\rho_C = \frac{V_c}{J(L - 2W)} \tag{13}$$

where V_c is the voltage across the crystallite neutral region. Total resistivity ρ, which includes ρ_B and ρ_C, is

$$\rho = \frac{V_g}{JL} = \rho_B\left(\frac{2W}{L}\right) + \rho_C\left(1 - \frac{2W}{L}\right). \tag{14}$$

Substituting (12) into this equation results in a general expression for polysilicon resistivity.

Interpretation of carrier mobility in the nonhomogeneous polysilicon material is based on the assumption that an effective mobility μ_{eff} exists such that

$$\rho = \frac{1}{q\bar{p}\mu_{\mathrm{eff}}}. \tag{15}$$

The average carrier concentration $\bar{p}$ is defined as

$$\bar{p} = \frac{\int_{-L/2}^{L/2} p(x)\,dx}{L} \tag{16}$$

and $p(x)$ is the carrier concentration at point x determined by Maxwell-Boltzmann statistics [26] to be

$$p(x) = n_i \exp\left[\frac{-qV(x) - E_F}{kT}\right]. \tag{17}$$

The validity of μ_{eff} was demonstrated by Seto [4] for small grains and, in this work, for either small or large grain sizes. By combining (14) and (15), μ_{eff} (including both barrier and bulk mobilities) can be obtained.

2) Calculations of W, V_B, E_F, $p(0)$, and $\bar{p}$: This section derives the quantities W, V_B, E_F, $p(0)$, and $\bar{p}$ required for the calculation of ρ and μ_{eff}. For small bias, E_F is assumed to be constant throughout the grain. The effective trapping state density Q_T^+ (the ionized trap density in the grain boundary) is related to the number of metallurgical traps Q_T through the Fermi-Dirac statistics at temperature T as follows [4], [31]:

$$Q_T^+ = \frac{Q_T}{1 + 2\exp(E_F - E_T)/kT}. \tag{18}$$

The degeneracy factor is 2 because the traps are assumed to be identical and without interaction, and each can trap one hole of either spin. It is also assumed that E_T is located at a constant energy e_T with respect to E_i at the grain boundary, which is bent down by $-qV_B$ with respect to E_{i0}; therefore,

$$E_T = e_T - qV_B. \tag{19}$$

Using the above two equations and the charge-neutrality condition, which equates the number of ionized dopants in the depletion region to the number of charged traps, results in

$$2NW = \frac{Q_T}{1 + 2\exp[(E_F - e_T + qV_B)/kT]}. \tag{20}$$

Because Q_T^+ and L are finite, a certain doping concentration N^* exists for which the grains are totally depleted if $N \leqslant N^*$ $(2W = L)$; otherwise, the grains are only partially depleted $(2W < L)$. At $N = N^+$, the Fermi level is not yet perturbed

from that in the neutral region and is

$$E_F = -kT \ln \left(\frac{N^*}{n_i}\right). \tag{21}$$

Based on (7), (20), (21), and $2W = L, N^*$ is iteratively determined[1] as

$$N^* = \frac{Q_T}{L} - 2n_i \exp(-e_T/kT) \exp(q^2 N^* L^2/8\epsilon kT). \tag{22}$$

Completely Depleted Region, $N \leqslant N^*$: When $2W = L$, and from (7)

$$V_B = \frac{qNL^2}{8\epsilon}. \tag{23}$$

From (20), E_F is determined to be

$$E_F = e_T - qV_B + kT \ln \left[\frac{1}{2}\left(\frac{Q_T}{LN} - 1\right)\right] \tag{24}$$

and, based on (6), (16), and (17), the average carrier concentration is

$$\bar{p} = n_i \exp(-E_F/kT) \left\{\left(\frac{1}{qL}\right)\left(\frac{2\pi\epsilon kT}{N}\right)^{1/2} \cdot \operatorname{erf}\left[\frac{qL}{2}\left(\frac{N}{2\epsilon kT}\right)^{1/2}\right]\right\} \tag{25}$$

which, when compared to Seto's derivation [4], demonstrates that Seto overestimated $\bar{p}$ by a factor of $\exp(qV_B/kT)$.

Partially Depleted Region, $N > N^*$: In midrange of the doping concentrations at medium and high temperatures for which silicon is nondegenerated [25], the crystallite has both depletion and neutral regions. In the neutral region, the ionized impurity concentration N^+ at temperature T [26], [31] is

$$N^+ = \frac{N}{1 + 2\exp[(E_A - E_F)/kT]} \tag{26}$$

where E_A is the acceptor impurity level within the forbidden band gap and, for boron, is [25]

$$E_A = \frac{-E_g}{2} + 0.08 - 4.3 \times 10^{-8} N^{1/3}. \tag{27}$$

Combining (9), (26), and the condition $p(0) = N^+$ yields

$$n_i \exp(-E_F/kT) = \frac{N}{1 + 2\exp[(E_A - E_F)/kT]} \tag{28}$$

and determines E_F. By using (7), (9), (20), and $p(0) = N^+$, W can be calculated by numerical iteration as follows:

$$W = \frac{Q_T}{2N[1 + 2(n_i/N^+)\exp(-e_T/kT)\exp(q^2NW^2/2\epsilon kT)]} \tag{29}$$

which is significantly different from the corresponding expression obtained by Seto [4] who implicitly stated that $W = Q_T/2N$. This difference is a result of the discrepancy between Q_T used by Seto and Q_T^+ in this work. In a medium-doping concentration and for a large grain size (>400 Å), Q_T^+ becomes much smaller than Q_T. If Q_T is used rather than Q_T^+, N^* is much larger than that calculated in (22), and a discontinuity occurs near N^* in the ρ versus N curve (Fig. 3). After W is determined, the average carrier concentration becomes

$$\bar{p} = n_i \exp(-E_F/kT) \left\{\left(1 - \frac{2W}{L}\right) + \left(\frac{1}{Lq}\right)\left(\frac{2\pi\epsilon kT}{N}\right)^{1/2} \cdot \operatorname{erf}\left[qW\left(\frac{N}{2\epsilon kT}\right)^{1/2}\right]\right\}. \tag{30}$$

In a very heavy doping concentration (such as $\geqslant 6.5 \times 10^{18}$ cm^{-3}) of boron in silicon, the conduction and impurity bands overlap and the sample degenerates [25], [26]. Because most impurity atoms are ionized and the depletion region becomes very narrow, the approximation $\bar{p} \approx p(0) \approx N$ is sufficient. The Fermi energy level can be calculated using the Fermi integral instead of the Maxwell-Boltzmann approximation [26], [32].

IV. Comparison Between Theory and Experiments

To compare theory to experimental results, it is necessary to determine m_h^*, ϵ, n_i, E_g, E_A, L, Q_T, and e_T. The values of single-crystal silicon are assumed in the first five parameters [33]. Equations (3) and (4) were used to calculate the temperature effect of n_i and E_g, respectively, and (27) derived the doping dependence of E_A for boron; L was determined by TEM measurements and from I-V characteristics, and Q_T and e_T were obtained from the ρ versus $1/kT$ curves.

A. Undoped Samples

Because the behavior of the ρ versus $1/kT$ curves in Fig. 9 is nearly Arrhenius [34] from 25° to 144°C for undoped and all-doped samples, an activation energy of ρ versus $1/kT$ can be defined as

$$E_a = \frac{\partial(\ln \rho)}{\partial(1/kT)}. \tag{31}$$

Experimental E_a versus N is shown in Fig. 12. For undoped samples, it is assumed that μ_n and μ_p are proportional to $T^{-3/2}$ [30]. By neglecting the ρ_{GB} term in (1), $E_a \approx E_g/2$. In silicon, $E_g \approx 1.12$ eV. For an undoped sample, therefore, E_a is predicted to be 0.56 eV which is in good agreement with the experimental value of 0.55 eV. In addition, at $T = 300°C$, $n_i = 1.45 \times 10^{10}$ cm^{-3}, $\mu_n = 1400$ $cm^2/(V \cdot s)$, and $\mu_p = 525$ $cm^2/(V \cdot s)$ [33], ρ_c is calculated as 2.3×10^5 $\Omega \cdot cm$. The experimental resistivity of undoped polysilicon, which depends on deposition conditions and grain size, is approximately 2 to 8×10^5 $\Omega \cdot cm$.

B. Doped Samples

The distribution of grain size by dark-field TEM was studied in Section II-A [14], and L was derived in (10) as follows. Both the small- and large-signal I-V characteristics were deter-

[1] The partial ionization of dopants is not taken into account because N^* generally occurs in a medium-doped range where the difference can be neglected so as to yield an analytical solution.

mined for rectangular resistors with doping concentrations of 1×10^{18} cm^{-3} and lengths of 80 and 120 μm (Fig. 5). Because measured resistivity is much higher than that of single-crystal silicon, grain voltage is assumed to drop across the barriers ($V_{ba} \approx V_g = V_a/N_g$). Equation (10) can now be rewritten as

$$I = JA = 2I_s \sinh\left(\frac{qV_a}{2N_gkT}\right) \tag{32}$$

where A is the cross-section area of the resistor, and I_s is the pre-sinh factor in (10) multiplied by A. If $V_a/N_g \ll 2kT/q$, resistance $R = V/I$ at small bias becomes $R \approx N_gkT/qI_s$. By eliminating I_s from the above

$$I \approx \left(\frac{2N_gkT}{qR}\right) \sinh\left(\frac{qV_a}{2N_gkT}\right). \tag{33}$$

As a result, N_g can be determined by measuring R at T and using (33) to fit the large-signal I-V data, and so L is obtained from the length between the two resistor contacts divided by N_g. The number of grains is in good proportion to resistor length, which supports our assumption that the transport in polysilicon is nearly one dimensional through cubic grains. The hyperbolic-sine I-V characteristic observed in ring-and-dot structures, however, indicates that the number of grains is not directly proportional to the length between the two contact rings because the conduction in these devices under large bias may be two-dimensional in contrast to one-dimensional in rectangular resistors. It was found that $L \approx 1220$ Å which is smaller than the average grain size but close to most values observed by TEM (Fig. 4); a small deviation occurs in different doping concentrations.

The parameters Q_T and e_T are determined as follows. For $N \leqslant N^*$, inserting (3), (9), (24), and $2W = L$ into (12) results in

$$\rho \propto T^{-1} \exp\left[\frac{(E_g/2) + e_T}{kT}\right] \tag{34a}$$

and, from (31)

$$E_a \approx \frac{E_g}{2} + e_T + kT. \tag{34b}$$

For $N > N^*$, the following conditions are considered:

1) If N is near N^*, $Q_T^+ \ll Q_T$, V_B becomes a complicated function of temperature as does ρ, and E_a cannot be expressed in a useful analytical form.

2) When N increases, $Q_T^+ \approx Q_T$ and $p(0)$ becomes a weak function of temperature. From (12)

$$\rho \propto T^{1/2} \exp(qV_B/kT) \tag{35a}$$

and, from (31)

$$E_a \approx qV_B - \tfrac{1}{2}kT. \tag{35b}$$

3) If the sample is more heavily doped, the resistivity contains barrier and bulk components and, therefore, its temperature behavior is affected by both components.

The experimental data demonstrate that condition 2) ranges from 5×10^{17} to 1×10^{18} cm^{-3} and is suitable for determining Q_T. The activation energy for $N = 5 \times 10^{17}$, 8×10^{17}, and 1×10^{18} cm^{-3} produces V_B from (35) and then W from (7). Based on $Q_T \approx Q_T^+ = 2NW$, Q_T can be determined at each doping level, respectively (Table II), and an average value of 1.9×10^{12} cm^{-2} was selected. The first-order estimation of e_T was obtained from the E_a of samples where $N = 1 \times 10^{16}$, 5×10^{16}, and 1×10^{17} cm^{-3} from (34) (Table II), and an average value of -0.17 eV was chosen. (Calculated N^* at room temperature is approximately 7.3×10^{16} cm^{-3}. Although $N = 1 \times 10^{17} > N^*$, its E_a is not far from the completely depleted conditions and still is applied for estimating e_T.) Because L and Q_T have been determined, the value of e_T was adjusted to produce the best fit of the ρ versus N, μ versus N, and ρ versus $1/kT$ curves; this is equivalent to Seto's method where $\bar{p}$ was used in the completely depleted samples to obtain that value.

TABLE II
TRAPPING STATE ENERGY AND DENSITY OF SAMPLES WITH DIFFERENT DOPING CONCENTRATIONS

N (cm^{-3})	E_a (eV)	e_T (eV)	Q_T (cm^{-2})
1×10^{16}	0.51	-0.076	—
5×10^{16}	0.43	-0.156	—
1×10^{17}	0.32	-0.266	—
5×10^{17}	0.115	—	1.8×10^{12}
8×10^{17}	0.10	—	2.1×10^{12}
1×10^{18}	0.060	—	1.9×10^{12}

After the parameters are determined, data for ρ versus N and μ versus N can be more accurately modeled by introducing f into (12) as follows:

$$\rho_B = \frac{1}{f} \frac{1}{2Wq^2p(0)} (2\pi m_h^* kT)^{1/2} \exp(qV_B/kT). \tag{36}$$

Fig. 13 is a flow chart of the computer program for this modeling, and the parameter values chosen to fit the data are listed in Table III. An artificial factor n used by Seto [4] and in [7] is not required in (36) to model the ρ versus N curve above room temperature because, based on thermionic theory [17], [26], $p(0)$ is used instead of $\bar{p}$. By comparing (9) to (25) or (30), it can be seen that, in the near N^* region, $p(0)$ is particularly larger than $\bar{p}$ which causes ρ to be much smaller than that calculated by use of $\bar{p}$ which is equivalent to the function of the n factor. Calculation of $\bar{p}$, however, is still helpful in interpreting effective mobility and in observing how traps reduce the number of mobile carriers. The reduction of carriers in lightly and medium-doped ranges is mostly the result of traps but, in the highly doped regions, the partial ionization of dopants caused by the existence of an impurity level becomes more important. For example, at a doping level of 1×10^{18} cm^{-3}, approximately 16 percent of the dopants are unionized, but less than 10 percent of the carriers are trapped at room temperature. This effect becomes significant at lower temperatures and, in addition to the segregation effect [17], it contributes to the smaller carrier concentration

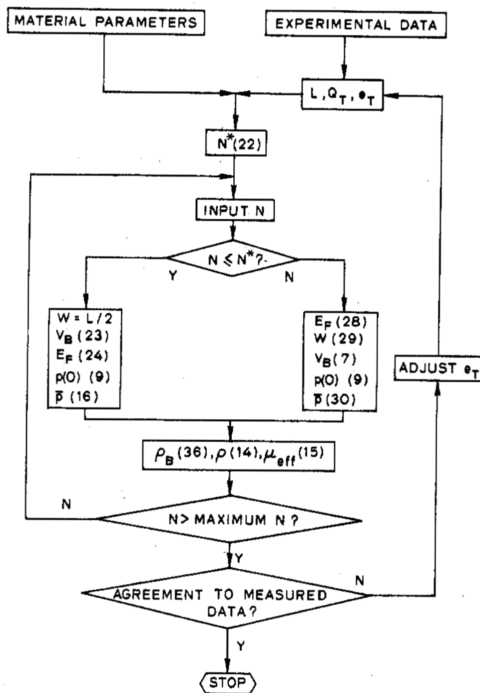


Fig. 13. Flow chart of the computer program for the model. Numbers within the parentheses refer to the equations in text.

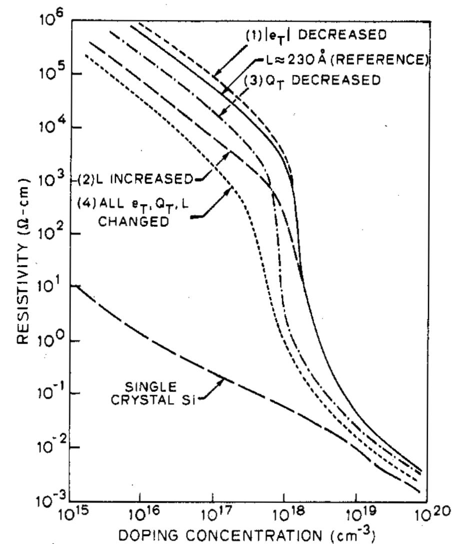


Fig. 14. Influence of e_T, L, and Q_T on the slope of room-temperature resistivity versus doping concentration. The curve for Seto's data [4] is used as a reference, and its parameter values are listed in Table III. Curve (1) shows the $|e_T|$ change from 0.18 to 0.17 eV; curve (2) results from increasing L from 230 to 1220 Å, and curve (3) is obtained by reducing Q_T from 3.34×10^{12} to 1.9×10^{12} cm^{-2}. In these plots, $f = 0.12$ and single-crystal resistivity is included. Curve (4) is based on the parameter values for our data in Table III, and $f = 0.06$.

TABLE III
PARAMETER VALUES TO FIT DATA OF POLYSILICON FILMS WITH DIFFERENT GRAIN SIZES

Data Source From	e_T (eV)	Q_T (cm^{-2})	L (Å)	f
Ref. 4	-0.18	3.34×10^{12}	230	0.12
This work	-0.17	1.9×10^{12}	1220	0.060

than doping concentration in highly doped samples.

The theoretical μ versus N curve in Fig. 8 demonstrates the importance of the crystallite bulk mobility. In the range of $N < N^*$ in Fig. 12, the calculated almost constant E_a is not in accord with the experimental E_a which increases up to 0.55 eV as the doping concentration reduces to the intrinsic conditions.[2] This is because the trapping states are assumed to have a δ-shaped distribution; however, in the real substance, these states must have some type of distribution over an energy range. In addition, the simplified assumptions that all grains are of the same size and become completely depleted at the same N^* and that the abrupt depletion approximation is used to derive the energy band cause the calculated values to deviate from the data, especially around N^*.

The effect of grain size on the electrical properties of polysilicon is shown in Table III. The trapping state energy remains approximately at the same level as the grain size varies, and Q_T reduces with increasing grain size. This can be expected as a result of a drop in the degree of disorder in the material as it changes from polycrystalline toward single crystal. The sensitivity of the ρ versus N curve in Fig. 1 also decreases as grain size increases; it is instructive to use this model to determine the influence of the material parameters on the slope. In Fig. 14, the solid line plots the theoretical results for Seto's data [4] for reference. It can be seen that the slope of curve (1) becomes worse as $|e_T|$ changes from 0.18 to 0.17 eV. As L increases from 220 to 1220 Å in curve (2), ρ decreases in the completely depleted region and the slope falls; in curve (3), ρ drops mainly in the partially depleted region as Q_T is reduced from 3.34×10^{12} to 1.9×10^{12} cm^{-2}. If Q_T and L change at the same time as does curve (4) and the crystallite bulk effect is added, the slope of ρ versus N falls sharply.

The artificial factor f, which increases ρ by $(1/f)$ times with respect to the calculated values, requires further investigation; one of the first steps is to study its temperature behavior. Assuming that Q_T, e_T, and L are temperature independent and based on the temperature effect of n_i and E_g in (3) and (4) and the slight variations in ρ_C [29], [30], the theoretical results of the ρ versus N curves in Fig. 10 demonstrate the validity of the model over a wide temperature range. It is also found that f is almost temperature independent. Because the calculated and measured $\bar{p}$ and V_B are in good agreement, the increases in ρ as a result of f cannot be attributed to segregation or modeling inaccuracy. In addition, the doping concentration is too low to cause localization or clustering of dopants. Two explanations are possible. One is that the effective Richardson constant (effective hole mass) is much smaller than in the single crystal, which may occur in such disordered structures as polysilicon. The second is that some transmission probability exists when carriers pass

[2]Because of the mistake in Seto's derivation [4], his theoretical curve in Fig. 9 shows an erroneous prediction in the range of $N < N^*$. The sharp change of E_a versus N near N^* in [17] is eliminated by exact computer calculations.

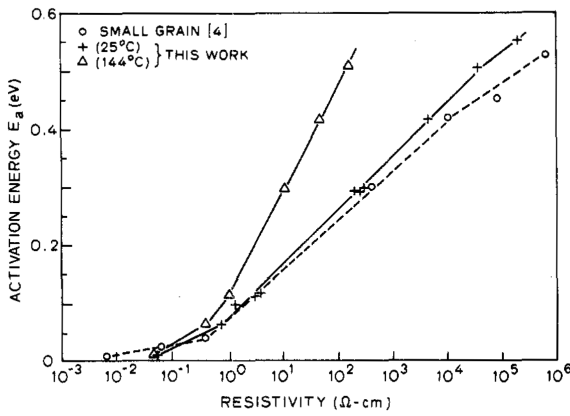


Fig. 15. Measured activation energy versus resistivity of polysilicon films with different grain sizes at 25° and 144°C.

through the complicated grain boundary by either scattering or recombination.

V. Design Criteria

Based on the experimental success of the modified trapping model, the following criteria to optimize resistivity control, linearity, and temperature sensitivity in the design of polysilicon resistors [2], [23] are discussed in this section.

For good resistivity control, grain size must be increased.

For high linearity, V_g must be small. Polysilicon resistors are nonlinear as $V_g \approx 2kT/q$. Although the nonlinearity of an 80-μm resistor becomes appreciable above 30 V (Fig. 5), the same nonlinearity appears even at 2 V in a 5-μm resistor by proper scaling [23]. Because $V_g = V_a/N_g$, a lower applied bias across the resistor, a longer resistor, or a smaller grain size can reduce V_g to enhance linearity. The voltage coefficient ratio of resistance (VCR) is defined and used for quantitative characterization of linearity; that is

$$\mathrm{VCR} \equiv \frac{dR/R}{dV/V} = 1 - \frac{qV_g}{2kT} \coth \frac{qV_g}{2kT} \tag{37}$$

For less temperature dependence, resistivity must be lowered. From the nearly Arrhenius behavior of ρ versus $1/kT$, the curve of E_a versus ρ should be a straight line when $\rho_B \gg \rho_C$ and the slope is $\approx kT$. Fig. 15 plots the experimental results obtained from six runs and data from Seto [4] at 25° and 144°C. This demonstrates that, independent of the polysilicon-resistor fabrication process, a specific ρ has a specific E_a; for higher ρ, E_a is larger. The matching of polysilicon resistors with respect to the operating temperature is comparable to diffused resistors over the above temperature range. In applications where resistivity ratio matching [35] or the absolute value [3] is critical, E_a can be suitably selected based on the specified resistivity variations over the operating temperature range and Figs. 9 and 15 to reduce circuit-temperature sensitivity and, therefore, to optimally determine ρ.

For low-temperature sensitivity, V_g must be large. If the resistors are operated over a nonlinear range, V_g becomes a factor in addition to E_a. The dc temperature-coefficient ratio $\mathrm{TCR_{dc}}$ is defined as $\mathrm{TCR_{dc}} = (1/R)\,(dR/dT)$ which shows that TCR depends on E_a and V_g. In a partially depleted region where $p(0)$ is independent of T and $V_{ba} \approx V_g$

$$\mathrm{TCR_{dc}} = -\frac{1}{T}\left[\frac{qV_B}{kT} + \frac{1}{2} - \frac{qV_a}{2N_gkT} \coth\left(\frac{qV_a}{2N_gkT}\right)\right]. \tag{38}$$

Because of a minus sign before the V_g term, TCR can be reduced by increasing V_g (raising V_a or reducing N_g) [2].

If the resistor is operated at higher temperatures, the sensitivity of ρ versus N will be improved (Fig. 10) and TCR can also be reduced in (37).

For good isolation, reduced parasitic effects, and less substrate bias dependence, the oxide underneath the resistor must be thick.

There are some tradeoffs, however, among these criteria. Large grain size can result in better resistivity control and a lower TCR but less linearity; high resistivity can save die area but produces larger temperature sensitivity. These criteria derived quantitatively from the model become important, therefore, in the optimization of resistor design.

VI. Conclusions

A modified trapping model for polysilicon with either small or large grain sizes under different applied voltages has been developed and has been successfully applied to p-type polysilicon. It is equally applicable to 0.67-μm thick n-type polysilicon films [7] where an electron trapping level exists at $\approx$0.2 eV above E_i at the grain boundary. In addition, because the postannealing electrical properties of low-pressure CVD (LPCVD) and atmospheric-pressure CVD polysilicon films are similar [8] and the modeling parameters are determined from experiments, the applicability of the model to thin LPCVD polysilicon films is feasible. It has also been demonstrated theoretically and experimentally that the long-existing problem of resistivity control can be solved by increasing the grain size and stabilizing the dopant distribution. In addition, criteria concerning temperature sensitivity and linearity have been established to optimize device design.

In this work, a high deposition temperature or thick polysilicon film was used to increase grain size. For LPCVD films or in some processes that cannot withstand high temperatures, laser annealing [21], [36], [37], the neutron-transmutation method for doping polysilicon to reduce Q_T and to lower the anneal temperature so as to avoid segregation [12], and hydrogen-plasma annealing to change Q_T [38] become attractive. For more critical control of resistivity, nitride instead of oxide can be used as the passivation layer to avoid boron leaching.

The model has the advantage of being analytical. It is somewhat inadequate, however, for the following reasons.

Although the δ-function approximation of trapping-state density obtains better results than does continuous distribution [12], [17], the assumption of a δ-shaped approximation limits the theoretical prediction that E_a versus N is constant when $N \leqslant N^*$, which is not in agreement with the experimental results. It is likely that the trapping states are distributed over a specific energy range. In our estimation, a Gaussian distribution with a small standard deviation is the most probable

solution because it maintains the results of the ρ versus N curves and increases E_a as N is reduced when $N \leqslant N^*$.

Our use of a single-value grain size is obviously not possible in the real material, especially when the size is larger than several micrometers. The effect of a wide distribution of grain sizes can be taken into account only by statistical modeling [39].

The assumption of the depletion approximation leads to inaccurate values of the barrier heights which may cause a large error near N^*, especially for a very large grain size [4] such as in polysilicon rods for solar-cell applications.

The grain-boundary resistivity, which is neglected in this work, may be important in very lightly or highly doped samples where the potential barrier effect becomes small.

Although thermionic field emission is very important at low temperatures [28], it also is not included in this work.

All of these inadequacies are being investigated [40]. Our analytical model, however, is sufficient to address the essential features of polysilicon with small and large grain sizes above room temperature and to determine the design rules to optimize the device and to predict the scaling limits [23].

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References

[1] *Polycrystalline and Amorphous Thin Films and Devices*, L. L. Kazmerski, Ed. New York: Academic, 1980.

[2] L. Gerzberg, "Monolithic power-spectrum centroid detector," Ph.D. dissertation, TR No. G557-2, Stanford Univ., Stanford, CA, May 1979.

[3] T. R. O'Connel, J. M. Hartman, E. D. Errett, G. S. Leach, and W. C. Dunn, "A 4K static clocked and non-clocked RAM design," in *IEEE ISSCC Dig. Tech. Papers*, pp. 14-15, Feb. 1977.

[4] J.Y.W. Seto, "The electrical properties of polycrystalline silicon films," *J. Appl. Phys.*, vol. 46. pp. 5247-5254, 1975.

[5] M. M. Mandurah, K. C. Saraswat, C. R. Helms. and T. I. Kamins, "Dopant segregation in polycrystalline silicon," *J. Appl. Phys.*, vol. 51, pp. 5755-5763, 1980.

[6] T. J. Rogers, "Advanced integrated-circuit technology for micropower ICs," Ph.D. dissertation, Stanford Univ., Stanford, CA, Aug. 1975.

[7] N.C.C. Lu, L. Gerzberg, and J. D. Meindl, "A quantitative model of the effect of grain size on the resistivity of polycrystalline silicon resistors," *IEEE Electron Device Lett.*, vol. EDL-1, no. 3, pp. 38-41, 1980.

[8] M. M. Mandurah, K. C. Saraswat, and T. I. Kamins, "Phosphorus doping of low-pressure chemically-vapor-deposited silicon films," *J. Electrochem. Soc.*, vol. 126, pp. 1019-1023, 1979.

[9] T. I. Kamins, J. Manolin, and R. N. Tucker, "Diffusion of impurities in polycrystalline silicon," *J. Appl. Phys.*, vol. 43, pp. 83-91, 1972.

[10] Y. Wada and S. Nishimatsu, "Grain growth mechanism of heavily phosphorus-implanted polycrystalline silicon," *J. Electrochem. Soc.*, vol. 125, pp. 1499-1504, 1978.

[11] J. R. Monkowski, J. Bloem, L. J. Giling, and M.W.M. Graef, "Comparison of dopant incorporation into polycrystalline and monocrystalline silicon," *Appl. Phys. Lett.*, vol. 35, pp. 410-412, 1979.

[12] C. H. Seager and T. G. Castner, "Zero-bias resistance of grain boundaries in neutron-transmutation-doped polycrystalline silicon," *J. Appl. Phys.*, vol. 49, pp. 3879-3889, 1978.

[13] T. H. DiStefano and J. J. Cuomo, "Reduction of grain boundary recombination in polycrystalline silicon solar cells," *Appl. Phys. Lett.*, vol. 30, pp. 351-353, 1977.

[14] N.C.C. Lu, L. Gerzberg, J. Peng, and J. D. Meindl, "Distribution of polysilicon grain size," to be published.

[15] M. E. Cowher and T. O. Sedgwick, "Chemical vapor deposited polycrystalline silicon," *J. Electrochem. Soc.*, vol. 119, pp. 1565-1570, 1972.

[16] T. I. Kamins, "Hall mobility in chemically deposited polycrystalline silicon," *J. Appl. Phys.*, vol. 42, pp. 4357-4365, 1971.

[17] G. Baccarani, B. Ricco, and G. Spadini, "Transport properties of polycrystalline silicon films," *J. Appl. Phys.*, vol. 49, pp. 5565-5570, 1978.

[18] G. J. Korsh and R. S. Muller, "Conduction properties of lightly doped polycrystalline silicon," *Solid-State Electron.*, vol. 21, pp. 1045-1051, 1978.

[19] M. L. Tarng, "Carrier transport in oxygen-rich polycrystalline-silicon films," *J. Appl. Phys.*, vol. 49, pp. 4069-4076, 1978.

[20] G. E. Pike and C. H. Seager, "The dc voltage dependence of semiconductor grain-boundary resistance," *J. Appl. Phys.*, vol. 50, pp. 3414-3422, 1979.

[21] N.C.C. Lu, Y. I. Nissim, R. Maltiel, and L. Gerzberg, "Thermal and laser processings of polycrystalline silicon films for high-value resistors," in EE412 report by J. D. Meindl, Dept. of Elec. Eng., Stanford Univ., Stanford, CA, 1979.

[22] S. R. Combs, "KITCHIP—A superior low-power monolithic device array," Ph.D. dissertation, TR No. 4958-6, Stanford Univ., Stanford, CA, Dec. 1977.

[23] L. Gerzberg, N.C.C. Lu, and J. D. Meindl, "Scaling and limits of monolithic polycrystalline silicon resistors," presented at the IEEE Device Research Conf., June 1980; also in *IEEE Trans. Electron Devices*, vol. ED-27, p. 2184, Nov. 1980.

[24] W. R. Runyan, *Semiconductor Measurements and Instrumentations*. New York: McGraw-Hill, 1975, pp. 131-151.

[25] G. L. Pearson and J. Bardeen, "Electrical properties of pure silicon and silicon alloys containing boron and phosphorus," *Phys. Rev.*, vol. 75, pp. 865-883, 1949.

[26] S. M. Sze, *Physics of Semiconductor Devices*. New York: Wiley, 1969, ch. 1, 4, 8.

[27] M. Hirose, M. Taniguchi, and Y. Osaka, "Electronic properties of chemically deposited polycrystalline silicon," *J. Appl. Phys.*, vol. 50, pp. 377-382, 1979.

[28] N.C.C. Lu, L. Gerzberg, C. Y. Lu, and J. D. Meindl, "Thermionic field emission in polycrystalline-silicon film," Abstract No. 528, Electrochem. Soc. Fall Meet., Hollywood, FL, Oct. 1980, pp. 1321-1323.

[29] W. R. Runyan, *Silicon Semiconductor Technology*. New York: McGraw-Hill, 1965, ch. 8.

[30] H. F. Wolf, *Silicon Semiconductor Data*. Oxford, England: Pergamon, 1969, ch. 2.

[31] E. Spenke, *Electronic Semiconductors*. New York: McGraw-Hill, 1958, pp. 387-394.

[32] S. K. Ghandhi, *The Theory and Practice of Microelectronics*. New York: Wiley, 1969, ch. 11.

[33] R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits*. New York: Wiley, 1977, ch. 1, Tables 1.1, 1.2.

[34] L. G. Bassett *et al.*, *Principles of Chemistry*. Englewood Cliffs, NJ: Prentice-Hall, 1970, p. 456.

[35] L. Gerzberg, N.C.C. Lu, and J. D. Meindl, "A monolithic power-spectrum centroid detector," in *IEEE ISSCC Dig. Tech. Papers*, THPM 13.1.A, Feb. 1981, pp. 164-165.

[36] A. Gat, L. Gerzberg, J. F. Gibbons, T. J. Magee, J. Peng, and J. D. Hong, "CW laser anneal of polycrystalline silicon: Crystalline structure, electrical properties," *Appl. Phys. Lett.*, vol. 33, pp. 775-778, 1978.

[37] G. Yaron, L. D. Hess, and G. L. Olson, "Electrical characteristics of laser-annealed polysilicon resistors for device applications," in *Laser and Electron Beam Processing of Materials*, C. W. White and P. S. Peercy, Eds. New York: Academic Press, 1980, pp. 626-631.

[38] T. Makino and H. Nakamura, "The influence of plasma annealing in electrical properties of polycrystalline Si," *Appl. Phys. Lett.*, vol. 35, pp. 551-552, 1979.

[39] A. F. Mayadas and M. Shatzkes, "Electrical resistivity model for polycrystalline films: The case of arbitrary reflection at external surfaces," *Phys. Rev. B*, vol. 1, no. 4, pp. 1382-1389, 1970.

[40] N.C.C. Lu, L. Gerzberg, C. Y. Lu, and J. D. Meindl, "A new conduction model for polycrystalline silicon films," *IEEE Trans. Electron. Device Lett.*, vol. EDL-2, pp. 95-98, Apr. 1981.