

應用於無線基頻之動態取樣訊號處理研究

研究生：林祐賢

指導教授：陳昌居 博士

指導教授：許騰尹 博士

國立交通大學資訊工程學系 研究所碩士班

摘要

採用直接序列展頻調變的標準包含802.11, 802.11b 以及802.11g 等無線區域網路系統。無線通訊比有線通訊多了更多的不確定性，因此，無線通訊系統的封包裡一般都會定義preamble 欄位作為接收端同步之用。在本論文中，我們利用Barker 碼展頻的preamble 欄位來消除通道中的非理想效應，例如高斯雜訊、載波頻率誤差、載波相位誤差、以及取樣頻脈誤差等等。在這些非理想效應加成下，會導致接收器的訊號會失真，所以我們提出的演算法並須可以在高斯雜訊、和多重路徑…等通道效應下，正確、有效的可以解出並補償取樣頻脈誤差。

因此，本論文所提出的演算法，以使接收器只需要利用PLCP 中的preamble 欄位就可以得知通道的重要參數，而不須MPDU 的任何協助，此法可減低互補編碼(CCK) 解碼器的成本，其成本佔了整個收發器的大部分。此法更對802.11g 有助益，因為802.11g 中有CCK-OFDM模式，也就是Barker 碼展頻的PLCP接上正交多工分頻(OFDM) 的MPDU。

為了瞭解整個系統，我們使用Matlab 建立了系統模擬平台。我們可以觀察系統中任一訊號的波形，並且可以得知通道中的非理想效應對整個系統或某些訊號有何影響 — 此平台更可以用來驗證我們所提出的同步演算法。最後，在實作硬體部分，提出利用非同步電路設計，使電路可以獲的非同步設計好處。

The Study of Dynamic Sampling Loop For Wireless Baseband Applications

Student: You-Hsien Lin

Advisor: Dr. Chang-Jiu Chen

Advisor: Dr. Terng-Yin Hsu

Department of Computer Science and Information Engineering,
National Chiao Tung University

Abstract

Direct sequence spread spectrum (DSSS) technique is used in IEEE 802.11, 802.11b and 802.11g wireless LAN systems. Unlike the wire channel, wireless communication uses radio as its medium and has more uncertainty with it. Therefore, WLAN frame format generally contains preamble field for synchronization. In this thesis, use the Barker spread preamble field to eliminate non-ideal channel effects including Additive White Gaussian Noise (AWGN), carrier frequency offset (CFO), carrier phase offset (CPO), and sampling clock offset. Therefore, the signal is degraded under non-ideal channel effects, and the exact and effectual timing synchronization algorithms were proposed.

By the proposed algorithms, the baseband receiver can extract all the channel parameters only with the PLCP preambles and does not need any help from the MPDU which will reduce the CCK demodulator cost, dominated the cost of the system. In addition, the proposed algorithms can benefit the IEEE 802.11g system, which includes the CCK-OFDM signal flow — PLCP frame consists of the Barker and OFDM MPDU. Some simulation results, based on the proposed Matlab platform, have shown in this thesis. Finally, architectures of key components are discussed with gate counts of listed as well, where asynchronous-circuit techniques are used to implement the proposed architectures.

Dedicate the thesis to my family and friends

Acknowledgements

I would like to express sincerely my gratitude to those people for their invaluable help during the past two years, stayed in Hsin-Chu. Especially, I want to express my deepest gratitude to my advisor Prof. Terng-Yin Hsu and advisor Prof. Chang-Jiu Chen for his enthusiastic guidance and encouragement to overcome many difficulties throughout the research, and I give him and his family my best wish faithfully.

Also, I want to thank my ISIP group mates, Blues Yu(游瑞元), Shih-Lin Lo (羅仕麟), Ming-Fu Sun(孫明福), Jin-Hwa Guo(郭錦華), Ming-Yeh Wu(吳明曄), Ming-Feng Shen(沈明峰), Light Lin(林弘全), Chueh-An Tsai(蔡爵安), for their suggestions and great helps during my research. I would like to thank all members in ISIP laboratory for their plenty of fruitful assistance.

Finally, I give the greatest respect and love to my family and my girlfriend. I express my highest appreciation and dedicate the thesis to them for their assistance and attention during the most important stage in my life.

Contents

page

中文摘要	i
英文摘要	ii
誌謝	iii
目錄	iv
圖目錄	vi
表目錄	ix
CHAPTER1 INTRODUCTION	1
CHAPTER2 CHANNEL MODELS	3
2.1 Channel effects	3
2.1.1 Path Loss	4
2.1.2 Multipath	4
2.1.3 CFO	9
2.1.4 Clock Drift	10
2.2 Matlab receiver platform architecture	11
CHAPTER3 THE TIMING SYNCHRONIZATION	14
3.1 Introduction	14
3.2 Packet detection	14
3.3 Symbol boundary decision	16
3.3.1 Symbol boundary decision before timing synchronization	16
3.3.2 Symbol boundary decision after timing acquisition	19
3.4 The proposed timing synchronization algorithm	19
3.4.1 Timing synchronization introduction	19
3.4.2 The proposed timing acquisition method	25
3.4.2.1 The general proposed timing acquisition method	25

3.4.2.2 The extend buffer timing acquisition method	26
3.4.2.3 The dual correlator differential base method	33
3.4.3 The proposed timing tracking method	42
CHAPTER4 SIMULATION PLATFORM	45
4.1 Choosing a suitable tool	45
4.2 System block diagram	46
4.3 Transmitter	47
4.4 Receiver	48
4.5 Simulation results	51
CHAPTER5 HARDWARE IMPLEMENTATION	55
5.1 Architecture	55
5.2 Matlab platform translation to HDL simulation method	56
5.3 Proposed hardware component	57
5.4 Asynchronous Circuit Design	59
CHAPTER6 CONCLUSIONS AND FUTURE WORKS	62
6.1 Conclusions	62
6.2 Future works	63
REFERENCES	64
ABOUT THE AUTHOR	66

List of Figures

page

Figure 2-1 Typical wireless communication system	3
Figure 2-2 Constellation of transmitted signal	5
Figure 2-3 SPW11b multipath impulse response and constellation of signal	6
Figure 2-4 SPW11a multipath impulse response and constellation of signal	7
Figure 2-5 IEEE Multipath impulse response and constellation of signal	8
Figure 2-6 Constellation of signal through CFO=50 ppm	9
Figure 2-7 The sinc waveform of clock drift model effect	10
Figure 2-8 DSSS system architecture	12
Figure 2-8 Dual correlator system platform architecture	12
Figure 2-10 IEEE 802.11b platform architecture	13
Figure 3-1 PAPR information at SNR 0 dB with IEEE Multipath	15
Figure 3-2 Symbol boundary under the situation of only AWGN	18
Figure 3-3 Symbol boundary under AWGN and IEEE Multipath	18
Figure 3-4 The symbol boundary decision rule before timing acquisition	20
Figure 3-5 Symbol boundary after timing acquisition	21
Figure 3-6 The symbol boundary decision rule after timing acquisition	21
Figure 3-7 Eye diagram with different sampling phase	22
Figure 3-8 The eye diagram under the situation of only AWGN	22
Figure 3-9 The eye diagram under the situation of AWGN and multipath	23
Figure 3-10 The block diagram of fix sampling	23
Figure 3-11 The block diagram of dynamic sampling	24
Figure 3-12 The general method of early late algorithm	27
Figure 3-13 The state diagram of the general timing acquisition method algorithm	28
Figure 3-14 The error function versus timing phases under AWGN	29
Figure 3-15 The sample clock phase error after general method	29
Figure 3-16 The state diagram of the extend buffer timing acquisition algorithm ..	30
Figure 3-17 The extend buffer method of early late algorithm	31
Figure 3-18 The error function versus timing phases under AWGN and multipath	31

Figure 3-19	The sample clock phase error after the extend buffer method	32
Figure 3-20	The filter effect in the proposed platform	32
Figure 3-21	The dual correlator architecture	33
Figure 3-22	The Block diagram of proposed dual correlator differential base	35
Figure 3-23	The select method of odd correlator	35
Figure 3-24	The select method of even correlator	36
Figure 3-25	The error function versus timing phases under AWGN and Multipath	36
Figure 3-26	The state diagram of the dual correlator differential base method	37
Figure 3-27	The binary decision search flow diagram	38
Figure 3-28	The sample clock phase error after dual correlator differential base ..	40
Figure 3-29	The received signal pass through timing acquisition with noise free ...	40
Figure 3-30	The received signal pass through timing acquisition with noise	41
Figure 3-31	The MSE versus SNR of three timing acquisition method	41
Figure 3-32	The binary decision search flow diagram in timing tracking state	43
Figure 3-33	The state diagram of the dual correlator differential base method	44
Figure 4-1	System block diagram	46
Figure 4-2	Block diagram of transmitter	47
Figure 4-3	Coding architecture of finite state machine based	48
Figure 4-4	State diagram of receiver	50
Figure 4-5	Noise attached to the head and tail of the frame	51
Figure 4-6	PER of 1 Mbps	52
Figure 4-7	BER of 1 Mbps	53
Figure 4-8	PER of 2 Mbps	54
Figure 4-9	BER of 2 Mbps	54
Figure 5-1	The Block Diagram of DSSS-based Wireless Baseband Processor	55
Figure 5-2	Matlab simulation to Hardware implement flow	56
Figure 5-3	Shift register based Barker correlator	57
Figure 5-4	PAM based Barker correlator	58
Figure 5-5	Dynamic sampling and timing synchronization architecture	58
Figure 5-6	The first method to design asynchronous circuit	60
Figure 5-7	The controller handshake circuit diagram	60

Figure 5-8 The synthesis result by Balsa61
Figure 5-9 The second method to design asynchronous circuit61



List of Tables

page

Table 2-1 Two parts of channel model	3
Table 3-1 Comparison of three proposed timing acquisition	39
Table 4-1 Comparison of C/C++ and Matlab	45

