# CHAPTER 1

# INTRODUCTION

With the advance of modern wireless communication techniques, there are more and more wireless communications systems play an increasingly important role in our daily life, like Wireless LAN(IEEE 802.11, 802.11b [1], 802.11a [2], 802.11g [3], UWB), Personal Communication System(GSM, PHS, 3G), Sensor Network or GPS, … etc. All has the property that a received frame is valid only when all data bits in it are correct. Unlike the wire channel, wireless communication uses radio as its medium and has more uncertainty with it. Therefore, WLAN frame format generally contains preamble field for timing synchronization and other synchronization. For completely understanding the timing synchronization problem and solving it, the Direct Sequence Spreading Spectrum (DSSS) system is chosen to be my research area, so the IEEE 802.11b standard is used to build the demo platform to verify the proposed algorithms.

In the IEEE 802.11b standard, the PLCP preamble is used to do the signal process, such as synchronization and channel estimation which use the Barker spreading code to eliminate non-ideal channel effects including Additive White Gaussian Noise (AWGN), distance path loss, Multipath fading, carrier frequency offset (CFO) and sampling clock offset (SCO). Not only IEEE 802.11b has included a preamble frame, but also many WLAN standards have done that. During this preamble, the signal process, such as timing synchronization, frequency synchronization and channel estimation must be done and some of channel effects have to be eliminated and compensated until the preamble finishes. Although the preamble formats are not the same in many WLAN standards, the problems that must be solved are all the same. If all these problems on IEEE 802.11b platform are solved, it can quickly find algorithms or solutions that solve these problems on other wireless platforms — IEEE 802.11a, IEEE 802.11g or UWB. In this thesis, the characteristics of channel models would be described the information of PN spreading

code during received preamble.

This thesis includes six chapters. Chapter 1 describes the introduction. Chapter 2 discusses the Channel Model. Chapter 3 discusses the timing synchronization proposed methods in detail. In Chapter 4 discusses the Matlab simulation platform and system performance. In Chapter 5 discusses Hardware implementation. Finally, Chapter 6 describes the conclusion and future work for further research.

# CHAPTER 2

# Channel Model

## 2.1 Channel effects

In wireless communications system, there are three important blocks that must be considered; the first is Transmitter (TX), the second is channel model and the last is Receiver (RX). Among these three blocks, the channel model is especially important than the others, because the channel effects truly reflect how the channel effects truly reflect how the channel reacts in the real world. The two parts that composite the channel model is shown in Table 2-1, and Figure 2-1 shows a typical wireless communication system. It could be seemed that one part of channel model is atmosphere model and the other is system inconsistency from Table 2-1.

| Atmosphere model | System inconsistency |
|---|---|
| Path Loss | Carrier Frequency Offset |
| Multipath | Clock Drift |
| AWGN | |

Table 2-1 Two parts of channel model

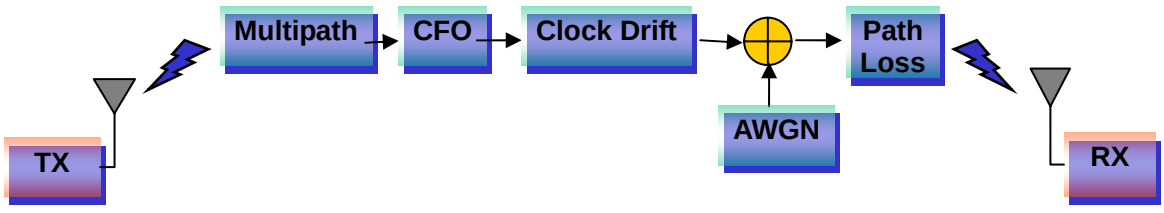



Figure 2-1 Typical wireless communication system

### 2.1.1 Path Loss

Because the signal power will decrease with the distance between TX and RX increasing, at the RX an amplifier that needed is called Variable Gain Amplifier (VGA) to enhance the received signal power. If not, the wireless system will difficultly detect any signal. Assume that the transmitted signal is $s(t)$ and the received signal is $R(t)$, then path loss effect can be modeled as

$$R(t) = s(t) \bullet path\_loss \quad \text{.....(2-1)}$$

where path_loss is a constant and its value is from 0 dB to –several hundred dB.

If the path loss effect is very crucial, the receiver will be not detect any signal without VGA. However it is difficult to known that how exact the path loss effect is. So the goal of AGC is to estimate the suitable path loss effect and justify the VGA gain to let the system can work under the situation of having steady signal.

### 2.1.2 Multipath

For a common system, the transmitted signal through a multipath fading channel can be written as

$$r(t) = \int_{-\infty}^{\infty} s(\tau)h(t,\tau)d\tau = s(t) \otimes h(t,\tau) \quad \text{.....(2-2)}$$

where t represents the time and $\tau$ represents the channel multipath delay for a fixed value of t, another $h(t,\tau)$ is represents impulse response. If the multipath channel is assumed to be a bandlimited bandpass channel and time invariant, then the channel impulse response may be simplified as

$$h_b(\tau) = \sum_{i=0}^{N-1} a_i \exp(j\theta_i)\delta(\tau - \tau_i) \quad \text{.....(2-3)}$$

Where $a_i$ and $\tau_i$ are the real amplitudes and excess delays, respectively, of $i_{th}$ multipath component. The phase term $\theta_i$ represents the phase shift due to free space

propagation of the $i_{th}$ multipath component, plus any additional phase shifts which are encountered in the channel. Any one who interested in multipath fading can reference [4].

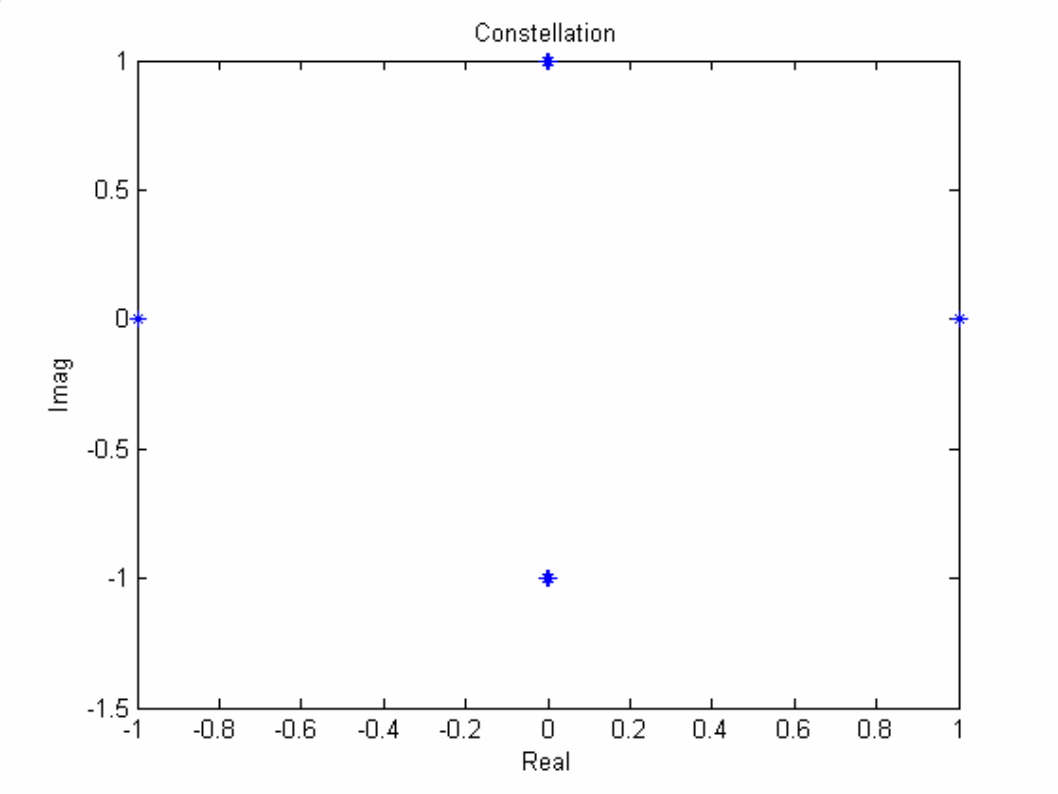



Figure 2-2 Constellation of transmitted signal

In the proposed platform, three public multipath model (SPW11b [5], SPW11a [5] and IEEE Multipath) is used to simulate and some figures to explain what the multipath effects is. From Figure 2-2, it shows the constellation of a transmitted signal, which is modulated by DQPSK, hence Figure 2-3 ~ 2-5 shows three types of multipath impulse response to convolute channel with the transmitted signals

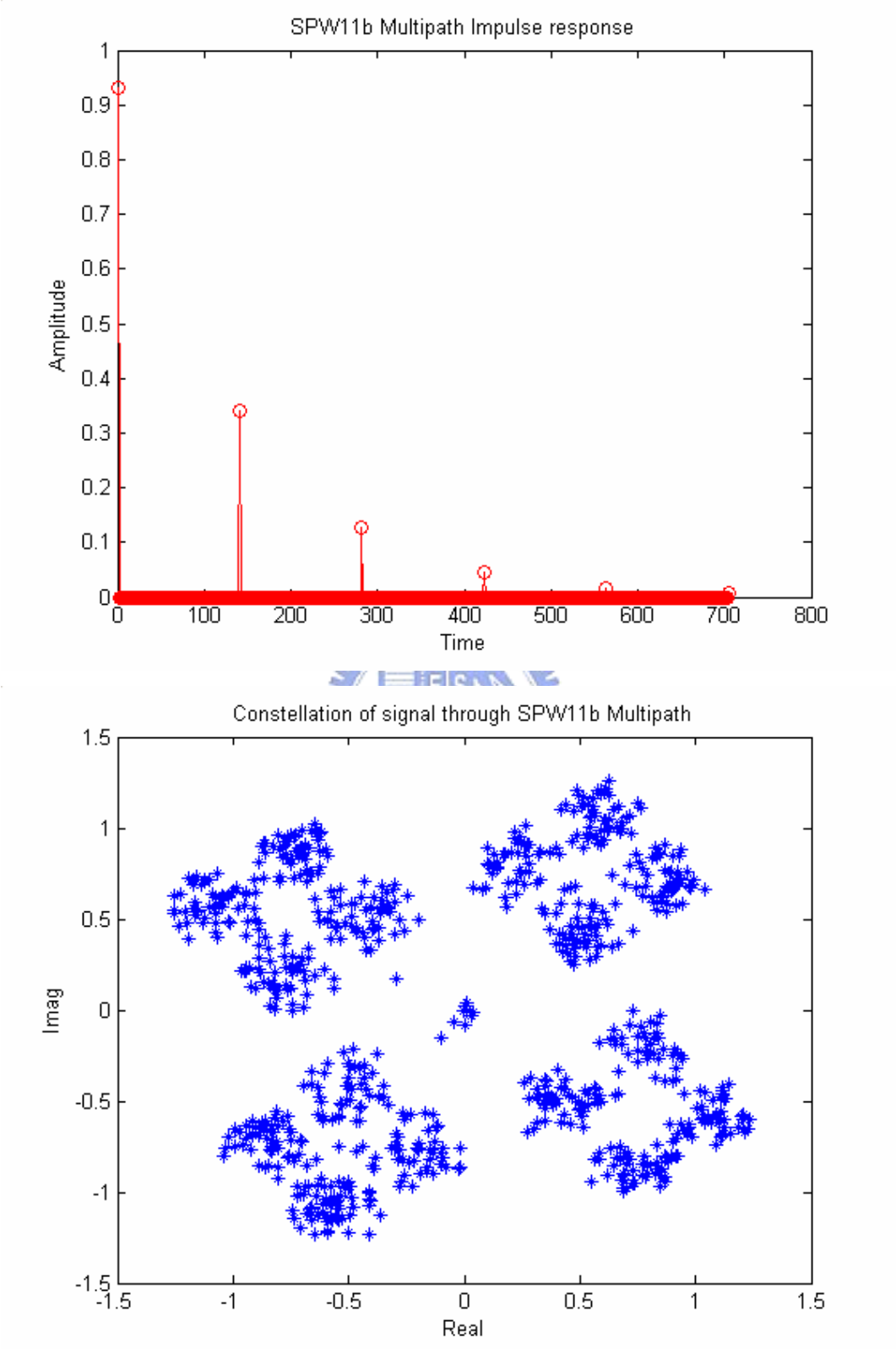



Figure 2-3 SPW11b Multipath impulse response and constellation of signal

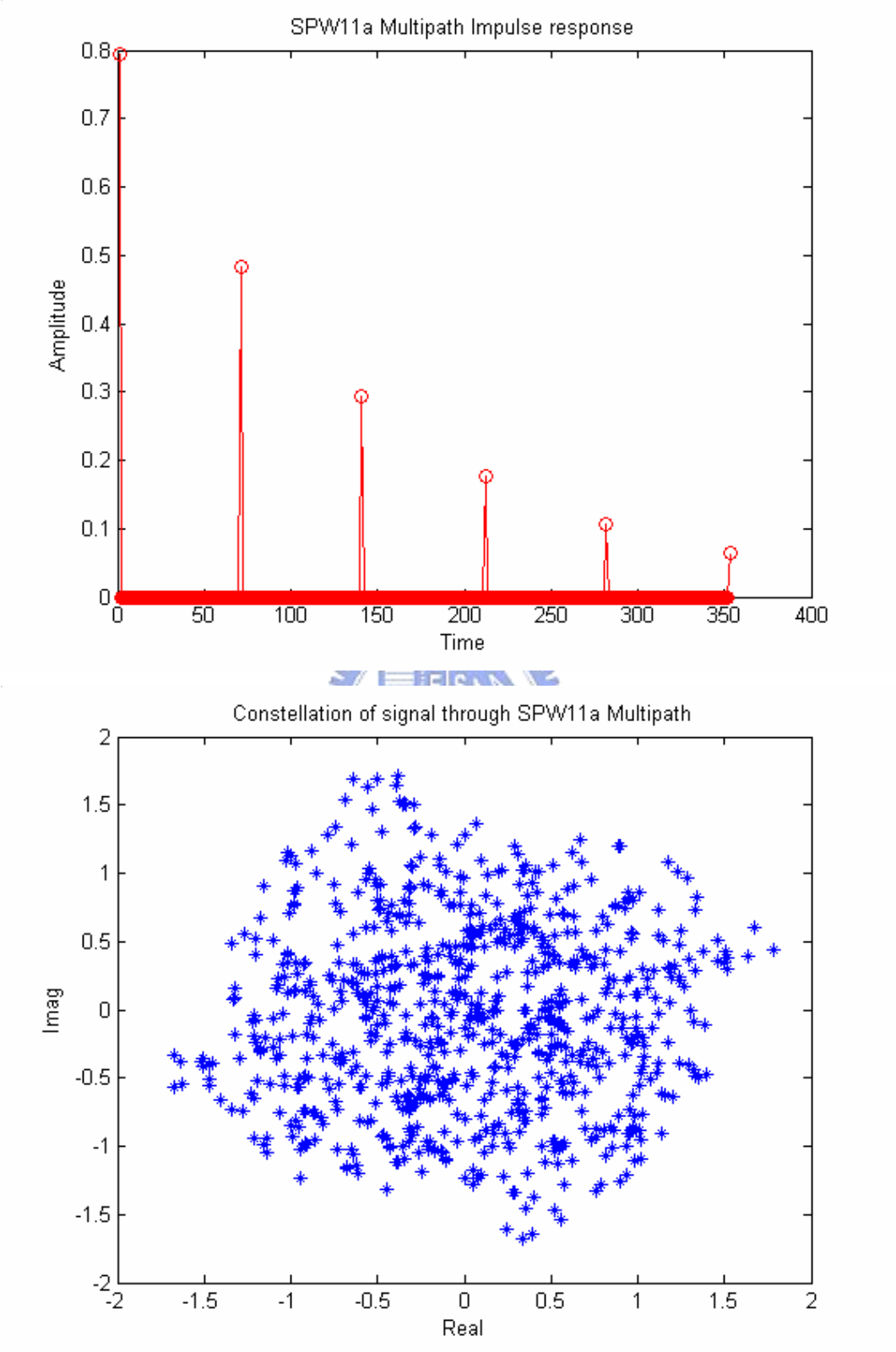



Figure 2-4 SPW11a Multipath impulse response and constellation of signal

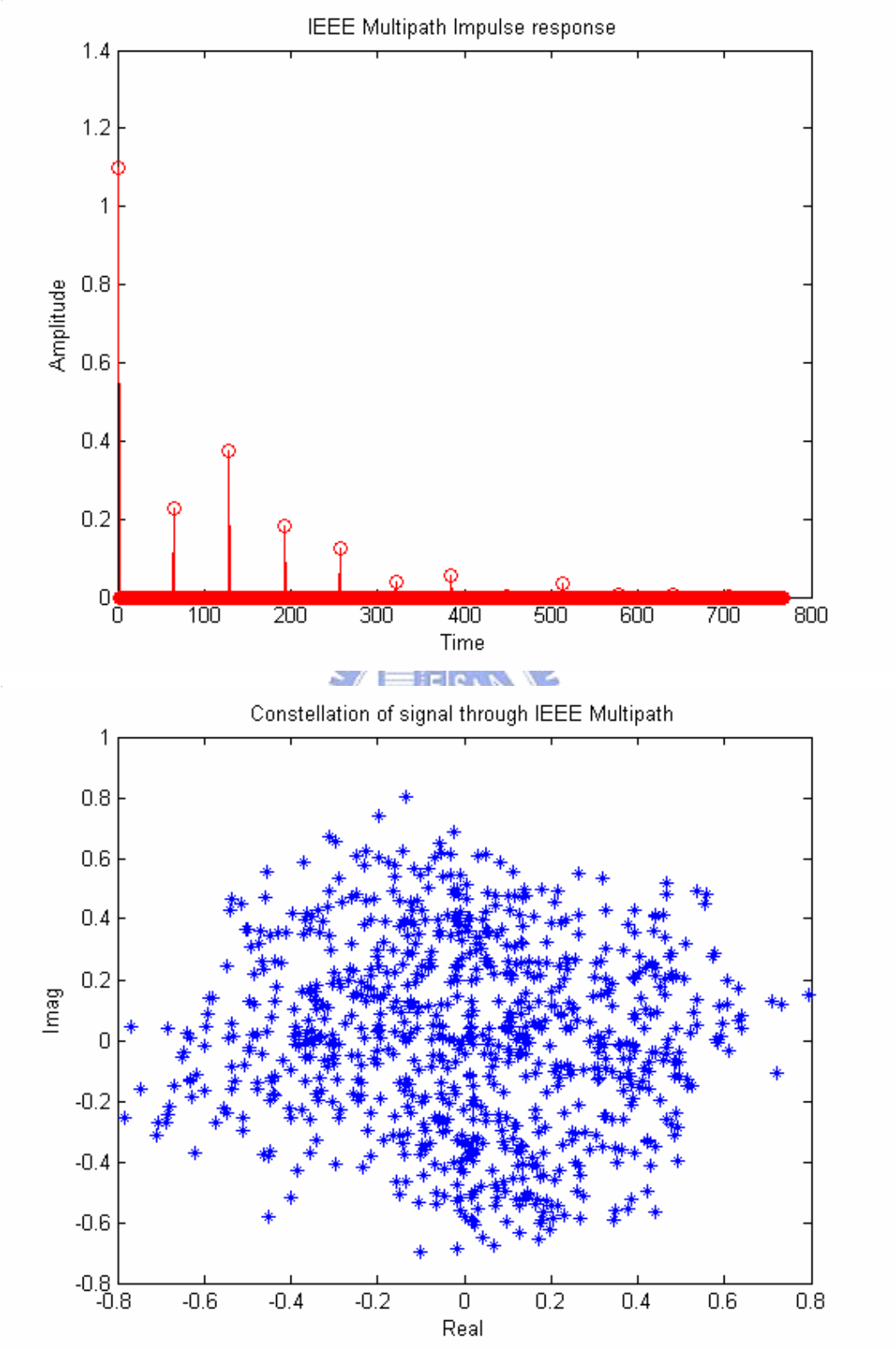



Figure 2-5 IEEE Multipath impulse response and constellation of signal

### 2.1.3 CFO

CFO is caused by the inconsistency between RF of TX and RX and its effect can be written as

$$R(t) = \sum_{n} s(t) \bullet \exp(j(2\pi \Delta f t + \theta)) \quad \text{.....(2-4)}$$

where $\Delta f$ and $\theta$ are the carrier frequency and carrier phase difference between TX and RX respectively. Figure 2-6 shows the constellation of signal through CFO=50 ppm and it shows that the CFO will cause the constellation of the transmitted signal become a circle, that means phase of the transmitted signal will rotate with time.

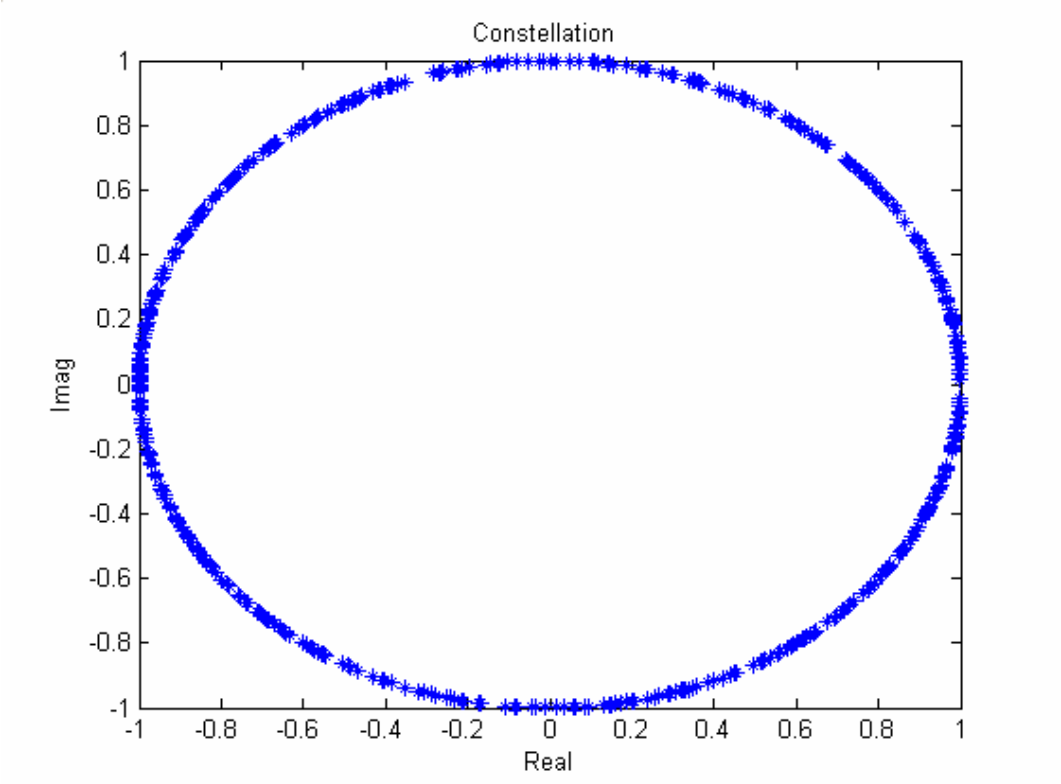



Figure 2-6 Constellation of signal through CFO=50 ppm

### 2.1.4 Clock Drift

The clock drift means the different between the sampling frequency of the digital to analog converter (DAC) and the analog to digital converter (ADC). Because of sampling frequency offset, even if the initial sampling point is optimized, the following sampling points will still slowly shift with time. This model is using compress sinc waveform to cause the clock drift effect, and its effect can be written as

$$R(nT_s) = R_{preADC}(nT_s) * \mathrm{sinc}(\frac{nT_s - \Delta T_n}{T_s}) \quad \text{.....(2-5)}$$

where $R_{preADC}$ represents the ADC original output signal, $\Delta T_s$ represents shift sampling period and to get $R(nT_s)$ signal by convoluting the ADC original output signal and shifted sinc waveform. Figure 2-7, shows the clock drift model effect; initial can samples at optimum sampling points, then slightly incorrect sampling instants will cause the SNR degradation.

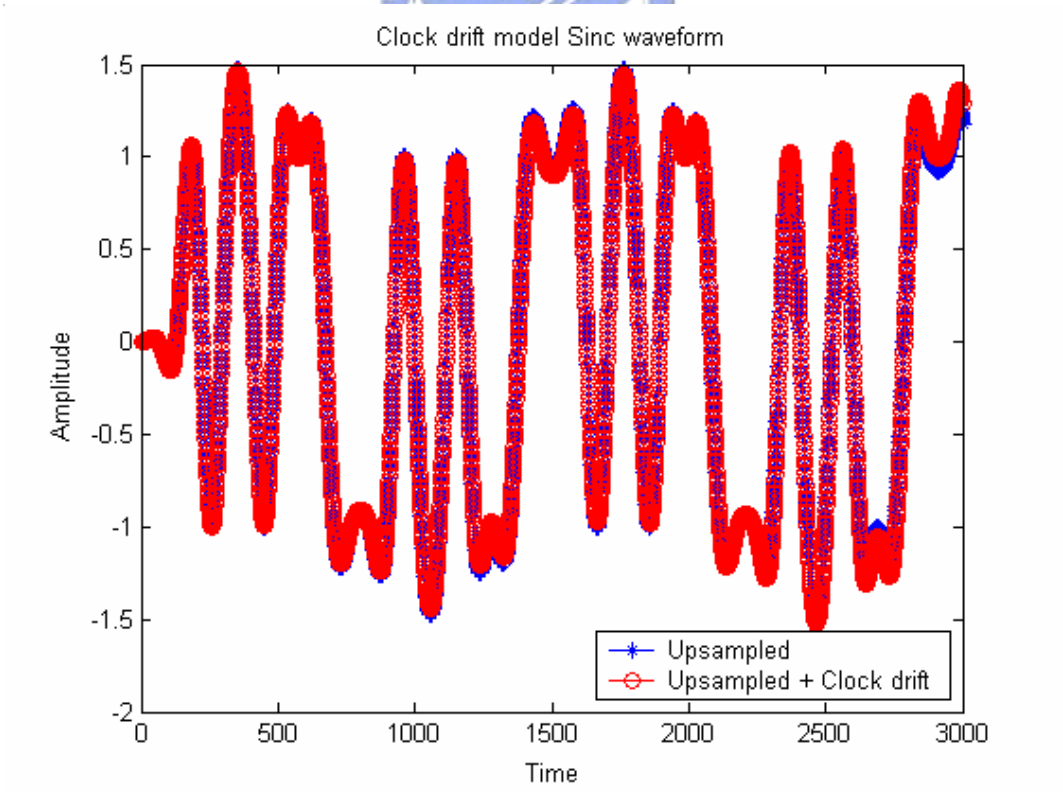



Figure 2-7 The sinc waveform of clock drift model effect

## 2.2 Matlab receiver platform architecture

There are three systems that are used for this thesis. Figurer 2-8 shows a DSSS system that is used to do the signal process, frequency and timing synchronization; Figure 2-9 the proposed system platform is constituted of dual correlator, this system is used to test the proposed timing synchronization algorithm. This timing synchronization algorithm is introduced in chapter 3. Figure 2-10 shows a complete 802.11b system that is used to calculate Bit-Error-Rate (BER) and Packet-Error-Rate (PER).

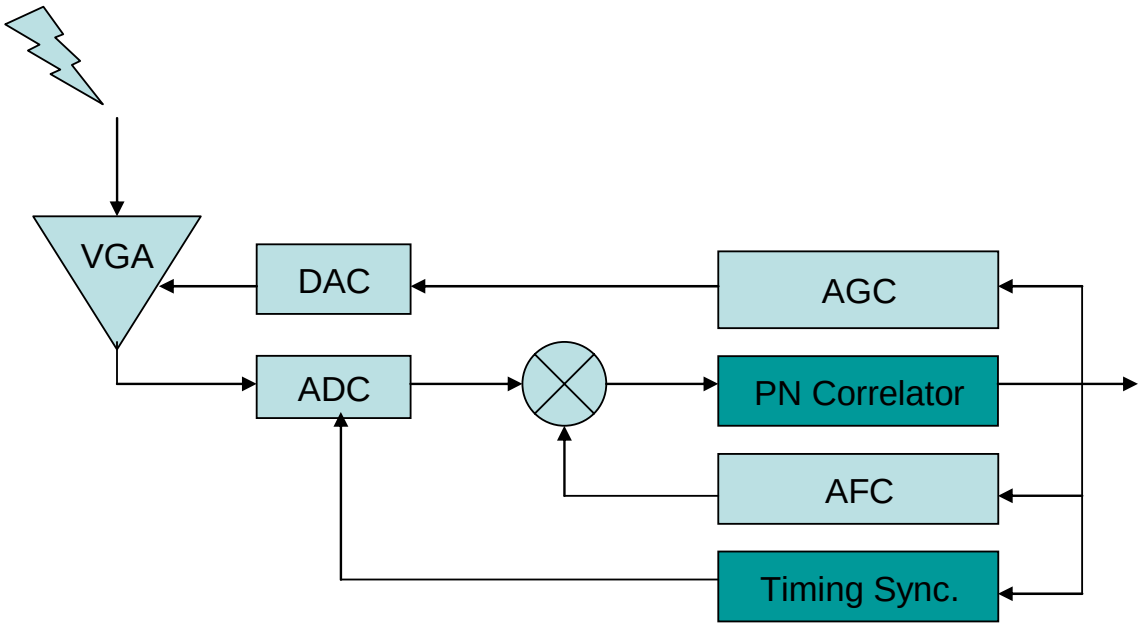



Figure 2-8 DSSS system architecture

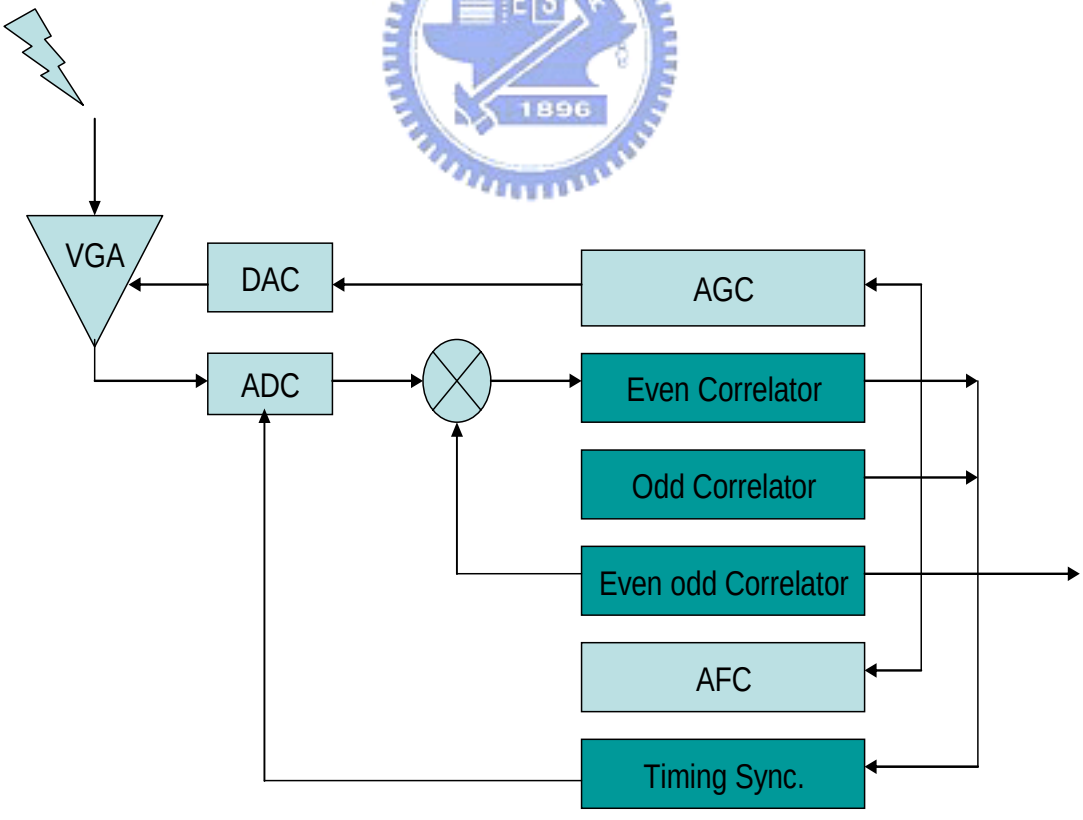



Figure 2-9 Dual correlator system platform architecture

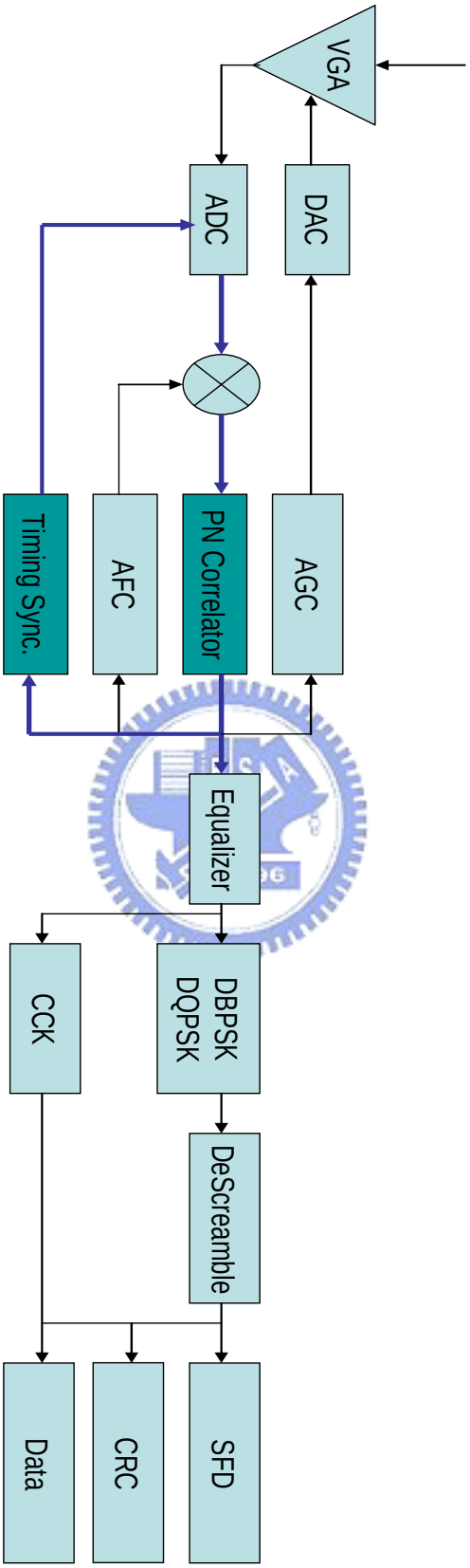



Figure 2-10 IEEE 802.11b platform architecture

# CHAPTER 3

# THE TIMING SYNCHRONIZATION

## 3.1 Introduction

For wireless DSSS systems, the PN correlator output is the most important information to estimate synchronized information, hence in 802.11b system the Barker correlator output is used to do this operation. The proposed timing synchronization algorithm is constructed based on the PN correlator output. The peak means that the point having maximum correlator output power in one symbol time and its formula is

$$Peak\_power = Max(\mathrm{Re}(r(t-nT)\bullet B)^2 + \mathrm{Im}(r(t-nT)\bullet B)^2) \quad \text{.....(3-1)}$$

where T is symbol time duration and $R(t)$ (the received signal) is

$$R(t) = (s(t-\tau(t)) \otimes h(t)\bullet e^{j(2\pi\Delta f t+\theta)} + n(t))\bullet path\_loss \quad \text{.....(3-2)}$$

where $S(t)$ is the signal, $h(t)$ is multipath impulse response, $\Delta f$ is CFO, $\theta$ is phase offset, $\tau(t)$ is the clock sample rate and $n(t)$ is AWGN. In the proposed platform, the first step is detected packet come, then doing the first symbol boundary decision. After symbol boundary decision, then starting timing synchronization; the timing synchronization includes two parts: the first is timing acquisition, in this part is fast to get the nearly optimum sampling clock phase; the second is timing tracking, in this part to keep sample point at optimum sample clock phase. Next, about timing synchronization will be described in detail. After timing acquisition, it must be to decide symbol boundary again. So, in the proposed platform, it is used two methods to do symbol boundary decision.

## 3.2 Packet detection

The packet detection mechanism must be acting simultaneously with AGC

estimating. First, a kind of value-Peak-to-Average-Power Ratio (PAPR) is introduced, and it can be formulated as

$$PAPR = \frac{Peak\_power}{Average\_power} \quad \text{.....(3-3)}$$

$$= \frac{Max(\mathrm{Re}(r(t-nT)\bullet B)^2 + \mathrm{Im}(r(t-nT)\bullet B)^2)}{\frac{Sum(\mathrm{Re}(r(t-nT)\bullet B)^2 + \mathrm{Im}(r(t-nT)\bullet B)^2)}{k}}$$

The information-PAPR is used for detecting packet more precisely. The SNR increase, the PAPR information of noise and packet will be separated more clearly. But under seriously multipath situation the PAPR information is also become useless and Figure 3-1 shows this kind of situation. So, in this situation can affect the symbol boundary decision perform correctly. This packet detection method is proposed by Shih lin Lo [6]. In the above situation, it will be effected below component perform when seriously multipath and can degraded the performance, as shown in the Figure 3-1.

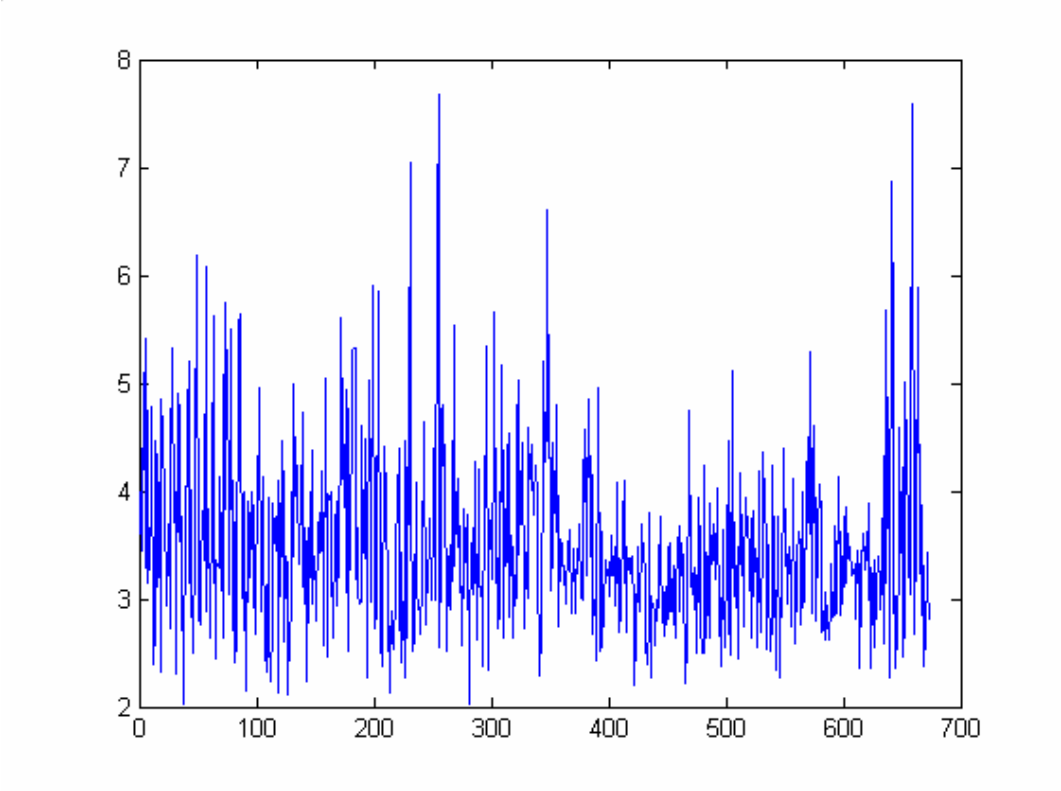



Figure 3-1 PAPR information at SNR 0 dB with IEEE Multipath

### 3.3 Symbol boundary decision

After the packet detection, the symbol boundary is also need to decide. The symbol boundary decision is an important role at before and after timing acquisition. The symbol boundary decision is called symbol synchronization. In the DSSS system, it is using the property of spectrum spreading to determine symbol boundary. In the proposed platform, it need two part symbol boundary decision, to keep symbol boundary is correct; before timing acquisition, because must to ensure the symbol boundary is correct, then to start timing acquisition. After timing acquisition, because through the timing acquisition to justify sample clock phase and turn to down sample, must to ensure symbol boundary is correct again.

#### 3.3.1 Symbol boundary decision before timing synchronization

Under the situation of AWGN, only, if the peak information is used to define the symbol boundary, then the error rate will be the same as noise-free conditions, where the symbol boundary can always be found at the duration of two continuous peaks. Figure 3-2 shows an example of symbol boundary under the situation of AWGN, only, where the two solid lines are the symbol boundary defined based on the peak information. However, under the situation of AWGN and multipath fading, the original peak power may be degraded by multipath and another power of a point that originally is not a peak and may be heightened by multipath. Hence, it may cause a decision of wrong symbol boundary. That situation is shown in Figure 3-3. In the proposed platform, using symbol boundary decision method after timing acquisition can be shown in Figure 3-4. This symbol boundary decision method is proposed by Shih lin Lo [6]. There is a new information called pilot that mentioned in previous. The pilot is

$$pilot = t - nT + i_1 T_c \quad \text{.....(3-4)}$$

*where*

$\mathrm{Re}(r(t-nT+i_1T_c)\bullet B)^2+\mathrm{Im}(r(t-nT+i_1T_c)\bullet B)^2 > threshold$

*and*

$i_1=\min(\{i_1,i_2,...,i_p\})$

and the pre_pilot is

$pre\_pilot=t-(n-1)T+i'_1T_c$ ……(3-5)

*where*

$\mathrm{Re}(r(t-(n-1)T+i'_1T_c)\bullet B)^2+\mathrm{Im}(r(t-(n-1)T+i'_1T_c)\bullet B)^2 > threshold$

*and*

$i'_1=\min(\{i'_1,i'_2,...,i'_p\})$

The information of peak_loc and pre_peak_loc are also used here. Figure 3-4, the numbers 1, 2, 3, 4 mean the priority that would be chosen to be the symbol boundary. That is there are four results of equations and then the chosen symbol boundary is according to the priority of the decision rule. Then the decision rule could be formulated as

$$symbol\_bounday=\begin{cases} peak\_loc & \triangle 1=\triangle 2 \\ pilot\_loc & \triangle 1\neq\triangle 2\ \&\ \triangle 3=\triangle 4 \\ peak\_loc & \triangle 1\neq\triangle 2\ \&\ \triangle 3\neq\triangle 4\ \&\ \triangle 1=\triangle 4 \\ pilot\_loc & \triangle 1\neq\triangle 2\ \&\ \triangle 3\neq\triangle 4\ \&\ \triangle 1\neq\triangle 4\ \&\ \triangle 2=\triangle 3 \end{cases} \quad \text{……(3-6)}$$

*where* $\triangle 1=peak\_loc, \triangle 2=pre\_peak\_loc, \triangle 3=pilot\_loc, \triangle 4=pre\_pilot\_loc$

After the symbol boundary decision, the peak power is

$peak\_power$ ……(3-7)

$=\mathrm{Re}(r(t-nT+symbol\_boundary\bullet T_c)\bullet B)^2+\mathrm{Im}(r(t-nT+symbol\_boundary\bullet T_c)\bullet B)^2$

After the symbol boundary decision, will be to start timing synchronization.

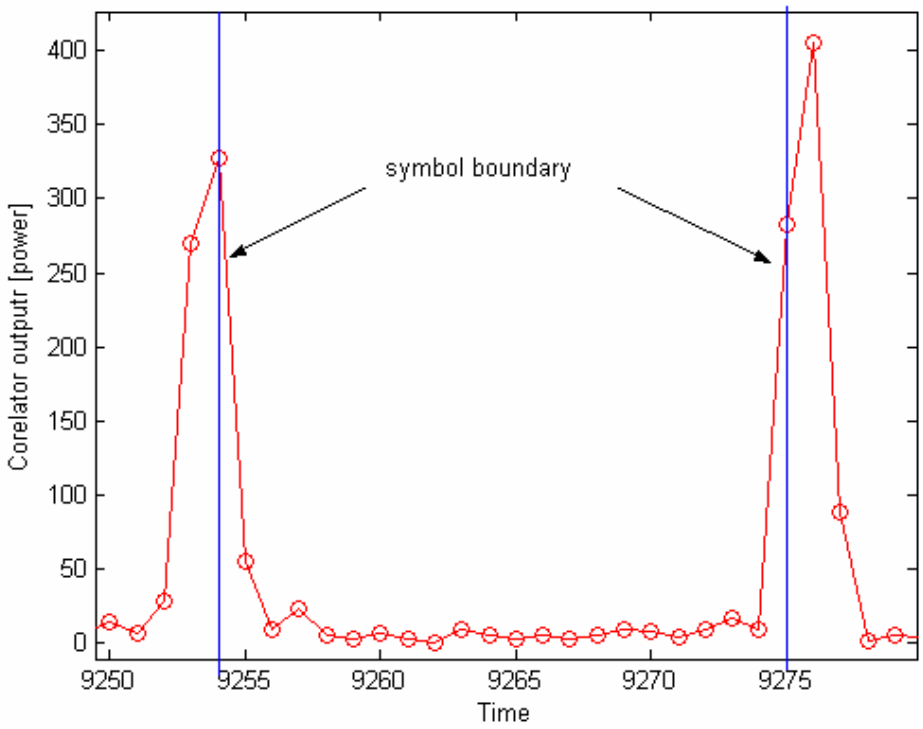



Figure 3-2 Symbol boundary under the situation of only AWGN

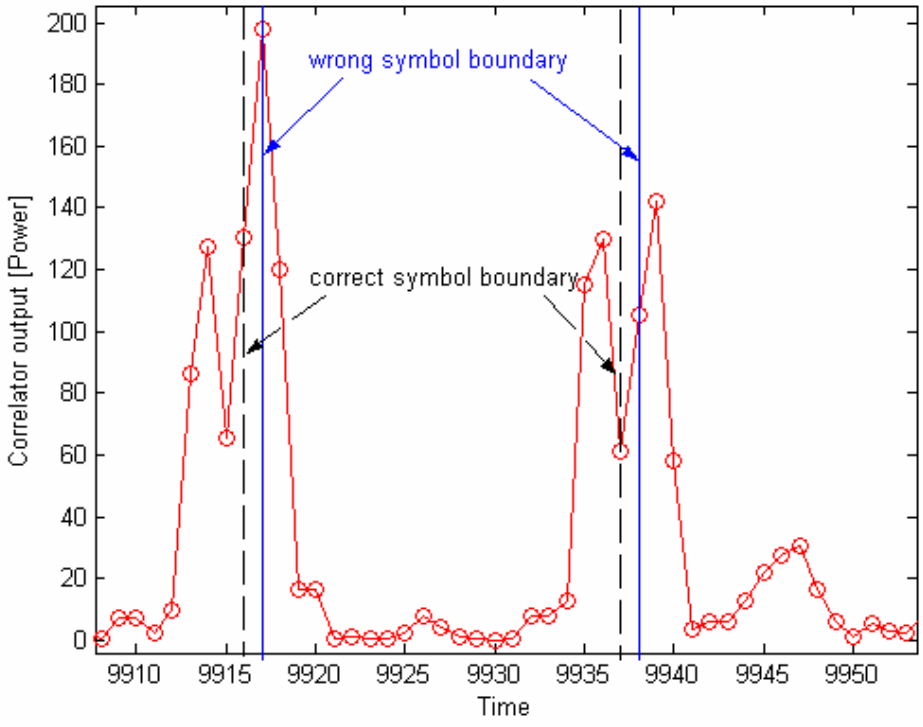



Figure 3-3 Symbol boundary under AWGN and IEEE Multipath

### 3.3.2 Symbol boundary decision after timing acquisition

After the timing synchronization, the sampling clock rate will be turn to down sample. So, another symbol boundary decision method is needed to keep tracking accuracy. When down sample and timing acquisition finish, the sampling clock phase is nearly optimum sample clock phase. The peak information is not like Figure 3-3. Figure 3-5 shows the symbol boundary after timing acquisition, the two solid lines is defined the symbol boundary by the peak information. The information of peak_loc and pre_peak_loc are also used in this work. Figure 3-6, the numbers 1, 2 mean the priority that would be chosen to be the symbol boundary. That is there are three results of equations and then the chosen symbol boundary is according to the priority of the decision rule. And the decision rule could be formulated as

$$symbol\_bounday = \begin{cases} peak\_loc & \triangle 1 = \triangle 2 \\ peak\_loc & \triangle 1 \neq \triangle 2 \,\&\, \triangle 1 > \triangle 2 \\ pre\_peak\_loc & \triangle 1 \neq \triangle 2 \,\&\, \triangle 1 < \triangle 2 \end{cases} \quad \text{.....(3-8)}$$

$$where \triangle 1 = peak\_loc, \triangle 2 = pre\_peak\_loc$$

### 3.4 The proposed timing synchronization algorithm

### 3.4.1 Timing synchronization introduction

The interfaces of RF and baseband data are DAC in the transmitter and ADC in the receiver side. The ADC is the first stage of baseband, so it dominates the receiving signal to noise ratio (SNR). To perform synchronization, the sampling rate of ADC has to be at least double higher than the incoming signal by Nyquist theorem. So, in the proposed platform is used two times sampling for timing synchronization. To get the highest input SNR, the ADC is hoped to sample at the eye open position where it has the maximum signal power as shown in Figure 3-7, sampling phase number 1. However, the initial sampling phase could be anywhere in the eye diagram, so timing synchronization is necessary. The eye diagram will be not obvious to see eye open option under AWGN and

multipath. Figure 3-8 shows the eye diagram under the situation of only AWGN; in this figure quadrature is zero because the imaginary part is constant. Figure 3-9 shows the eye diagram under the situation of AWGN and multipath. The ADC has two kinds of clock source: free running clock and phase lock loop (PLL) output clock. With free running clock, this method also called non-synchronous sampling or fix sampling, clock frequency and phase are fixed. Once timing error estimated, the compensation would be performed with interpolator [7] [8].

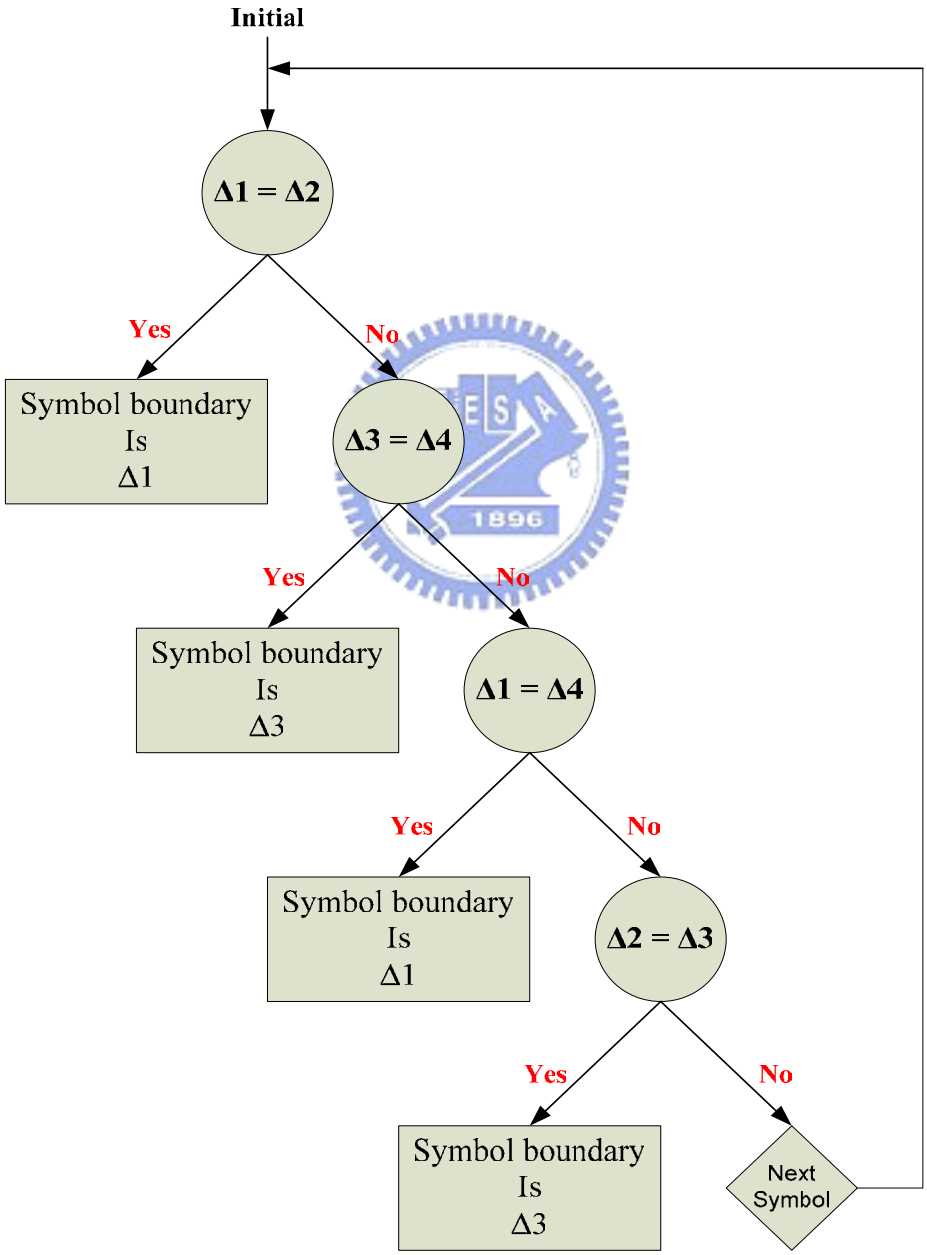



Figure 3-4 The symbol boundary decision rule before timing acquisition

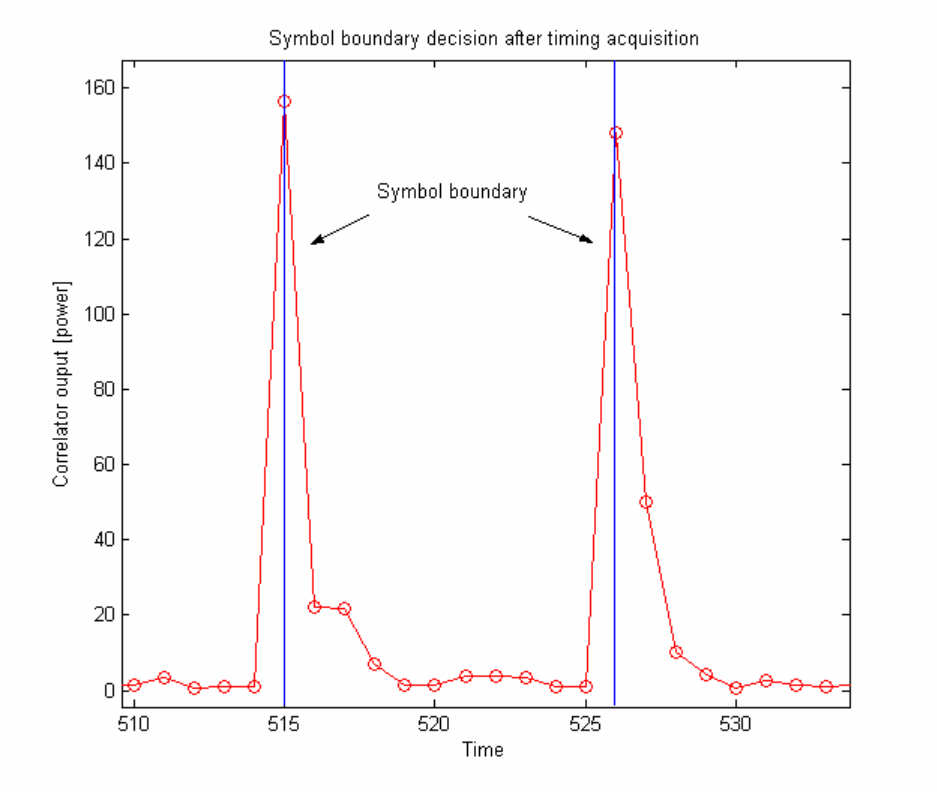



Figure 3-5 Symbol boundary after timing acquisition

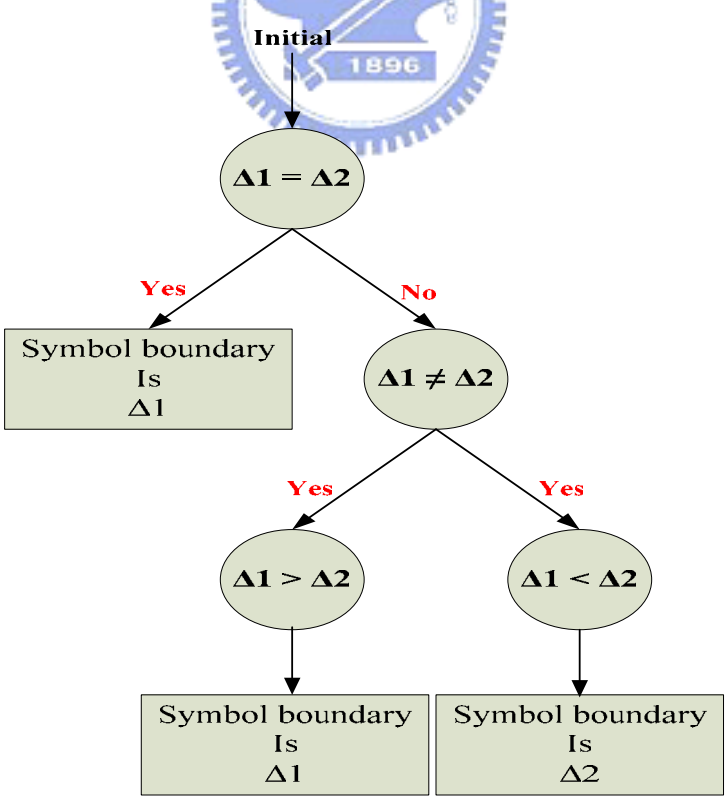



Figure 3-6 The symbol boundary decision rule after timing acquisition

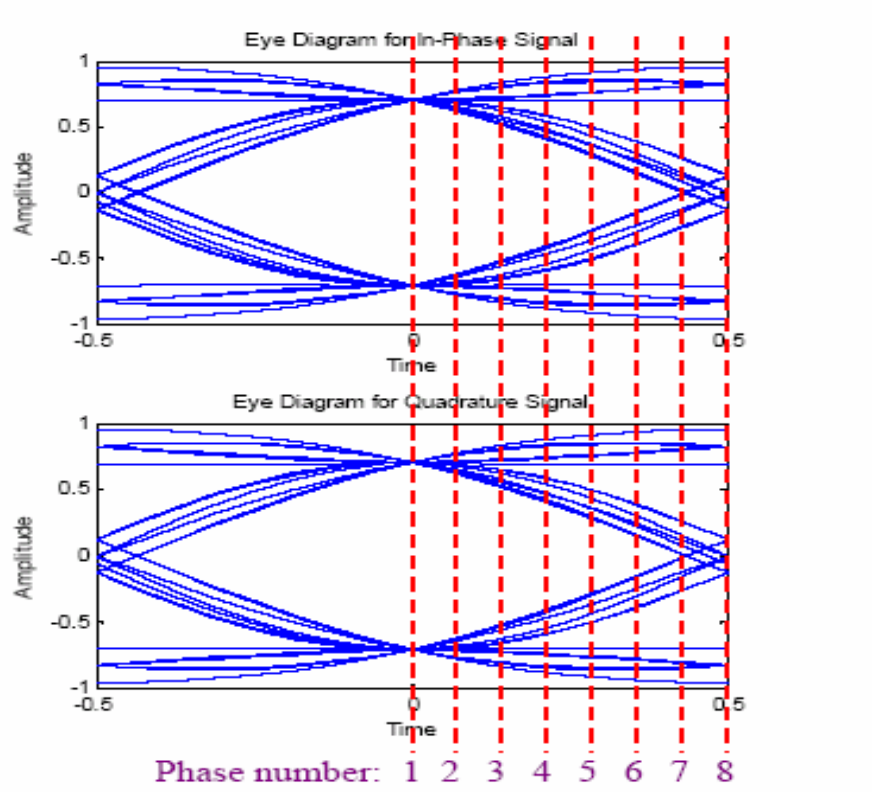



Figure 3-7 Eye diagram with different sampling phase

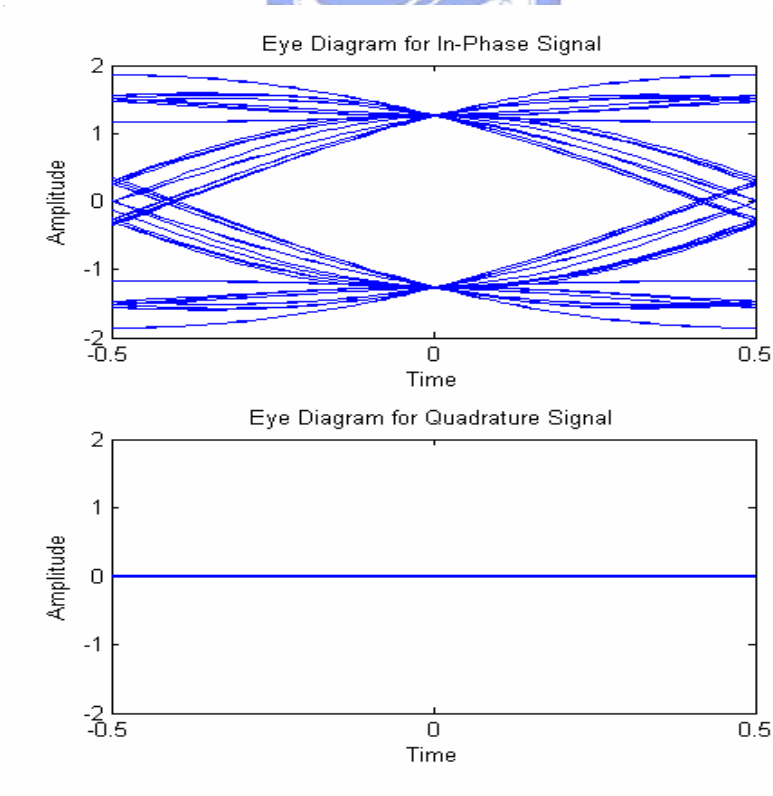



Figure 3-8 The eye diagram under the situation of only AWGN

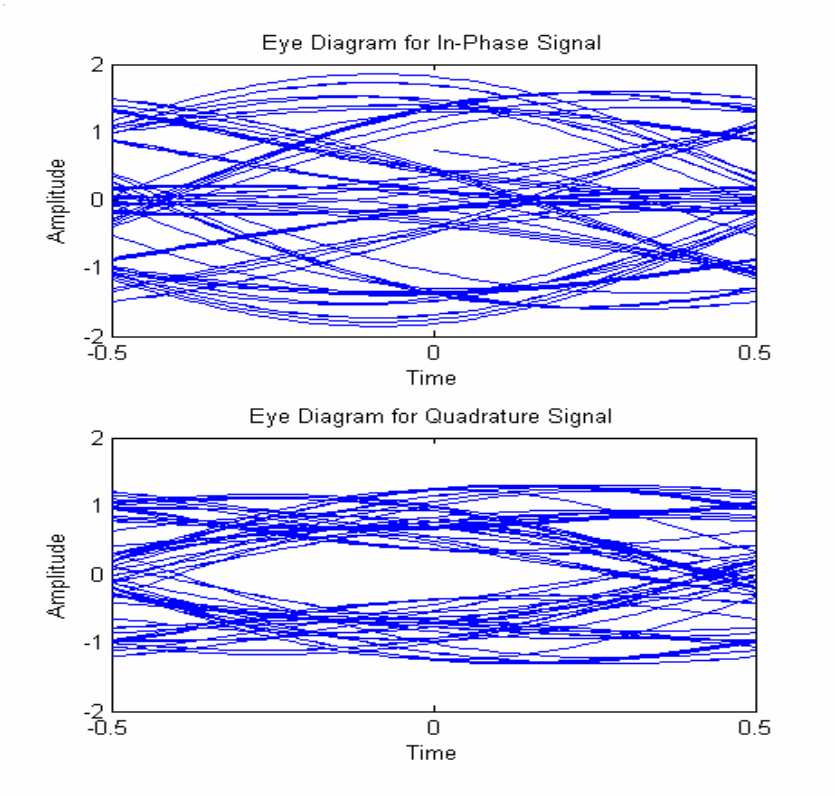



Figure 3-9 The eye diagram under the situation of AWGN and multipath

With PLL output clock, also called synchronous sampling or dynamic sampling, it receives the timing error and adjusts its frequency and phase to compensate the error. Figure 4-10 shows the block diagram of fix sampling. The clock source is a free running clock which frequency requires being close to the desired. Timing error detector (TED) [9] estimates the timing error from the demodulator output and feeds it to the interpolator and decimator to compensate the error. The decimator is to add or remove one sample point, whenever the timing error accumulates up to one sample.

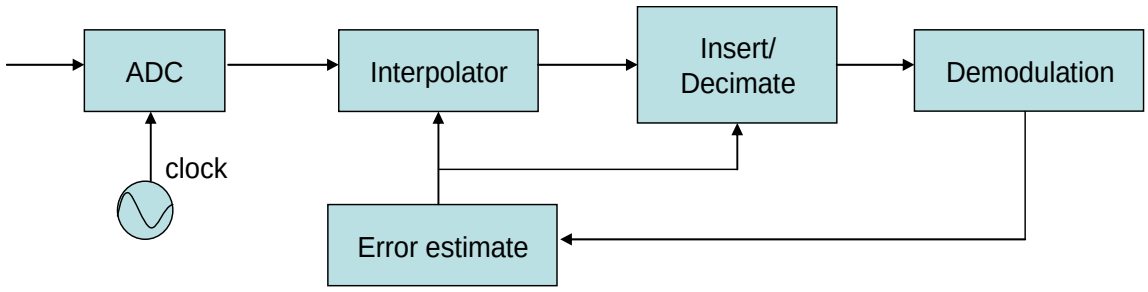



Figure 3-10 The block diagram of fix sampling

Figure 3-11 illustrates the block diagram of dynamic sampling. The clock source is the PLL output. Different from the usual, the proposed PLL is implemented with all-digital circuits, and replaced by all-digital delay lock loop (ADDLL) [10] which has the same function and similar architecture as PLL. ADDLL would adjust the sampling clock frequency and phase directly once the timing error is estimated. It would not induce inter symbol interference (ISI) like interpolator and has better performance with less cost.

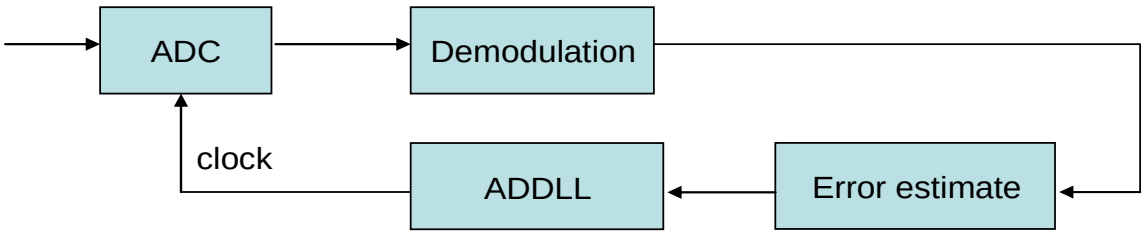



Figure 3-11 The block diagram of dynamic sampling

The dynamic sampling is batter than fix sampling, however traditional approach almost is the mix mode design [11] [12]. — the mix mode design usually pay a cost more expensive than all-digital design. In this thesis, the timing synchronization algorithm is chosen dynamic sampling method to compensation the error phase. Before timing synchronization, the ADC in the receiver samples the input signal with the initial phase which could be any one of the proposed algorithm to provide initial the sample phases, and after timing synchronization, make the sample clock phase sample correct on the eye open position, or the peak of the sinc. The timing synchronization includes two parts: the first is timing acquisition; another is timing tracking. In the proposed platform, the timing synchronization to provide the 32 sampling phases with match filter and Dynamic sampling technology, to ensure sample correctly. Hence this method is precisely more than 8 sampling phases. In this thesis, it is proposed three methods of timing acquisition algorithm, which are general [13], extend buffer, and dual-correlator differential based method; and one method about timing tracking combine with dual-correlator differential based method, but this thesis focus on timing acquisition algorithm. In order to resist both AWGN and multipath channel effect, the dual correlator differential based of timing acquisition method can make and lock sample clock phases within four “correct” phases.

### 3.4.2 The proposed timing acquisition method

#### 3.4.2.1 The general timing acquisition [13] method

In the transmitter passband, the transmitting signal is

$$s_p(t) = s(t) \bullet B \bullet e^{j2\pi f_c t} \quad \text{.....(3-9)}$$

where $f_c$ is the RF carrier frequency at the transmitter. And in the receiver passband

$$\begin{aligned} R_p(t) &= s_p(t-\tau(t)) \bullet e^{-j2\pi f_{c'} t} \quad \text{.....(3-10)} \\ &= s(t-\tau(t)) \bullet B \bullet e^{j2\pi f_c t} \bullet e^{-j2\pi f_{c'} t + \Delta\theta} \\ &= s(t-\tau(t)) \bullet B \bullet e^{j2\pi (f_c - f_{c'}) t + \Delta\theta} \\ &= s(t-\tau(t)) \bullet B \bullet e^{j2\pi \Delta f t + \Delta\theta} \\ &= \mathrm{Re}(s(t-\tau(t)) \bullet B) \bullet \cos(2\pi \Delta f t + \Delta\theta) + \mathrm{Im}(s(t-\tau(t)) \bullet B) \bullet \sin(2\pi \Delta f t + \Delta\theta) \end{aligned}$$

where $f_{c'}$ is the RF carrier frequency at the receiver, $\Delta f$ is the CFO, $\Delta\theta$ is the phase offset, $\tau(t)$ is he clock sampling rate. The timing synchronization algorithm is proposed to eliminate $\tau(t)$. The clock drift sinc waveform is show Figure 2-7. From this figure, it can see the sample clock phase shifted as time goes by. So, in the receiver signal must to synchronize the clock sample rate same as transmitter signal. The general timing acquisition method [13] is based on the early-late algorithm [14] [15] [16], using the PN correlator output to calculate the error function. In this work, PN correlator is Barker correlator. The proposed error function is defined as

$$e(\tau) = \underbrace{P_{cor}(nT+\tau)}_{Late} - \underbrace{P_{cor}(nT-\tau)}_{Early} \quad \text{.....(3-11)}$$

where $P_{cor}$ is a barker correlator output, and $nT$ is period of correlator output, and $e(\tau)$ is error function value. In this method, the best timing is place where timing error is to zero, or the solution of

$$e(\tau) = 0 \quad \text{.....(3-12)}$$

In the general timing acquisition algorithm, the differential threshold method is used to estimate the compensate sample clock phase error. It is chosen how many symbol counts to calculate error function, according the simulation can find best choice number is equal

four, not two or eight, because the timing acquisition is need to complete within 20 symbols for our system specifications. Figure 3-12 shows the general timing acquisition method based on early-late algorithm how to select of barker correlater output to calculate the error function. In Figure 3-13, it shows the general timing acquisition method state diagram. In this method, it can work well under no channel effect. But it doesn't work well under AWGN or multipath channel effect, because the error function is not suitable irresistible to AWGN or multipath. Figure 3-14 shows why this error function is irresistible to AWGN or multipath, because error function haven't clearly distinguishable situation; it can see the error function error range very large by AWGN or multipath effect. Figure 3-15 shows the sample clock phase error is used the general timing acquisition method under AWGN. In the figure, it could see phase error difference is large, because the error function is changed by the correlator power. In order to perform under AWGN, the modified method will be proposed.

### 3.4.2.2 The extend buffer timing acquisition method

The method is modified the general acquisition method based on the early-late algorithm, using the correlator output to calculate the error function, where the proposed error function is defined as

$$e(i)=\underbrace{\sum_{i=1}^{21}P_{cor}(nT+\frac{T}{2}-i)}_{Late}-\underbrace{\sum_{i=1}^{21}P_{cor}(nT-\frac{T}{2}+i)}_{Early} \quad \text{.....(3-13)}$$

In this method, the best timing is place where timing error is approximate to zero, or the solution of

$$e(i)\approx 0 \quad \text{.....(3-14)}$$

In the extend buffer acquisition method, the differential threshold method is used to estimate the compensate error phase. Figure 3-16 shows the extend buffer timing acquisition method state diagram. In this method, it is chosen symbol is equal four. Figure 3-17 shows the extend buffer method based on early-late algorithm how to select of barker correlater output to calculate the error function. In this method, it can work well under AWGN channel effect. But it can not work under multipath channel effect, because

the error function is not suitable irresistible to multipath. Figure 3-18 shows why this error function is irresistible to multipath, because error function haven't clearly distinguishable situation; here see that error function range not very large, and haven't the clearly region. Figure 3-19 shows the sample clock phase error used the extend buffer timing acquisition method under IEEE multipath. In the figure, it could see phase error difference which is large and have to move up and down situation. In addition, the proposed platform under AWGN and multipath has filter effect to make error function variation. In order to solve perform problem under multipath and filter effect, the dual correlator differential based method can be proposed.

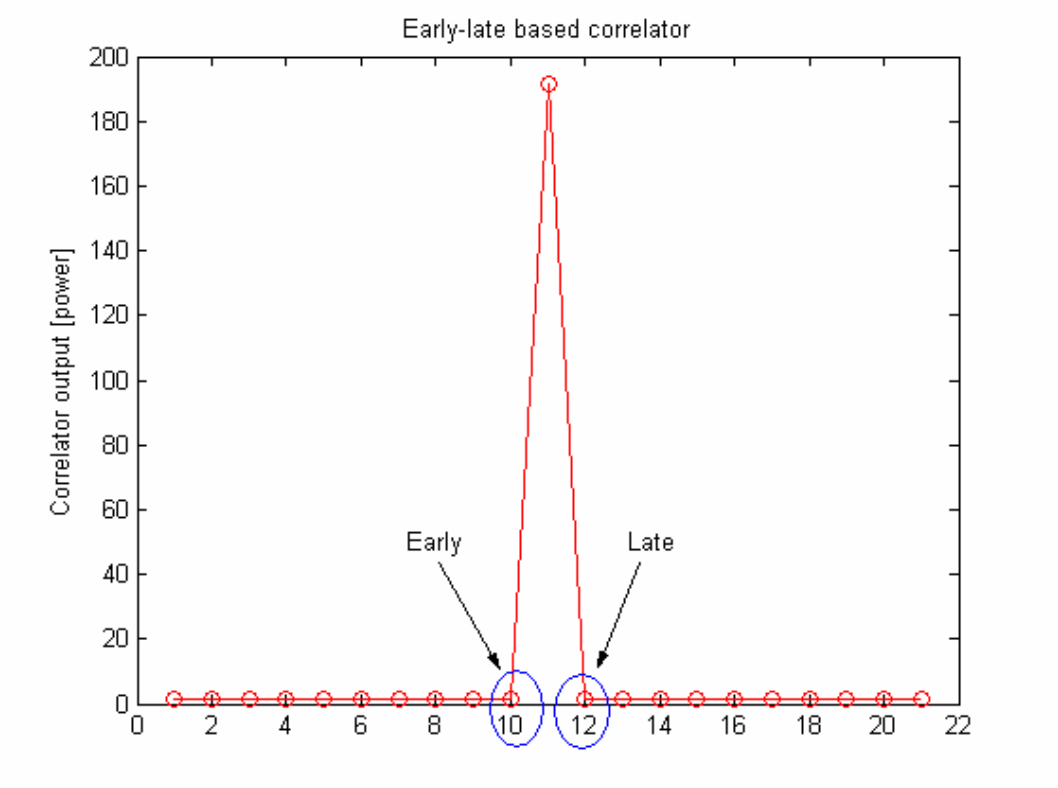



Figure 3-12 The general method of early late algorithm

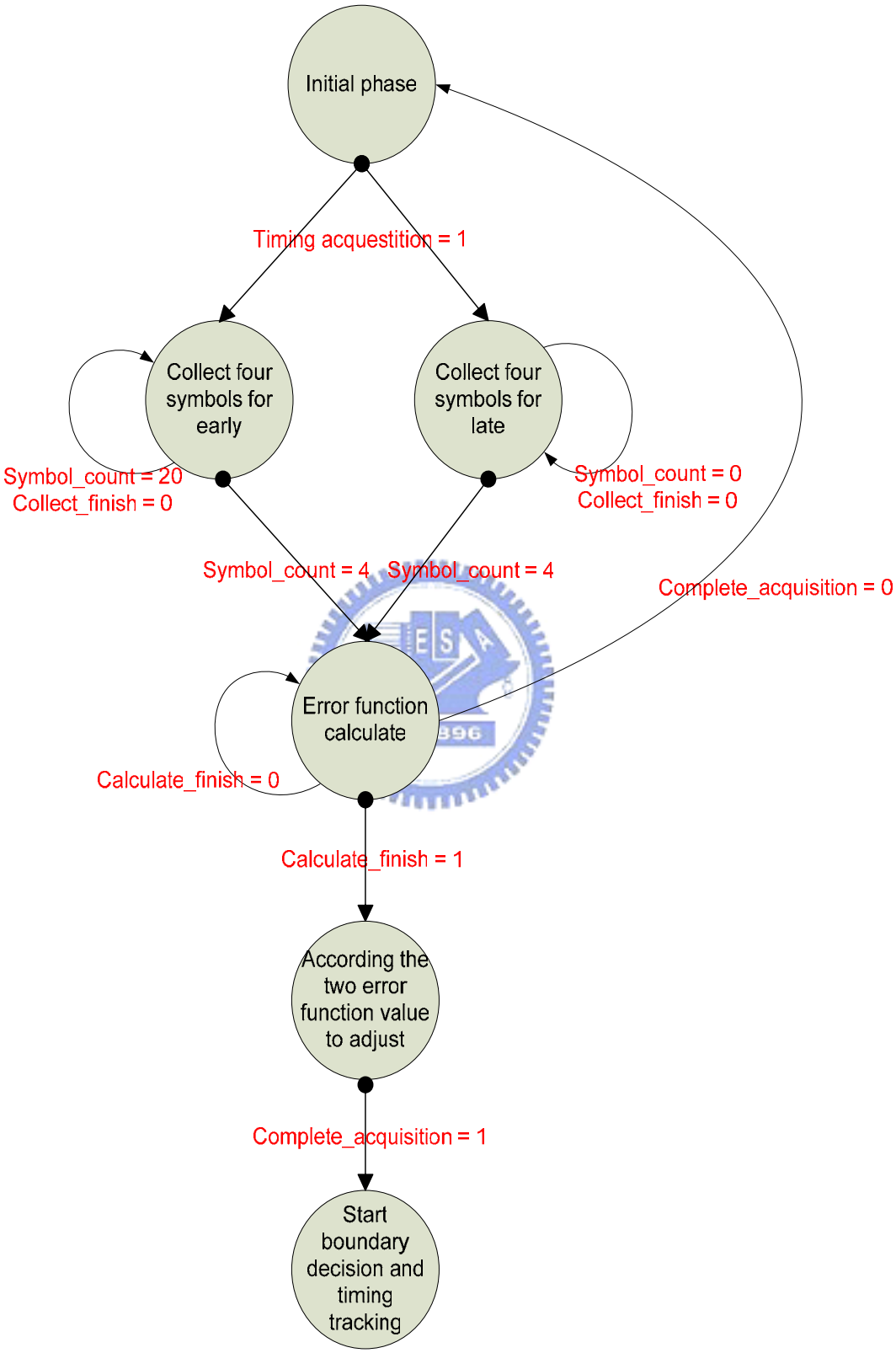



Figure 3-13 The state diagram of the general timing acquisition algorithm

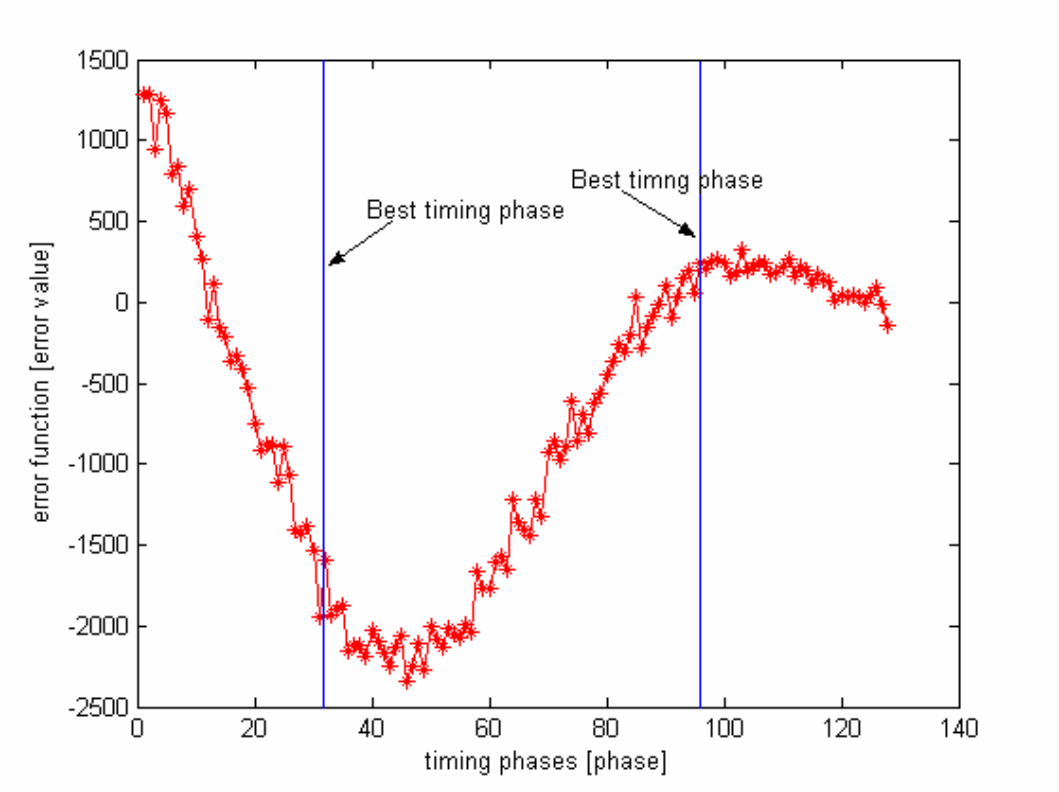



Figure 3-14 The error function versus timing phases under AWGN

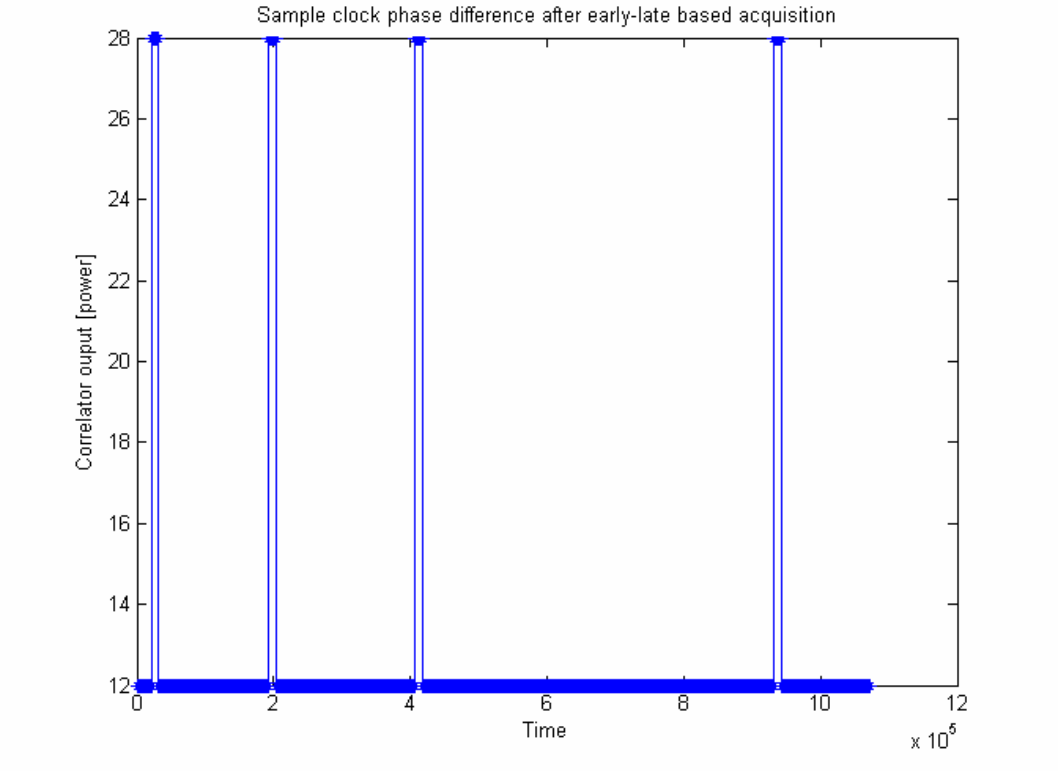



Figure 3-15 The sample clock phase error after general acquisition method

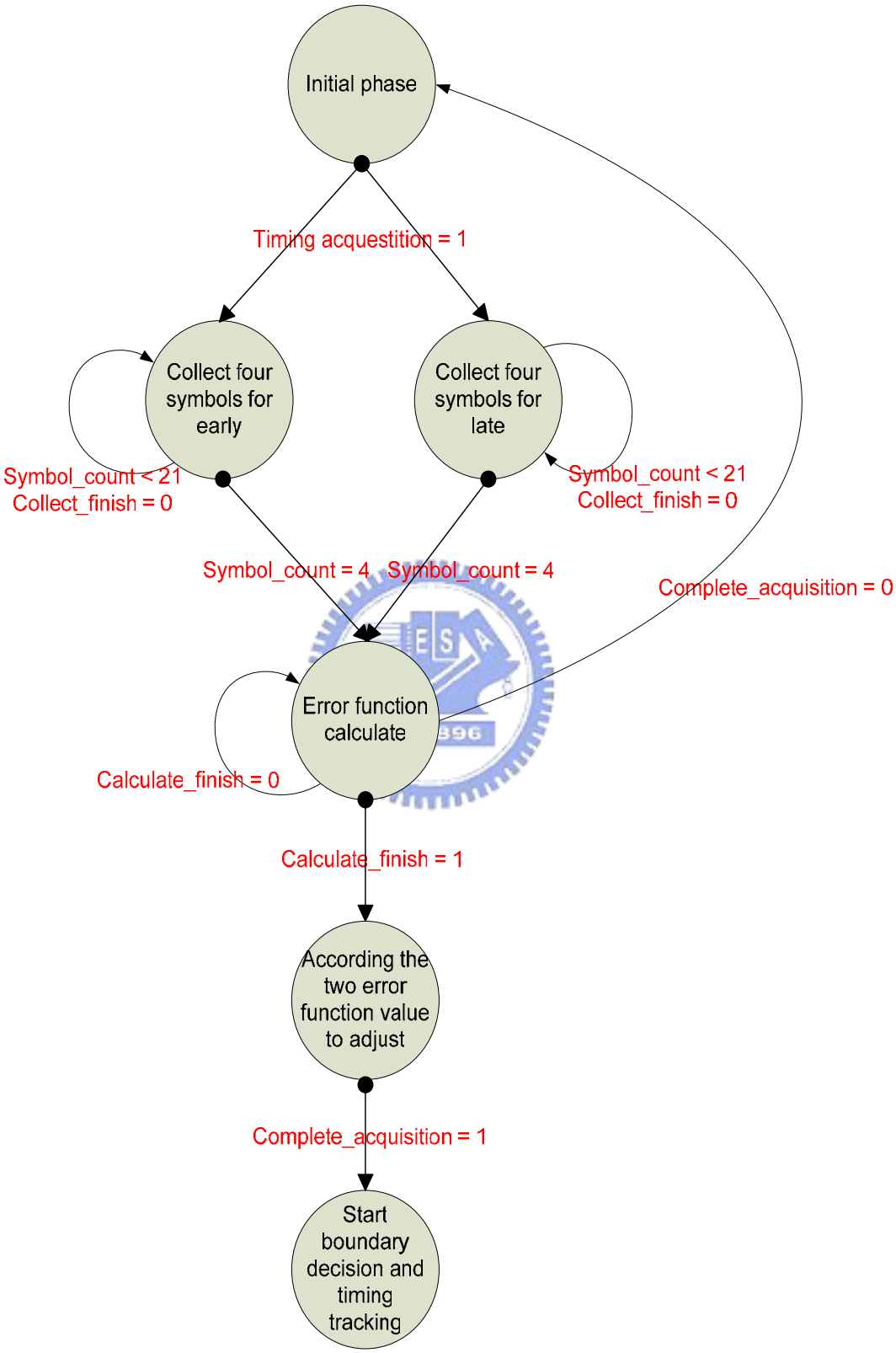



Figure 3-16 The state diagram of the extend buffer timing acquisition algorithm

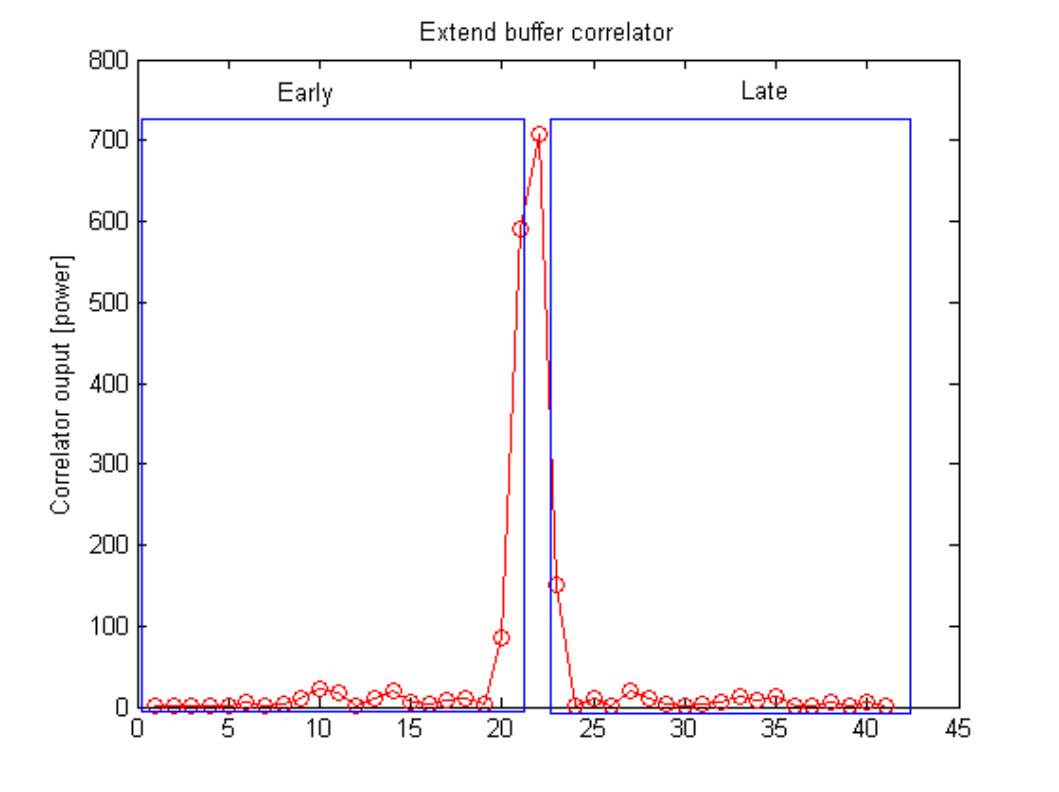



Figure 3-17 The extend buffer method of early late algorithm

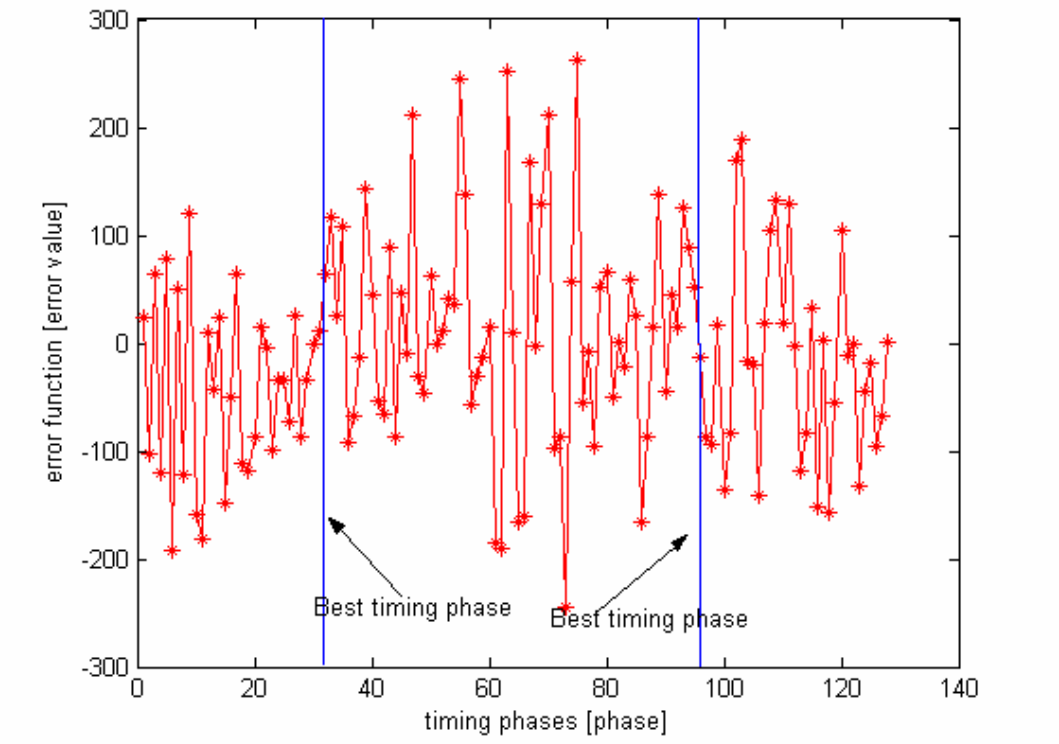



Figure 3-18 The error function versus timing phases under AWGN and multipath

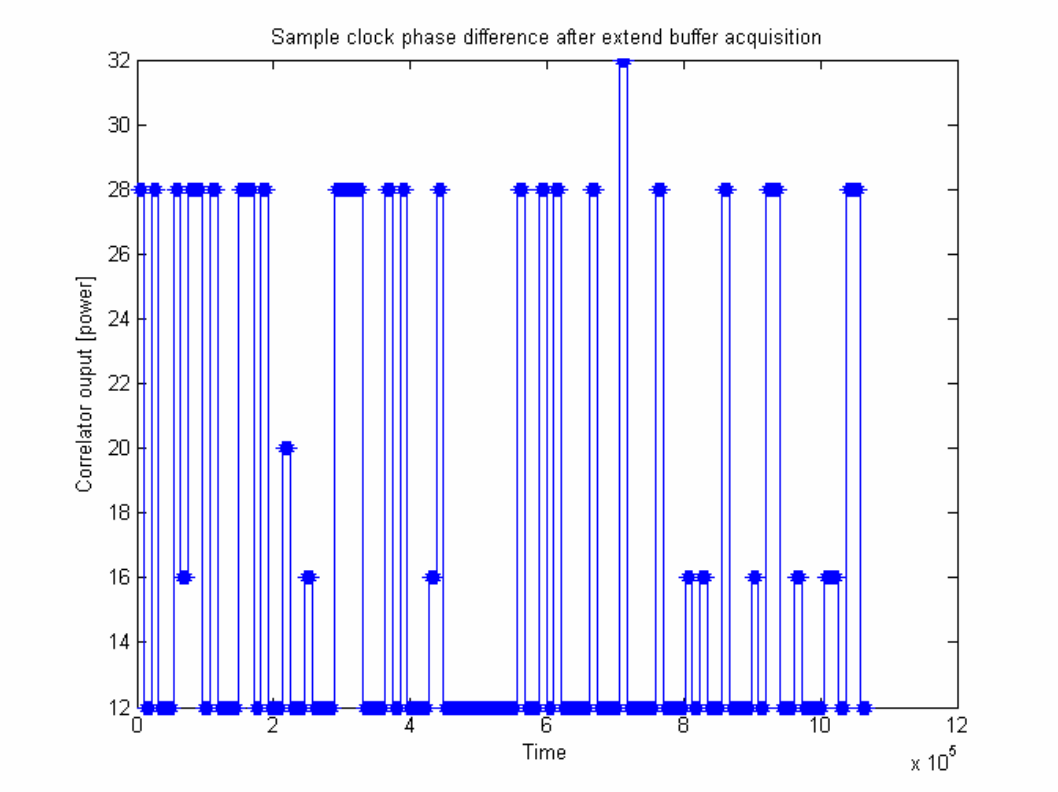



Figure 3-19 shows the sample clock phase error after the extend buffer method

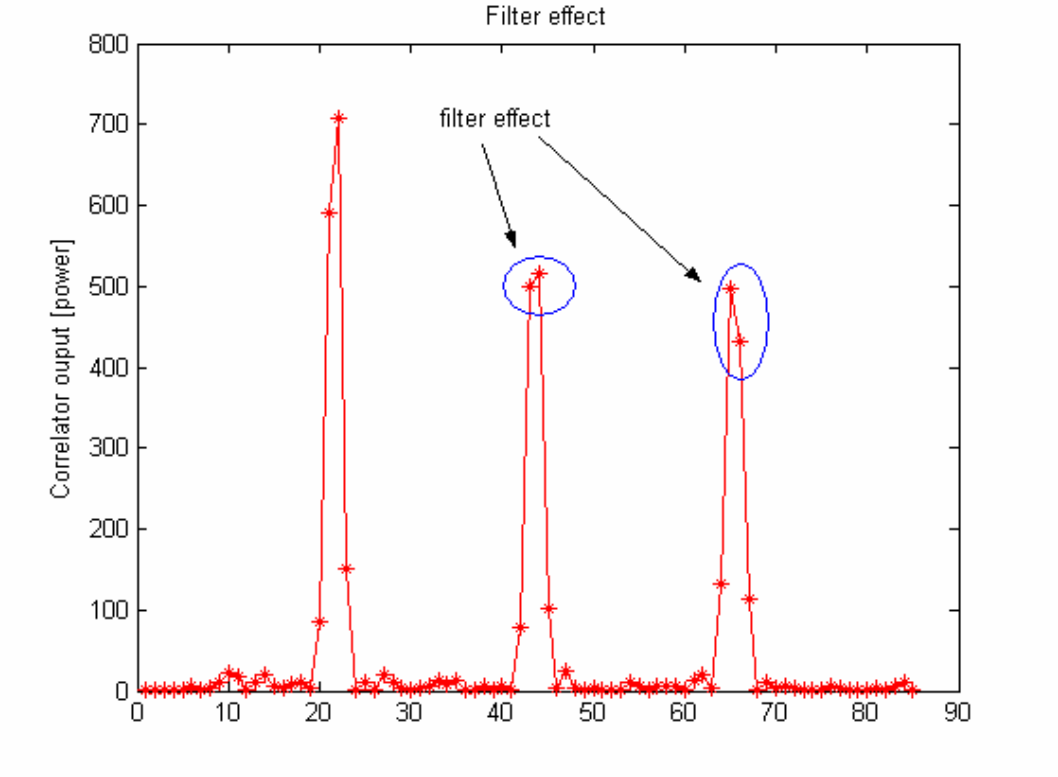



Figure 3-20 The filter effect in the proposed platform

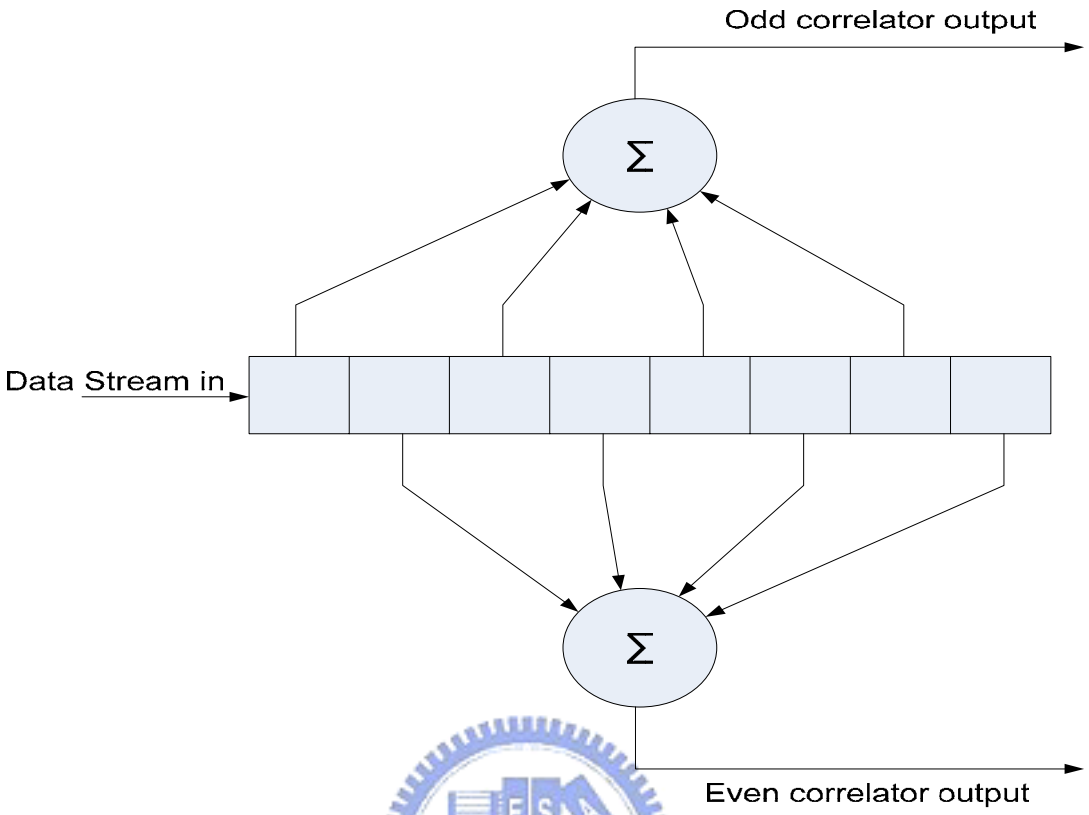



Figure 3-21 shows the dual correlator architecture

### 3.4.2.3 The dual correlator differential base timing acquisition method

The proposed method is can resistible to multipath channel effect; it also can find the filter effect occur in proposed platform. In the multipath channel with mixed filter effect are making error function variation, not is stable. Figure 3-20 shows the filter effect situation. So, the proposed method is resistible to these mix imperfections. In order to reduce filter effect and to find clearly distinguishable error function, we propose the dual correlator architecture to solve this system situation. Figure 3-21 shows the dual correlator architecture diagram, or named dual correlator differential based timing acquisition method. Figure 3-22 shows the dual correlator differential based timing acquisition block diagram. In this method, the proposed error function is defined as

$$e(i) = \underbrace{\sum_{i=-4}^{6} P_{odd\_window}(nT+i)}_{Late} - \underbrace{\sum_{i=-4}^{6} P_{even\_window}(nT+i)}_{Early} \quad \text{..... (3-15)}$$

where $P_{odd\_window}$ is odd correlator power that select method is shown in Figure 3-23; $P_{even\_window}$ is even correlator power that select method is shown in Figure 3-24. In this method, the best timing is place where timing error is approximate value at $\max(odd\_window - even\_window)$, or the solution of

$$e(i) \approx \max(P_{odd\_window} - P_{even\_window}) \quad \text{.....(3-16)}$$

The error function has max value at $odd\_window - even\_window$, it mean that sampling clock phase nearly optimum point. Figure 3-25 shows the error function versus timing phases under AWGN and multipath channel effect; it could see error function have clearly distinguishable situation. For calculate the error function accurately, four symbols correlator output are taken to estimate the error function. Figure 3-26 shows the even odd timing acquisition state diagram; where shift phase is used to adjust the sample clock phase. So, in the dual correlator differential base timing acquisition, it used to adjust the sample clock phase by slope based binary decision. As a result, the slope is defined as

$$slope = \frac{(P_{odd} - P_{even})_{shift\_2} - (P_{odd} - P_{even})_{shift\_1}}{shift2\_sample\_loc - shift1\_sample\_loc} \quad \text{.....(3-17)}$$

where shift1_sample_loc is the first sample clock phase, shift2_sample_loc is the second sample clock phase. The left side of best sample clock phase line the slope is positive, the right side of best sample clock phase line the slope is negative; that situation could find in Figure 3-25. According the slope positive or negative is used to determinate shit backward or shift forward. Figure 3 -27 shows the binary decision search flow diagram. In this figure, the shift phase means to adjust sample clock phase one of proposed 32 phases in acquisition state, the tracking phase is mean adjust sample clock phase in tracking state. The binary decision is used the local optimum property. Every times is chosen the sample clock phase better one of present sample clock phase or next sample clock phase to adjust. The next sample clock phase distance is one half between of former sample clock phase and present sample clock phase.

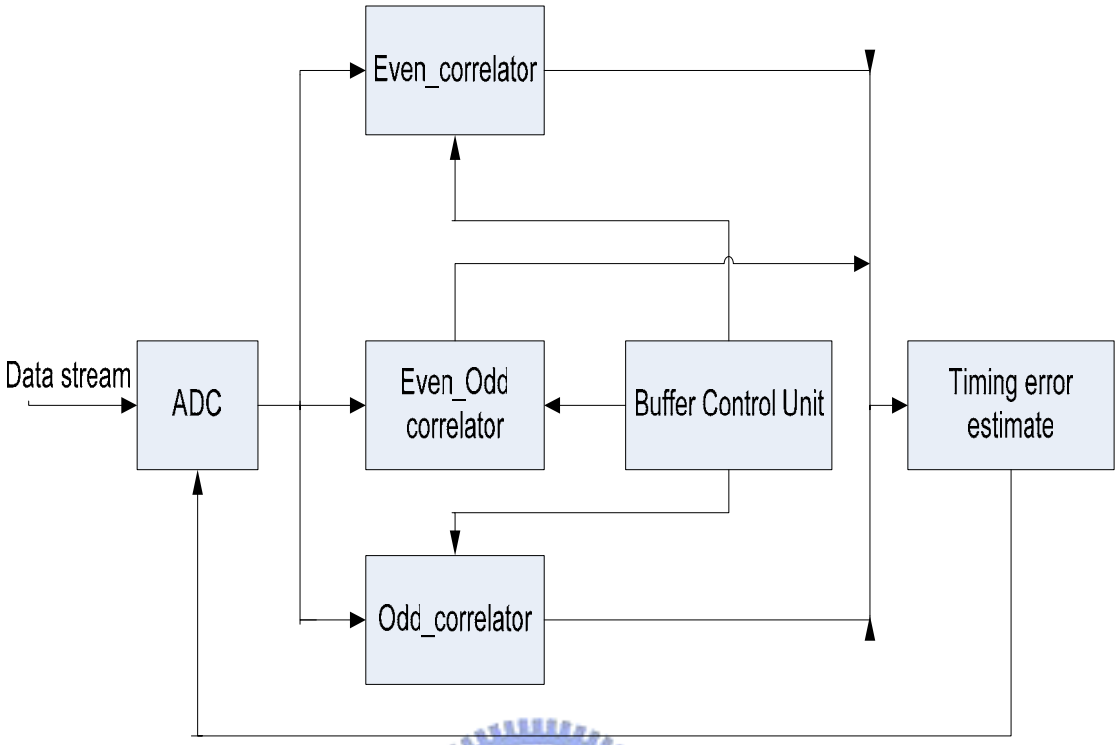



Figure 3-22 The Block diagram of dual correlator differential base timing acquisition

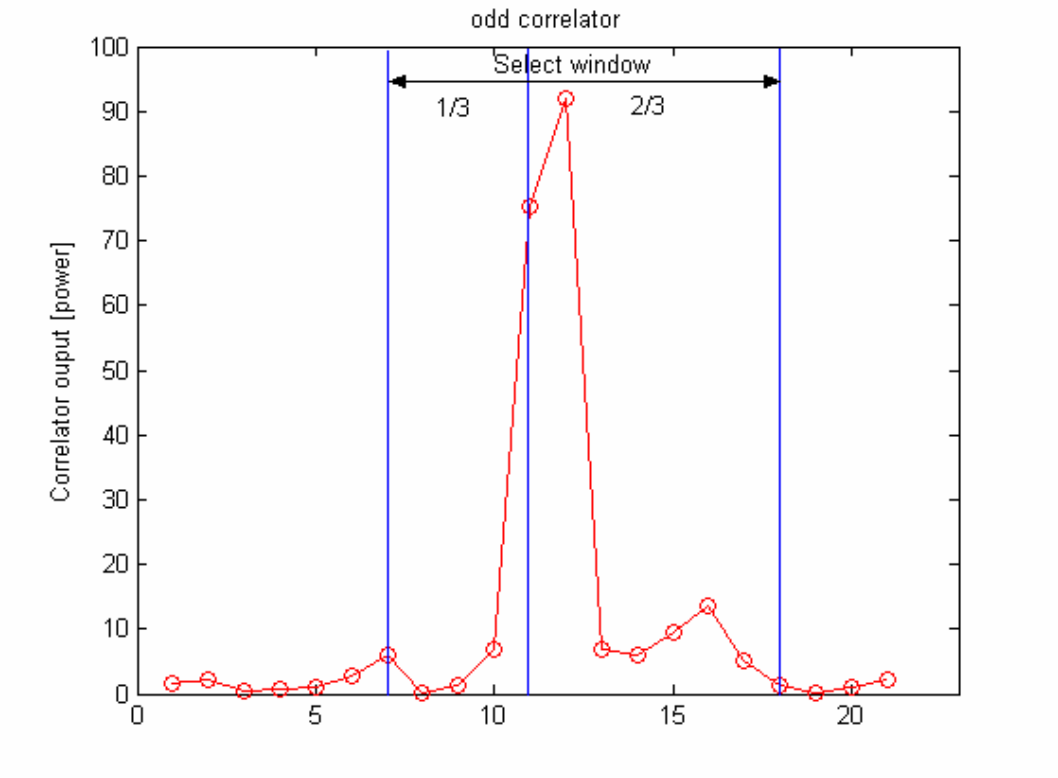



Figure 3-23 The select method of odd correlator

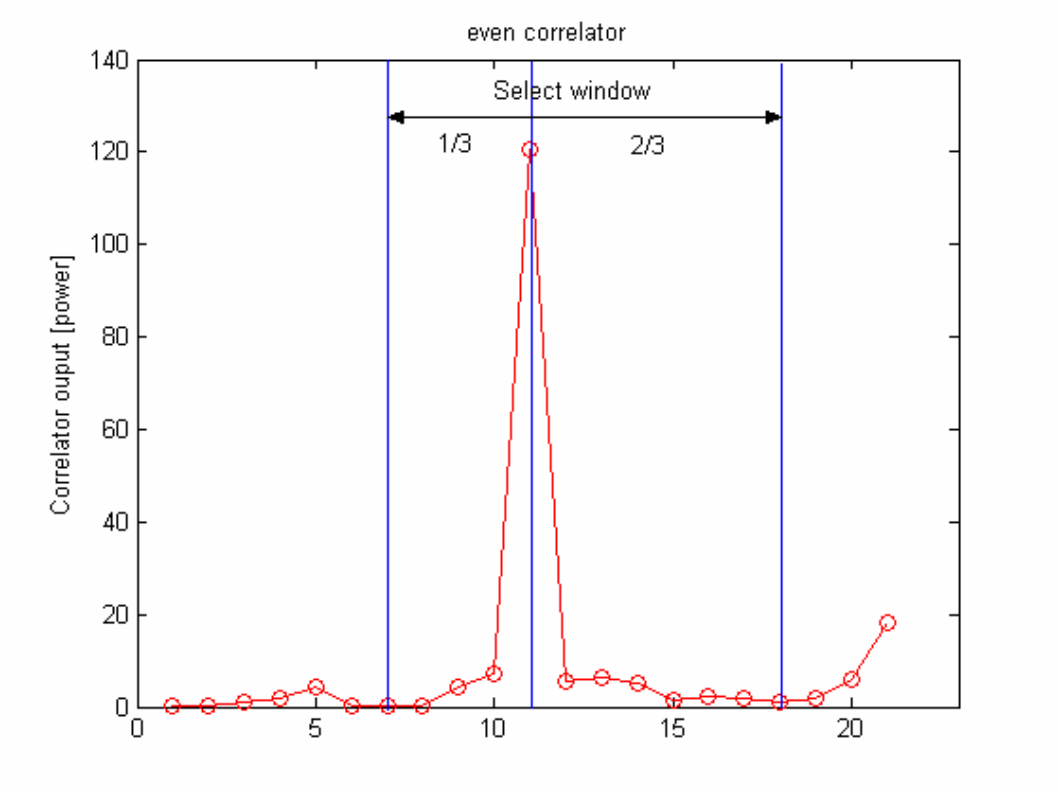



Figure 3-24 The select method of even correlator

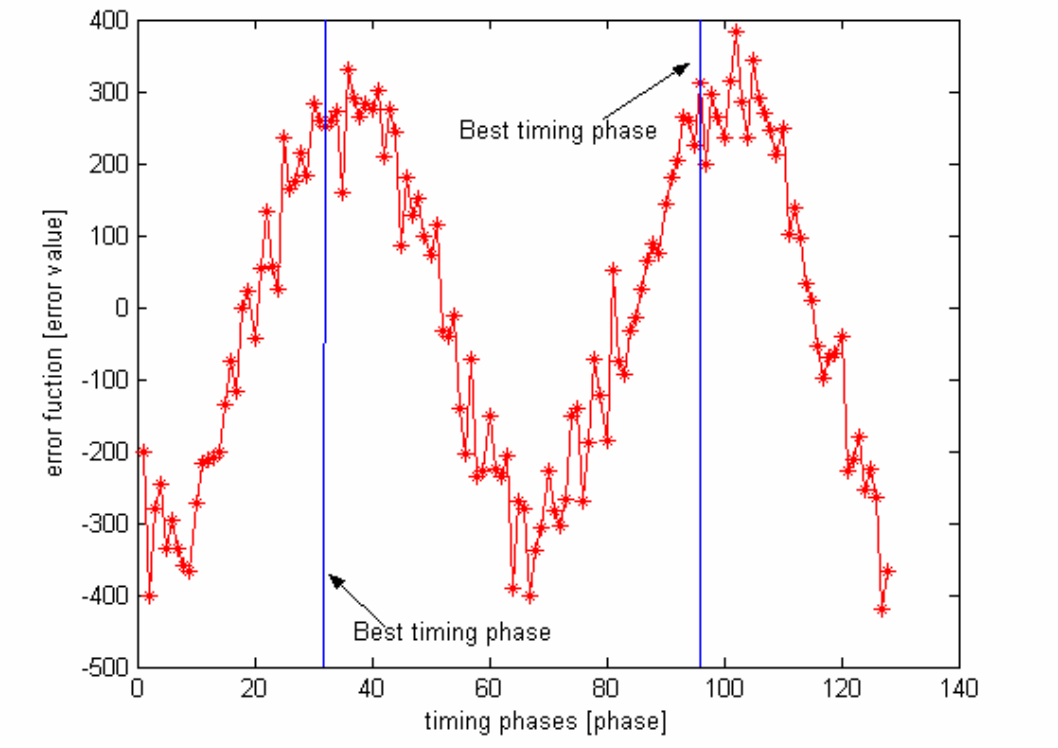



Figure 3-25 The error function versus timing phases under AWGN and Multipath

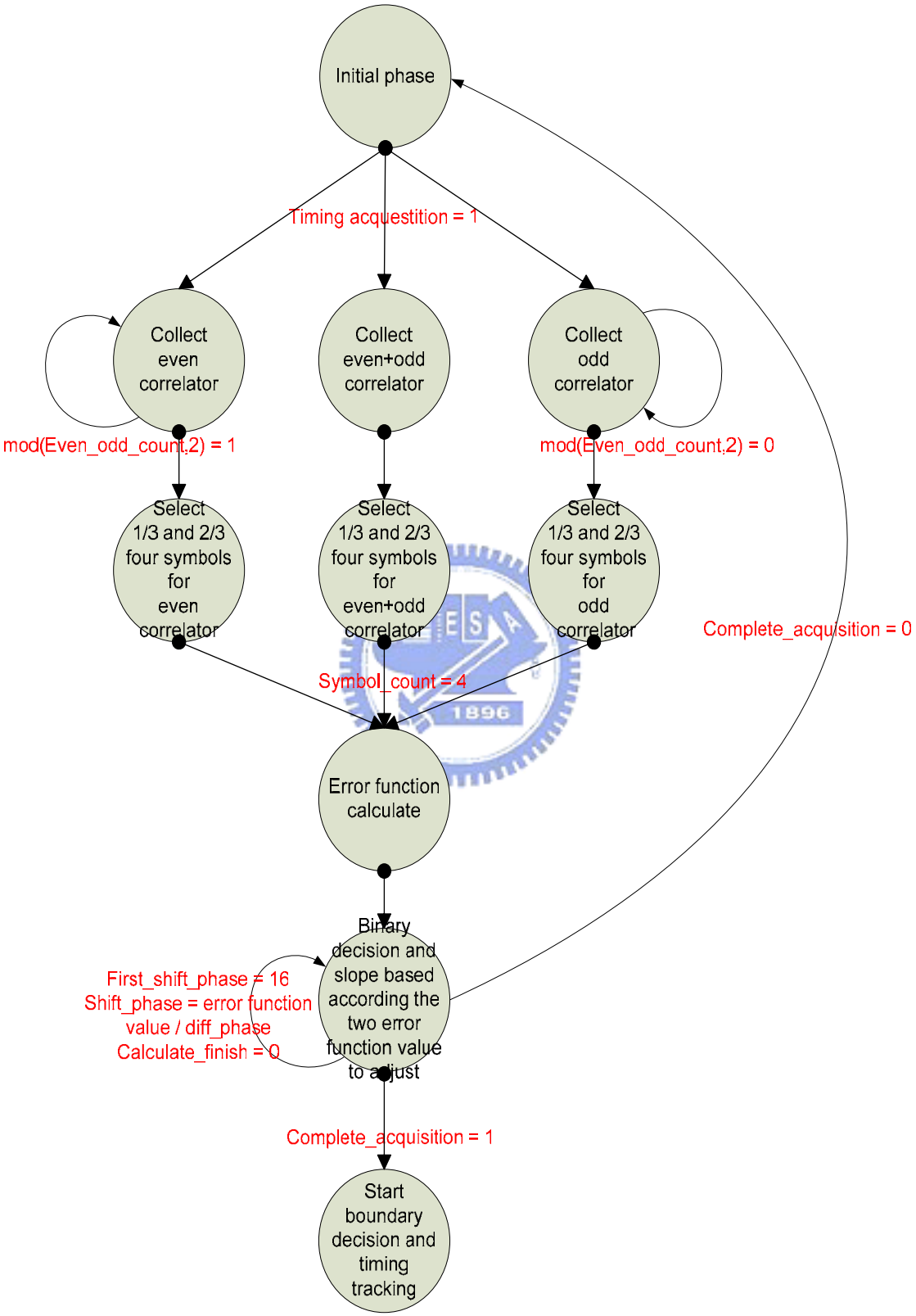



Figure 3-26 The state diagram of dual correlator differential based timing acquisition

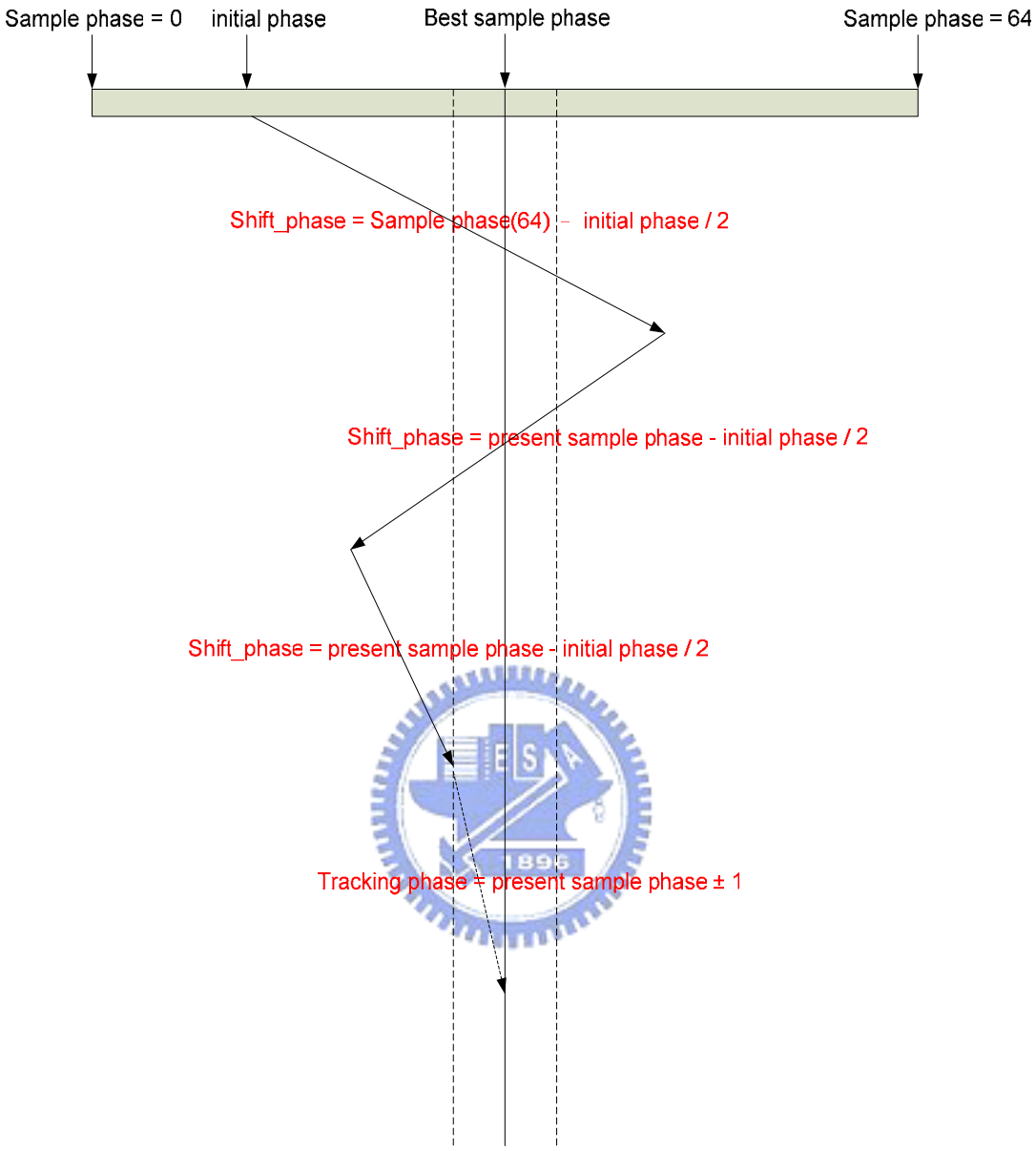



Figure 3-27 The binary decision search flow diagram

Finally, we will show some performance analysis and simulation result about third timing acquisition method. The sample clock phase error after dual correlator differential based timing acquisition at SNR= 5dB, Packet number is 100 and IEEE multipath channel effect show in Figure 3-28. In the figure, the dual correlator differential base timing acquisition can convergence at between positive four phases and negative four phases. But some seriously multipath channel effect can make the sample clock phase error is large. In the figure, it can see the sample clock phase error large situation is not usually,

so it can be reduce by timing tracking. Both Figures 3-29 and 3-30 show the situation of the received signal pass through timing acquisition with noise or noise-free. Figure 3-31 shows the MSE versus SNR of three timing acquisition method. In this figure, it can see the dual correlator differential base method will convergence. After the study one sample rate and proposed new timing synchronization algorithm is one of our future works. Finally, there make some summary and comparison. Table 3-1 shows the comparison of three proposed methods.

Table 3-1 Comparison of three proposed timing acquisition

| | *general [13]* | *Extend buffer* | *Dual correlator differential based* |
|---|---|---|---|
| *Computing Complexity* | 1 correlator (length=22)<br>1 Buffer (length=2*4+2)<br>1 comparator | 1 correlator (length=22)<br>1 buffer (length=42*4+2)<br>1 comparator | 2 correlator (length=11)<br>1 buffer (length=11*2*4+2)<br>1 comparator |
| *Robustness for DSSS* | Easily interfered by AWGN | Resistance to AWGN | Resistance to AWGN and multipath |

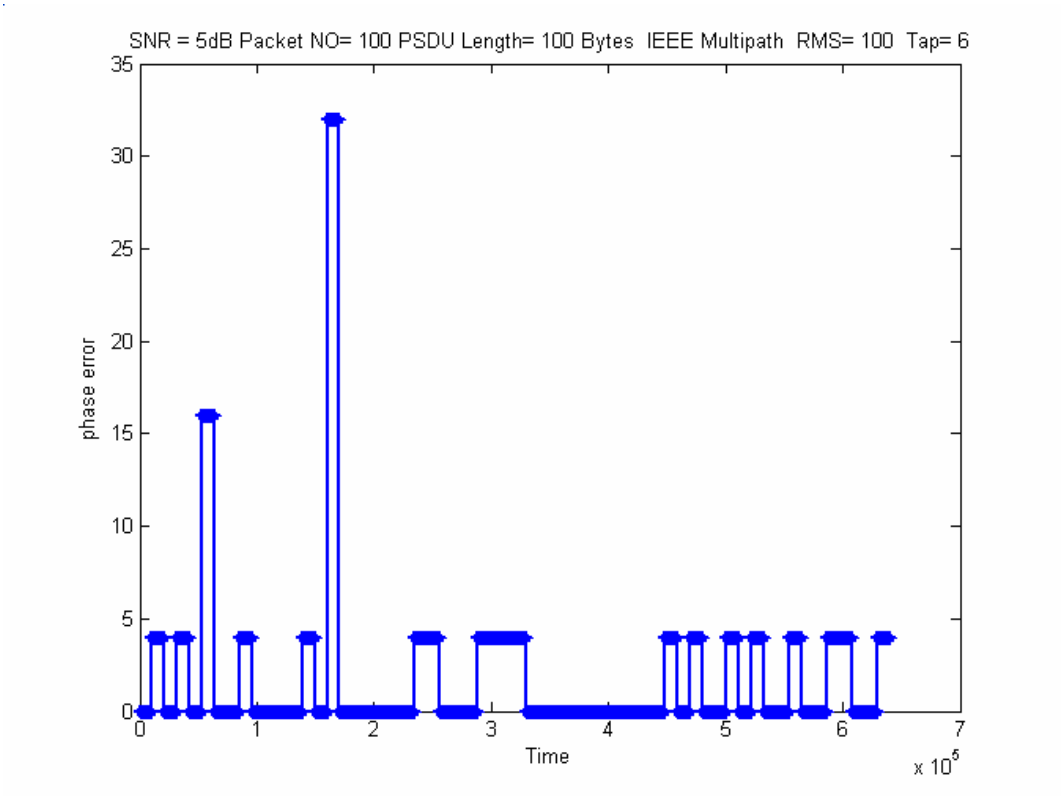



Figure 3-28 The sample clock phase error after dual correlator differential base method

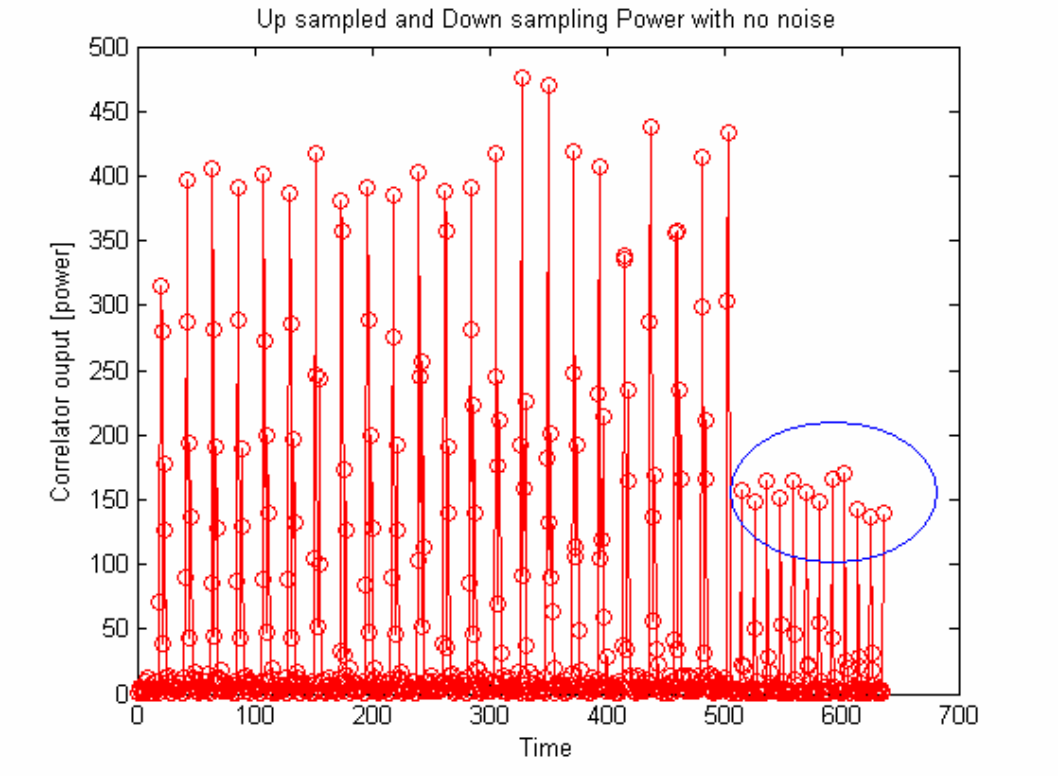



Figure 3-29 The received signal pass through timing acquisition with noise free

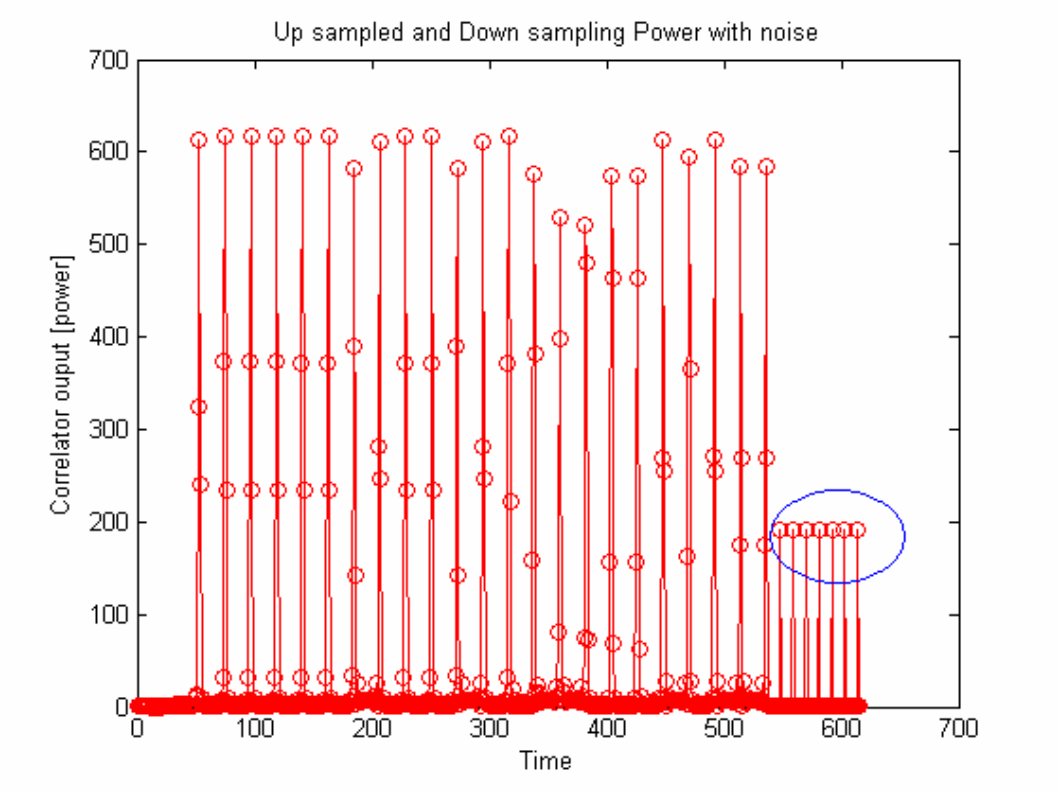



Figure 3-30 The received signal pass through timing acquisition with noise

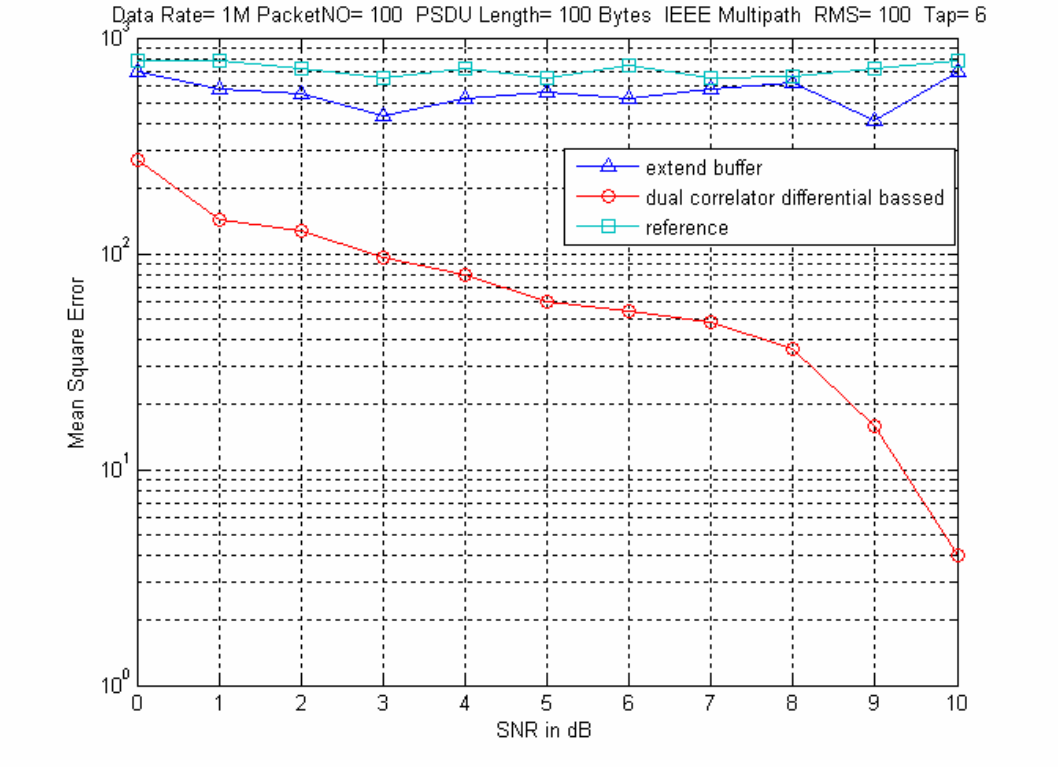



Figure 3-31 The MSE versus SNR of three timing acquisition method

### 3.4.3 The proposed timing tracking method

Because our thesis is focus on timing acquisition algorithm of timing synchronization, it is proposed one method of timing tracking algorithm [17] [18] [19]. After timing acquisition, the sample clock phase is nearly optimum sample clock phase, but the sample clock phase is to change through a span of several symbols. The sample clock phase drift is marked the performance degradation. In order to avoiding the performance degradation, the timing tracking is needed. In the timing tracking state, it is used error function is defined the same as (3-13), but in this to select of barker correlater output to calculate the error function like as dual correlator differential base timing acquisition. In this method, the best timing is place where timing error is approximate to zero, or the solution of $e(i) \approx 0$, it mean that sampling clock phase nearly optimum point. But the difference with timing acquisition, it used long span of several symbols, to make the error function have more accuracy. The timing tracking is perform until no receive any packets. This time and next time tracking is divide the span of several symbols. In timing tracking includes two parts; the first is coarse search tracking; the second is fine search tracking. In the coarse search tracking state, the first step is search region is large; the second step is search region to reduce small. Figure 3-32 shows the binary decision search flow diagram in timing tracking state. Figure 3-33 shows the state diagram of the dual correlator differential base timing tracking method algorithm.

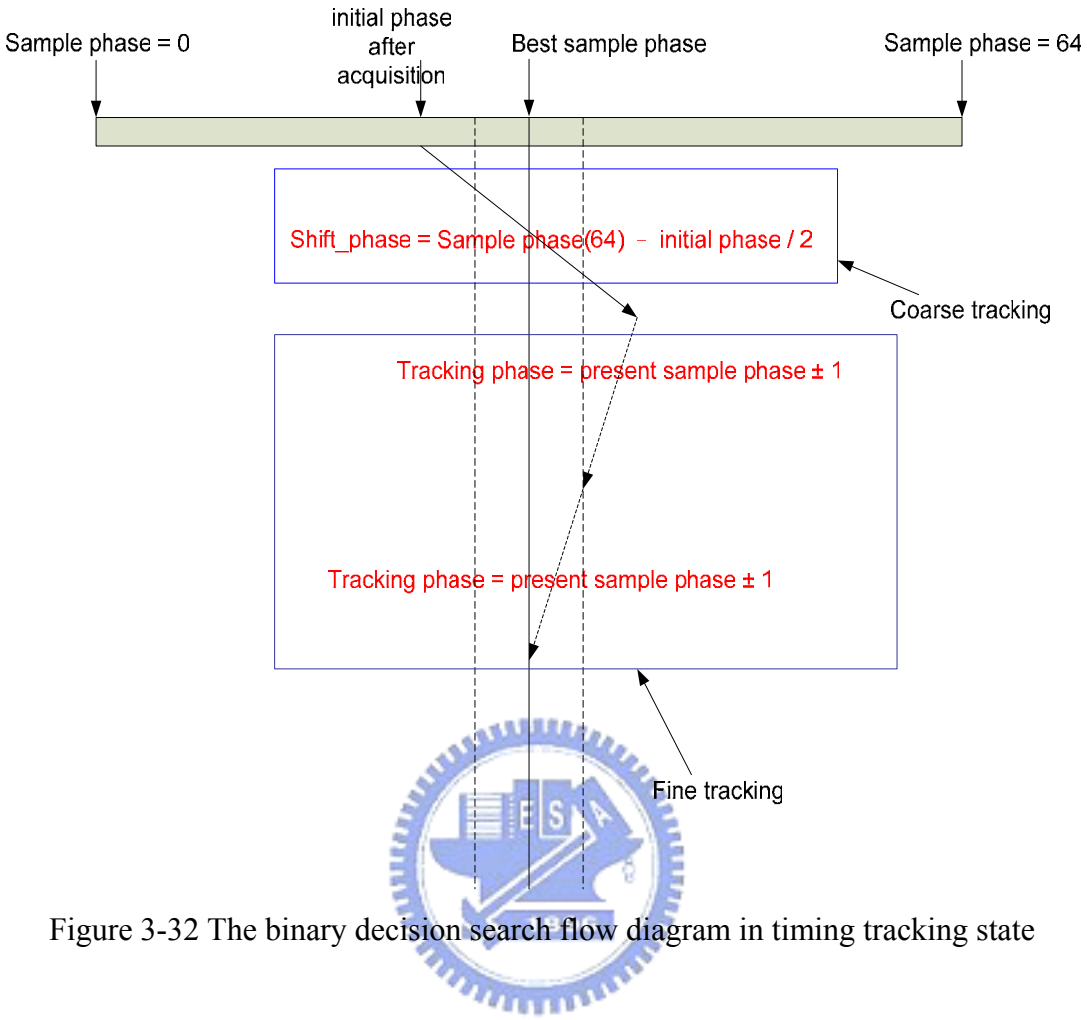



Figure 3-32 The binary decision search flow diagram in timing tracking state

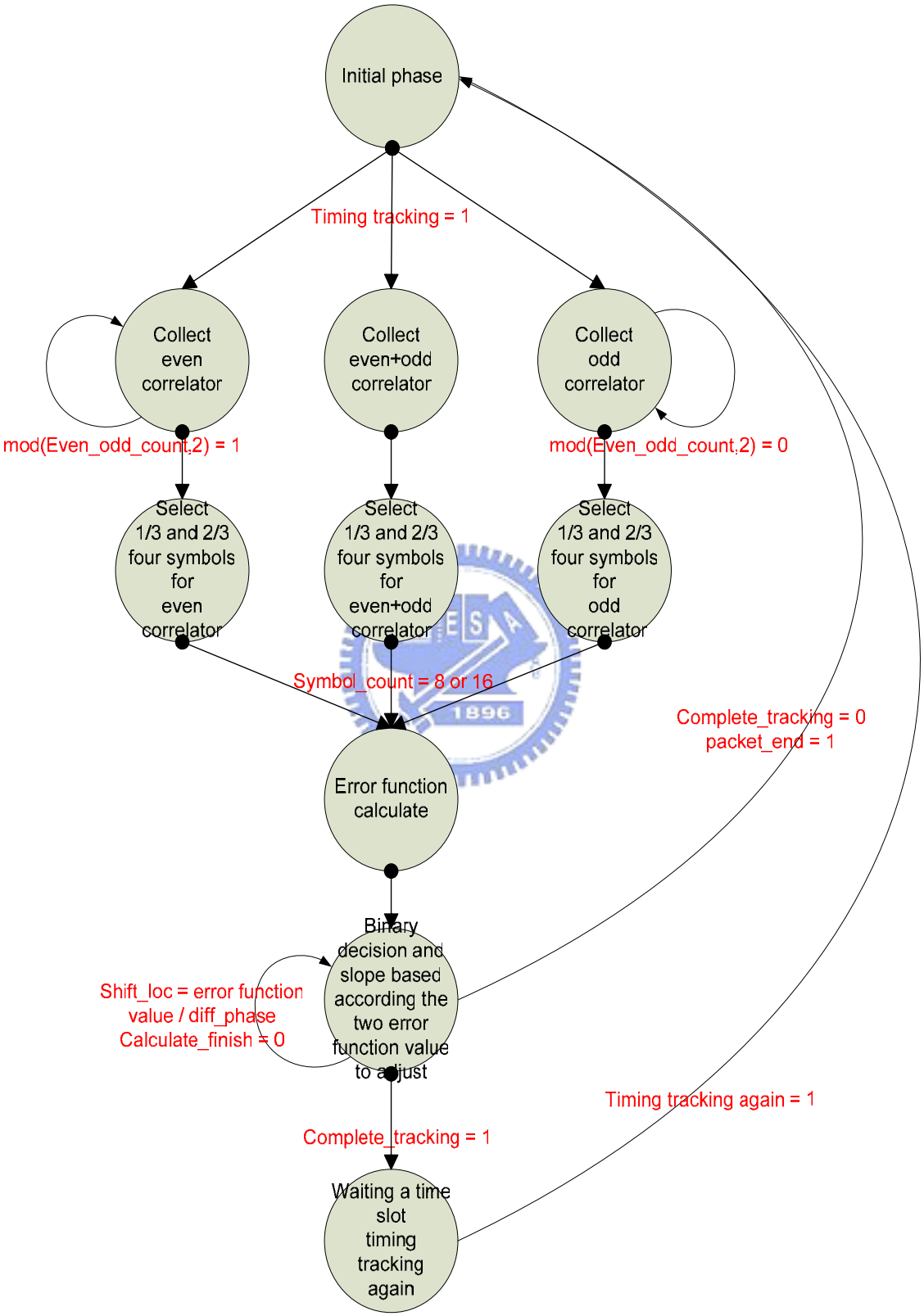



Figure 3-33 The state diagram of the dual correlator differential base timing tracking

# CHAPTER 4

# SIMULATION PLATFORM

## 4.1 Choosing a suitable tool

The architecture of system platform is shown in Figure 2-10. The initial step that we must care is that choosing a suitable tool – language. Two languages, C/C++ and Matlab are the nice choices, because these two languages have a lot of advantages during the process of constructing platform. These advantages are listed below

a. Complete standard library and document of help
b. Easy to learn programming style
c. High simulation speed
d. Quickly algorithm verification
e. Co-simulate with Verilog
f. Easily porting to HDL

Matlab is chosen as the suitable tool to construct the system platform for the reason of powerful matrix and mathematic functions, friendly Graphical User Interface (GUI), simple debugging tool and many different kinds of figure plotting functions. Although C/C++ has the highest simulation speed, but lack of mathematical functions and less friendly GUI cause us give up it to choose Matlab as the tool. Table 4-1 shows the comparison of C/C++ and Matlab.

Table 4-1 Comparison of C/C++ and Matlab

| | Comparison |
|---|---|
| C/C++ | **high simulation speed**<br>**more close to HDL** |
| Matlab | **friendly GUI**<br>**easy to debug**<br>**powerful matrix operations** |

The time that spend on constructing the basic system platform is about two months and the time that spend on algorithm verifying and debugging is about four months. The spending time is less than the expected time, because Matlab give us the most convenience on algorithm level coding and debugging. But more convenience also means that more mapping complexity between algorithm and HDL level. So it needs more experience and more time when Matlab algorithm level is porting to HDL level. Here IEEE 802.11b standard is taken to be the simulation platform, and the PER and BER figures are both produced on this platform.

### 4.2 System block diagram

Figure 4-1 shows the block diagram of whole system. All important system parameters could be show in this figure. There three components in this system, transmitter, channel and receiver, and a top file is used to control these three components and call them. The top file controls a parameter-packet number, that parameter defines how many packets the system will execute at the same conditions with increasing SNR.

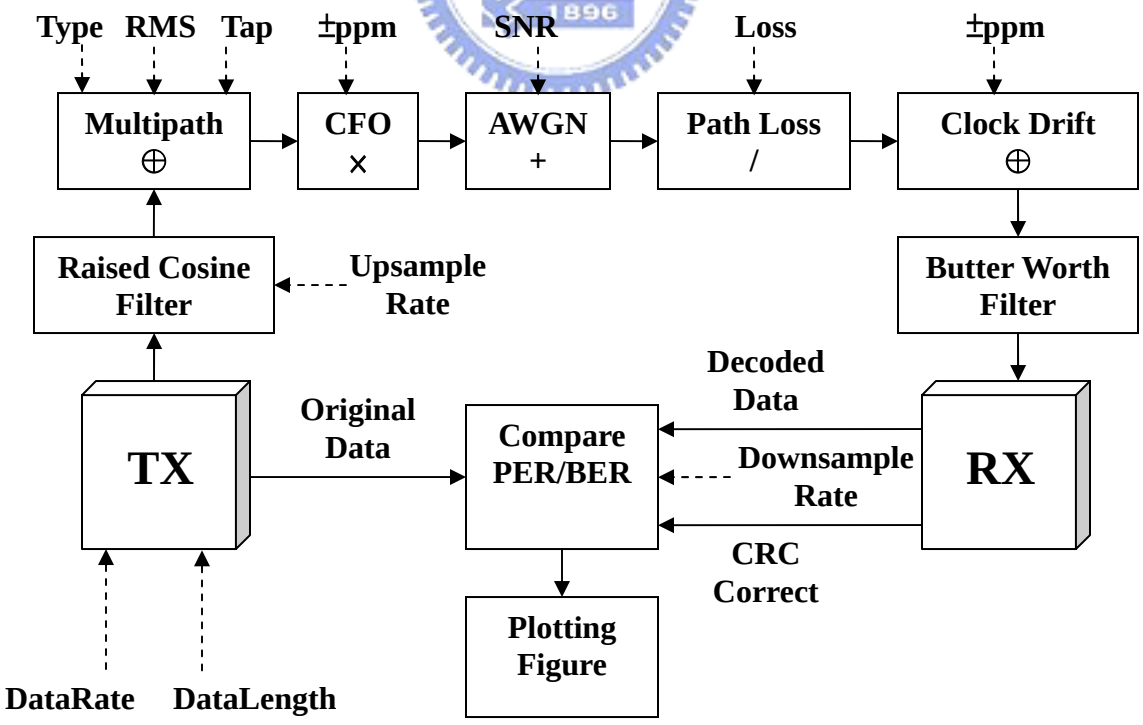



Figure 4-1 System block diagram

### 4.3 Transmitter

Two parameters control the transmitter component-DataRate and DataLength. The parameter DataRate specifies the signal will be transmitted in which data rate and there are four types of data rate that could be chosen-1 Mbps, 2 Mbps, 5.5 Mbps and 11 Mbps. In 802.11b standard 5.5 Mbps and 11 Mbps are very different to 1 Mbps and 2 Mbps, because data of 5.5 Mbps and 11 Mbps uses CCK code as modulation and spreading code, not like data of 1 Mbps and 2 Mbps uses BPSK, QPSK as modulation and Barker code as spreading code. Although our system can support 5.5 Mbps and 11 Mbps CCK demodulation and decoding, all proposed algorithm focus on DSSS system, so the performance figure PER and BER are both produced at 1 Mbps and 2 Mbps. Figure 4-2 shows the block diagram of transmitter. Because the channel model has been described in chapter 2, we skip it then describe the details of receiver side.

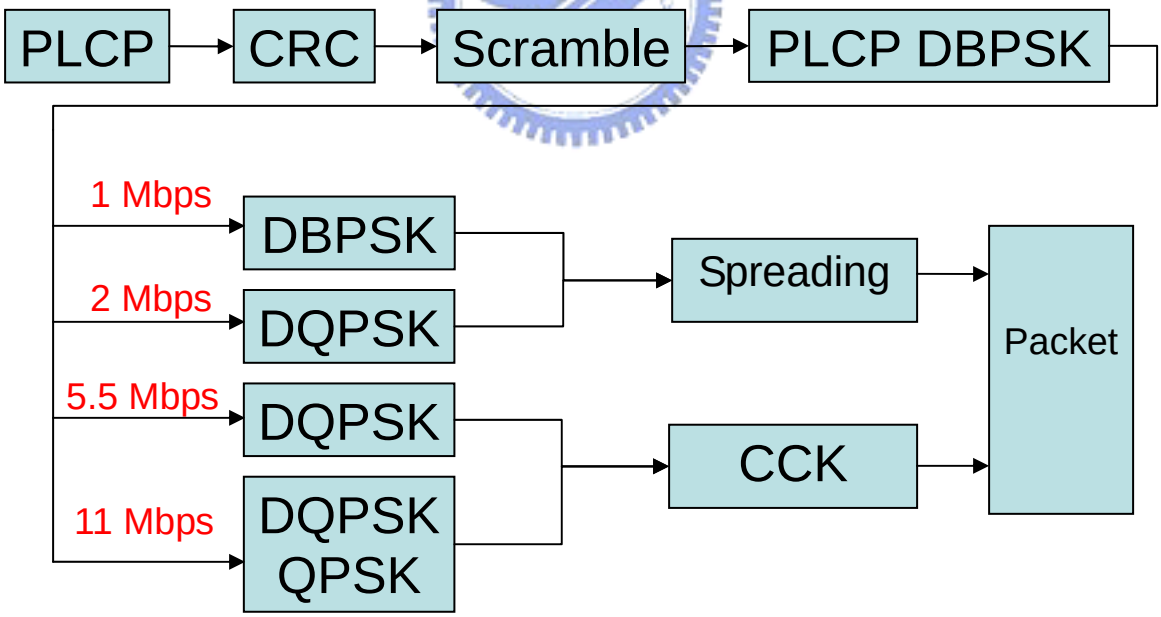



Figure 4-2 Block diagram of transmitter

## 4.4 Receiver

At the receiver, a finite state machine based coding architecture is used. There are three main advantages listed below

a. Easy to control the process of processing received signal
b. Easily comparing the result between Matlab code and verilog code
c. High extension on adding another components on system

The receiver coding architecture of finite state machine based is shown in figure 4-3. With this kind of coding architecture, we can easy control the flow of processing received signal and anyone can also easy add his algorithm or component to our system. The parameters AGC_on, Timing_on, AFC_on and EQ_on are switches that enable the corresponding components, hence, we can use this kind of coding architecture to simulate the control flow of hardware. For example, the sample point at this moment will do AGC, AFC, Timing Sync and EQ, so the finite state machine just need set AGC_on, AFC_on, Timing_on and EQ_on to 1. Figure 4-4 shows the whole state diagram of receiver. Receiver is the main part of the simulation platform, it contains not only the demodulation function blocks but also the synchronization block which are used to compensate the non-ideal channel effects.

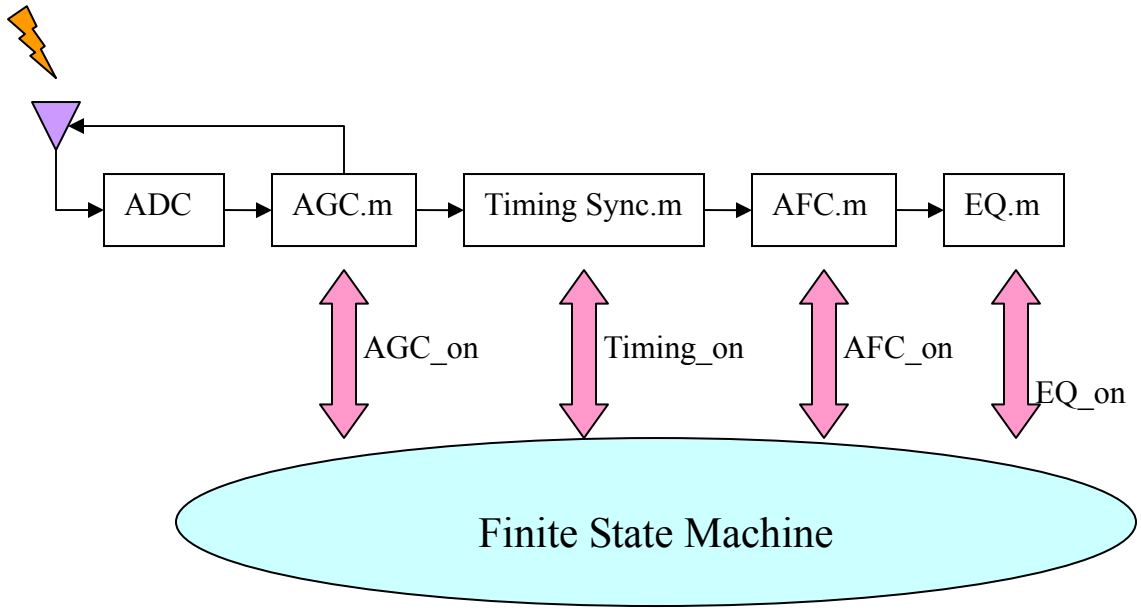
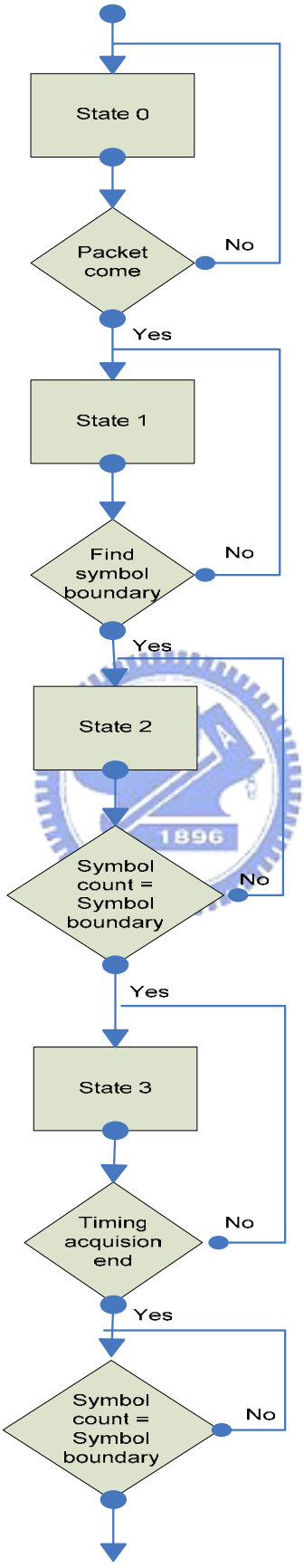



Figure 4-3 Coding architecture of finite state machine based


State 0
Packet come
No
Yes
State 1
Find symbol boundary
No
Yes
State 2
Symbol count = Symbol boundary
No
Yes
State 3
Timing acquision end
No
Yes
Symbol count = Symbol boundary
No

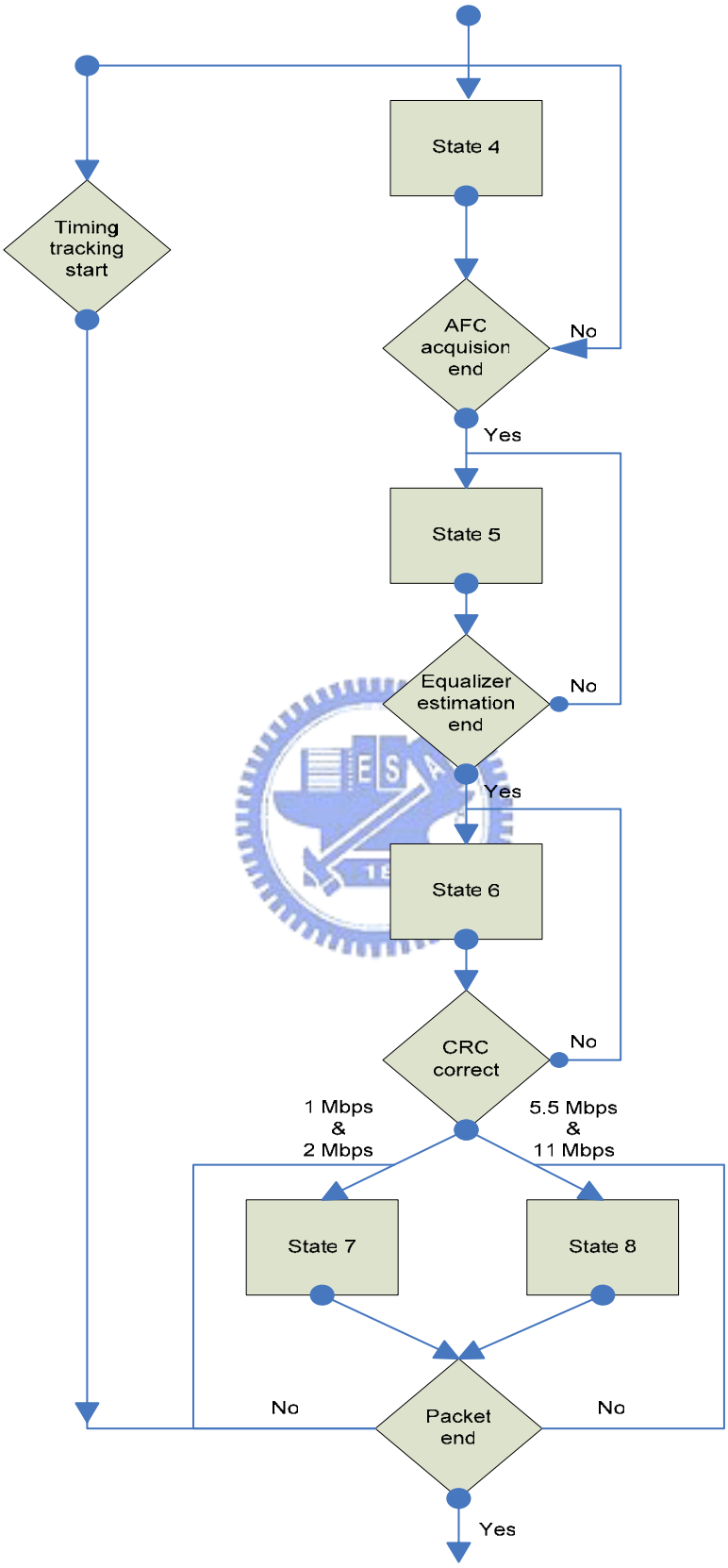



Figure 4-4 State diagram of receiver

## 4.5 Simulation results

AWGN, multipath, CFO, path loss and Clock drift effects are simulated in our system. To simulate the decision of symbol boundary, random length noise are attached to the head and the tail of the frame as shown in Figure 4-5 when SNR is 10 dB.

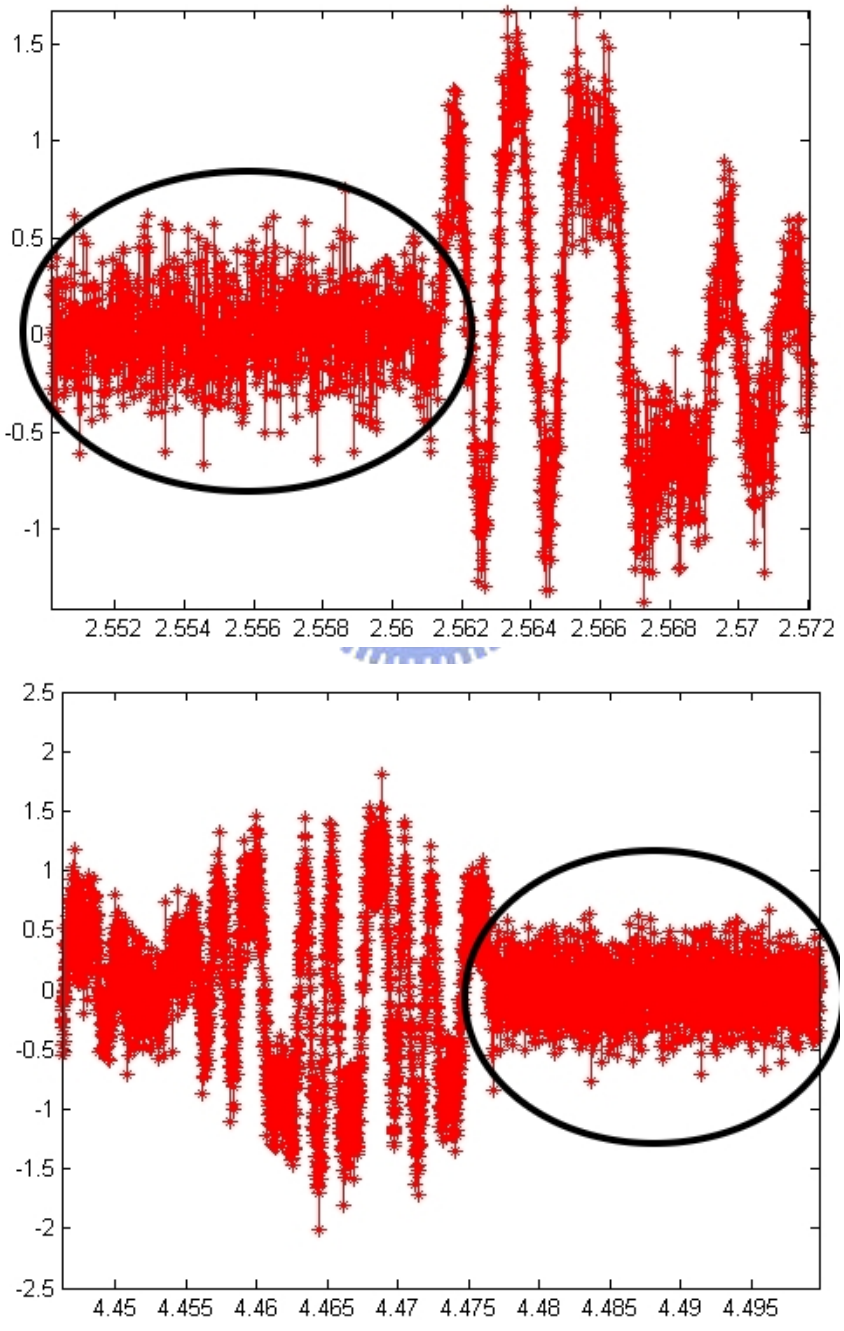



Figure 4-5 Noise attached to the head and tail of the frame

Figure 4-6, 4-7, 4-8 and 4-9 show the PER and BER versus SNR plots. The simulation environments have AWGN, CFO, multipath, path loss and sample clock phase is best. Because all proposed algorithm focus on DSSS, there will on 1 Mbps and 2 Mbps simulation result. The simulation of 5.5 Mbps and 11 Mbps will be skip here, because they are based on CCK and anyone who interested in CCK can refer to thesis [20]. All simulation results are simulated with 100 packets, 1024 symbols long, AWGN from -5 dB to 10 dB, CFO 50 ppm and path loss -25 dB. Figure 4-6 shows the PER of 1 Mbps with no multipath and three multipath model.

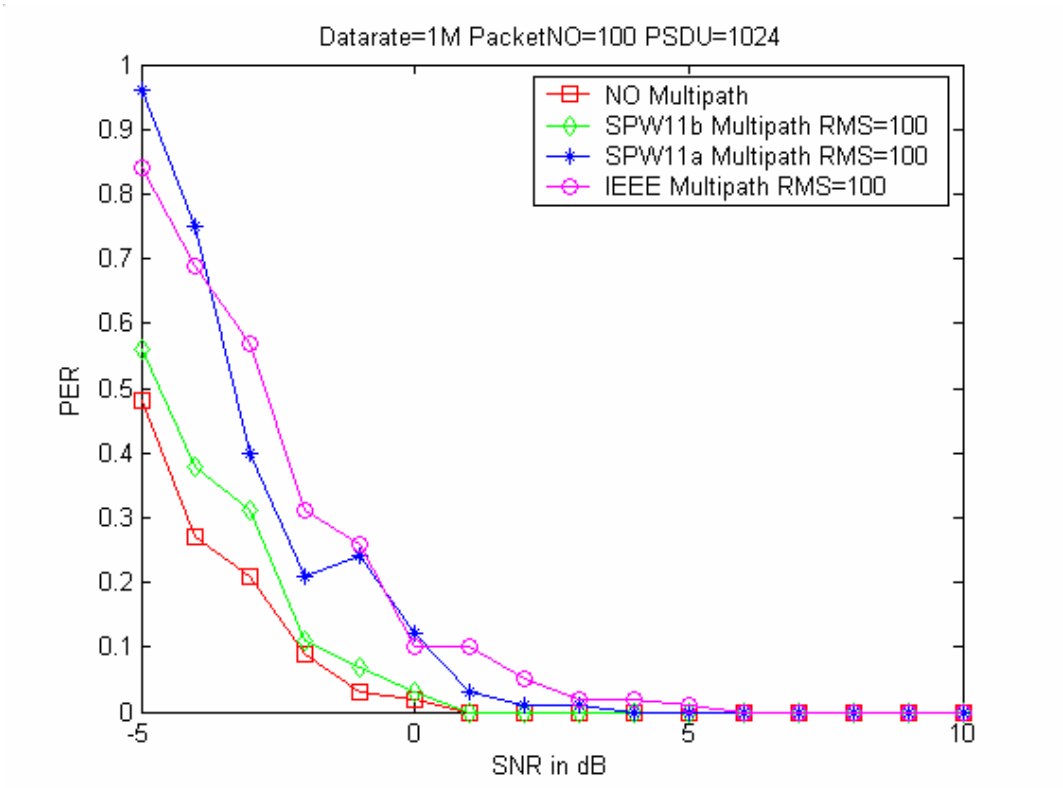



Figure 4-6 PER of 1 Mbps

From Figure 4-6 and 4-7, our system will meet the requirement defined by WiFi at SNR 3 dB with IEEE Multipath model. The WiFi organization defines the requirement of PER and BER are 0.1 and $10^{-5}$ respectively.

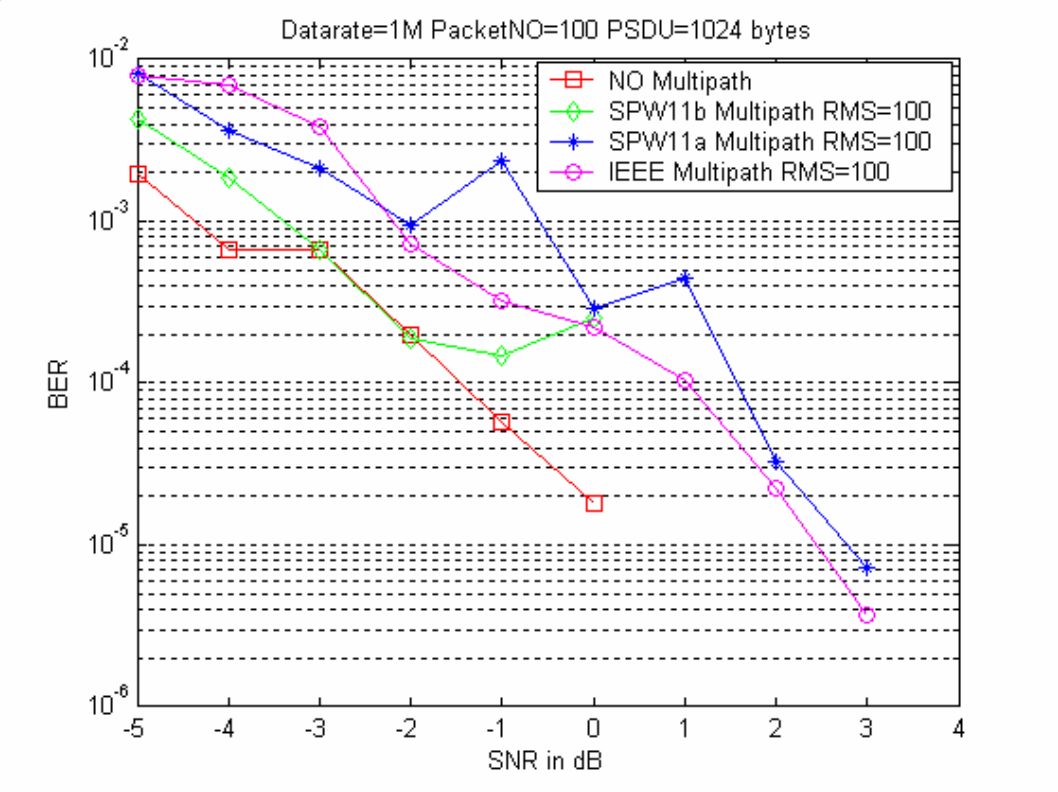



Figure 5-7 BER of 1 Mbps

Figure 4-8 and 4-9 show the PER and BER of 2 Mbps with no multipath and three multipath model respectively. Our system will meet the requirement defined by WiFi at SNR 10 dB with IEEE Multipath model. From these four figures, we can find that the signal with higher data rate will be affected more seriously than the signal with lower data rate.

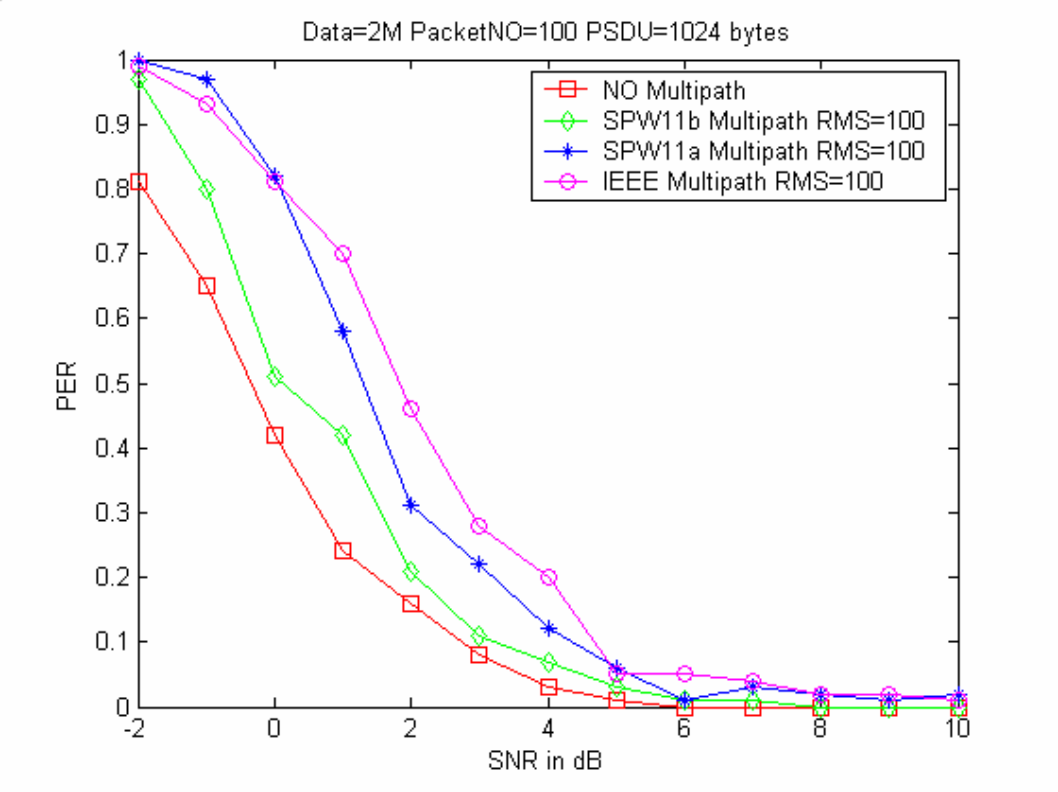



Figure 4-8 PER of 2 Mbps

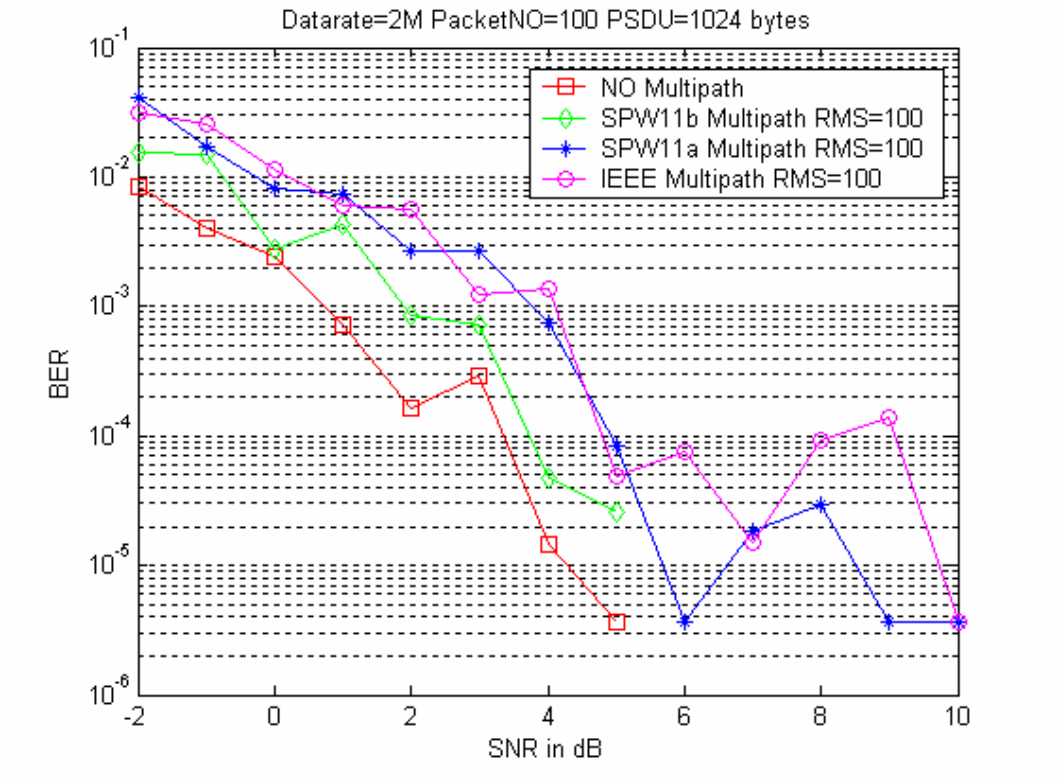



Figure 4-9 BER of 2 Mbps

# CHAPTER 5

# HARDWARE IMPLEMENTATION

## 5.1 Architecture

Figure 5-1 shows the whole architecture of the proposed platform baseband processor. Upper part is the receiver path and lower is the transmitter path. The baseband processor is includes both modules; Modulator, Spreading, Shaping Filter, Channel Equalizer, Dual Correlator, Demodulator, Synchronization Loop, Data Coding/Decoding、CPU, and I/O Interface. In the proposed platform baseband processor, in this thesis is don't to implement all modules. Therefore, at below sections, don't illustrate all the proposed architectures.

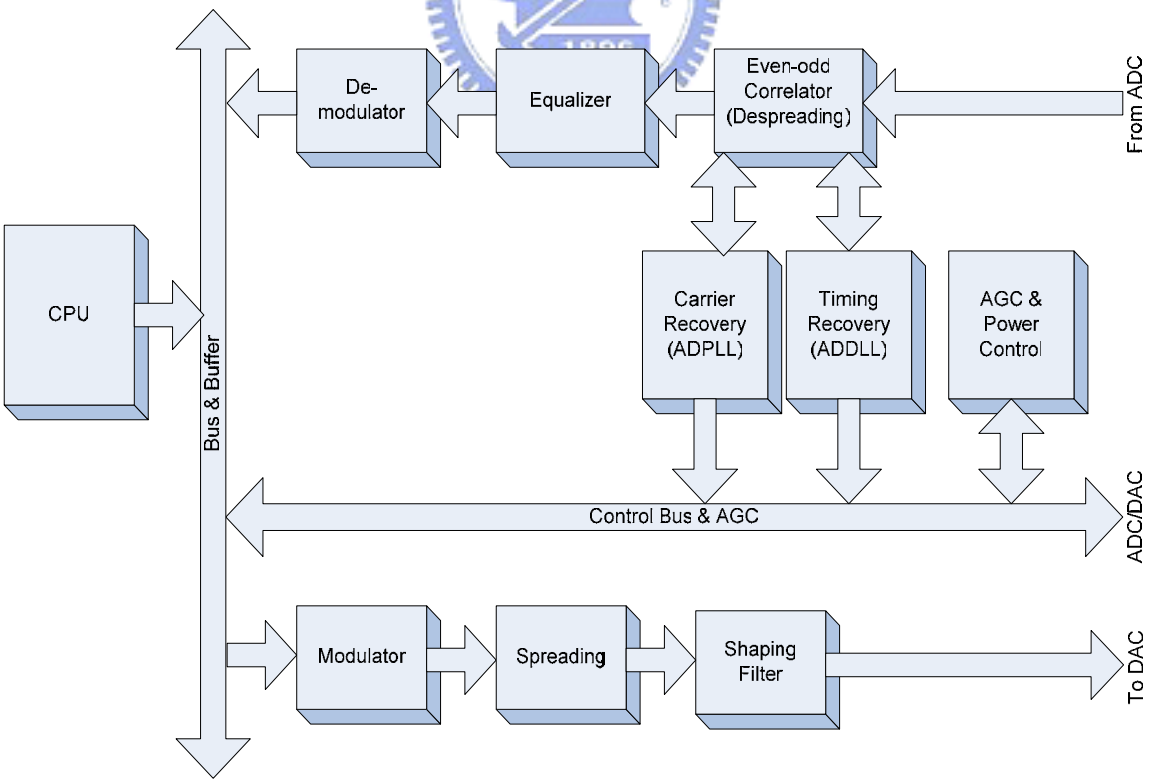



Figure 5-1 The Block Diagram of DSSS-based Wireless Baseband Processor

## 5.2 Matlab platform translation to HDL simulation method

Figure 5-2 shows the proposed platform design flow from Matlab simulation to hardware implementation. The first step of system design is chosen the suitable algorithm to avoid the channel effect. The second step is measured the proposed algorithm work well, then design architecture. System specifications are needed obeyed and performance needs to be maintained. Hence change the high level function description block to low level architecture hardware model one by one. The Matlab hardware models are built and system simulation is performed to keep the performance. After deciding the architecture, we have to perform the fixed point simulation. This is a trade-off between the hardware cost and system performance.

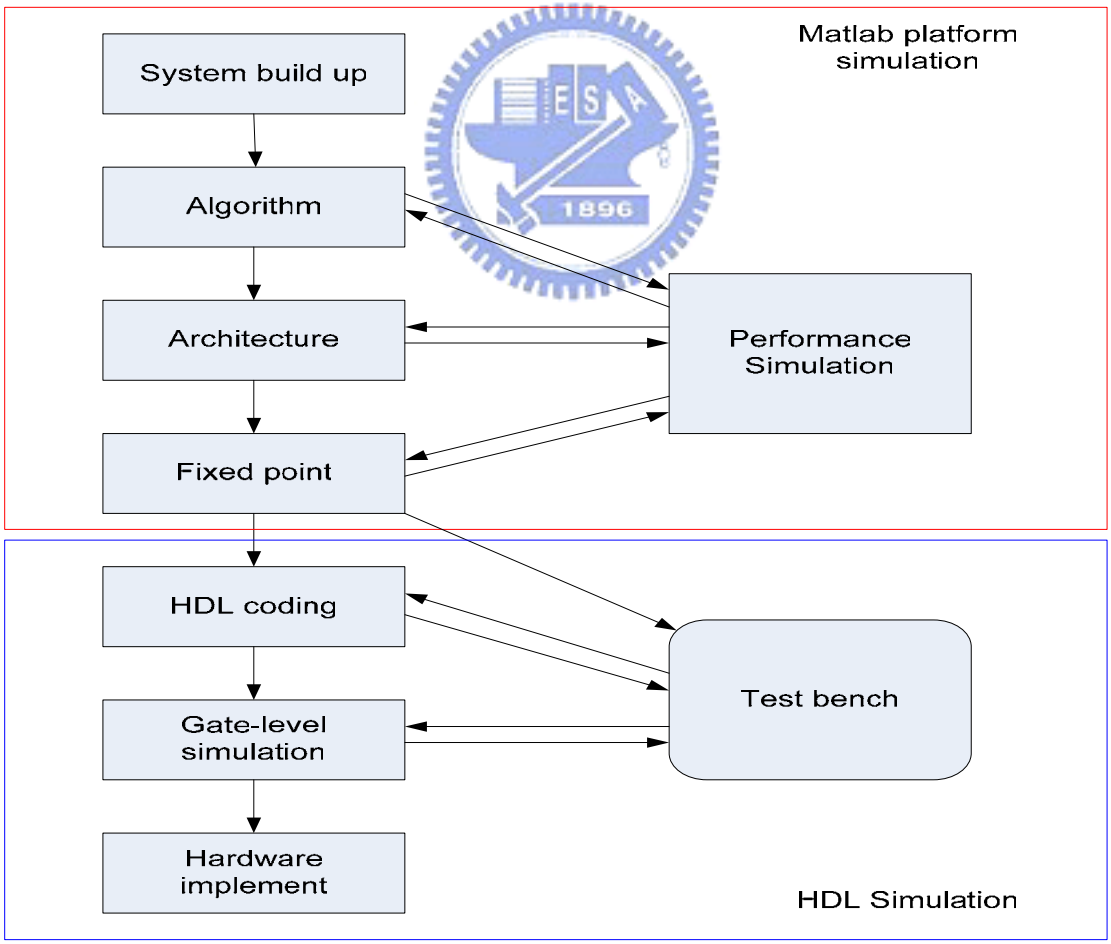



Figure 5-2 Matlab simulation to Hardware implement flow

## 5.3 Proposed hardware component

In the whole architecture of the proposed platform baseband processor, some component will to represent at below. In the proposed timing synchronization algorithm is needed the PN correlator. In this work the PN correlator is barker correlator. There are two ways to implement Barker correlator: one is shift register based and another is point address memory (PAM) based. The shift register based Barker correlator in Figure 5-3 is easy to implement but consumes more power, however, the PAM based correlator in Figure 5-4 only change two registers each time, so it consumes less power but the control is much more complicated. In the proposed platform, the barker correlator is need, but it must to modify to dual correlator architecture for timing synchronization.

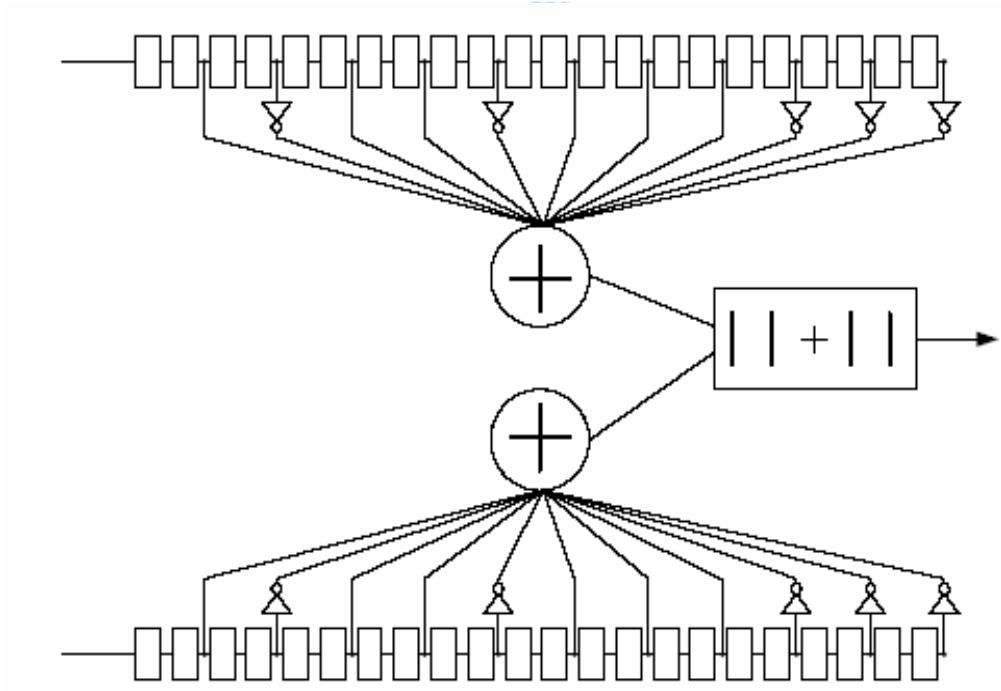


Figure 5-3 Shift register based Barker correlator

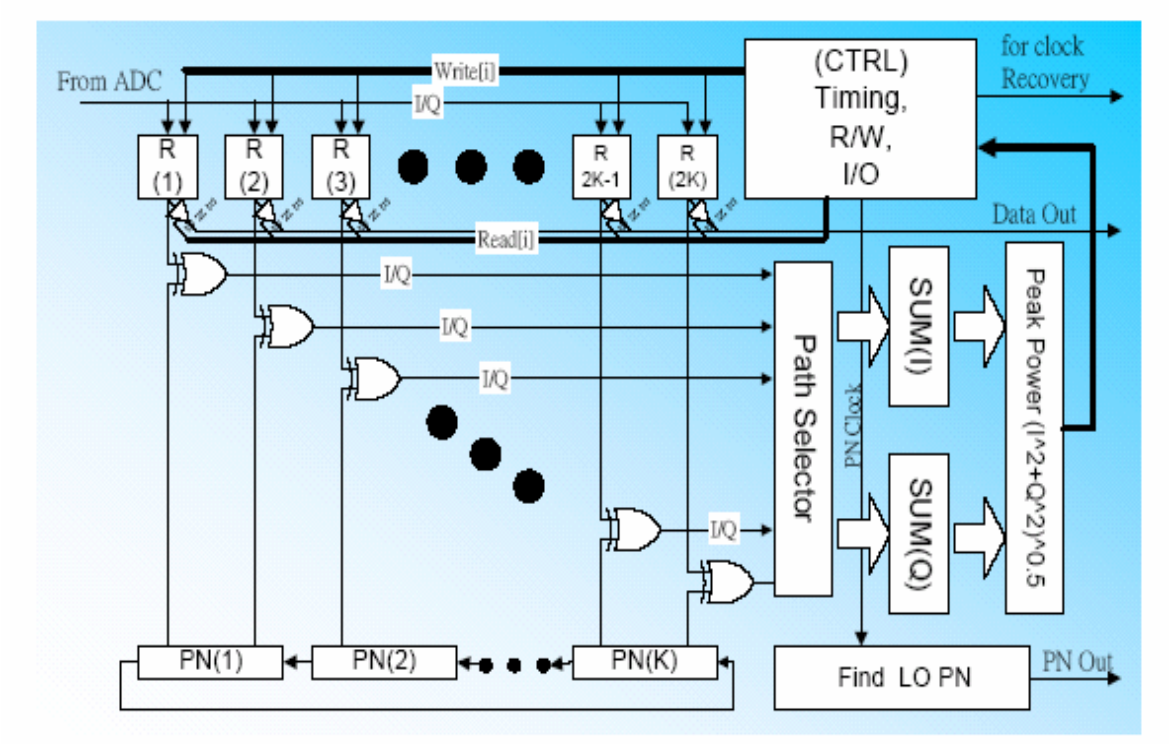



Figure 5-4 PAM based Barker correlator

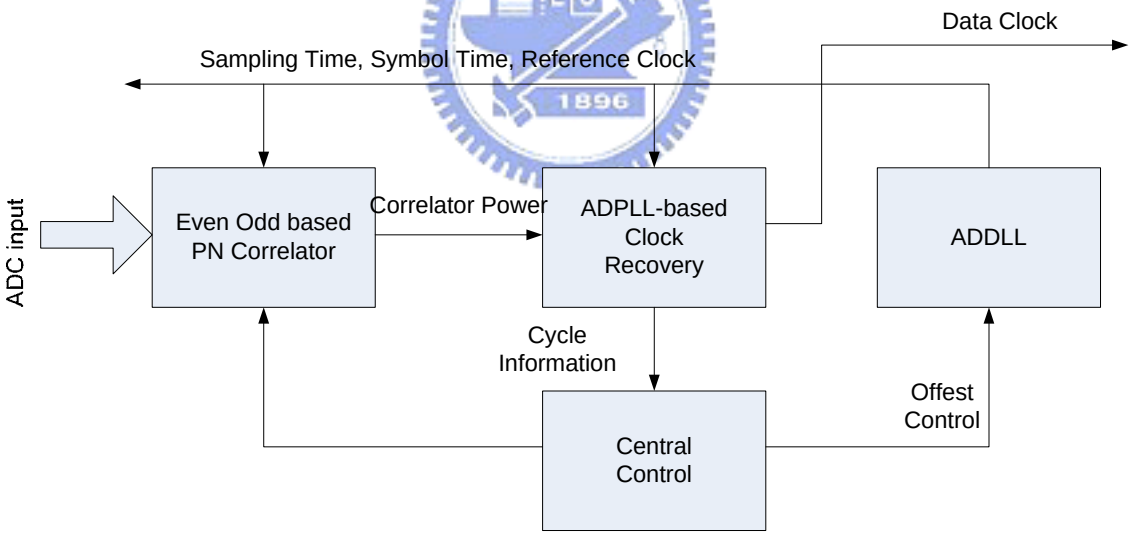



Figure 5-5 Dynamic sampling and timing synchronization architecture

Figure 5-5 shows the proposed dynamic sampling and timing synchronization architecture. But timing synchronization architecture is don't transaction to HDL hardware. After the timing synchronization translation to HDL hardware is one of my future works.

## 5.4 Asynchronous Circuit Design

Recently, people pay much attention on power consumption of chips. Traditionally, a central synchronous clock is required in circuit design. In a large circuit design, however, the clock needs considerable portion in area and power consumption, namely 30% power consumption of the circuit. Therefore, improving the power efficiency in circuit design is deserved to be heavily concerned. In asynchronous circuit design [21] [22], every component works in its own handshake instead of a central clock. A central clock is usually required to fit the worst case of the whole circuit. Hence, asynchronous circuit can work in approximate average performance instead of worst case. Besides performance, asynchronous circuit naturally spends less power consumption than synchronous counterpart because of lack of the clock. Additionally, the asynchronous system is also suitable for module of SoC (System on Chip) design because the inherent ease of composing asynchronous modules into larger one. So, in this thesis will propose two method of asynchronous circuit design. Figure 5-6 shows the first asynchronous circuit design method. The first method is used asynchronous design tool; another is used full-custom design method. In the first method, the asynchronous design tool is includes Balsa, Caltech, TANGRAM, 3D…etc. In the proposed timing acquisition algorithm, the encoder/decoder is chosen the “Balsa” to implementation hardware. Figure 5-7 shows the controller handshake circuit diagram. Figure 5-8 shows the synthesis result by Balsa. Figure 5-9 shows the second asynchronous circuit design method. In the second asynchronous circuit design method is best chosen to integration with synchronous circuit design. Because the asynchronous circuit component is used full custom design delay insensitive cell library. Another the first method is not used in cell based design flow. So, the cell library design is important, it can use cell library to design asynchronous circuit module. After integration the synchronous circuit component and the asynchronous circuit component is one of my future works.

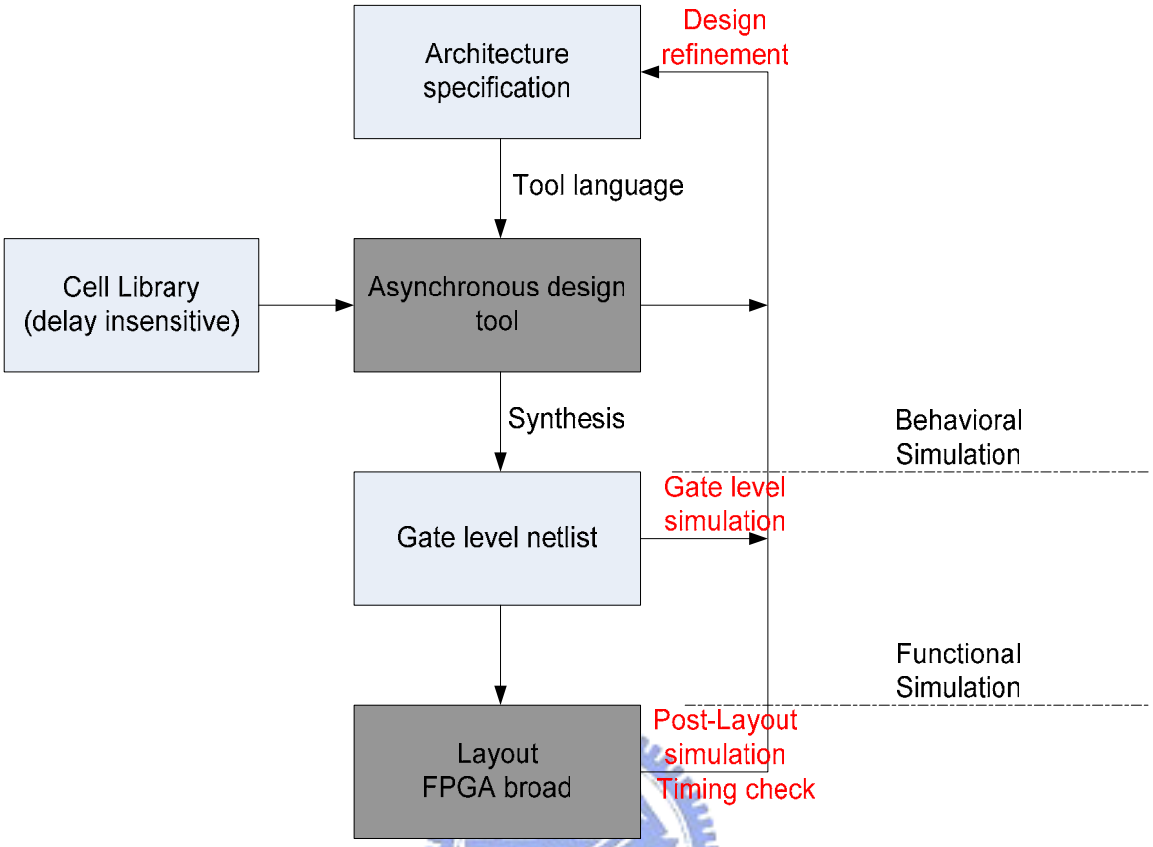



Figure 5-6 The first method to design asynchronous circuit

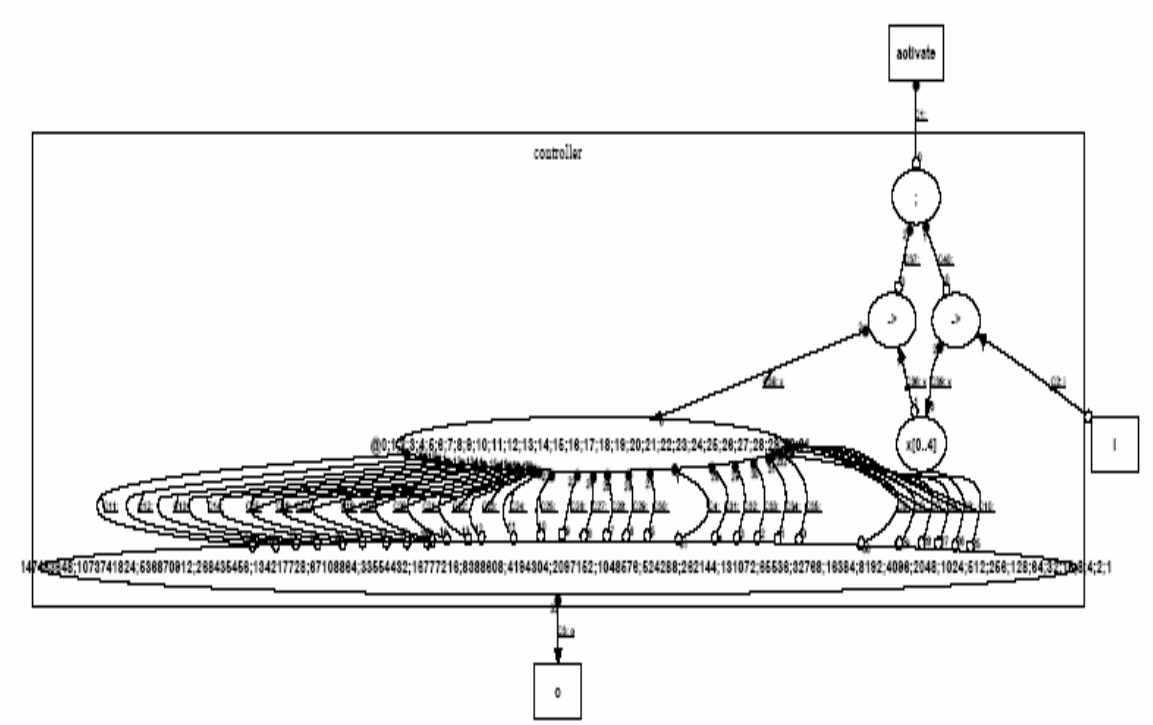



Figure 5-7 The controller handshake circuit diagram

```
Output StdOut
Part: WriteMessage

Total cost: 0

Part: StringAppend

Total cost: 0

Part: controller
(0 (component "$BrzFetch" (5) (40 2 39)))
(0 (component "$BrzFetch" (5) (37 36 38)))
(0 (component "$BrzEncode" (32 32 "2147483648;1073741824;536870912;268435456;134217728;67108864
;33554432;16777216;8388608;4194304;2097152;1048576;524288;262144;131072;65536;32768;16384;8192;
4096;2048;1024;512;256;128;64;32;16;8;4;2;1") ((35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20
 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4) 3)))
(49.5 (component "$BrzSequence" (2) (1 (40 37))))
(123.75 (component "$BrzVariable" (5 1 "x[0..4]") (39 (36)) (at 7 2 "controller.balsa" 0)))
(1571.0 (component "$BrzCase" (5 32 "0;1;2;3;4;5;6;7;8;9;10;11;12;13;14;15;16;17;18;19;20;21;22
;23;24;25;26;27;28;29;30;31") (38 (4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25
26 27 28 29 30 31 32 33 34 35))))

Total cost: 1744.25

Total costs:
controller = 1744.25
StringAppend = 0
WriteMessage = 0
```

Figure 5-8 The synthesis result by Balsa

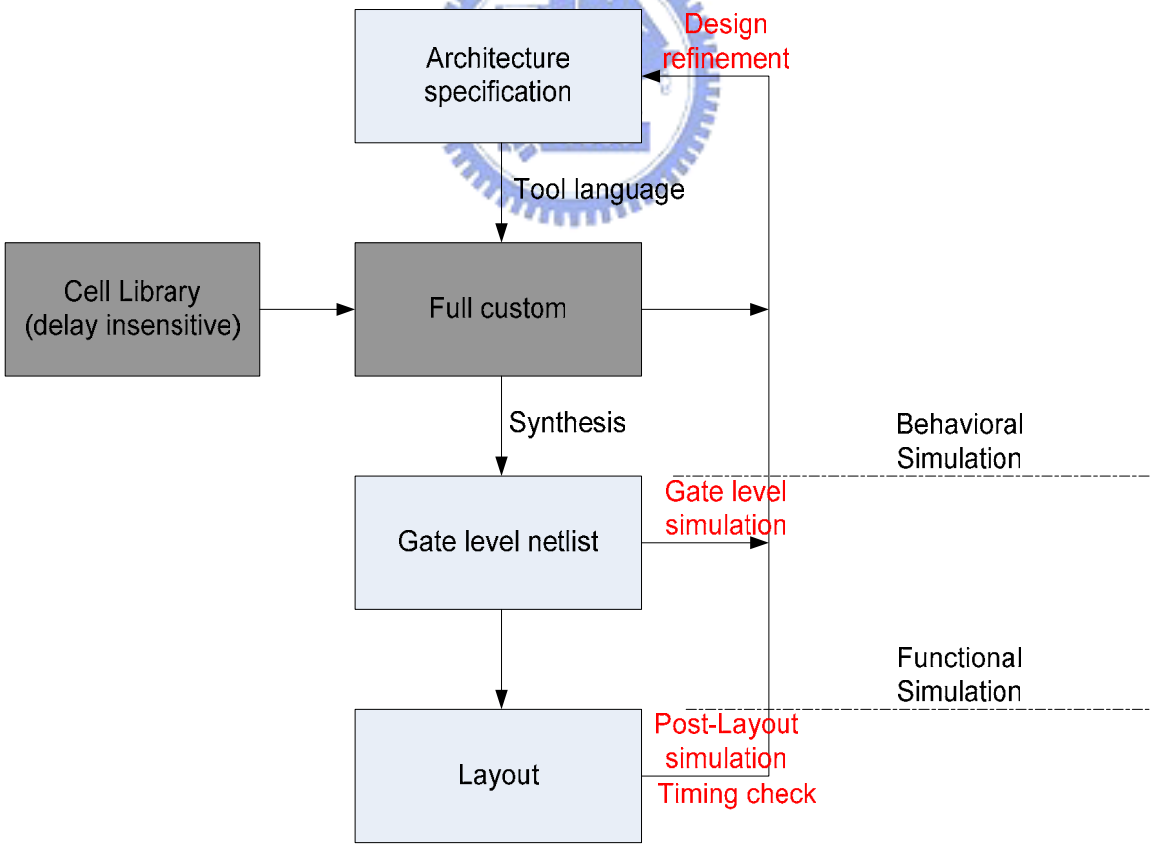



Figure 5-9 The second method to design asynchronous circuit

# CHAPTER 6

# CONCLUSIONS AND FUTURE WORKS

## 6.1 Conclusions

The timing synchronization algorithms are proposed for DSSS based wireless baseband applications. For deeply verifying these proposed algorithms is don't affect the data decoding and whole system performance. So the IEEE 802.11b system is used to combine with the proposed algorithms. From the BER and PER of 1 Mbps and 2 Mbps, the proposed algorithms don't seem to affect the process of data decoding and demodulation. With the proposed algorithms, these can use on any other wireless communications for DSSS based, like DSSS UWB system and sensor network system, etc. In this thesis is focus on timing acquisition algorithm. So, the proposed dual correlator differential base timing acquisition algorithm can resist multipath fading and clock drift with signal of lower data rate like 1 Mbps and 2 Mbps, and it can converge the sample clock phase at between positive four phases and negative four phases. In the seriously multipath channel effect, there can't converge between positive four phases and negative four phases situation. After the timing acquisition is must to check symbol boundary, here is used the symbol boundary decision method to guarantee the symbol boundary correct. The timing tracking is very important to resist the clock drift by time. In this thesis, there is focus on timing acquisition algorithm of timing synchronization. So, in this work is proposed one method of timing tracking algorithm. In the proposed platform, there hopes phase error very small, it guarantee the tracking algorithm can be find the best sample clock phase with less step. Another topic of asynchronous circuit design, the proposed method is used the "Balsa" tool for design. In the proposed dual correlator differential base timing acquisition method, the encoder/decoder block is used balsa to implementation. So, the circuit is delay insensitive and hazard free circuit.

## 6.2 Future works

For implementing a chip finally, the fixed-point simulation is needed. So, the current floating-point (algorithm level) platform must been changed to fixed-point platform. During the process of constructing a fixed-point platform, many considerations must be concerned, for example, what the number of bits of ADC is, how to decide the number of bits after each operation, how to make a Look-Up-Table (LUT) for mapping and what size the LUT is, etc. A lot of time is needed for fixed-point platform constructing and simulating. The timing acquisition algorithm use less several symbols to get the high performance is needed. And the timing synchronization is work at one sample rate. After the Matlab simulation, it translation to HDL hardware is needed. In the hardware implementation, there is chosen other design method of asynchronous circuit design, to get the low power consumption property. And integration synchronous circuit and asynchronous circuit design in a system. I will learn more knowledge and do more research in my future work.

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# About the Author

You Hsien Lin, male, was born in Taipei County, Taiwan (R.O.C.), on October 12th, 1978. He make efforts in master degree at Nation Chiao Tung University from September 2002. His research focuses on wireless communication systems, especially on WLAN. In the two years of graduate, he learned a lot of theoretical and practical courses, like Wireless LAN, Algorithm, Computer Architecture, Digital Communications, IC Design LAB(1)(2), Embedded Operating System and Asynchronous Circuit Design. These courses give a huge help on his research and master thesis. The title of his master thesis is "The Study of Dynamic Sampling Loop for Wireless Baseband Applications".