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An Analysis and the Fabrication Technology of the Lambda Bipolar Transistor

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Abstract—**A new type of voltage-controlled negative-differential-resistance device using the merged integrated circuit of an n-p-n (p-n-p) bipolar transistor and an n(p)-channel enhancement MOSFET, which is called the Lambda bipolar transistor, is studied both experimentally and theoretically. The principal operation of the Lambda bipolar transistor is characterized by the simple circuit model and device physics. The important device properties such as the peak voltage, the peak current, the valley voltage, and the negative differential resistance, are derived in terms of the known device parameters. Comparisons between the characteristics of the fabricated devices and the theoretical model are made, which show that the analysis is in good agreement with the observed device characteristics.**

I. Introduction

NEGATIVE-differential-resistance semiconductor devices have offered increasing interest in oscillator circuit and memory applications. So far, there are several realized structures which had been proposed. Among these, Kano *et al.* [1] reported a structure with two terminals called the Lambda diode, which consisted of two integrated complementary JFET's. Several important applications of the Lambda diode had also been proposed [2]-[6]. Baliga *et al.* [7], [8] reported an integrated structure with three terminals called the GAMBIT which consisted of the merged structure of a p-n-p bipolar transistor and an n-JFET. High-power operation of the GAMBIT had been demonstrated, which can be used in some high-power signal generation. Mimura [9] proposed a voltage-controlled DNR device with unijunction structure. Lehovec and others [10] proposed an integrated structure with an enhancement insulated-gate field-effect transistor (IGFET) and a bipolar transistor. The operation of this modified IGFET needs one external resistor and the onset of junction breakdown. Thomas *et al.* [11], [12] proposed an n-type voltage-controlled negative-resistance device called the NEGIT using a bipolar transistor and an extended field plate over the emitter-base junction. The operation of the NEGIT was realized by controlling base surface recombination in a bipolar transistor by biasing a gate on the oxide over the emitter-base junction, which is strictly dependent on the uncontrollable parameters such as surface recombination velocity and surface states. Wu *et al.* [13]-[15] have proposed several new Λ-type voltage-controlled negative resistance devices with three terminals using the MOSFET's called the Lambda MOSFET. The Lambda MOSFET is shown to be easily fabricated by existing high-density MOS technologies and has several useful applications. Recently, a new Λ-type negative-resistance device called the Lambda bipolar transistor has been proposed by us [16] which has three terminals with a very simple structure, and has the feasibility of simultaneous integration with the existing bipolar transistor and MOSFET integrated circuits.

In this paper, the Lambda bipolar transistor which exhibits Λ-type voltage-controlled negative differential-resistance characteristic, will be analyzed. The Lambda bipolar transistor has three terminals (emitter, base, collector) which are similar to those of a conventional bipolar transistor except that an additional same carrier type MOSFET should be merged, in order to produce the voltage-controlled negative resistance, during

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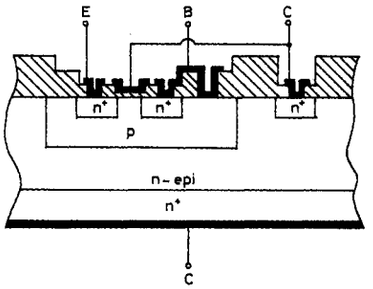

Fig. 1. The basic device structure of an n-p-n Lambda bipolar transistor.

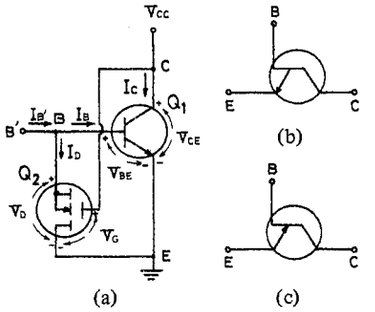

Fig. 2. (a) The equivalent circuit construction and the biasing condition of an n-p-n Lambda bipolar transistor. (b) The proposed device symbol for an n-p-n Lambda bipolar transistor. (c) The proposed device symbol for a p-n-p Lambda bipolar transistor.

the fabrication. The detailed description of the device operation and the mechanism controlling the negative differential resistance are given in Section II of this paper, where the first-order device theory will be developed. In Section III, the layout design and the fabrication procedures will be described. Comparisons between the fabricated devices and the theoretical analyses will be made in Section IV. Conclusions will be given in the last section.

II. Device Physics and Modeling

The basic structure of the Lambda bipolar transistor and its electrical equivalent circuit connection are shown in Fig. 1 and Fig. 2(a), respectively, and the proposed symbols of this new device are shown in Fig. 2(b) and (c). From Fig. 1, an n-channel enhancement-mode MOSFET is fabricated upon the base region of an n-p-n bipolar transistor. The source and the emitter, the base and the substrate, are internally connected; while the drain and the base, the gate and the collector are externally connected by metallization.

The Lambda bipolar transistor is operated in the same way as the conventional bipolar transistor with a fixed external base current drive. When the collector-emitter voltage V_{CE} is smaller than the threshold voltage V_T' of the MOSFET with V_T' modified by substrate bias V_{BE}, and MOSFET is off, and the emitter-collector characteristic is the same as that of a bipolar transistor. Once V_{CE} exceeds V_T', the MOSFET is on, and the base current drive I_B' is partially taken out by I_D. As a result, the actual base current I_B of the bipolar transistor is decreased, the collector current I_C is also decreased, and the differential negative resistance will occur. Further increase of V_{CE} will cause the conductance of the MOSFET to increase,

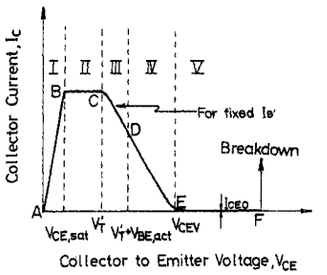

Fig. 3. Basic I_C-V_{CE} characteristic of an n-p-n Lambda bipolar transistor with a fixed base current drive I_B' which is used to illustrate the five regions of device operation.

so more I_B' is taken out by I_D, and I_C will continue to decrease. From the moment the base current I_B' is wholly taken out by I_D of the MOSFET, the bipolar transistor is now operated in the cutoff region, where the collector current of the Lambda bipolar transistor is equal to the collector reverse saturation current I_{CEO}. If we assume the threshold voltage V_T' of an n-channel enhancement-mode MOSFET is larger than the emitter-collector saturation voltage $V_{CE,\text{sat}}$ of the n-p-n transistor, i.e., $V_T' \geq V_{CE,\text{sat}}$, then the general I_C-V_{CE} characteristic of the Lambda bipolar transistor with a fixed external base current drive I_B' is shown in Fig. 3, where the characteristic curve can be divided into five regions according to the operating points of the separate bipolar transistor and a MOSFET.

From the terminal characteristic of the separate devices, the general current equations of the Lambda bipolar transistor, according to the circuit model of Fig. 2(a), can be written as

$$I_C = \beta I_B + I_{CO}(1+\beta) \tag{1}$$

$$I_B = I_B' - I_D \tag{2}$$

where β is the dc common-emitter current gain of the n-p-n bipolar transistor; and $I_{CEO} = I_{CO}(1+\beta)$, is the common-emitter-collector reverse saturation current.

In order to see the quantitative operational principles of the Lambda bipolar transistor, the five region analyses are given as follows.

Region I

When the emitter-collector voltage V_{CE} is smaller than or equal to $V_{CE,\text{sat}}$, i.e., $V_{CE} \leq V_{CE,\text{sat}}$, the n-p-n transistor is in saturation, and the MOSFET is off, then I_B is equal to I_B', and the collector current with respect to the emitter-collector voltage can be written as [17]

$$V_{CE} = \frac{k_B T}{q} \ln \left| \frac{\alpha_R [1 - (I_C/I_B')]}{1 + [I_C(1-\alpha_R)/I_B']} \right| + I_E r_{SE} + I_C r_{SC} \tag{3}$$

where r_{SE} and r_{SC} are the series resistances of the emitter and the collector regions, respectively, and α_R is the common-base current gain in the reverse operation. It should be noted that the argument of the logarithm will not equal zero within this region, and the collector current will increase as the collector-emitter voltage increases.

Region II

When the emitter-collector voltage V_{CE} is larger than or equal to $V_{CE,\text{sat}}$, but is smaller then V_T', i.e., $V_{CE,\text{sat}} \leqslant V_{CE} < V_T'$, where V_T' is the threshold voltage of Q_2 with the positive substrate bias of $V_{BE,\text{act}}$, the n-p-n transistor is operated in the active region, and the n-MOSFET is still in the cutoff region, then I_B is equal to I_B', and the collector current can be written as

$$I_C = \beta I_B' + I_{CEO} \tag{4}$$

where the common-emitter current gain β can be defined and is approximately independent of the collector-emitter voltage V_{CE} as shown in Fig. 3.

The threshold voltage V_T' of the n-channel enhancement MOSFET with the substrate bias of $V_{BE,\text{act}}$ can be written as [18]

$$V_T' = \phi_{MS} + 2\phi_{fp} - \frac{Q_{ss}}{C_o} + \frac{\sqrt{2K_s\epsilon_0 qN_A(2\phi_{fp} - V_{BE,\text{act}})}}{C_o} \tag{5}$$

where ϕ_{MS} is the work function difference of the gate metal and the silicon substrate (p type), ϕ_{fp} is the potential difference between the Fermi level and the intrinsic energy level, C_o is the gate oxide capacitance per unit area of the n-MOSFET, Q_{ss} is the surface fixed charge of the Si-SiO_2 interface, N_A is the surface concentration of the base acceptor diffusion, K_s is the silicon dielectric constant, and ϵ_0 is the permittivity of free space.

Region III

When the emitter-collector voltage V_{CE} is larger than or equal to V_T', but is smaller than the sum of V_T' and $V_{BE,\text{act}}$, i.e., $V_T' \leqslant V_{CE} < V_T' + V_{BE,\text{act}}$, the n-p-n transistor is operated in the active region, and the n-MOSFET is operated in the saturation region, then $V_G = V_{CE}$, and the drain current can be written as

$$I_D = \frac{Z\mu_n C_o}{2L}(V_{CE} - V_T')^2 \tag{6}$$

$$\mu_n = K(V_{CE} - V_T')^{-r} \tag{7}$$

where Z is the width of the n-MOSFET, μ_n is the effective electron channel mobility, L is the channel length, r is an empirical constant [19], which is negative for the case of inversion layer electron scattered with the positive surface charge, and is positive for the case of inversion layer electron scattered with the inversion layer lattice, and K is also an empirical constant.

From (1) and (2), the collector current of the n-p-n transistor can be combined and written as

$$I_C = \beta\left[I_B' - \frac{ZC_oK}{2L}(V_{CE} - V_T')^{2-r}\right] + I_{CO}(1+\beta). \tag{8}$$

By differentiating I_C with respect to $(V_{CE} - V_T')$, the negative differential resistance of this region can be written as

$$R_N = \frac{\partial V_{CE}}{\partial I_C} = -\frac{2L}{\beta Z\mu_n(2-r)(V_{CE} - V_T')} \tag{9}$$

where the variation of $V_{BE,\text{act}}$ with respect to the change of V_{CE} is neglected.

Region IV

When the emitter-collector voltage V_{CE} is larger than or equal to $V_T' + V_{BE,\text{act}}$; but is smaller than the valley voltage V_{CEV}; i.e., $V_T' + V_{BE,\text{act}} \leqslant V_{CE} < V_{CEV}$, the n-p-n transistor is operated in the active region, and the n-MOSFET is operated in the linear region, then the drain current can be written as

$$I_D = \frac{Z\mu_n C_o}{L}[V_{CE} - V_T']\, V_{BE,\text{act}}. \tag{10}$$

The collector current of the n-p-n transistor can also be written as

$$I_C = \beta\left[I_B' - \frac{Z\mu_n C_o}{L}(V_{CE} - V_T')\, V_{BE,\text{act}}\right] + I_{CO}(1+\beta). \tag{11}$$

The negative resistance of this region can be calculated and written as

$$R_N = -\frac{L}{\beta Z\mu_n(1-r)\, C_o V_{BE,\text{act}}}. \tag{12}$$

Region V

When the emitter-collector voltage is larger than or equal to the valley voltage V_{CEV}, i.e., $V_{CE} \geqslant V_{CEV}$, the n-p-n transistor is in the cutoff region, and the n-MOSFET is operated in the linear region, then the collector current will be equal to the reverse saturation current of the emitter and collector terminals, i.e., $I_C = I_{CEO}$. From the moment the n-p-n transistor is in the cutoff region, and the base current I_B is equal to zero, then the external base current drive I_B' will be equal to drain current I_D in the linear region, i.e.,

$$I_D = \frac{Z\mu_n C_o}{L}(V_{CEV} - V_T'')\, V_{BE,\text{cut-in}} = I_B' \tag{13}$$

where V_T'' is the threshold voltage of the n-MOSFET with the substrate bias of $V_{BE,\text{cut-in}}$, which can be written as

$$V_T'' = \phi_{MS} + 2\phi_{fp} - \frac{Q_{ss}}{C_o} + \frac{\sqrt{2K_s\epsilon_0 qN_A(2\phi_{fp} - V_{BE,\text{cut-in}})}}{C_o} \tag{14}$$

so the valley voltage V_{CEV} can be written as

$$V_{CEV} = \frac{I_B' L}{Z\mu_n C_o V_{BE,\text{cut-in}}} + V_T''. \tag{15}$$

If the peak voltage V_{CEP} of the Lambda bipolar transistor is defined as the magnitude of the emitter-collector voltage at which the collector current starts to decrease and the negative differential resistance begins, then the peak voltage V_{CEP} will be equal to V_T', so that the voltage range of the negative resistance region can be written as

$$V_{CEV} - V_{CEP} = \frac{I_B' L}{Z\mu_n C_o V_{EB,\text{cut-in}}} + V_T'' - V_T'. \tag{16}$$

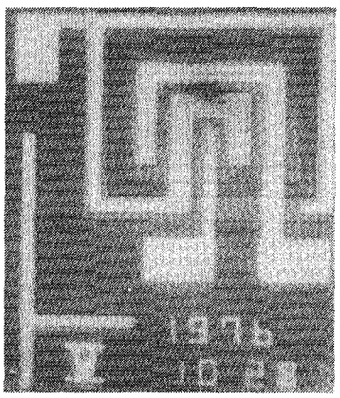

Fig. 4. The metallization patterns of the fabricated Lambda bipolar transistors.

III. The Layout Design and the Fabrication Procedures of the Lambda Bipolar Transistor and Integrated-Circuit Construction

The layout structure of the fabricated Lambda bipolar transistor with the minimization of the area occupied and with the external metallization interconnection, is shown in Fig. 4. It is clearly seen that the n-channel enhancement-mode MOSFET is fabricated very compactly within the p-type base region of the n-p-n bipolar transistor. The base contact of the n-p-n transistor and the substrate are internally connected together, whereas, the drain contact and the gate contact of the n-MOSFET, and the collector contact of the n-p-n transistor, are connected by metallization. The masking steps are similar to those of the double-diffused planar n-p-n transistor fabrication except that an additional mask is needed to form the gate oxide of the n-channel MOSFET. The basic fabrication procedures of the discrete Lambda bipolar transistor are listed in Table I.

It should be noted that the starting silicon wafer should be an n/p epi-wafer for bipolar integrated-circuit fabrication with n^+ buried layer and p-type diffusion isolation as shown in Fig. 5(a), where the resistor, diode, and bipolar transistor can be simultaneously fabricated. It is clearly seen that the combination of the Lambda bipolar transistor with bipolar integrated circuits need only an additional noncritical mask to etch the gate oxide region of the MOSFET if low-power integrated circuits are needed. In general, this additional mask is not required, because, in the present structure, the substrate bias effect (see (5)) is enough to reduce the threshold voltage of the MOSFET. For the combinations of the Lambda bipolar transistor and the n-channel MOSFET integrated circuits, the p-type diffusion for isolation is not necessary, hence, five masks are necessary for Al-gate n-channel MOS integrated-circuit fabrication, as is shown in Fig. 5(b). As regard to the simultaneous fabrication of the n-p-n Lambda bipolar transistor and CMOS integrated circuits, additional two masks are needed for the buried layer and p^+ isolation, because the p channel of CMOS may interact with n^+ collector diffusion of the n-p-n Lambda bipolar transistor, as is shown in Fig. 5(c), but the additional masks are also noncritical. If the buried layer of the n-p-n Lambda bipolar transistor is not necessary for performance requirements in MOS and CMOS integrated circuits, one mask can be saved. For discrete Lambda bipolar-transistor fabrication, the n-type wafer or n/n^+ epitaxial wafer can be used to fabricate a high-power Lambda bipolar tran-

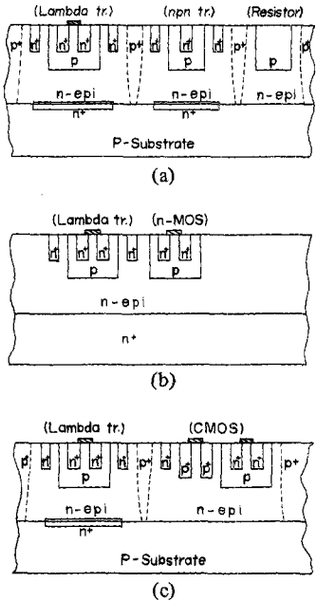

Fig. 5. (a) A structure for incorporation of an n-p-n Lambda bipolar transistor into the conventional bipolar integrated circuits. (b) A structure for incorporation of an n-p-n Lambda transistor into the conventional n-channel MOS integrated circuits. (c) A structure for incorporation of an n-p-n Lambda transistor into the conventional CMOS integrated circuits.

TABLE I
The Basic Fabrication Procedures of the Discrete Lambda Bipolar Transistor

- Strictly clean the n-type (or n/n^+) silicon wafer surface.
- Thermally grow a layer of SiO_2 about 8000Å.
- Use the first mask to define the base diffusion region of n-p-n transistor.
- Boron predeposition (950°C).
- Boron glass removal.
- Boron drive-in (1200°C) and the silicon oxide growth.
- Use the second mask to define the emitter and the collector windows of the n-p-n transistor, and the drain window of n-channel MOSFET.
- Phosphorous predeposition (1000°C).
- Phosphorous-silicate glass removal.
- Phosphorous drive-in (1050°C) and silicon oxide growth.
- Use the third mask to remove the n-channel gate oxide within the base, and clean the gate surface.
- Thermally grow a silicon dioxide of 1000Å with dry O_2 at 950°C.
- Phosphorous-silicate glass gettering, glass removing, and annealing.
- Use the fourth mask to define the base, the emitter, the collector contact windows.
- Al metalization (E-beam).
- Use the fifth mask to define the metalization pattern.
- Sintering and testing.

sistor with interdigitated structure. It is clearly seen that the Lambda bipolar transistor can be easily incorporated with the existing integrated-circuit technologies. It should also be noted that ion implantation, silicon gate, and SOS technologies also may be used for high-performance applications.

IV. Experimental Results and Theoretical Comparisons

The typical characteristics of the common-emitter configuration of the fabricated n-p-n Lambda bipolar transistor are shown in Fig. 6. The starting wafer is the n-type silicon substrate with ⟨111⟩ surface orientation and sheet resistivity of 3-5 $\Omega \cdot$ cm. For the n-channel Al-gate MOSFET, the effective channel length L is about 19 μm, the channel width Z is 75 μm, the gate oxide t_{ox} thickness is 1000 Å, the depth of the source and the drain n^+ diffusion W_E (equal to the depth of emitter diffusion) is about 3 μm, the base junction depth is about 6 μm, the threshold voltage without substrate bias is about 7.8 V which is roughly in agreement with the surface concentration of $4 \times 10^{17}/cm^3$ and surface fixed charge of $5 \times 10^{11}/cm^2$ for ⟨111⟩ silicon surface orientation. For the n-p-n bipolar transistor within the Lambda bipolar transistor, the base junction depth is about 6 μm and the emitter junction depth is 3 μm, which gives the effective basewidth of 3 μm, and the sheet resistivities of the base and the emitter are established to be 170 and 2 $\Omega/\square$, respectively. The common-base output characteristic of the same device is also shown in Fig. 7.

Since the substrate bias effect increases with the base current drive for high base surface concentration, the onset voltage of the negative differential resistance is much reduced as the base current drive I_B' is increased, no matter how high the threshold voltage of the n-MOS at zero bias is. Although the surface concentration of the n-MOS is high, which will give lower source-drain breakdown voltage, the emitter-base voltage drop $V_{BE,sat}$ of the n-p-n transistor is only 0.8 V which is just the source-drain voltage of the MOSFET, hence, the n-channel MOS will never be in breakdown for a practical base diffusion process. This is one of the merits of the Lambda bipolar transistor configuration. The breakdown voltage of the Lambda transistor is completely controlled by the following factors: n-channel MOS gate oxide dielectric field strength and oxide thickness, and the base-collector junction breakdown of the n-p-n bipolar transistor. Hence high breakdown voltage of the Lambda bipolar transistor can be easily obtained by lowering the collector doping concentration and increasing the n-MOS gate oxide thickness. In the present case, the emitter-to-collector breakdown voltage, BV_{CEO}, is about 100 V.

In order to check the theoretical calculations presented in Section II, the circuit model with nonlinear β of 32, 34, and 37 for I_B' of 10, 20, and 30 μA, respectively, and the empirical parameters of $K = 180$ and $r = -0.48$ for effective n-channel surface mobility, and the collector series resistance of $r_{SC} = 466\ \Omega$, are used to fit the experimental data as shown in Fig. 8. The slight discrepancy for the characteristic of low base current drive I_B' is mainly due to the ambiguous definition of the threshold voltage and the subthreshold effect of n-channel MOSFET. Hence, the threshold voltage V_T' defined by (5) is not accurate for the best fit at low base current drive, but is more accurate as the base current is high. In regard to the empirical relation of surface mobility, the positive coefficient of

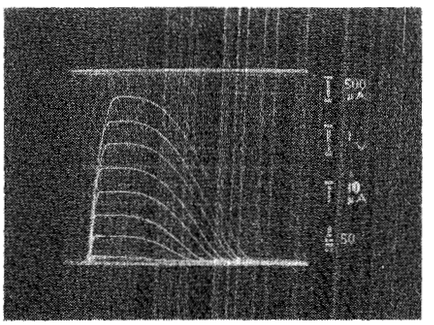

Fig. 6. The common emitter output characteristic of the fabricated Lambda bipolar transistor operated with the current steps driven at the base terminal B'.

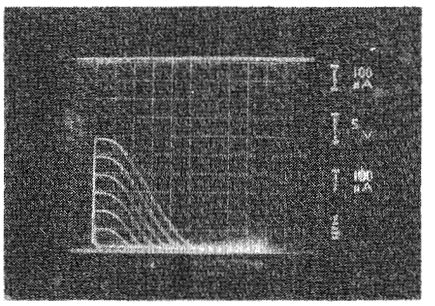

Fig. 7. The common-base output characteristic of the fabricated n-p-n Lambda bipolar transistor as shown in Fig. 6.

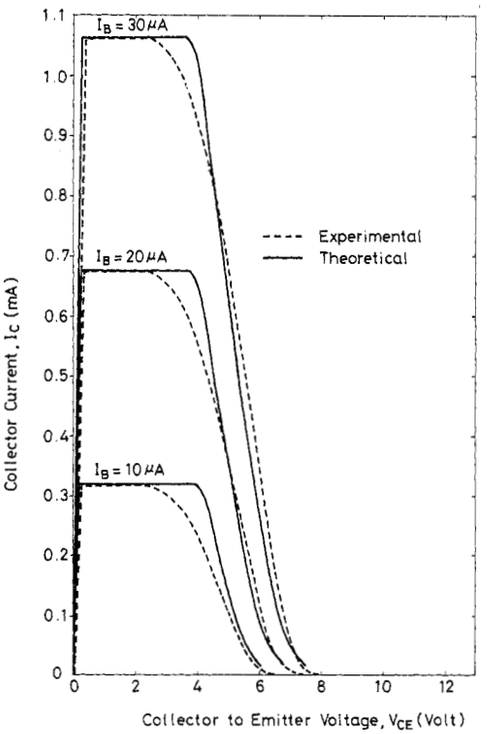

Fig. 8. Comparisons between the collector-emitter output characteristic obtained from the dc analysis (solid lines) with the experimental curves (dotted lines).

gate voltage dependence shows that electrons in the inversion layer of the n-channel MOS are mainly scattered by surface impurity below the peak mobility curve as indicated by other authors [19], [20] for high-threshold-voltage n-channel MOSFET with substrate bias. It should be noted that the general agreement for high base current drive is good for the present theory.

V. Conclusion

A new integrated three-terminal voltage-controlled negative-resistance transistor, the Lambda bipolar transistor, obtained by an integrated device consisting of a bipolar transistor merged with a MOSFET of the same carrier type, is studied both experimentally and theoretically. It is shown that the Lambda bipolar transistor can easily be incorporated into the existing fabrication technologies of bipolar transistor integrated circuits and MOS integrated circuits. It has a remarkably simple structure, small dimensions, and a controllable negative-resistance region. The sectional model developed is in good agreement with the experimental characteristics observed with the fabricated Lambda bipolar transistor. A wide variety of applications [21] for the Lambda bipolar transistor, such as: oscillator, switch, amplifier, and memory function, are expected. The detailed device ac performance, characterization, and system applications are still being explored and will be addressed in future publications.

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