Day for helpful discussions, and the Director of Research of the British Post Office for permission to publish this letter.

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EASILY TESTABLE SEQUENTIAL MACHINES WITH EXTRA INPUTS AND EXTRA OUTPUTS

Indexing terms: Logic, Sequential machines, Switching

In a recent paper, Fujiwara *et al.* presented an efficient procedure for designing checking experiments for sequential machines. In this procedure any arbitrary sequential machine is augmented to an easily testable machine by adding only two special input symbols to the original machine. An easily testable machine is defined by the authors as a reduced and strongly connected machine which possesses a distinguishing sequence as well as a synchronising sequence of length $[\log_2 q]$, and a transfer sequence with a length that is at most $[\log_2 q]$ to take the machine from a specific state S_1 to a state S_i for all *i*, where *q* is the number of machine states, and $[r]$ denotes the smallest integer greater than or equal to *r*. For a *q*-state, *p*-input symbol easily testable machine, the authors' procedure provides an upper bound on the length of the checking experiment that approximately equals $pq[\log_2 q]$. Furthermore, the entire checking experiment happens to be preset. This letter reports an extension of the aforementioned work of Fujiwara *et al.* In the procedure developed through this extension, any arbitrary sequential machine is augmented to an easily testable machine, by adding not two special input symbols alone, but simultaneously adding $[\log_2 q]$ output terminals to the original machine. This modification gives a reduced upper bound on the lengths of the checking experiments, and also permits coverage of fault types that may cause an increase in the number of machine states.

Introduction: With increasing use of modules and integrated circuits in today's digital systems, it has become necessary to be able to decide from terminal measurements alone whether or not a given sequential circuit operates properly. Simultaneously more efforts are also being made to design circuits which are easy to maintain, and for which rather simple and practical fault detection experiments can be designed. In his pioneering work of 1956, Moore[1] first considered the problem of determining if a machine under investigation accurately represents the behaviour specified by its state table, or its transition diagram, by simply observing the machine's response to various applied input sequences. Since then the problem of fault detection, and design of checking sequences for sequential machines, has been considered by many authors.[2–10] The majority of the procedures developed so far for designing checking experiments for sequential machines are primarily based on the transition checking approach originally proposed by Hennie.[3]

Hennie's method yields quite satisfactory results for machines that possess distinguishing sequences, and for machines that are reduced and strongly connected, and further, when the actual machine has no more states than the correctly operating machine. However, for machines which do not possess distinguishing sequences, Hennie's procedure turns out to be extremely complicated, and also yields very long experiments, which renders it somewhat impractical. To overcome this obvious shortcoming, several authors have suggested methods for modifying a given sequential machine into a new one for which short checking experiments can be readily designed.[4,6–10] The different modification schemes proposed in this context are based on (*a*) a method of adding extra outputs, (*b*) a method of adding extra inputs and (*c*) a method that represents a combination of both. The main objective in these modifications is to obtain distinguishing sequences when the original machine does not possess any, to reduce the lengths of the distinguishing sequences, to get transfer sequences of relatively short lengths to take the machine from a specific state to its other states, or even to obtain synchronising sequences besides distinguishing sequences to reduce the overall lengths of the checking experiments for the machine under consideration, and to render it easily diagnosable. Note here that a modified machine is always strongly connected even if the original machine is not. For a *q*-state, *p*-input symbol sequential machine, method *a* provides an upper bound on the lengths of checking experiments[4] that is $(p-1)q^3$, method *b* furnishes an upper bound on the lengths[6] that is $(q + [\log_2 q])(1 + pq)$, and method *c* gives an upper bound[10] that equals $(q + 1) + p(q^2 + 3q)/2$, where $[r]$ denotes as usual the smallest integer greater than or equal to *r*.

In a recent paper, Fujiwara *et al.*[7] described a method of augmenting an arbitrary sequential machine to an easily testable machine by adding two special input symbols, and also gave an efficient procedure for designing a checking experiment for the augmented machine. An easily testable machine as defined by the authors is a reduced and strongly connected machine that possesses a distinguishing sequence as well as a synchronising sequence of length $[\log_2 q]$, and a transfer sequence with a length that is at most $[\log_2 q]$ to take the machine from a specific state S_1 to a state S_i for all *i*, where *q* denotes the number of machine states as before. For a *q*-state, *p*-input symbol machine, the authors' procedure gives an upper bound on the lengths of checking experiments that equals $(3q + 1) \times [\log_2 q] + pq(2[\log_2 q] + 1)$. For large *p* and *q*, this bound is smaller than the bound reported earlier by Holborow,[6] which provides the best bound in the previous methods. Furthermore, the total checking experiment happens to be preset, and hence requires no adaptive initialising sequence that adaptively brings the machine under test to the starting state. The present letter reports an extension of the aforementioned work of Fujiwara *et al.* In the procedure developed in this extension, an arbitrary sequential machine is augmented to an easily testable machine, by adding not two special input symbols alone, but simultaneously adding $[\log_2 q]$ output terminals to the original machine. This modification provides a reduced upper bound on the lengths of the checking experiments, and also allows coverage of fault types that may cause an increase in the number of machine states.

Assumptions and basic definitions: The sequential machines considered in this letter are assumed to be finite, deterministic and synchronous machines of the Mealy type, and are not required to be reduced, strongly connected and completely specified. A sequential machine *M* will be represented by the quintuple $M = \langle I, S, O, f, g \rangle$, where $I = I_1, I_2, \ldots, I_p$ denotes the input alphabet, $S = S_1, S_2, \ldots, S_q$ denotes the state alphabet, and $O = O_1, O_2, \ldots, O_r$ the output alphabet, and *f* and *g* denote the two characterising functions of machine *M* given by $j : SXI \rightarrow S$, called the next state function, and $g : SXI \rightarrow O$, called the output function. By an experiment on a machine *M* we mean the application of input sequences to the input terminals, and the recording of the corresponding responses from its output terminals. If the experiment is designed to take the machine through all its state transitions in such a way that a definite conclusion can be arrived at as to whether or not the machine operates correctly, it is said to be a fault detection experiment, or a checking experiment. At the beginning of an

experiment the machine is said to be in the initial state. An experiment is said to be preset if the entire applied input sequence is completely determined in advance, and it is said to be adaptive if the choice of the next input sequence to be applied depends upon the output response previously produced. A synchronising sequence $\bar{I}_s$ for a machine M is an input sequence whose application is guaranteed to leave the machine in a certain final state, regardless of the particular initial state of the machine. A distinguishing sequence $\bar{I}_d$ for a machine M is an input sequence whose application helps to determine the unknown initial state of the machine by observing the corresponding output response that the machine produces. A transfer sequence from a state S_i to a state S_j, $\bar{I}_{tj}$, of a machine M is the shortest input sequence which transfers the machine from state S_i to state S_j. A machine $M' = \langle I', S', O', f', g' \rangle$ is called a submachine of a machine $M = \langle I, S, O, f, g \rangle$, if and only if $I' \subseteq I, S' \subseteq S, O' \subseteq O$, and $f' = f$ restricted to $S' X I'$, and $g' = g$ restricted to $S' X I'$. An easily testable machine as was originally defined by Fujiwara et al. is one for which a short preset checking experiment can be readily designed following a simple algorithm. This is possible because such a machine possesses a short distinguishing sequence, a short synchronising sequence and short transfer sequences. In this letter, an easily testable machine is defined in a slightly different form. We define an easily testable machine as a reduced and strongly connected machine with the following attributes: it possesses (a) a distinguishing sequence $\bar{I}_d$ of length 1, (b) a synchronising sequence $\bar{I}_s$ of length $[\log_2 q]$, and (c) transfer sequences $\bar{I}_{ti}$ with a length that is at most $[\log_2 q]$ to move the machine from some specific state S_1 to a state S_i for all i, q denoting the number of states of the machine, and $[r]$ denoting the smallest integer greater than or equal to r as usual. Such an easily testable machine can be realised by the state table of a q-state, 2-input symbol binary shift register with $[\log_2 q]$ output terminals, as we shall see next.

Augmenting an arbitrary machine to an easily testable machine by adding extra inputs and extra outputs: We now present a procedure to augment a given q-state, p-input symbol machine to an easily testable machine by adding two extra input symbols, and $[\log_2 q]$ output terminals. Suppose that any failure that is likely to occur may as well occur throughout the fault detection experiment, and further, failures may cause an increase in the number of machine states. For a machine realised by binary devices, we may note that the probability of occurrence of faults that may cause an increase in the number of machine states is indeed rather small when the number of states q happens to be an integral power of 2, since in this case physical creation of new state variables would have been implied. However, when q is not an integral power of 2, or when more than $[\log_2 q]$ state variables are used in the realisation, such faults are very likely to occur. Hence it is only realistic to include such faults in the class of allowable failures. Assume now that $M = \langle I, S, O, f, g \rangle$ is a given machine; without any loss of generality, further assume that the number of states q of the machine M satisfies the inequality $2^{m-1} < q < 2^m = q'$, where $m = [\log_2 q]$ is the total number of memory elements or state variables used in the realisation of M. We use the following procedure to augment M so that the augmented machine M^* becomes an easily testable machine:

(a) Add new states $S_{q+1}, S_{q+2}, \ldots, S_{q'}$ to machine M, where $q' = 2^m$, and $m = [\log_2 q]$, the number of state variables.

(b) Assign an m-bit binary code to each state of M, with each state having exactly one assignment.

(c) Add new input symbols I_{e0}, I_{e1}, and $m = [\log_2 q]$ output terminals $z_1, z_2, \ldots, z_m$ to machine M.

The next state function f corresponding to the new input symbols I_{e0}, I_{e1} are defined as follows: for each present state S_i of M, with a state assignment $y_1 y_2 \ldots y_m$, where an y_i, $i = 1, 2, \ldots, m$, represents a present state variable, $f(S_i, I_{e0}) = S_j$, and $f(S_i, I_{e1}) = S_k$, where the next states S_j and S_k have state assignments $0 Y_1 Y_2 \ldots Y_{m-1}$ and $1 Y_1 Y_2 \ldots Y_{m-1}$, respectively, an Y_i, $i = 1, 2, \ldots, m$, denoting a next state variable. The output functions g corresponding to the new input symbols I_{e0}, I_{e1} are: $g(S_i, I_{e0}) = i$; $1 \le i \le q$; $g(S_r, I_{e0}) = 0$; $q + 1 \le r \le q'$; $g(S_j, I_{e1}) = j$; $1 \le j \le q' - 1$; $g(S_{q'}, I_{e1}) = 0$. The outputs

corresponding to the added inputs I_{e0}, I_{e1} appear at the added output terminals, the decimal values of the outputs being α and β, elements of the sets: $0, 1, \ldots, q$ and $0, 1, \ldots, q' - 1$, for inputs I_{e0} and I_{e1}, respectively. The effect of the state transitions corresponding to the added inputs is to shift the state assignments simply one digit to the right, and to introduce thus a 0 or a 1 as the new leftmost digit according as the input is I_{e0} or I_{e1}, respectively. Hence this 2-column submachine restricted to inputs I_{e0} and I_{e1} is isomorphic to an m-stage, 2-input symbol binary shift register with $m = [\log_2 q]$ output terminals. The m-stage binary shift register is evidently an easily testable machine as defined earlier, and so also the 2-column submachine restricted to inputs I_{e0} and I_{e1}. The submachine has a distinguishing sequence I_{e0} of length 1, with admissible set[2] $A_1 = S_1, S_2, \ldots, S_q$, and a distinguishing sequence I_{e1} of length 1, with admissible set $A_2 = S_1, S_2, \ldots, S_{q'}$, a synchronising sequence of length $[\log_2 q]$ consisting of inputs I_{e0} and I_{e1}, and similarly transfer sequences with a length that is at most $[\log_2 q]$ to move the machine from an arbitrary state to any of its other states. Since this 2-column submachine is an easily testable machine, the augmented machine M^* with q' states and $(p + 2)$ input symbols is also easily testable.

Example: Consider the sequential machine M_1 given by Table 1. The machine M_1 is not strongly connected and does not have a distinguishing sequence. By using the procedure stated above, we obtain the augmented machine M_1^* as shown in Table 2. The machine M_1^* has a distinguishing sequence I_{e1} with admissible set S_1, S_2, S_3, S_4, a synchronising sequence $I_{e0} I_{e0}$ that takes the machine to the state S_1 (the machine has other synchronising sequences as well), and transfer sequences: $\lambda, I_{e1} I_{e0}, I_{e1}, I_{e1} I_{e1}$, to move it from state S_1 to states: S_1, S_2, S_3, S_4, respectively. Hence the augmented machine M_1^* is an easily testable machine.

Table 1 MACHINE M_1

Input State	0	1
S_1	$S_2, 1$	$S_1, 1$
S_2	$-, -$	$S_3, 0$
S_3	$S_2, 0$	$-, 1$

Table 2 AUGMENTED MACHINE M_1^*

Input State	0	1	I_{e0}	I_{e1}
$S_1(00)$	$S_2, 1$	$S_1, 1$	$S_3, 1$	$S_1, 1$
$S_2(01)$	$-, -$	$S_3, 0$	$S_3, 2$	$S_1, 2$
$S_3(10)$	$S_2, 0$	$-, 1$	$S_4, 3$	$S_2, 3$
$S_4(11)$	$-, -$	$-, -$	$S_4, 0$	$S_2, 0$

The checking experiments for easily testable machines with extra inputs and extra outputs can be designed following the procedure of Fujiwara et. al. The initialising part as well as the validating part of the experiment remains identical to that in Fujiwara et al., whereas the transition checking part needs an additional application of the synchronising sequence to reset the machine to the initial state after checking each transition, because in the present case the distinguishing sequence is simultaneously not a synchronising sequence. The total length L of the checking experiment can be found to be at most

$$|\bar{I}_s| + \sum_{i=1}^{q}(|\bar{I}_{ti}| + |\bar{I}_d| + |\bar{I}_s|)$$
$$+ \sum_{j=1}^{p}\sum_{i=1}^{q}(|\bar{I}_{ti}| + |I_j| + |\bar{I}_d| + |\bar{I}_s|)$$
$$= (2q + 1)[\log_2 q] + q + pq(2[\log_2 q] + 2),$$

$|X|$ denoting the length of X, and this is always less than the bound of Fujiwara et al. so long as $q([\log_2 q] - 1 - p)$ is positive. Thus the length of the checking experiment is reduced in general. Further, in the present approach the faults that cause an increase in the number of machine states can be readily detected. Suppose on the application of a particular input symbol I_j, the transition leads the machine to a faulty state S_x, $q + 1 \le x \le q'$. In such a case an application of the input I_{e0}

will produce an output 0 for S_x; the state S_x can then be definitely identified by applying the input I_{e1} only once, and noting down the decimal value of the output produced.

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KINK-FREE NARROW-STRIPE PROTON-ISOLATED GaAlAs/GaAs INJECTION LASERS

Indexing term: Lasers

Totally kink-free and very-narrow-stripe proton-isolated injection lasers are presented. The standard gold-indium metal-contact bonding system has been investigated, and as a result an improved bonding technique is presented. Kink-free lasers with output power up to 20 mW have been accelerated at 80°C ambient for 1000 h without any change in thermal resistance and with an expected lifetime of above 10^6 h at room temperature.

Much attention has been paid to the problem of how to obtain double-heterostructure lasers with kinkfree light-output/current characteristics. A number of authors have reported different geometrical configurations to solve this particular problem. However, several of these configurations are not very suitable for large-scale production[1-6] or are limited by low output-power capability.[7] Furthermore, several laboratories have reported an increase in the thermal resistance, particularly during accelerated aging of the lasers.[8-10]

We report here the successful operation of a new development of the proton-implanted GaAlAs/GaAs stripe laser. It includes narrow stripes down to around 2 µm width and an

improved metal-contact bonding system. These lasers are totally kinkfree up to output powers where mirror damage occurs, typically around 20 mW (Fig. 1). They are multimode lasers with linear fast pulse response.
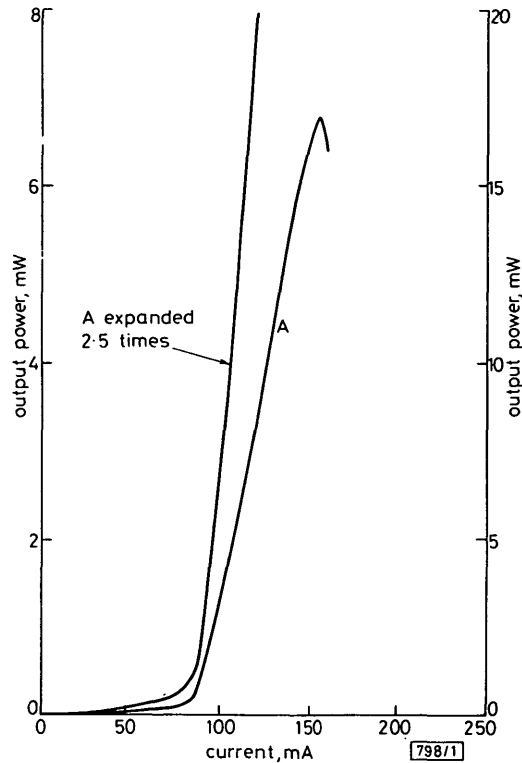

Fig. 1 *C.W. output power as recorded for a narrow-stripe laser showing kink-free behaviour up to the mirror degradation limit. 87 BC-210, 3 µm stripe, uncoated*

Lasers mounted with the improved bonding system have so far been operating for 1000 h at 80°C ambient temperature with low degradation rates and with no increase in thermal resistance. The fabrication technique is straightforward with high yields, and is suitable for large-scale production.

The devices were made from double-heterostructure l.p.e. wafers grown with the same technique used for our earlier lasers,[11] with the addition of aluminium to the active layer. The latter has been shown to dramatically decrease the degradation rate in our lasers. To the n-type substrate, ordinary AuGeNi contacts were evaporated and alloyed. On the heavily p-doped contact layer a thin film of platinum was sputtered. This was followed by a 2 µm thick gold film acting as a mask for the later proton implantation. By a conventional photolithographic process and chemical etching technique, narrow stripes with 2-3 µm width were formed in the gold film. The wafers were then exposed to proton irradiation with an energy just enough to penetrate the contact layer, thus leaving a distance exceeding 1 µm to the active layer. After removal of the gold mask, a thin film of gold was sputtered and the wafers cleaved to chips with cavity lengths of 250 µm.
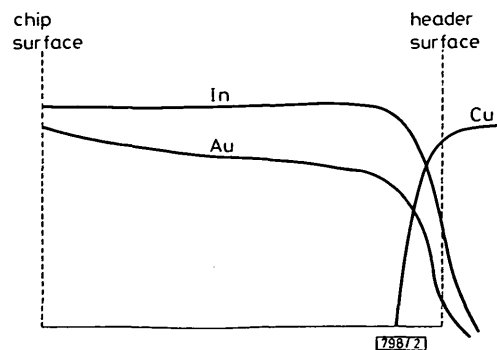

Fig. 2 *S.I.M.S. study of indium and gold on copper header after 300 h at 80°C. Distance between chip surface and header surface is 4 µm*