Chapter 4

Results and Discussion

In this study, in order to characterize and compare the device performance of different recess widths, devices with two different gate recess times were fabricated. Sample *A*, is with a shorter recess time, and the gate recess etch width is 0.2 μm, while Sample *B*, is with a longer recess time, and the gate recess etch width is 0.8 μm. The SEM micrographs of sample *A* and *B* are shown in Fig. 4.1. The optimum ICP dry etching conditions with a high selectivity between SiN_x and SiO_x was applied to achieve a high uniformity of device characteristics across the wafer. The DC, RF, noise and power performance of these two samples are presented and compared as follows.

4.1 DC characteristics

4.1.1 *I-V* characteristics

The current-voltage characteristics of 4 X 40μm devices were measured on wafer using HP 4142 and are shown in Fig. 4.2 and Fig. 4.3. The transconductance g_m and saturation drain current $I_{ds,sat}$ as a function of gate-to-source voltage were measured at V_{ds}= 1.5V. Sample *A* exhibits a higher $I_{ds,sat}$ and V_{th} (620 mA/mm, －1.1 V) than sample *B* (256

mA/mm, －0.6 V). The maximum transconductance of sample *A* is 930 mS/mm at a gate bias voltage of －0.6 V. However, sample *B* shows a higher g_m value of 980 mS/mm at V_{gs}= 0 V. The recess time of sample *B* is longer than sample *A*. By reducing the Schottky layer thickness, a larger g_m but lower I_{ds} can be obtained. The value of g_m is increased because when the distance between gate and channel is reduced, the electron controllability of the gate electrode is improved.

4.1.2 Breakdown voltage

As shown in the Fig. 4.4, the reversed gate to drain breakdown voltage (V_{br}), defined by 1 mA/mm of gate leakage current, are 9 V and 6.6 V for sample *A* and sample *B* respectively. The breakdown voltage of sample *B* is decreased because of slightly gate leakage occurred. We obtained the lower V_{br} by decreasing the thickness of the Schottky layer. Thinner Schottky layer results in higher g_m but it sacrifice the breakdown performance.

4.2 RF characteristics

4.2.1 Unit current gain cutoff frequency (f_T) & maximum frequency of oscillation (f_{max})

Before RF measurements, we must find the optimum DC bias to obtain the maximum current gain and power gain. Figure 4.5 shows the

I_{ds} and V_{ds} dependence of f_T curves for both samples. In this case, f_T is defined as the frequency extrapolated at 10 GHz by a -20 dB/decade slope. From the figure, sample *A* could exhibits the highest f_T value at V_{ds} = 1V and I_{ds} at the range of 30 mA to 40 mA. While the optimum bias conditions of sample *B* are at V_{ds} = 1.25V and I_{ds} at the same range of 30 mA to 40 mA. These bias conditions would be used in the later measurements.

S-parameters were extracted from 1 to 40 GHz under optimum DC bias. The extrinsic current gain cutoff frequency f_T and maximum unilateral gain cutoff frequency f_{max} are determined from the unit current gain and the unilateral gain by extrapolating with a -20 dB/decade slope. As shown in Fig. 4.6, the current gains are 9.8 dB and 10 dB at 40 GHz for samples *A* and *B*, respectively. The MAG/MSG are 13 dB and 10 dB at 40 GHz for samples *A* and *B*. Finally, the current gain cutoff frequency and maximum oscillation frequency of the sample A are 130 GHz and 200 GHz, respectively, under the bias conditions of V_{ds} = 1V and I_{ds}= 35 mA. The f_T and f_{max} of the sample B are 150 GHz and 180 GHz, respectively, under the bias conditions of V_{ds} = 1.25 V and I_{ds} = 40 mA. Apparently, the f_T for sample *B* is higher than that for sample *A* owing to the higher transconductance value.

4.2.2 Noise characteristics

Since higher drain current will lead to noise by electrons scattering

effect, the noise can be reduced as the current decreases. However, decreasing the current will lower the transconductance, the smaller transconductance causes higher noise figure with lower gain. Therefore, there exists an optimum bias condition to achieve the lowest noise performance. Figure 4.7 shows the drain-source current dependence of the minimum noise figure (NF_{min}) at fixed frequency of 16 GHz. The applied drain voltage is fixed at 1.2 V. The lowest NF_{min} can be observed around I_{ds} of 10 mA and 25 mA for samples *A* and *B*, respectively. The noise performances shown in Fig. 4.8 are measured over a frequency range of 1 GHz to 16 GHz with the optimum bias conditions. The measured minimum noise figure (NF_{min}) at 16 GHz were 0.69 dB and 1.42 dB for samples *A* and *B*, respectively. In addition, the associated gain of sample *A* and sample *B* at 16 GHz were 9.767 dB and 13.33 dB, respectively.

4.2.3 Power performance

The microwave power characteristics were evaluated by a load-pull system with automatic tuners, which provided conjugate matched input and load impedances simultaneously for the maximum output power. Figure 4.9 is the output power contours. In order to obtain the maximum output power, the source gamma of $0.8\angle 27.3^\circ$ was fixed. As shown in Fig. 4.9, with a -5dBm input power, the load-impedance locations for the maximum output power was 16.57 dBm at $G_L = 0.125\angle 154^\circ$ from the load-pull measurement.

Load-pull power performance was measured at 2.4 GHz and 6 GHz respectively under drain bias of 2 V, 2.4 V. The gate bias was chosen at class AB operation. Figures 4.10 and 4.11 show P_{out}, Gain, and PAE as a function of the input power (P_{in}) for the 4 x 40 μm devices. Sample *A* exhibits a saturated P_{out} of 17.67 dBm (power density of 365.49 mW/mm), a linear power gain of 27.83 dB, and a PAE of 57.7% at 2.4 GHz. For sample *B*, the linear power gain was 24.56 dB, and the maximum output power density was 114.5 mW/mm with a maximum PAE of 45% at 2.4 GHz.

As to the power performances at 6 GHz, sample A demonstrated a saturated P_{out} of 14.86dBm (power density of 191.3 mW/mm), a PAE of 57.1% and linear power gain of 27.04 dB. For sample B, the linear power gain was 23.71 dB, and the maximum output power density was 126.14 mW/mm with a maximum PAE of 49.3% at 6 GHz.

4.3 Uniformity

In order to verify that the sidewall gate process can achieve good device performance with high yield, we evaluated 168 devices on the sample A. The performance of 4 x 40 μm devices are shown in Fig. 4.12. Most of the sidewall gate devices achieved a threshold voltage of -1.1V with a standard deviation (S.D.) of 0.2 V. The average g_m of these device was 631.59 mS/mmm, corresponding to a standard deviation of 69.42

mS/mm. This result confirms the merit of the sidewall gate process in the device fabrication.

4.4 Summary

Table 4.1 summarized these DC characteristics of the devices with different recess widths. Based on the measured dc performance evaluations, devices with small drain saturation current demonstrated a larger dc gain, which is directly associated with the facts that the gate was closer to the channel. Tables 4.2 and 4.3 also show a summary of the RF, noise and power performances. It can be seen that sample *B* had the higher value of f_T. But this sample also had slight gate leakage current, the breakdown, noise and power performances of sample *B* were degraded due to this reason. In summary, Sample *A* demonstrated a better device performance than that of sample *B*.