Chapter 5

Conclusions

The 90nm sidewall gate process was developed in this work. By adjusting the dry etching parameters, a high SiN_x/SiO_x etching selectivity of 16 can be achieved within a SF₆ plasma system (SF₆= 10 sccm, ICP power= 50 W, RF power =50 W, chamber pressure =15 mTorr). The surface roughness analysis was carried out by AFM measurement. From the results, SF₆ gas system dose not cause significant surface roughness. It is suitable to use this process for the formation of the first opening of the gate. Owing to the high selectivity between SiN_x/SiO_x , we could efficiently control the gate length below 100 nm without the constraint resolution of e-beam from the lithography. Sub-100nm In_{0.52}Al_{0.48}As/In_{0.52}Ga_{0.48}As MHEMTs have been successfully developed by the sidewall gate process. The sidewall gate process also achieves a good uniformity of the device performance.

We also compare the devices fabricated by sidewall gate process with different gate recess widths. Although device with the wider recess width gave a higher f_T value due to a higher transconductance, other device characteristics were sacrificed, such as breakdown voltage, noise and power performance etc. Based on the experiment results, we can conclude that sidewall gate process with optimum recess width could be used for MHEMT fabrication and achieve a high performance. The MHEMT fabricated by optimum recess condition had a maximum

transconductance of 930 mS/mm, and the saturation drain current density was 620 mA/mm at 1.5 V. The current gain cut-off frequency and maximum oscillation frequency were 130 GHz and 180 GHz, respectively. The device exhibited a minimum noise figure of 0.69 dB with 9.767 dB associated gain at 16 GHz. The device had power density of 365.49 mW/mm, and the linear power gain was 27.83 dB with a maximum PAE of 57.7% at 2.4 GHz.

In conclusions, a 90 nm sidewall gate process was successfully applied to the In_{0.52}Al_{0.48}As/In_{0.52}Ga_{0.48}As MHEMT manufacturing. The fabricated MHEMTs demonstrated very high RF performances. This highly reproducible and damage-free sidewall gate technology could be used for nano gate fabrication for high frequency device application in the future.