# Reference

[1.1] S.M. Sz, “High speed semiconductor device”, Murray Hill, New Jerey.

[1.2] T. Mimura, S. Hiyamizu, T. Fujii and K. Nanbu, ” A new field-effect transistor with selectivity doped GsAs/n-$Al_xGa_{1-x}As$ Heterojunctuins, ” in Jap. J. Appl. Phys. 19, pp. L225-L227,1980.

[1.3] Frederick H. Raab, Peter Asbeck, Steve Cripps, Peter B. Kenington, Zoya B. Popovic, Nick Pothecary, John F. Sevic and Nathan O. Sokal, ”RF and Microwave Power Amplifier and Transmitter Technologies-Part 1”, May 2003 High Frequency Electronics.

[1.4] M. I. Alsun et al., IEDM Tech. Digest, P. 822, 1986.

[1.5] Dr. A. Bessemoulin, “Achievements and Results”, Fraunhofer IAF 2000.

[1.6] P.M. Smith, et al. BAE SYTEMS, 2001 IEEE GaAs Digest.

[1.7] Tetsuya Suemitsu, Haruki Yokoyama, Tetsuyoshi Ishii, Takatomo Enoki, Yasunobu ISHII, and Toshiaki TAMAMURA, ”30-nm-Gate InP-Based Lattice-Matched High Electron Mobility Transistors with 350 GHz Cutoff Frequency”, Jpn. J. Appl. Phys. Vol. 38(1999) pp. L154-L156.

[1.8] Yoshimi Yamashita, Akira Enodoh, Keisuke Shinohara, Masataka Higashiwaki, ”Ultra-short 25-nm-Gate Lattice-Matched InAlAs/InGaAs HEMTs within the Range of 400 GHz Cutoff Frequency”, IEEE ELECTRON DEVICE LETTER, VOL. 22, NO. 8, AUGUST 2001

[1.9] Szu-Hing Chen, Huang-Choung CHANG, David K. Fu, Edward Y.

CHANG, Yeong-LAI and Li CHANG, ”Novel I-Line phase shift Mask Technique for Submicron T-shaped Gate Formation”, Jpn. J. Appl. Phys. Vol. 41(2002) pp. 4489-4492.

[1.10]Yi-Chung Lien et al.,” A metamorphic high electron-mobility transistor with reflowed submicron T-gate for high-speed optoelectronics applications” IEEE (2003).

[1.11] Huang-Ming LEE et al.,”New Nanometer T-Gate Fabrication by Thermally Reflowed Resist Technique” Jpn. J. Appl. Phys. Vol. 41(2002) pp. L1508-L1510

[2.1] S A McAuley, H Ashraf, L Chambers, S Hall, J Hopkins and G Nicholls, ” Silicon micromachining using a high-density plasma source”, J. Phys. D: Appl. Phys. 34 (2001) 2769-2774.

[2.2] 楊世丞”活性離子時刻技術於磷化銦鎵鋁/砷化銦鎵通道滲雜場效應電晶體元件之製作與分析”,中央大學電機工程研究所博士論文 (2003)

[2.3] C. Reyes-Betanzo et al., ”Silicon nitride etching in high- and low-density plasmas using $SF_6/O_2/N_2$ mixtures”, J. Vac. Sci. Technol. A 21(2), Mar/Apr 2003.

[3.1] Dae-Hyun Kim, Suk-Jin Kim, Young-Ho Kim, Sung-Wong Kim, and Kwang-Seok Seo,” Damage-free SiO/sub 2//SiN/sub x/ side-wall gate process and its application to 40 nm InGaAs/InAlAs HEMT's with 65% InGaAs channel ” ,Indium Phosphide and Related Materials, 2003. International Conference on 12-16, May 2003

[3.2] Kamal Tabatabaic-Alavi et al.,” Evolution of T-Shaped Gate Lithography for Compound Semiconductors Field-Effect Transistor”,

IEEE Transactions on Semiconductor Manufacturing, vol.16. NO. 3. August 2003

[3.3] William Liu," Fundamentals of Ⅲ-Ⅴ Devices, HBTs, MESFETs, and HFETs/HEMTs ".

[3.4] DIETER K. SCHRODER, "SEMICONDUCTOR MATERIAL AND DEVICE CHARACTERIZATION", WILEY INTERSCIENCE.

[3.5] H. Philip Li, Olin L. Hartin, and Marcus, "An Updated Temperature-Dependent Breakdown Coupling Model Including Both Impact Ionization and Tunneling Mechanisms for AlGaAs/InGaAs HEMTs ", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 49, NO. 9, SEPTEMBER 2002.

[3.6] Sun-Chin Wei, "Electrical Analysis and Low-Frequency Noise Investigations of the AlGaN/GaN High Electron Mobility Transistors", Department of Electrical Engineering National Cheng Kung University, Tainan, Taiwan, R.O.C

[3.7] 本城和彥,"微波通訊半導體電路," 全華科技圖書.

[3.8] OSAMU WADA et al.," InP-Based Materials and Devices Physics and Technology", p.361.