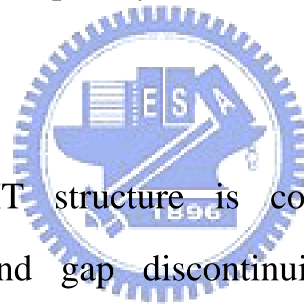
Chapter 1
Introduction

In recent years, the development of high frequency devices has become a hot topic. The demand for high-frequency devices is increasing greater with respect to two major applications: high-speed optical fiber communication systems and high-frequency wireless systems. With the rapid development of the wireless communication systems such as the CMOS and PCS (personal communication system), the requirements of low cost, low power consumption, high-level integration and high frequency operation become more and more significant. For high frequency applications, compound semiconductor devices such as GaAs PHEMTs, MHEMTs, InP PHEMTs, have shown superior performance, in high-speed applications. Many effects have been made to improve the device performance. Devices with better carrier, higher electron mobility and shorter gate length by use of refined heterojunction structure and novel gate shrinkage technique have shown outstanding performances. In this study, a high RF performance lattice-matched MHEMT with nanometer gate was developed by using a sidewall gate technology.

1.1 Overview of high speed devices

In the past, there is a great demand in developing high performance GaAs transistors for wireless communication applications. As compared

with the silicon-based transistors, such as metal-oxide-semiconductor field effect transistors (MOSFETs) and bipolar-junction transistor (BJTs), GaAs transistors exhibit inherent advantages over Si-based transistors for high frequency applications [1.1]. GaAs high electron mobility transistor (HEMT) is a kind of the field-effect transistors invented by a Japance, Takashi Mimura [1.2]. GaAs HEMTs have been successfully manufactured and commercialized in many applications. The special epitaxial layers of the HEMT structure are designed to form two-dimension electron gas (2-DEG) in the channel layer and band-gap discontinuity to separate the ionized donors from the channel to increase the electron mobility. Consequently, GaAs HEMTs have superior carrier transport properties.



Conventional HEMT structure is consisted of AlGaAs/GaAs heterostructure. The band gap discontinuity between AlGaAs/GaA increases as the Al content increases and the large discontinuity in the band gap results in better confinement of the electrons in the channel. However, the deep-complex center (DX center) phenomenon exists while Al content is over 20% [1.1].The DX center traps the electrons and influencse the device performance. To avoid the DX center phenomenon and increase electron mobility, AlGaAs/InGaAs/GaAs pseudomorphic HEMT (PHEMT) structure was introduced. InGaAs is a preferred channel material for HEMT's because of its excellent transport properties. The In content in the channel has been increased to enhance the electron transport properties and the confinement of the carrier in the channel. However, InGaAs channel in PHEMTs is limited to an In content of 25%

[1.3] to avoid lattice relaxation of the channel.

Higher In mole fractions are feasible in the HEMT structure on InP substrates, *e.g.*, lattice matched $In_{0.52}Al_{0.53}As/In_{0.53}Ga_{0.47}As$ heterostructures in InP. InP-based HEMTs have shown very high frequency characteristics, low noise figure, high gain, and efficiency compared to PHEMTs [1.4]. However, InP substrates are more expensive, smaller in size, and more brittle than GaAs substrates. GaAs substrates of 6” diameter are commercially available, while the largest available InP substrates only have a diameter of 4” [1.5]. Therefore, a new device structure, metamorphic HEMT (MHEMT) structure, is developed on GaAs substrates. In the MHEMT structure, the device active layers are grown on a strain relaxed, compositionally graded, metamorphic buffer layer. The buffer layer provides the ability to accommodate the lattice mismatch between InGaAs channel and GaAs substrate. Therefore, the In content of the InGaAs channel can be chose in a large extent in spite of the large lattice mismatch between the active epilayers and the substrate. The relation between lattice constant and bandgap of $In_xAl_{1-x}As$ and $In_yGa_{1-y}As$ is shown in Fig. 1.1. Using the metamorphic buffer layer, PHEMT structure lattice matched to InP can be grown on the GaAs substrates for a substantial cost reduction and manufacturability improvement. Table 1-1 shows the comparisons of the properties between MHEMT and InP HEMT. According Table 1-1 [1.6], MHEMT has the advantage over InP HEMT in cost and fabrication yield. Therefore, this study will focus on the development of MHEMTs. The high frequency performance of HEMT can be improved by optimizing the device

structure and reducing the gate length. A shorter gate is very essential for achieving ultra-high RF performance. Therefore, in next section we will discuss the technologies of gate length shrinkage.

1.2 Technologies of shrinking the gate length

Tetsuya et al. [1.7] had proposed a nanocomposite resist (a mixture ZEP-520 and fullerences C_{60}) system that incorporated sub-nm carbon particles into a resist film to enable an ultra thin resist process for nanometer pattern fabrication. Fullerence-incorporated nanocomposite resist, which can enhance dry-etching resistance and pattern contrast, was able to achieve high resolution. Gate footprint by electron beam direct writing can achieve a fine feature size of 30nm as shown in Fig. 1.2. The gate pattern was defined and replicated on SiO_2 /SiN_x layers. After forming the gate opening, both SiO_2 nd SiN_x were etched by C_2F_6 RIE and then the side-etching of SiN_x was done by using SF_6 RIE in order to reduce the aspect ration of the gate foot. Figure 1.3 was the SEM photography of the cross section of the 30-nm T-shaped gate.

Fabrication of ultra-short 25-nm-gate has been demonstrated by Yoshimi Yamasita et al. [1.8] using the two-step SiO_2 dielectric layer deposition and two-step recess to confirm the ultra short gate. Firstly, a 20 nm SiO_2 was deposited over the cap layer. The gate pattern was written and replicated on the SiO_2 film by RIE using CF_4 gas. After RIE, the first gate recess in cap layer was formed by wet-chemical etching (C.A. and H_2O_2 mixture). The second 20 nm SiO_2 film was re-deposited over the

wafer and etched again by RIE with CF_4 gas. Finally, the foot of the T-shaped gate was formed, then with second gate recess. The second gate recess was formed by using the same solution as that for the first one. Figure 1.4 showed the final cross-section structure after gate metal deposited.

Szu-Hung Chen et al. [1.9] developed a phase shift mask (PSM) technique to define the 0.16μm gate length by I-line lithography. The 2000Å SiN_x was first deposited by chemical vapor deposition (CVD). Then the 8% half-tone PSM was used for the definition of the SiN_x opening. After the PSM exposure, the SiN_x was etched by RIE, and a 0.2-μm-wide opening was formed. In order to further reduce the dimension of opening, an addition SiN_x was deposited by CVD and etched back by RIE without any mask. Using the silicon nitride re-deposition and etch-back technologies could reduce the dimension of the openings. Finally the T-shaped gate with a length of 0.16μm was achieved. The overall process is depicted in Fig. 1.5.

Yi-chung Lien et al. [1.10] had demonstrated that resist reflowed T-gate [1.11] is another alternative for gate shrinkage. Photo resist of T-shaped gate profile after e-beam lithography was thermally treated by hotplate and the gate foot opening then shrinks from 0.25 μm down to 0.1 μm (see Fig. 1.6). Reflow gate process is a simple, relatively inexpensive, and flexible process for the fabrication of nano-scale T-shaped gate.

1.3 Outline of this dissertation

It is well recognized that the high frequency performance of the HEMTs will be improved when the gate length is reduced. Many technologies about shrinking the gate length were described in the previous section. In this dissertation, a newly developed gate shrinkage technique, sidewall gate process is introduced in order to overcome the restriction of resolution limit of the equipment.

In chapter 2, we first introduce the system of Inductive coupled plasma (ICP), including the ICP apparatus and principle of ICP. Then, we will discuss SiN_x and SiO_x etching mechanisms and characteristics. By changing different provess parameters, *e.g.*, Ar flow, chamber pressure, RF power….*et al.*, we can obtains adequate etching rate and selectivity are described.

In chapter 3, a detailed description of sidewall process is given. The fine pattern is obtained through the formation of the sidewall gate spacer which results from sequent depositing and etching dielectric layers (SiN_x and SiO_x) (see Fig.1.7). As long as the selectivity of SiN_x over SiO_x is high enough, the uniformity of the gate length could be well-controlled with a large tolerate variation of etching process time. Therefore sidewall gate process is reproducible and can achieve a good uniformity.

In chapter 4, the optimum dry etching condition for the sidewall gate process is applied to fabricate high-performances. The DC, RF, noise and

power performances of the MHEMTs will be presented. Then, in the final chapter, we will summarize and conclude the experiment results in this thesis and present give some suggestions for future studies.

property	InP HEMT	MHEMT
Substrate Availability, Cost	- 4-inch now,higher cost	+ 6-inch available now
MBE Growth Time	+ ～1/2 hour	- 1-2 hours
Process Difficulty Yield	- Higher breakage, more difficult /slower backside process	+ Lower breakage, standard GaAs backside process
Performance, Impedance char.	No difference	No difference
Achievable Channel In Content	53-80 %	30-80 %
Thermal Resistance	+ InP has 50% higher thermal cond. than GaAs	Comparable to GaAs PHEMT, effect of buffer unclear
Reliability	Proven for low noise, unproven for power	Excellent initial data for low noise, power unknown

Table 1.1 Comparison of lattice-matched InP HEMT and metamorphic GaAs HEMT

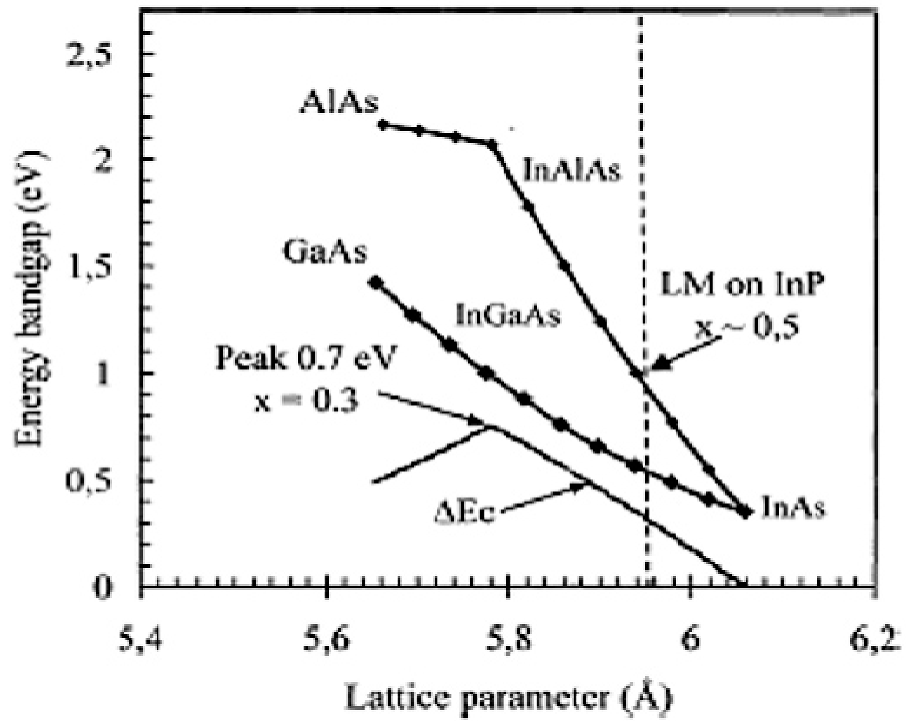


Fig. 1.1 Energy band gap v. s. lattice constant for $In_xAl_{1-x}As/In_yGa_{1-y}As$ system

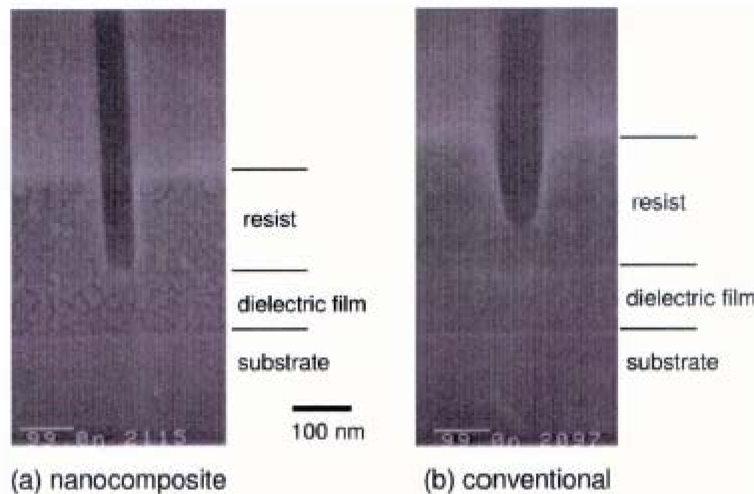


Fig. 1.2 SEM photographs of the EB resist pattern for nanocomposite and conventional ZEP

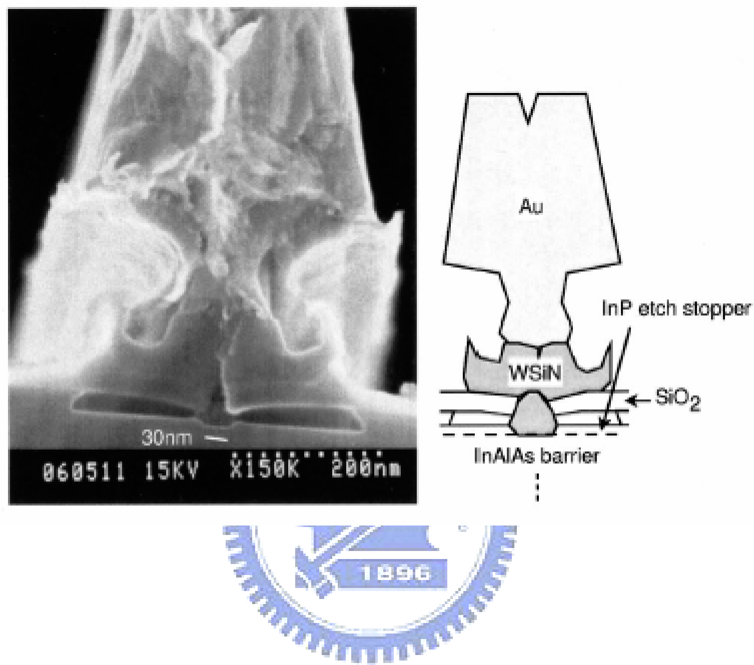
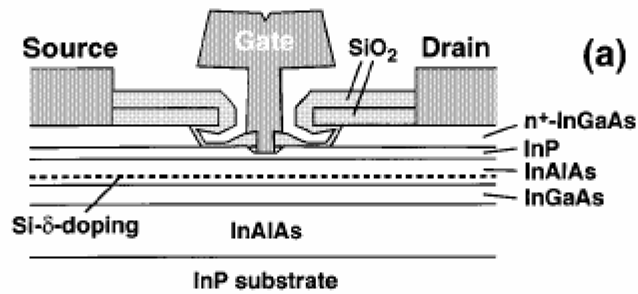


Fig. 1.3 Cleaved cross section of a 30-nm T-gate. Each material is specified in the figure.



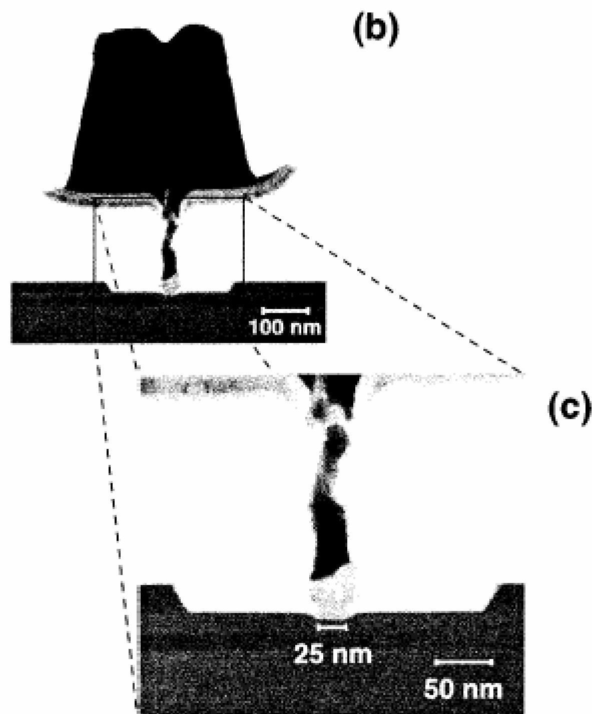


Fig. 1.4 (a) Schematic cross-section view of the HEMT,(b) Cross-sectional TEM image of the 25-nm-long T-shaped gate, and (c) Magnification of the TEM image around the bottom of the 25-nm-long T-shaped gate.

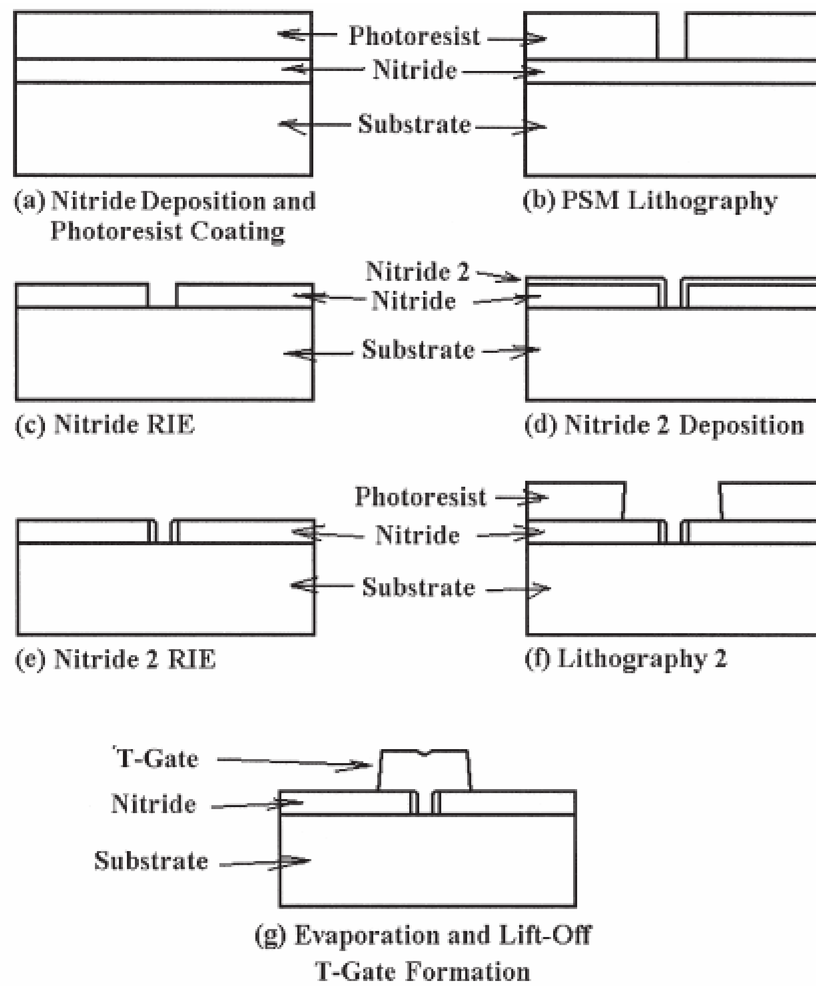


Fig. 1.5 T-gate process flow of the PSM technique

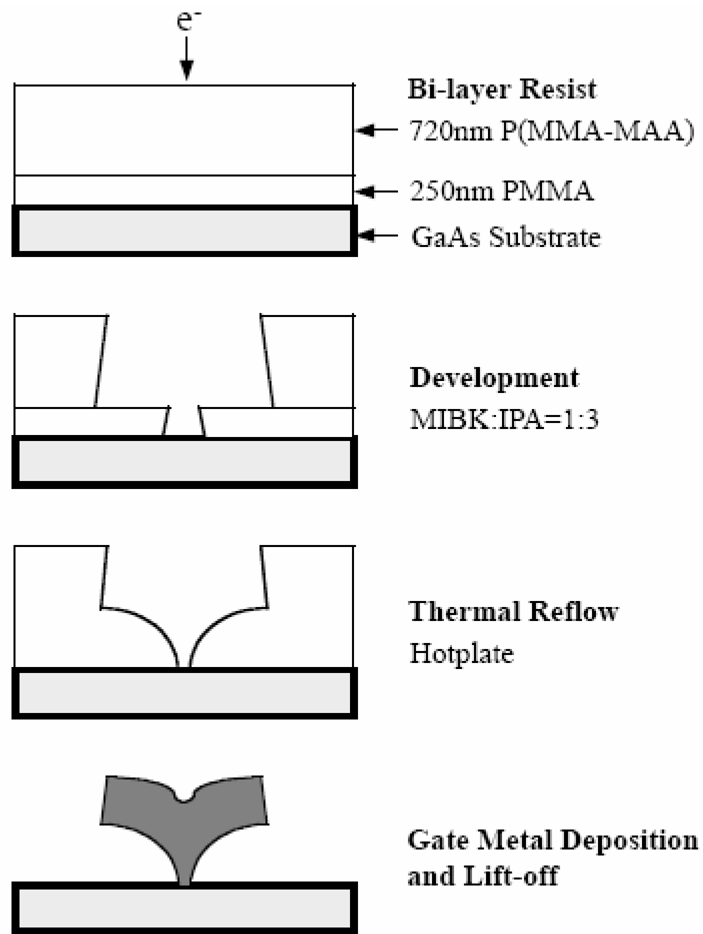
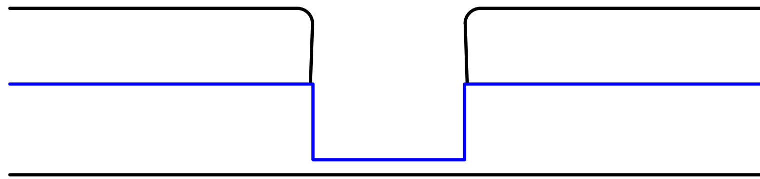
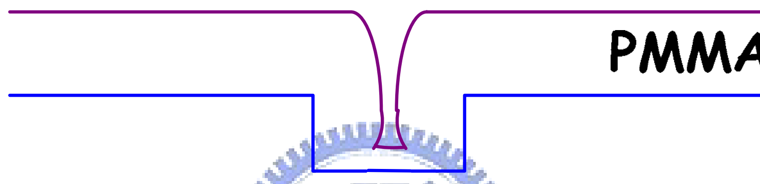


Fig. 1.6 Process flow of the thermally reflowed T-gate

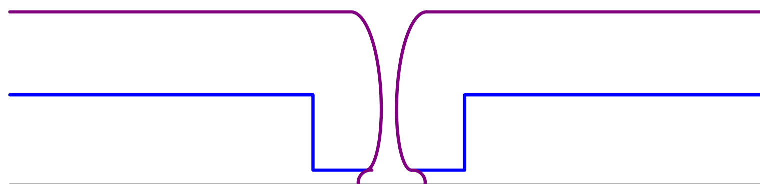


Pattern transfer on SiN_x



SiNx

SiO_2 re-deposition



Over-etch

Fig. 1.7 Sidewall gate diagram

SiO2

SiNx