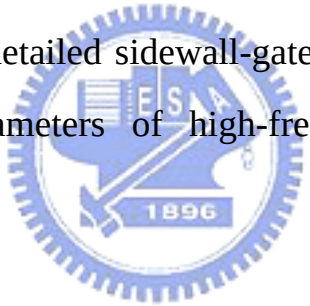
Chapter 3
Experiment and basics of DC & RF characteristics

Recently, the HEMT device characteristics have been improved by reducing the gate length to nano scale and adapting the highly strained InGaAs channel in the device structure. Conventional e-beam lithography machine with an acceleration voltage of 40kV and a tungsten filament might offer about 150 nm resolution on single PMMA layer. To reduce the gate length to sub-100 nm scale, the sidewall gate process was adopted to overcome the lithography limitations. The gate footprint is obtained through the formation of sidewall spacer which results from dielectric layer deposition, etch, re-deposition and etch-back. Among these various process steps, precise control of the etch-back time is very important. Because, it will affect the shape of the final sidewall spacer (gate foot dimension). Unfortunately, it's not easy to control the etch-back time exactly. We chose the two materials, SiO_x and SiN_x, which have high etching selectivity to solve this problem. The shape of the final side-wall spacer (gate foot dimension) is determined by the difference of etching selectivity between SiO_x and SiN_x dielectric layers and the etch-beck time is not so critical [3.1].

Except for achieving a gate length, we also want to reduce the gate resistance and thereby improve the high RF performance of the devices,

as a result, T-shaped gate was used. In practice, we would like to enlarge the T-shaped gate head dimension as much as possible in order to reduce the gate resistance [3.2]. However, for conventional T-shaped gate, the gate head and gate foot are related to each other. For the fabrication of an ideal T-shaped gate, formation of the gate head is independent. The sidewall gate process developed in this study can satisfy this requirement. Furthermore, this technology possesses also provides high reproducibility and uniformity. With these advantages, the device performances can be improved. Finally, a well-controlled gate technology for the fabrication of gate length below 100 nm was developed.

In this chapter, the detailed sidewall-gate process is described. The basic DC and RF parameters of high-frequency devices are also introduced.



3.1 Device structure

The epitaxial layers of the metamorphic HEMT with $In_xAl_{1-x}As$ grading buffer layer were grown by molecular beam epitaxy (MBE). A cross-section structure of the MHEMT is shown in Fig. 3.1. The In graded $In_xAl_{1-x}As$ metamorphic buffer layer was grown on a 3-inch semi-insulating GaAs wafer, followed by an undoped $In_{0.52}Al_{0.48}As$ buffer layer. We used 15 nm $In_{0.52}Ga_{0.48}As$ as the channel layer. The top and bottom Si-planar doping (2×10^{12} cm^{-2}) layers were separated from the channel layer by 4 nm thin undoped $In_{0.52}Al_{0.48}As$ spacer, respectively.

The undoped $In_{0.52}Al_{0.48}As$ Schottky layer was 15 nm. Then, the 18 nm thick $In_{0.52}Ga_{0.48}As$ cap layer was highly doped with Si of 2×10^{18} cm^{-3} for ohmic contact formation.

3.2 Device Fabrication

3.2.1 Mesa isolation

Isolation process defines the active on the wafer for the fabrication of the device. In these specific areas, the current flow is restricted to the desired path and the fabricated devices are isolated from each other. There are three typical ways to achieve device isolation: wet etching, ion bombardment, and selective implantation. The wet etching is the simplest way among them. Mesa isolation was done by a phosphoric based solution. According to the device structure, the device was etched to the buffer layer to provide a good isolation. Finally, the etching depth was measured by α-step or surface profiler after the photo-resist was stripped and the etched profile was checked by Scanning electron microscopy (SEM). To inspect the mesa isolation process, a test pattern with a 10 μm gap is used to measure the leakage current.

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3.2.2 Ohmic contact

After wafer cleaning by using ACE and IPA, the negative photo resist and I-line aligner were used to define the ohmic region and form

undercut profile. Then the ohmic metals Au/Ge/Ni/Au were deposited in the appropriate composition by e-gun evaporation system. After lift-off process, and alloyed at 330℃ for 20 sec in nitrogen atmosphere, source and drain ohmic contacts were formed. After ohmic formation, the contact resistance was measured by the transmission line method (TLM) in the process control pattern monitor (PCM). The typical measured contact resistance was < 1 X10^{-6} Ω-cm^2 (Fig. 3.2).

3.2.3 Sidewall T-shaped gate process

T-shaped gates are essential to improve high frequency performance of the HEMTs. The small gate foot forms the Schottky contact with the HEMT, while the wider gate head provides a low gate resistance. For gate foot definition, a 100 nm thick SiN_x film, which provides good resist adhesion and higher resolution, was deposited by PECVD. Then, the gate foot was defined on a single layer of PMMA. The open size of PMMA was about 150 nm. Figure 3.3 showed the dose dependence of the gate foot size in a single PMMA resist after development. The resist opening was transferred into the nitride layer by dry etching. The ICP etching conditions were optimized as described in chapter 2 to precisely replicate the fine resist patterns on the SiN_x film.

After transforming the patterns on the SiN_x film, another dielectric layer SiO_x of 100nm was re-deposited. The dielectric layers were over-etched, thereby formed the T-shaped gate foot. The final gate length

was reduced by the formation of the two sidewall spacers. Because the shape of the final sidewall spacer was changed during dielectric etch-back, we must control etching rate and etching selectivity carefully to obtain the desirable gate length. By utilizing optimum etching conditions described in the chapter 2. The head of the T-shaped gate was defined by a bi-layer resist system consisting of PMMA and copolymer (PMMA-MMA). The sensitivity of the PMMA to e-Beam was higher than the copolymer, so the developing time for PMMA and copolymer in the solution of MIBK (Methyl-iso-butylketon) and IPA (isopropyl alcohol) were different. This process was based on the differential developing rates of exposed copolymer and PMMA. Figure 3.4 shows the line dose dependence of the gate head of a dual-layer Copolymer/PMMA resist after development. Figure 3.5 represents the sidewall gate process. Figure 3.6 shows the associated SEM micrograph of the sidewall T-shaped gate process.

3.2.4 Gate recess

After patterning the T-shaped gate, the recess etching was performed using pH-adjusted solution of succinic (S.A.) and H_2O_2 mixture to selectively etch the heavily doped InGaAs cap layer over InAlAs schottky layer. The etching selectivity of InGaAs cap layer over InAlAs Schottky layer was over 100. The target current after the gate recess is a critical parameter affecting the HEMT performance. In order to get the desired recess depth, the recess process was controlled by monitoring the ungated $I_{ds.}$ After recess etching, Ti/Pt/Au gate metal was evaporated and lifted off.

Fig. 3.7 shows the SEM micrograph of the cross-section of the sidewall T-shaped gate structure before and after gate metal deposion.

3.2.5 Device passivation and contact via formation

FETs are very susceptible to the surface condition, especially in the gate region. As the device scales down, the gate length and spaces between source-to-drain and gate-to-drain become smaller. Under such conditions, the devices are very sensitive to the contaminations (such as chemicals, gases, and particles) and damages. The passivation layer protects the device from damage during process handling (such as “airbridge”) and wafer probing. The dielectric layer for device passivation is usually SiN_x.

The SiN_x film was grown by the PECVD system. The precursors were SiH_4/Ar, NH_3 and N_2, the deposition temperature was 250℃ while the RF power was 35 W. The thickness of the silicon nitride film was 1000Å and the reflection index was about 2.0, which was inspected by Ellipsometer. Then the contact openings of the devices were formed by photo lithography. The RIE was used to open the contact via hole region of the source and drain pads for interconnection. The plasma gases source to etch SiN_x were CF_4 and O_2.

3.2.6 Airbridge formation

In order to reduce the total device area, finger-type layout was adopted. As a result, airbridge process was necessary to contact the fingers. The use of airbridge had several advantages including lowest dielectric constant of air, low parasitic capacitance, and the ability to carry substantial currents. The airbridge process flow is shown in the Fig. 3.8. The first layer of photo-resist was opened at the regions of the source and drain pads. The thin seed-metal Ti/Au/Ti was deposited by e-gun evaporation system. Ti serves as the adhesion layer and Au serves as the seed layer and conductive layer for electroplating. The second layer of photo-resist was defined for the regions of the gold plated. Then, airbridge were formed after the remove of thin metal and photo-resists. The air-gap could be formed beneath the bridge, and all source pads could be connected by bridge pier. After airbridge formation, the RF characteristics of the devices were measured. The SEM micrograph of the air-bridge profile is given in Fig. 3.9.

3.3 DC Characteristics

3.3.1 I-V characteristics [3.3]

The band diagrams at three different positions along the channel are illustrated in Fig. 3.10 There is a potential drop in the direction parallel to the channel, causing q'_{CH} to be a function of position x. Therefore, the channel charge sheet density is expressed as:

$$q'_{CH} = -C'_{OX}[V_{GS} - V_T - V_{CS}(\chi)] \tag{3-1}$$

The channel current is proportional to the cross-section area of conduction, the charge density, the mobility, and the electric field. We can define that:

$$I_{CH}(\chi) = -WC'_{OX}\,\mu_n[V_{GS} - V_T - V_{CS}(\chi)]\frac{dV_{CS}(\chi)}{d\chi} \tag{3-2}$$

We note that q'_{CH} is a negative quantity in HEMT, since electrons accumulated in the channel are negative charges. In fact, if we choose $x = L$ at the drain, this constant channel current is equal to the negative of the drain current. Hence, we have $I_D = -I_{CH}$, we find:

$$\int_0^L I_D dx = -\int_{V_{CS}(o)}^{V_{CS}(L)} W\,C'_{OX}\,\mu_n[V_{GS} - V_T - V_{CS}(\chi)]\frac{dV_{CS}(\chi)}{d\chi} \tag{3-3}$$

In the following analysis, we consider the long-channel HEMTs whose channel mobility is assumed to be as a constant. The short-shannel HEMTs with velocity saturation will be analyzed:

$$V_{drift} = \mu_{n,0}|\varepsilon|/(1+\frac{|\varepsilon|}{\varepsilon_{sat}}) \qquad \text{if} \quad \varepsilon < \varepsilon_{sat}$$

$$= v_{sat} \qquad \text{if} \quad \varepsilon \geqq \varepsilon_{sat} \tag{3-4}$$

To carry out the integration in Eq. (3-3), we assume temporarily that

we are working in the linear region such that current saturation due to channel pinch off at the drain dose not occur. The *I-V* characteristics after pinch off will be dealt with shortly. In the linear operating region, the boundary conditions are $V_{CS}(L) = V_{DS}$ and $V_{CS}(0) = 0$. Hence, Eq. (3-3) leads to:

$$I_D = \frac{W_g C'_{OX} \mu_n}{L_g}[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}] \tag{3-5}$$

Eq. (3-5) is plotted schematically in Fig. 3.11, with I_D shown as a function of V_{DS}. The value of V_{DS} corresponding to the attainment of $I_{D,sat}$ is denoted as $V_{DS,sat}$, the saturation voltage. The saturation voltage can be obtained by taking the derivative of I_D will respect to V_{DS} and setting the result to zero. We find that:

$$V_{DS,sat} = V_{GS} - V_T \tag{3-6}$$

At this saturation voltage, q'_{CH} calculated from Eq. (3-1) is identically zero at the drain (pinch off). However, we realize that this conclusion originates from the fact that we are extending the validity of Eq. (3-1) all the way to where $q'_{CH}(L)$ is identically zero. Physically, the channel at the drain dose not pinch off completely. Instead, there is a finite thickness of accumulation of charges at which q'_{CH} $x=L$ is nonzero. The drift velocity is high, but nonetheless finite, so a constant current is maintained throughout the channel. Therefore, a complete model of the

drain current is given by:

$$I_D = \frac{W_g C'_{OX} \mu_n}{L_g}[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}] \qquad \text{for } V_{DS} < V_{DS,SAT}$$

$$= \frac{W_g C'_{OX} \mu_n}{L_g}[\frac{(V_{GS} - V_T)^2}{2}] \qquad \text{for } V_{DS} \geqq V_{DS,SAT} \qquad (3\text{-}7)$$

For HEMTs, it is convenient to define the saturation index (α) as:

$$\alpha = 1 - \frac{V_{DS}}{V_{DS,sat}} \qquad \text{for } V_{DS} < V_{DS,SAT}$$

$$= 0 \qquad \text{for } V_{DS} \geqq V_{DS,SAT} \qquad (3\text{-}8)$$

The drain current increases due to the perturbations in V_{GS} and V_{DS}. The mutual transconductance measures the amount of current increase due to the increment in the gate bias.

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS} = const.} \qquad (3\text{-}9)$$

We also can write:

$$g_m = \frac{W_g C'_{OX} \mu_n}{L_g}(V_{GS} - V_T) * (1 - \alpha) \qquad (3\text{-}10)$$

3.3.2 Transmission line model (TLM) [3.4]

The most widely used method for determining specific resistance is the method of Transmission Line Model (TLM). In this particular approach, a linear array of contacts is fabricated with various spacing between them as shown in Fig 3.12. The distances between TLM electrodes are 3 μm, 5 μm, 10 μm, 30 μm, and 36 μm, respectively in this study. The resistance between two adjacent electrodes can be plotted as a function of the space between electrodes. The plot is shown in the Fig. 3.13. Extrapolating the data to L=0, one can calculate a value for the term R_c (Ω-mm).

$$R = 2R_C + \frac{R_S L}{W} \tag{3-11}$$

R: measured resistance

R_c: contact resistance

R_s: sheet resistance of the channel region

W: electrodes width

L: space between electrodes

Another important parameter is the specific contact resistance ρ_c (Ω-cm^2), which is defined as

$$\rho_C = \frac{W^2 R^2}{R_S} \tag{3-12}$$

This specific contact resistance is a practical figure of merit for contact resistance. It includes a portion of the metal immediately above the metal-semiconductor interface, a part of the semiconductor below the interface, current crowding effects, spreading resistance under the contact, and any interfacial oxide that may present between the metal and the semiconductor.

3.3.3 Breakdown characteristics [3.5]

Breakdown mechanisms and models discussed in many articles. One of the models showing it is dominated by the thermionic filed emission (TFE) / tunneling current from the Schottky gate. This model predicts that the two-terminal breakdown voltage is lower at higher temperature because tunneling current increases with the temperature. Higher tunneling current occurs at higher temperature because carriers have higher energy to overcome the Schottky barrier. Other model suggests that impact-ionization determines the final two-terminal breakdown voltage, because the avalanche current decreases with increasing temperature. Lower avalanche current occurs at higher temperature because phonon vibrations as well as carrier-carrier scattering increase with increasing temperature. Either model is incomplete since coupling exists between TFE and impact ionization mechanisms. In addition, different devices may suffer from different breakdown mechanisms, depending on the details of the device design (insulator thickness, recess, channel composition, and so forth). In this study, the gate-to-drain breakdown voltage BV_{gd} is defined as the gate-to-drain voltage when the

gate current is 1mA/mm.

3.4 RF Characteristics& Measurements

3.4.1 Scattering parameters [3.6]

Scattering parameters, generally referred to as *S*-parameters, are fundamental to microwave measurement. This section discusses *S*-parameters and the motivation for their use. For a device such as field-effect transistor with the input and output terminals can be treated as a two-port network as shown in Fig. 3.14.V_1 and I_1 are the voltage and current at the input, and V_2 and I_2 are the voltage and current at the output. Major characteristics, such as gain, return loss, and impedance matching can be calculated from known relationship among the input and output signals. The impedance parameters (*z*-parameters), conductance parameters (*y*-parameters) and hybrid parameters (*h*-parameters) are used to characteristic the devices because the parameter can be measured by open or short termination. The *z*-, *y*- and *h*-parameters can therefore be stated by the following equations:

z-parameters: $\begin{bmatrix} V1 \\ V2 \end{bmatrix} = \begin{bmatrix} z11 & z12 \\ z21 & z22 \end{bmatrix} * \begin{bmatrix} i1 \\ i2 \end{bmatrix}$

y-parameters: $\begin{bmatrix} i1 \\ i2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} * \begin{bmatrix} V1 \\ V2 \end{bmatrix}$

h-parameters: $\begin{bmatrix} V1 \\ i2 \end{bmatrix} = \begin{bmatrix} h11 & h12 \\ h21 & h22 \end{bmatrix} * \begin{bmatrix} i1 \\ V2 \end{bmatrix}$

When the frequency is up to several GHz, the *z*-, *y*-, *h*- parameters can not be directly obtained by the open or short circuit because of the reflected wave from the open or short terminations. The open or short terminations will induce the network oscillation. Therefore the scattering parameters are used to characterize the performance of a device. Figure 3.15 shows the two-ports 1 and 2. The relation of the microwave signals and *s*-parameters can be described as

s-parameters: $\begin{bmatrix} b1 \\ b2 \end{bmatrix} = \begin{bmatrix} s11 & s12 \\ s21 & s22 \end{bmatrix} * \begin{bmatrix} a1 \\ a2 \end{bmatrix}$

a_1: the electric field of the microwave signal entering the component input

b_1: the electric field of the microwave signal leaving the component input

a_2: the electric field of the microwave signal entering the component output

b_2: the electric field of the microwave signal leaving the component output

By the definition, then,

$$s11 = \left.\frac{b1}{a1}\right|_{a2=0}$$

$$s21 = \left.\frac{b2}{a1}\right|_{a2=0}$$

$$s12 = \left.\frac{b1}{a2}\right|_{a1=0}$$

$$s22 = \left.\frac{b2}{a2}\right|_{a1=0}$$

Therefore, s_{11} is the electric field leaving the input divided by the electric field entering the input, under the condition that no signal enters the output.Tthe measurement includes instruments for the DC and RF measurement. Where a_1 and b_1 are electric fields, their ratio is a reflection coefficient. Similarly, s_{21} is the electric field leaving the output divided by the electric field entering the input, when no signal enters the output. Therefore, s_{21} is a transmission coefficient and is related to the insertion loss or the gain of the device. Similarly, s_{21} is a transmission coefficient related to the isolation of the device and specifies how much power leaks back through the device in the wrong direction. s_{22} is similar to s_{11}, but looks in the other direction into the device. The *s*-parameters have both the amplitude and phase.

3.4.2 Current gain cutoff frequency f_T

Traditionally, transistors are characterized using figures of merit such as the unity current-gain cut-off frequency (f_T).

Consider a transistor characterized by the following small-signal *y*-parameters

$$i_1 = y_{11}(\omega)V_1 + y_{21}(\omega)V_2$$

$$i_2 = y_{21}(\omega)V_1 + y_{22}(\omega)V_2$$

The currents and voltages are defined in Fig. 3.15. For example, we use the *y*-parameters of a FET in the common source configuration in Fig. 3.16.

$$i_g = y_{gg}(\omega)V_{gs} + y_{gd}(\omega)V_{ds}$$

$$i_d = y_{ds}(\omega)V_{gs} + y_{dd}(\omega)V_{ds}$$

The unity short-circuit current-gain cut-off frequency is defined as the frequency at which the short-circuit current gain is unity:

$$h_{21}(\omega) = \left|\frac{y_{21}(\omega_T)}{y_{11}(\omega_T)}\right| = 1$$

Since the HEMT is the common source configuration, the maximum short-circuit current gain can be approximated by

$$\left|\frac{y_{21}(\omega_T)}{y_{11}(\omega_T)}\right| = \left|\frac{y_{ds}(\omega_T)}{y_{gg}(\omega_T)}\right| \approx \frac{g_m}{\omega C_g W_g L_g}$$

Where g_m is the transconductance. Notice the $1/\omega$ decrease with frequency (20 dB per decade) using $20\log(y_{21}/y_{11})$ of the short-circuit

gain.

The intrinsic *S* parameters are used to determine the unity current-gain cut-off frequency (f_T). It can be determined by extrapolation of the short-circuit current gain h_{21} = 0dB. h_{21} can be defined as

$$h_{21} = \frac{2 s_{21}}{(1 - s_{11})(1 + s_{22}) + s_{12} s_{21}}$$

3.4.3 Maximum frequency of oscillation f_{max}

The microwave performance of a transistor is usually characterized by the maximum stable power gain as a function of frequency. The maximum power gain is obtained by simultaneously matching the input and output to obtain a conjugate match. Conjugate match means that the source impedance Z_S and the load impedance Z_L satisfy simultaneously:

$Z_S = Z^*_{IN}$

$Z_L = Z^*_{OUT}$

Where Z_{IN} is the input impedance of the two-port network measured at port 1 with the load impedance Z_L connected at port 2 and where Z_{OUT} is the output impedance of the two-port network measured at port 2 with the source impedance Z_S connected at port 1. The maximum power stable gain (G_{max}) consisting of the maximum available gain (MAG), and the maximum stable gain (MSG) were derived from the *S*-parameter data by

the equation:

$$G_{MAX}=\left|\frac{S_{21}}{S_{12}}\right|K-\sqrt{(K^2-1)},$$

where K is the Rollett stability factor

$$K=\frac{1-|S_{11}|^2-|S_{22}|^2+|D|^2}{2|S_{12}S_{21}|}$$

$$D=S_{11}S_{22}-S_{12}S_{21}$$

The MAG is the highest power gain of the two-port network with the impedance-matched input and output. The MAG of a transistor can only be obtained when the transistor is unconditionally stable, *i.e.* K>1. The MSG is the highest power gain of a two-port network with the resistive loaded in both input and output ports. The MSG can be obtained if the transistor where potentially unstable according to:

$$MSG=MAG|_{K=1}=\left|\frac{S_{21}}{S_{12}}\right|$$

The device maximum power gain cut-off frequency can then be defined as the frequency at G_{max} = 0 dB.

The comparison of the high-frequency performance of two-port devices is usually done using the unilateral power gain U derived by

Mason [3.7]:

$$U = \frac{\frac{1}{2}\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{K\left|\frac{S_{21}}{S_{12}}\right| - Re\left(\frac{S_{21}}{S_{12}}\right)}$$

U is the maximum available power gain (MAG is introduced in the previous section) of a device once it has been unilateralized ($y_{12} = 0$) using lossless feedback techniques.

The maximum frequency of oscillation f_{max} is then defined as the frequency at which U is unity. f_{max} is often referred to as the frequency at which a three-port device switches form active to passive. U can then be written

$$U(\omega) = \left(\frac{\omega_{max}}{\omega}\right)^2$$

The unilateral power gain will then decrease at a rate of 20 dB per decade (using 10logU) like the short-circuit current gain.

3.4.5 Noise figure [3.8]

Noise is related to the device channel and capacitive coupling between the channel and the gate. The gate noise is represented by a

gate-current noise generator i_{ng}^2 and is caused by charge fluctuation in the channel, which in turn induces the fluctuation of compensating charge on the gate electrode. The gate-noise is proportional to f^2 in HEMTs.

The channel noise is represented by a drain-current noise generator i_{nd}^2 and is caused by various physical mechanisms driven by the electric field in the channel. In the linear region of the device channel, the channel noise is caused by thermal noise (Johnson noise). A thermal noise voltage caused in the channel leads to a modulation of the channel resistance and causes a drain voltage fluctuation at the channel end (drain). The corresponding drain noise current is inversely proportional to $g_m I_{DS}$. In the high-field region, hot electron scattering, intervalley scattering, and high diffusion noise contribute to the channel noise.

Another noise source is gate leakage. A new model that takes this effect into account by an additional parallel resistor to the gate capacitance and the resistor R_i has been proven to a good correlation between predicted and measured minimum noise figures even at low frequencies. The negative influence of the gate leakage on the noise figure vanishes at higher frequencies.

Noise figure reflects the noise added to the signal by the imperfect amplifier, and is defined as the signal-to-noise ratio (S/N) of the input signal divided by the signal-to-noise ratio of the output signal,

$$F = (S_i/N_i)/(S_0/F_0)$$

It is usually expressed in dB:

$$NF = 10\log F$$

We shall use *F* to designate absolute noise figure and NF to designate figure expressed in dB. The noise performance of a FET may be quantified by the noise figure, NF, which is a function of frequency, FET bias voltages, and impedance matching. Another noise figure of FETs structure is shown as the following equation.

$$NF = 1 + \sqrt{2}\frac{f}{f_t}\sqrt{g_m(R_S + Rg)},\ f_t = \frac{g_m}{2\pi C_{gs}}$$

In general, high source-drain current contributes to noise by electron scattering, and this noise is reduced as the current is reduced. However, reducing the current too close to pinch-off reduces the transconductance, which causes increased noise figure because of decrease gain. There will exist an optimum gate bias that presents the best compromise.

3.4.6 RF measurement calibration [3.6]

Before the on-wafer measurement, the measuring system must be calibrated first to eliminate the extrinsic parasitic components of the cables, adaptors, probes and so on. The GSG (ground-signal-ground) probe tips are used in this study and shown in Fig. 3.17. The planar

calibration was first carried out to make the tips are at the same height to prevent the nonuniform contacts. After the planar calibration of the probe tips, the calibrations for the measurement were made. Figure 3.18 shows different calibration substrates (impedance Standard Substrate; ISS) for the open, short, load, through, and transmission calibrations. There are many calibration methods for the microwave measurement. In this study, the Short-Open-Load-Thru (through) (SOLT) calibration was dopted. Figure 3.19shows the calibration pads for the short, through and load, respectively. Flow chart of are the steps for the two-port SOLT calibration is illustrated in Fig. 3.20.