which is different for different values of R_T. In making measurements with large values of R_T it was necessary to insure that C_B, C_C, and other stray capacitances did not significantly load the test transistor base circuit at the modulation frequency. Also, it was necessary to locate the RFC's and C_B carefully to insure that microwave power did not enter the response measurement instrumentation. It was also found that in some RF generation equipment, the modulation scheme may introduce a video component on the RF line which, if not properly grounded through a dc path in the stub tuners, and otherwise decoupled through C_C, could be mistaken for test device response.

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Integrated Λ-Type Differential Negative Resistance MOSFET Device

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***Abstract*—A new type of the NELS (*n*-channel *e*nhancement mode with *l*oad operated at *s*aturation)-connected Λ-type differential negative resistance MOSFET, using the merged integrated circuit of a NELS inverter and an n-channel enhancement MOS driver, is studied both experimentally and theoretically. The principal operation of the lambda MOSFET device is characterized by the simple circuit model and device physics. The important device properties, such as the peak voltage, the peak current, the valley voltage, and the negative resistance, are derived in terms of the known device parameters. Comparisons between characteristics of the fabricated device and the theoretical model are made, which show the theoretical analyses are in good agreement with the observed device characteristics.**

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List of Symbols

C_0	Gate oxide capacitance per unit area.
G_0	Drain-to-source conductance with zero drain voltage.
G_{01}	G_0 of transistor $Q1$ for the NELS-connected structure.
G_{02}	G_0 of transistor $Q2$ for the NELS-connected structure.
G_{03}	G_0 of transistor $Q3$ for the NELS-connected structure.
G_r	Ratio of G_{02} and G_{01}.
I_{DS}	Drain–source current.
I_p	Peak current.
I_v	Valley current.
K	Modifying substrate factor.
L	Channel length.
N_A	Doping concentration of p-type substrate.
Q_{ss}	Surface state charge density.
Q_B	Surface depletion layer charge density.

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q	Electronic charge.
R_N	Negative differential resistance.
V_{DS}	Drain-source bias voltage.
V_{FB}	Flat-band voltage of MOS capacitor.
V_{GS}	Gate-source bias voltage.
V_{GG}	Applied gate voltage for the NELS-connected structure.
V_p	Peak voltage.
V_T	Threshold voltage.
V_V	Valley voltage.
Z	Channel width.
ϕ_{fp}	The potential difference between Fermi-potential and the intrinsic potential of p-type substrates at the flat-band condition.
ϕ_{MS}	Metal-semiconductor work function difference.
ϵ_s	Dielectric permittivity of silicon substrate.
μ_n	Surface mobility of the electron.
μ_{FE}	Field effect mobility.

I. Introduction

Recently, several types of voltage-controlled negative differential resistance devices with the integrated transistor structure have been reported [1]-[6]. Among these, Takagi and Kano [1] reported a structure of two complementary junction field effect transistors with two terminals, which involved rather complicated integrated circuit fabrication technology. Other structures [2]-[6] were reported which had three terminals, but were shown to have some disadvantages; namely, the combination of JFET and the bipolar transistor with a different carrier type [5], [6], the difficulty in controlling the negative resistance region [2], [4], [5], and a rather large valley current [3], [5].

A new type of voltage-controlled negative resistance device-lambda MOSFET, which has three terminals, has been developed [7]. It has been shown that the lambda MOSFET not only involves very simple existing MOS integrated circuit fabrication technology but also exhibits controllable and useful characteristics. An analytical model of the NELS-connected Λ-type differential negative resistance MOSFET will be presented in Section II where the important device properties, such as the peak voltage, the valley voltage, and negative resistance, are derived in terms of the known device parameters. Comparisons between the characteristics of the fabricated devices and the theoretical model will be given in Section III where the theoretical analysis is shown to be in good agreement with the observed device characteristics. In the last section, conclusions will be made.

II. Device Operation and Sectional Models

The basic circuit representation of the NELS-connected Λ-type MOSFET is shown in Fig. 1, which consists of three n-channel enhancement mode MOSFET's with a NELS-MOS inverter and an NMOS driver. Transistor $Q1$ acts as a load resistor with the gate shorted to the drain, which is used to modulate the input gate voltage of transistor $Q3$, and transistor $Q2$ behaves as an active switch with the gate electrode connected to the drain electrode of the driver transistor $Q3$. The substrate of the load transistor $Q1$, and the substrate and the source of transistors $Q2$ and $Q3$, are connected together.

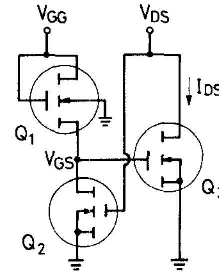

Fig. 1. A NELS-connected Λ-type negative resistance structure.

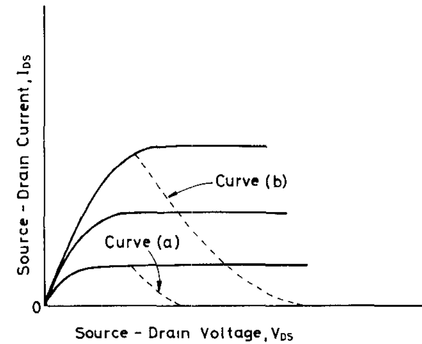

Fig. 2. Two possible cases with the negative differential resistance effect for a MOSFET driver.

There are two possible modes of operation of transistor $Q3$ which demonstrate differential negative resistance, as shown in Fig. 2. Curve (*a*) illustrates the case in which the peak current occurs in the saturation region of $Q3$ and curve (*b*) illustrates the case in which the peak current occurs in the linear region.

Under the conventional assumptions of gradual channel approximation being valid, channel-length modulation effect being negligible, and electron mobility being constant, the current equation for an n-channel MOSFET operating in the linear region can be written as

$$I_{DS} = G_0\left\{\left[V_{GS} - V_{FB} - 2\phi_{fp} - \frac{V_{DS}}{2}\right] V_{DS} - \frac{2}{3}K[(V_{DS} + 2\phi_{fp})^{3/2} - (2\phi_{fp})^{3/2}]\right\} \quad (1)$$

where

$$G_0 = \frac{\mu_n Z C_0}{L}, \quad K = \frac{(2\epsilon_s q N_A)^{1/2}}{C_0}.$$

In order to obtain analytical expressions, the back gate bias effect is assumed to be negligible. This assumption leads to simplified expressions as follows:

$$I_{DS} = G_0\left\{[V_{GS} - V_T]\, V_{DS} - \frac{V_{DS}^2}{2}\right\}, \quad \text{for the linear region} \quad (2)$$

$$I_{DS} = \frac{G_0}{2}[V_{GS} - V_T]^2, \quad \text{for the saturation region} \quad (3)$$

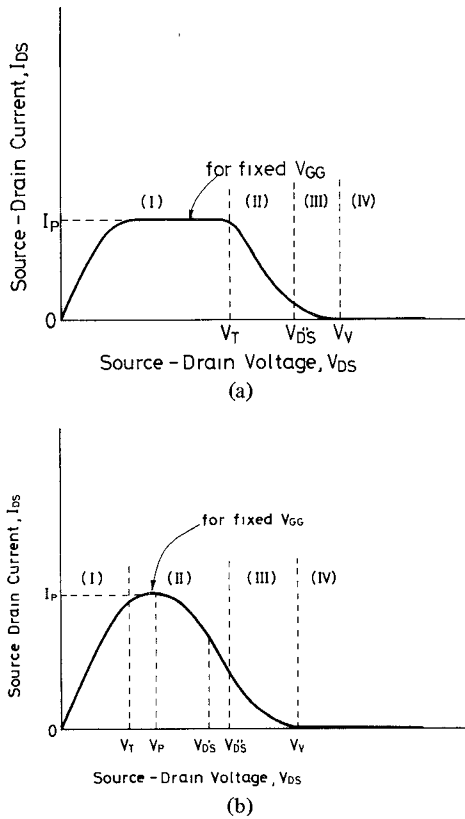

Fig. 3. Three section model for the analysis of a Λ-type negative resistance structure with V_P. (a) In the saturation region. (b) In the linear region.

where threshold voltage V_T and the drain-to-source conductance at zero drain voltage G_0 are two important parameters in the analysis. Conventionally, the threshold voltage of the n-channel MOSFET is defined as

$$V_T = \phi_{MS} - \frac{Q_{ss}}{C_0} + 2\phi_{fp} - \frac{Q_B}{C_0}$$

and the ratio of the drain-to-source conductance at zero drain voltage for $Q2$ to that of $Q1$ is expressed as

$$G_r = G_{02}/G_{01}. \tag{4}$$

For simplifying the analysis, the output characteristic of the NELS-connected MOSFET device is divided into four regions as shown in Fig. 3(a) and (b), which are analyzed separately as follows.

Region I

In this region, transistor $Q2$ is off and transistor $Q1$ is kept in saturation. In order to sustain sufficient voltage across the drain to source of transistor $Q1$ and maintain the channel nearly on, the gate-to-source voltage V_{GS} of Fig. 1 can be expressed as

$$V_{GS} = V_{GG} - V_T - K[\sqrt{(2\phi_{fp} + V_{GS}} - \sqrt{2\phi_{fp}}] \qquad 0 \leqslant V_{DS} < V_T \tag{5}$$

where the third term on the right-hand side is the threshold voltage change due to the substrate bias effect of transistor $Q1$.

Solving (5) for V_{GS} gives

$$V_{GS} = \left(V_{GG} - V_T + K\sqrt{2\phi_{fp}} + \frac{K^2}{2}\right) + K\left[V_{GG} - V_T + K\sqrt{2\phi_{fp}} + \frac{K^2}{4} + 2\phi_{fp}\right]^{1/2}. \tag{6}$$

Equation (6) shows that V_{GS} is a function of V_{GG} and is independent of V_{DS}. The output current I_{DS} depends upon whether transistor $Q3$ is operated in the linear region or in the saturation region. These conditions are classified as follows.

For V_{DS} of $Q3$ in the range $V_{DS} \geqslant V_{GS} - V_T$, $Q3$ is in saturation, and the drain current is given by

$$I_{DS} = \frac{G_{03}}{2}(V_{GS} - V_T)^2 \tag{7}$$

where V_{GS} is given by (6).

For V_{DS} of $Q3$ in the range $V_{DS} < V_{GS} - V_T$, $Q3$ is in the linear region, and the drain current is given by

$$I_{DS} = G_{03}[(V_{GS} - V_T)V_{DS} - \tfrac{1}{2}V_{DS}^2]. \tag{8}$$

Two different cases can now occur.

Case I-a: $Q3$ goes into saturation while in Region I [Fig. 3(a)].

Case I-b: $Q3$ remains in the linear region throughout Region I [Fig. 3(b)].

Region II

In this region, V_{DS} exceeds the threshold voltage of $Q2$, and the drain voltage is such that transistor $Q2$ remains in saturation. Since transistor $Q1$ is always kept in saturation, we have

$$V_{DS} - V_T = \frac{1}{\sqrt{G_r}}[(V_{GG} - V_T) - K(\sqrt{2\phi_{fp} + V_{GS}} - \sqrt{2\phi_{fp}}) - V_{GS}] \quad \text{for} \quad V_T \leqslant V_{DS} \leqslant V_{GS} + V_T. \tag{9}$$

Operation in this region may also be classified into two cases.

Case II-a: Transistor $Q3$ remains in saturation throughout Region II [Fig. 3(a)] when transistor $Q3$ is operated in the saturation region; (7) gives the current where V_{GS} is obtained from (9).

Case II-b: $Q3$ starts out in Region II in the linear region, and goes into saturation at V_{DS}' [Fig. 3(b)].

When transistor $Q3$ is in the linear region, (8) applies. This case always occurs for large values of V_{GG}.

The breakpoint V_{DS}' between Case II-a and Case II-b as shown in Fig. 3(b) is derived by substituting $V_{GS} = V_{DS} + V_T$ into (9); i.e.,

$$V_{DS}' = [2(G_r^{1/2} + 1)(V_{GG} + K\sqrt{2\phi_{fp}} - 2V_T) + K^2]/2(G_r^{1/2} + 1)^2 + \{[4K^2(G_r^{1/2} + 1) \cdot (V_{GG} + K\sqrt{2\phi_{fp}} - 2V_T) + K^4 - 4K^2(G_r^{1/2} + 1) \times (2\phi_{fp} + V_T)]^{1/2}\}/2(G_r^{1/2} + 1)^2. \tag{10}$$

TABLE I
THE OPERATING POINTS OF EACH TRANSISTOR FOR A NELS LAMBDA MOSFET

	Q_1	Q_2	Q_3
Region I	SAT	OFF	LIN → SAT (Case Ia)
			LIN (Case Ib)
Region II	SAT	SAT	SAT (Case IIa)
			LIN → SAT (Case IIb)
Region III	SAT	LIN	SAT
Region IV	SAT	LIN	OFF

Region III

In this region, $Q2$ is in the linear region. From Fig. 3(a) and (b), the breakpoint V''_{DS} between Region II and Region III can be found by substituting $V_{GS} = V_{DS} - V_T$ into (9), to obtain

$$V''_{DS} = [2(G_r^{1/2}+1)(V_{GG}+K\sqrt{2\phi_{fp}})+K^2]/2(G_r^{1/2}+1)^2 + \{[4K^2(G_r^{1/2}+1)(V_{GG}+K\sqrt{2\phi_{fp}})K^4 - 4K^2(G_r^{1/2}+1) \times (2\phi_{fp} - V_T)]^{1/2}\}/2(G_r^{1/2}+1)^2. \quad (11)$$

From the equality between the drain currents of $Q1$ and $Q2$, a transfer relation can be written as

$$V_{DS} - V_T = \tfrac{1}{2}\,\{V_{GS} + [(V_{GG} - V_T) - V_{GS} - K\sqrt{2\phi_{fp} + V_{GS}} - \sqrt{2\phi_{fp}}]^2/(G_r V_{GS})\}$$
$$\text{for} \quad V_{DS} \geq V_{GS} + V_T. \quad (12)$$

Since transistor $Q3$ is operated in saturation region; i.e., for $V_T \leq V_{GS} \leq V_{DS} + V_T$, we have

$$I_{DS} = \frac{G_{03}}{2}\,[V_{GS} - V_T]^2 \quad (13)$$

where V_{GS} can be found from (12).

Region IV

In this case, transistor $Q3$ is off for $0 \leq V_{GS} < V_T$, so we obtain

$$I_{DS} = 0. \quad (14)$$

In order to clarify these four regions the operating points of each transistor are shown in Table I.

III. THE DETERMINATION OF DEVICE DC PARAMETERS

In order to accurately determine the device dc parameters, the mobility variation with respect to the gate voltage should be considered. In general, the drain-to-source conductance at zero drain voltage G_{03} can be expressed by

$$G_{03} = A(V_{GS} - V_T)^{-r} \quad (15)$$

where A and r are two positive real constants.

From the considerations in Section II, the peak voltage and the peak current for the case shown in Fig. 3(a) can be expressed by

$$V_p = V_T \quad (16)$$

$$I_p = \frac{A}{2}(V_{GS} - V_T)^{2-r} \quad (17)$$

where V_{GS} is expressed by (6).

Unfortunately, it is difficult to find the peak voltage and the peak current for the case shown in Fig. 3(b) in the analytical form. An alternative method is proposed to calculate V_p and I_p by solving the following simultaneous equations, which are

$$V_{DS} = V_T + \frac{1}{G_r^{1/2}}\,[(V_{GG} - V_T) - K(\sqrt{2\phi_{fp} + V_{GS}} - \sqrt{2\phi_{fp}}) - V_{GS}]$$
$$\text{for} \quad V_T \leq V_{DS} \leq V_{GS} + V_T \quad (18)$$

$$I_{DS} = A(V_{GS} - V_T)^{1-r} V_{DS} - \frac{A}{2}(V_{GS} - V_T)^{-r} V_{DS}^2$$
$$\text{for} \quad V_{DS} + V_T \leq V_{GS}. \quad (19)$$

The valley voltage V_v of the output characteristic is found at the time when transistor $Q3$ is off. This can be obtained by substituting $V_{GS} = V_T$ into (12); i.e.,

$$V_v = \frac{3}{2}\,V_T + \frac{[(V_{GG} - 2V_T) - K(\sqrt{2\phi_{fp} + V_T} - \sqrt{2\phi_{fp}})]^2}{2G_r V_T}. \quad (20)$$

Theoretically, the valley current is assumed to be zero, but the thermal leakage current cannot be neglected for MOSFET; thus, we obtain

$$I_V = I_{DSS} \quad \text{(leakage)}. \quad (21)$$

In general, the typical value of the leakage current for MOSFET is about several tenths of a nanoampere.

The value of the negative differential resistance is defined as

$$R_N = \left.\frac{\partial V_{DS}}{\partial I_{DS}}\right|_{V_{GG} = \text{constant}}. \quad (22)$$

For Region II, the calculation of negative resistance must be classified into two cases which are cited in Fig. 3(a) and (b). For the case of Fig. 3(a), we have

$$R_N = \left.\frac{\partial V_{DS}}{\partial I_{DS}}\right|_{V_{GG} = \text{constant}} = \left.\left(\frac{\partial V_{DS}}{\partial V_{GS}}\right)\left(\frac{\partial V_{GS}}{\partial I_{DS}}\right)\right|_{V_{GG} = \text{constant}}$$
$$= \frac{-[K(2\phi_{fp} + V_{GS})^{-1/2} + 2]}{AG_r^{1/2}(2 - r)(V_{GS} - V_T)^{1-r}}$$
$$\text{for} \quad V_T < V_{DS} \leq V''_{DS} \quad (23)$$

where V''_{DS} is the breakpoint of Regions II and III, as shown in (11), and V_{GS} can be found from (9).

From Fig. 3(b), we also calculate the negative resistance in the range $V_p < V_{\text{DS}} \leqslant V'_{\text{DS}}$, where V_p is the peak voltage obtained from the simultaneous solution of (18) and (19); thus, we have

$$\begin{aligned} R_N = \{&-[K(2\phi_{\text{fp}} + V_{\text{GS}})^{-1/2} + 2]\}/\{-A(V_{\text{GS}} - V_T)^{1-r} \\ &\times \{[K(2\phi_{\text{fp}} + V_{\text{GS}})^{-1/2} + 2] \\ &+ 2A(1-r)\, G_r^{1/2}(V_{\text{GS}} - V_T)^{-r} f(V_{\text{GS}}) \\ &+ A(V_{\text{GS}} - V_T)^{-r}[K(2\phi_{\text{fp}} + V_{\text{GS}})^{-1/2} + 2]\, f(V_{\text{GS}}) \\ &+ rAG_r^{1/2}(V_{\text{GS}} - V_T)^{1-r} f^2(V_{\text{GS}})\} \end{aligned} \tag{24}$$

where

$$f(V_{\text{GS}}) = V_T + \frac{1}{G_r^{1/2}} \cdot [(V_{GG} - V_T) - K(\sqrt{2\phi_{\text{fp}} + V_{\text{GS}}} - \sqrt{2\phi_{\text{fp}}}) - V_{\text{GS}}]$$

and V_{GS} can be calculated from (9).

For Region III, by virtue of (12), the negative resistance is

$$\begin{aligned} R_N = \{&-[K(2\phi_{\text{fp}} + V_{\text{GS}})^{-1/2} + 2]\; V_{\text{GS}}\, g(V_{\text{GS}}) \\ &- g^2(V_{\text{GS}}) + G_r V_{\text{GS}}^2\}/[(2-r)AG_r(V_{\text{GS}} - V_T)^{3-r}] \\ &\text{for} \quad V''_{\text{DS}} \leqslant V_{\text{DS}} < V_v \end{aligned} \tag{25}$$

where

$$g(V_{\text{GS}}) = [(V_{GG} - V_T) - K(\sqrt{2\phi_{\text{fp}} + V_{\text{GS}}} - \sqrt{2\phi_{\text{fp}}}) - V_{\text{GS}}]$$

and V_v is the valley voltage expressed in (20), and V_{GS} can be calculated from (12).

IV. Experimental Results and Theoretical Comparisons

From Fig. 3 and the calculated results of Section III, transistors $Q1$ and $Q2$ play an important role in the control of the negative resistance range. For the purpose of high current operation, the layout dimension of transistor $Q3$ is the main factor. Moreover, the inversion layer effective mobility and substrate doping concentration should be responsible for the characteristic of the device.

Generally, the testing device used for the analysis is designed with $G_r \neq 1$. The layout parameters of the testing device are shown in Table II, where the geometric and effective dimensions are listed. The metallization pattern of the fabrication mask of the integrated device is shown in Fig. 4. The typical output characteristic of the fabricated Al-gate Λ-MOS device is shown in Fig. 5. The measured threshold voltage of the testing n-channel MOS is 0.9 V at $I_{\text{DS}} = 1\ \mu\text{A}$. From this, the fixed surface state charge density is estimated to be about $2 \times 10^{11}/\text{cm}^2$, which is consistent with the standard process of our laboratories.

The field effect mobility μ_{FE} is also measured from the testing pattern. It is found that the effective mobility can be expressed by $\mu_{\text{FE}} = 352.2(V_G - V_T)^{-0.45}$ for $V_{\text{GS}} - V_T \geqslant 0.5$ V and $564.2(V_{\text{GS}} - V_T)^{0.475}$ for $V_G - V_T < 0.5$ V, which will give $r = 0.45$, $A = 352.2$ for $V_{\text{GS}} - V_T \geqslant 0.5$ V, and $r = -0.475$, $A = 564.2$ for $V_G - V_T < 0.5$ V. Some physical constants used are listed in Table III.

TABLE II
Layout Parameters of the Testing Devices

parameters \ transistors	Q1	Q2	Q3
Geometrical Channel width (μm)	20	75	200
Geometrical Channel length (μm)	75	15	15
Effective Channel width (μm)	20	75	200
Effective Channel length (μm)	69.6	9.6	9.6

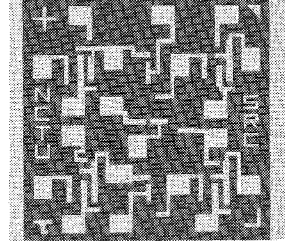

Fig. 4. Metallization pattern of the NELS-connected Λ-type negative resistance MOS device.

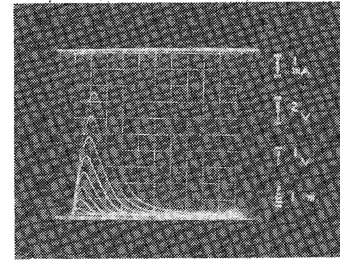

Fig. 5. Output characteristic of the fabricated device.

TABLE III
Some Physical Constants and Parameters Used for the Calculation of the Output Characteristic

N_A (cm^{-3})	$\approx 5\times10^{16}$	K	2.299
m	0.4	G_r	27.18
N_{AS} (cm^{-3})	$\approx 2\times10^{16}$	ε_o (F/cm)	8.854×10^{-14}
ϕ_{fp} (volt)	0.365	ε_{ox}	4
t_{ox} (A°)	1000	ε_s	11.7

The calculated and the measured output characteristics for three different gate voltage V_{GG} are shown in Fig. 6. It is evident that more than 30 percent discrepancy appears in the negative resistance region. Although the boron surface segregation effect that comes from the impurity redistribution during the thermal growth of SiO_2 is taken into consideration with segregation coefficient of $m = 0.4$, the slight discrepancy is still inevitable. The main reasons are due to assumptions of constant effective mobility in handling the current equation of the NELS inverter and the constant surface depletion charge density Q_B in the output current calculation.

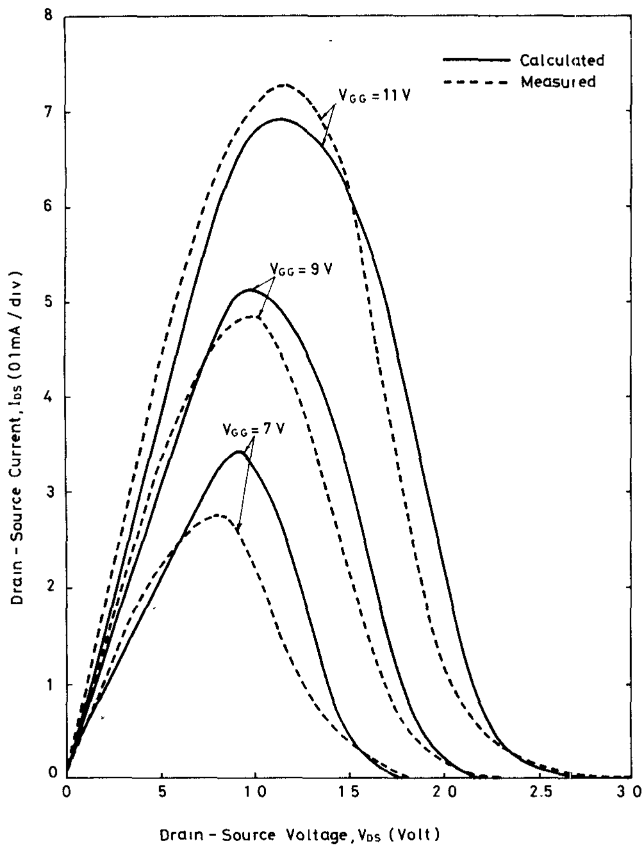

Fig. 6. Comparisons of theoretical and experimental output characteristics.

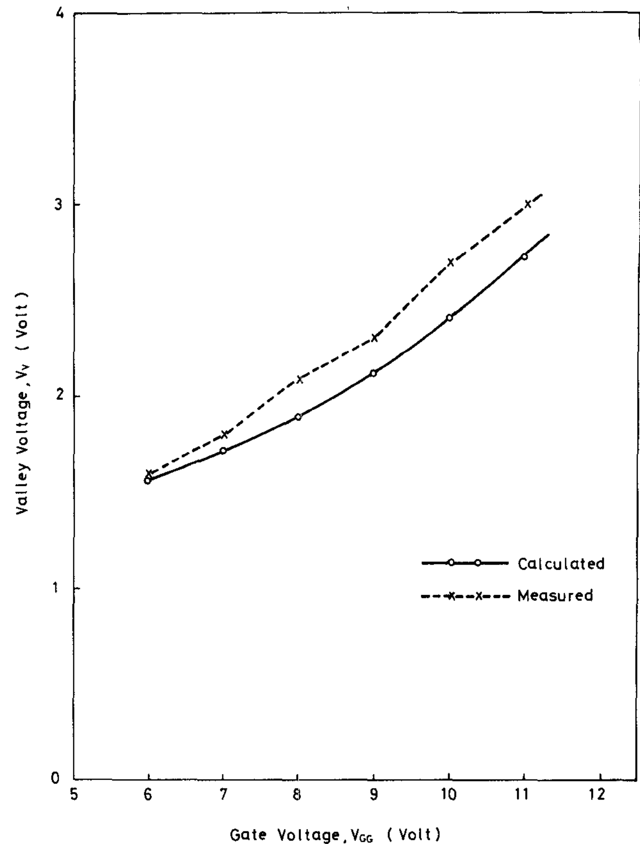

Fig. 8. Comparisons of theoretical and experimental valley voltage for different applied gate voltages V_{GG}.

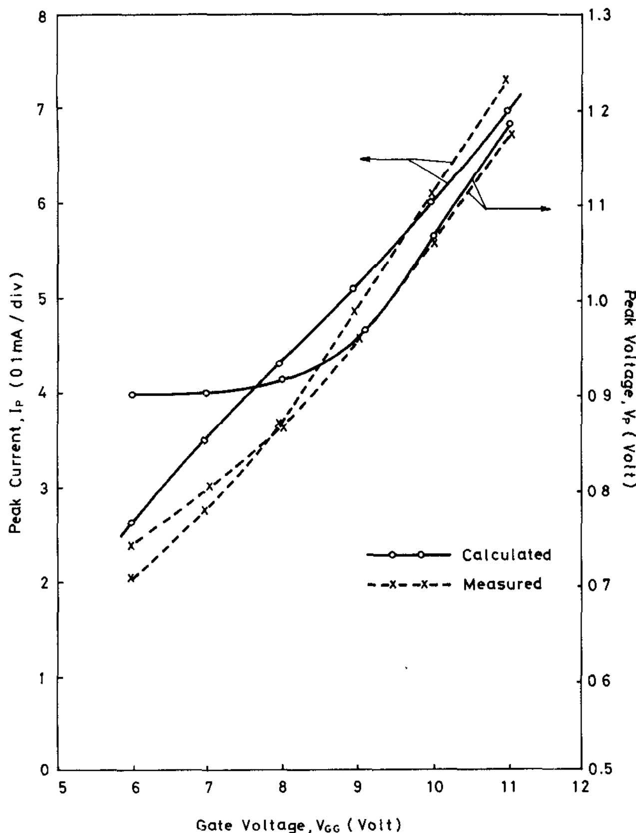

Fig. 7. Comparisons of theoretical and experimental peak voltage and peak current for different applied gate voltages V_{GG}.

From Fig. 7 it is found that there exists a good agreement between theoretical calculations and experimental results for the estimation of peak voltage and peak current at higher V_{GG}. The agreement becomes poor at lower V_{GG}, which is mainly attributed to the ambiguous definition of the threshold voltage and the effect of subthreshold leakage phenomena. The calculated and the measured valley voltages are shown in Fig. 8, where a good agreement is obtained under the assumption of valley current $I_V = 1\ \mu A$.

Comparisons of the calculated and experimental negative differential resistance are shown in Fig. 9 for three different gate voltages. A discrepancy of less than 50 percent is observed over the 0.5 V negative resistance range. All the negative resistance values, which are determined from (23) and (24) in Section III, are related to V_{GS} = 3.5 V, 3.25 V, 3.0 V, 2.75 V, 2.5 V, and 2.0 V. The corresponding drain-to-source voltage V_{DS} for each V_{GS} are cited on the abscissae of the figure.

Fig. 10 shows the peak voltage variations in the temperature range from -55 to 125°C. A theoretical coefficient of the threshold voltage variation with the temperature [8]; i.e., $dV_T/dT \approx 3.08 \times 10^{-3}$ V/°C is also given in the figure for comparison. The agreement between theory and the experimental result provides the fact that the peak voltage strongly depends on the threshold voltage of the device.

The peak current variations, in the temperature range from -55 to 125°C, are shown in Fig. 11, where the reciprocal temperature scale is used. The mobility variation with

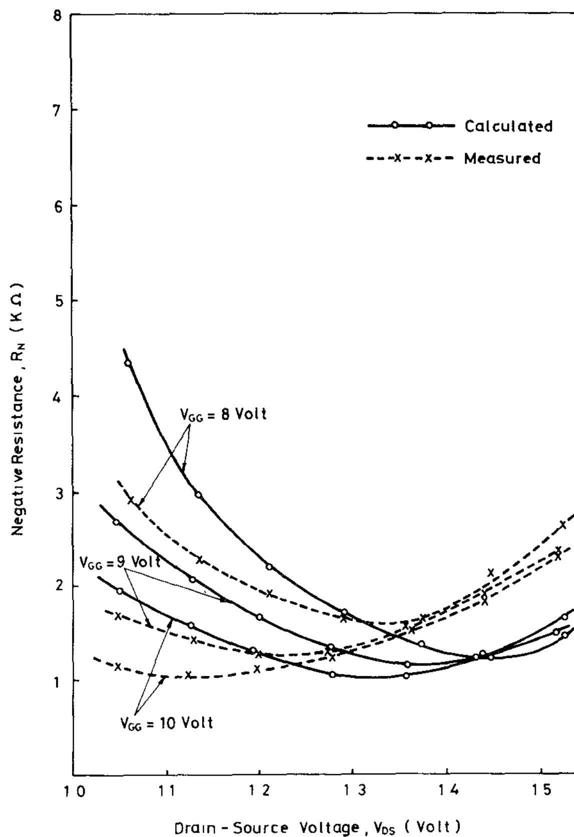

Fig. 9. Comparisons of theoretical and experimental negative resistance for V_{GG} = 8 V, 9 V, and 10 V.

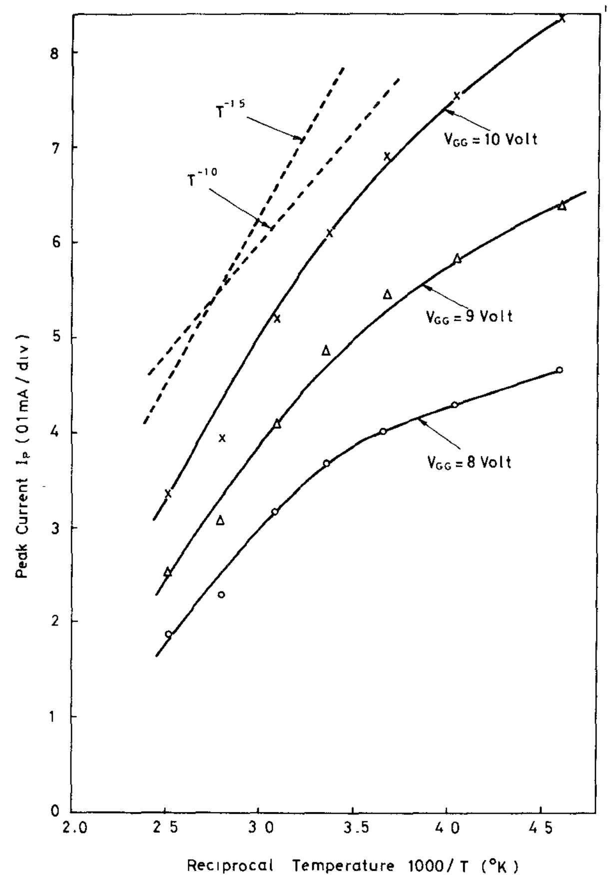

Fig. 11. Peak current variations with respect to temperature.

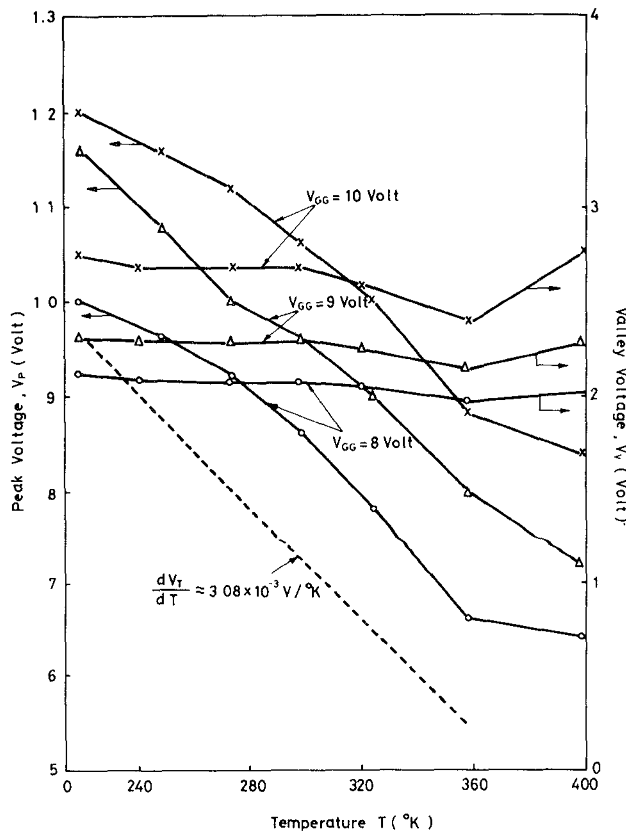

Fig. 10. Peak voltage and valley voltage variations with respect to temperature.

temperature plays an important role in determining the current-voltage characteristic of the MOSFET as a function of temperature. Two temperature functions of T^{-1} and $T^{-1.5}$ are also given in the same figure as a guide to determine the variation of mobility with temperature, which is also justified.

The valley voltage is found more stable at this temperature range, as shown in Fig. 10, which is in quite good agreement with the theoretical prediction cited in (20), where the temperature effect is compensated for high V_{GG}.

V. Conclusions

A NELS-connected three-terminal voltage controlled Λ-type negative resistance structure has been theoretically and experimentally analyzed. For a general description, a high ratio of zero drain voltage conductance of $Q2$ to that of $Q1$ is used; i.e., G_r = 27.18, the observed negative resistance output swing is more than 1 V for different applied gate voltages, and the peak-to-valley current ratio are about several hundred with the definition of I_v = 1 μA. Moreover, the negative resistance can be controlled from 1000 to 3000 Ω in the operating range of 0.5 V. Because of the substrate bias effect, the current handling capability of this NELS-connected structure is limited by using the conventional Al-gate MOSFET. An improvement can be carried out by using DMOS or VMOS fabrication technology. If three MOSFET's are replaced by three DMOS structures, the substrate and the source of transistor $Q1$ can be connected together, and the substrate bias effect can be eliminated. This will lead to higher power

operation. Moreover, the inherent property of high-frequency response of DMOS and VMOS will also improve the frequency response of the present device.

In general, the voltage controlled Λ-type negative resistance MOSFET has several important features. First, it can be easily fabricated by the conventional planar MOS technology at low cost; second, it has a wide range of negative resistance, output swing, and high peak-to-valley current ratio; and third, it has good temperature stability.

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