Al Coverage of Surface Steps at SiO_2 Insulated Polycrystalline Si Boundaries: Al Evaporation in Vacuum and Low Pressure Ar

V. J. Silvestri,* V. L. Rideout,* and V. Maniscalco

IBM Thomas J. Watson Research Center, Yorktown Heights, New York 10598

ABSTRACT

In integrated circuit technology, a potential reliability problem arises due to voids that form in aluminum interconnection lines where they cross the SiO_2-insulated polycrystalline silicon (polysilicon) regions. Not only do these voids cause thinning of the Al lines which may then burn out at high current densities, but the voids are also potential sites for accumulation of chemical residues which could lead to a long term deterioration of the integrated circuit. This study examined the formation and structure of step profiles at SiO_2-insulated polysilicon boundaries and voids in Al lines crossing the boundaries. The formation and structure were studied as a function of process variables including delineation of the polysilicon boundary, chemical vapor deposition or thermal growth of the SiO_2 insulation, evaporation of the Al layer, and delineation of the Al line pattern. The addition of Ar gas at a pressure of 0.1 to 10 milliTorr to the Al evaporation chamber resulted in excellent step coverage and eliminated the Al void formation, even in the case of very steep step profiles.

In field effect transistor (FET) integrated circuit technology a potential reliability problem arises due to voids that form in the Al interconnection lines where they cross the boundaries of polycrystalline silicon (polysilicon) regions. Not only do these voids cause thinning of the Al lines which may then burn out at high current densities, but the voids are also potential sites for accumulation of chemical residues which could lead to a long term deterioration of the integrated circuit. Chemical vapor deposited (CVD) polysilicon is commonly used for gate regions and interconnection lines. Additional interconnection capability is provided by vacuum evaporated Al lines which must cross over and be insulated from the polysilicon regions. Typically, the polysilicon lines are covered with an insulating layer of thermally grown or CVD SiO_2. Chemical etching is commonly used to define the Al lines, and large voids in the Al lines may occur at the polysilicon boundary. During chemical etching, any small opening between the Al and SiO_2 layers is enhanced at the crossing point, forming a void and thinning the line which can affect integrated circuit reliability (1). The scanning electron microscope (SEM) photograph in Fig. 1 shows a cross-sectional view of such an enhanced void in an Al line.

Several authors (1-8) have considered the reliability problem of Al line coverage over SiO_2 steps in integrated circuits and the means to alleviate it. For example, one technique utilizes high temperature (*e.g.* 1000°C) reflow of a deposited phosphorous-rich glass layer (4, 5), while another uses ion implantation to locally alter the etching rate of an insulating SiO_2 layer (6). Both techniques use additional processing to smooth the step profile. Additional thermal treatments or ion implantations, however, are not always practical or desirable. To the contrary, often the reduction of thermal treatments to reduce spreading of impurity profiles, and reduction in the number of implantation steps to simplify fabrication are important concerns, particularly in very high density integrated circuits (10). Therefore, one objective of this study was to try to determine the relationship of processing procedures to step profile formation and to subsequent Al void formation. The formation of the step profile and the void structure was monitored throughout the processing sequence in order to identify procedures that would minimize Al void formation. Early in the work, it was observed that voids often occurred only on one side of a line structure. This phenomena of preferential location suggested that gas directionality during SiO_2 deposition, and/or the Al evaporation geometry, might be contributing to void formation. Consequently, a second objective was to attempt to identify a solution to the void problem by altering the layer deposition process itself.

Experimental Conditions

A photolithographic masking pattern consisting of varying line widths and spaces (1-25 μm wide) was

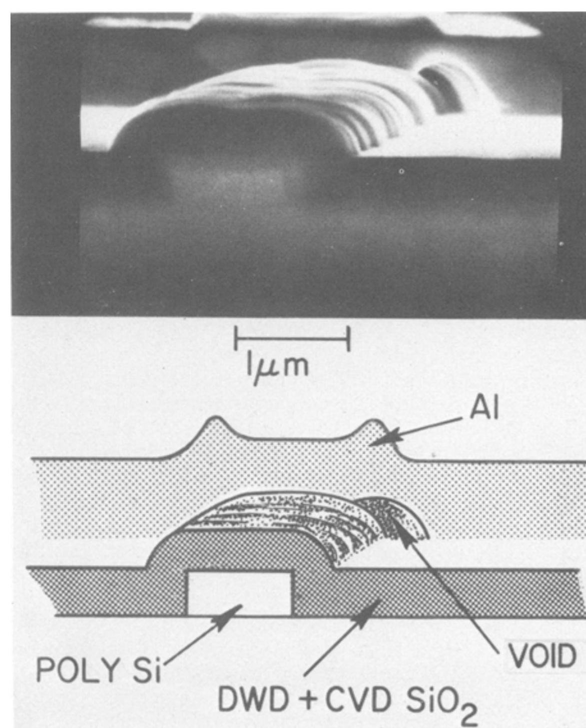

Fig. 1. Void formed in an Al line crossing an oxide-covered polysilicon step.

* Electrochemical Society Active Member.
Key words: vacuum, evaporation, deposition.

Downloaded on 2014-05-01 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

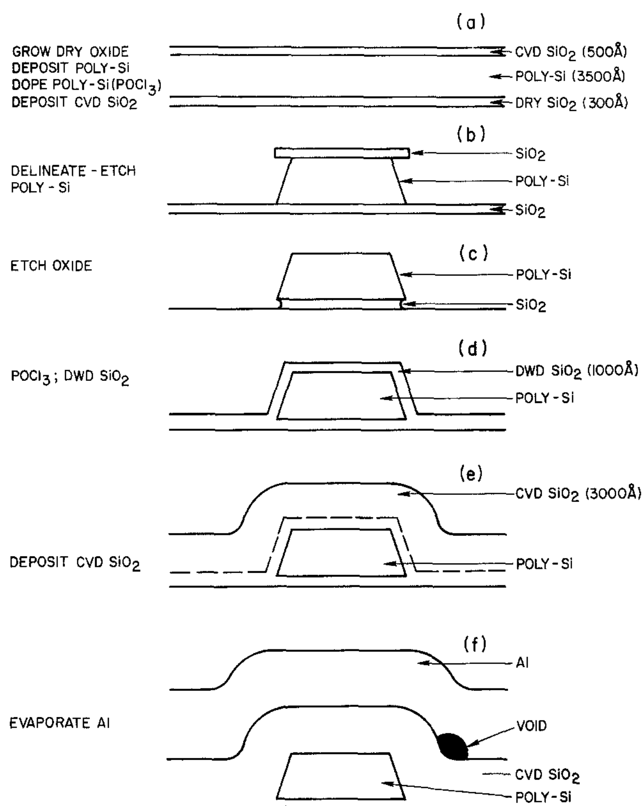

Fig. 2. Processing sequence

used in this study. Stripes were delineated in a 3500Å CVD polysilicon film deposited on a 300Å thermally grown SiO_2 on a silicon substrate. The processing sequence for fabricating the polysilicon stripes is shown in Fig. 2. The CVD polysilicon was deposited in a Nitrox reactor by decomposing SiH_4, 10% in N_2 (by volume); flowing at 0.67 liters/min in an N_2 carrier gas flow of 33.5 liters/min. The substrate temperature during deposition was 650°C. The calculated linear gas stream velocity was 7.3 cm/sec at room temperature. After delineation, the polysilicon stripes were covered with an insulating layer of thermally grown or CVD SiO_2, or a hybrid of the two oxide layers (9), as shown in Fig. 2D and 2E. The thermal oxidation process was carried out at 1000°C and employed dry oxygen-water vapor-dry oxygen gases sequentially which is referred to here as a dry-wet-dry (DWD) sequence. The CVD SiO_2 deposition conditions were: substrate temperature, 800°C; SiH_4 flow rate, 0.77 liters/min of 1% SiH_4 in N_2O (by volume); N_2O flow rate, 0.53 liters/min; and N_2 carrier gas flow rate 51.5 liters/min. The polysilicon stripes were oriented either parallel or perpendicular to the gas flow during the CVD SiO_2 deposition.

Aluminum layers (500-8000Å) were evaporated on top of the oxide. The Al was evaporated either in high vacuum or in an Ar background pressure of 0.1 to 10.0 milliTorr using a resistive heated crucible. The Al lines were delineated with wet chemical etching using a line mask pattern oriented at 90° to the underlying polysilicon stripes. The Al source was oriented at an angle of 13° to the normal to the substrate surface, and the polysilicon stripes were oriented either parallel or perpendicular to the Al flux.

During the processing, wafers were culled following all major fabrication steps. Samples were cleaved across the polysilicon stripes to examine etch angles and CVD step profiles. Extensive use was made of the scanning electron microscope in examining cross sections and surface topography. To detect voids at the Al crossover points, the surface topography was examined at shallow SEM angles of 20°-45°.

Step profiles.—The vertical topography or step profile at the boundary of an oxide-covered polysilicon line, if steep, is conducive to the formation of voids in Al interconnection lines. Four step profiles which can lead to void formation are shown in Fig. 3. An oxide pattern is used to delineate the polysilicon line, and the oxide is undercut during polysilicon etching as shown in Fig. 3A (X). If retained, this undercut oxide layer leads to a negatively sloped insulation oxide profile, even when CVD SiO_2 is used. Furthermore, any residue from the etching step may be trapped under the oxide ledge as shown in Fig. 3A (X), possibly leading to a long term contamination problem (3).

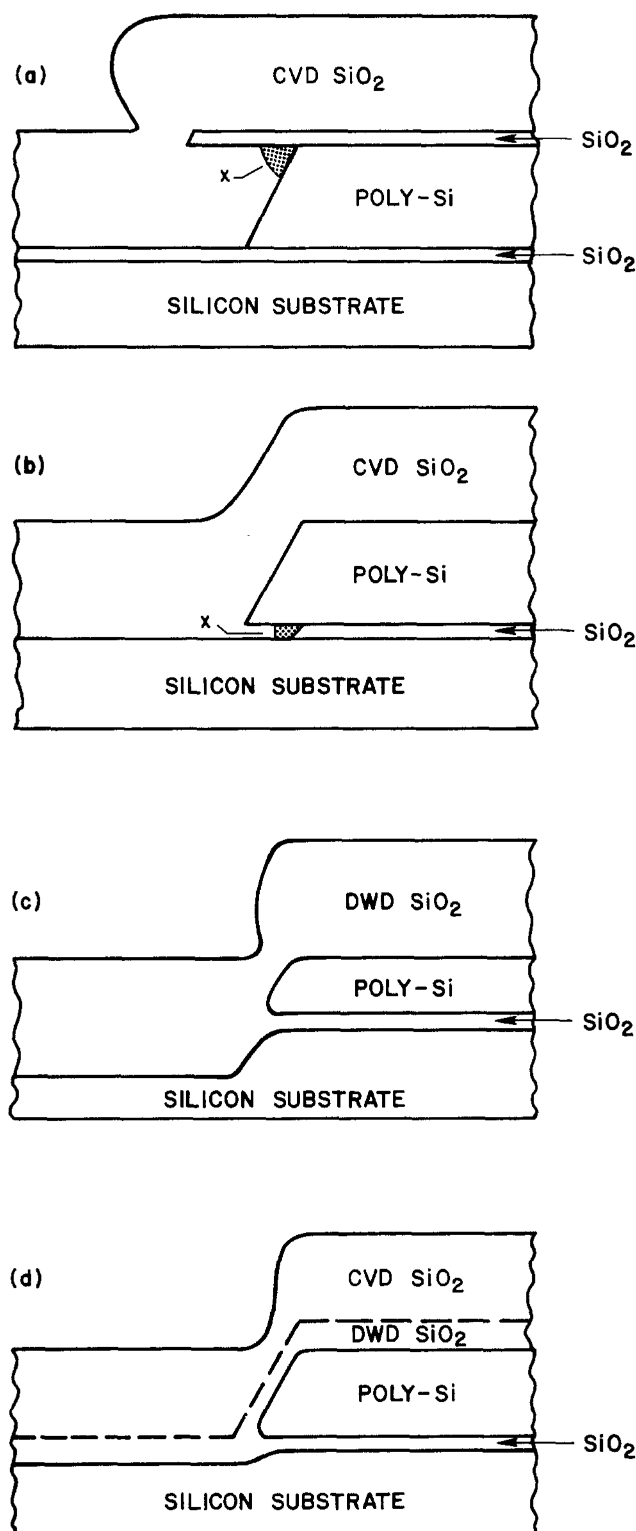

Fig. 3. Step profiles at the boundary of an oxide-covered polysilicon stripe: (A) CVD SiO_2, defining oxide retained, (B) CVD SiO_2, defining oxide removed, (C) DWD SiO_2, defining oxide removed. (D) DWD-CVD Hybrid SiO_2, defining oxide removed. The location of possible trapped contamination in A and B is noted by X.

Downloaded on 2014-05-01 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

As shown in Fig. 3B, if the undercut oxide defining layer is removed by dissolving in HF, then the thin SiO_2 gate insulator is etched away under the polysilicon stripe. Although CVD SiO_2 can give a favorable step profile for Al line coverage, in this case a thin oxide breakdown problem can occur at the edge of the polysilicon (X) due to the undercut gate oxide. Replacing the CVD insulation oxide with a thick thermally grown SiO_2 layer, as shown in Fig. 3C, overcomes the gate oxide breakdown problem but leads to a much steeper step profile. In addition, the long thermal cycle required to grow the DWD SiO_2 at high temperature is less attractive in terms of impurity profile control and processing time.

A hybrid insulation layer consisting of thermal oxide to prevent edge breakdown and CVD SiO_2 to improve the step profile and reduce processing time is shown in Fig. 3D (9). Compared to the thermal oxide profile of Fig. 3C, the hybrid oxide approach reduces but does not necessarily eliminate the negative oxide slope. In our work with 500Å gate oxides, we have examined a variety of layer thicknesses for the thermal CVD hybrid case, and prefer to use a 1000Å DWD SiO_2 layer followed by a 3000Å CVD oxide film.

Of the four insulation approaches illustrated in Fig. 3, only those of C and D which use thermal oxide to avoid gate edge breakdown are electrically acceptable. However, the structures shown in Fig. 3C and 3D have abrupt oxide profiles and a small opening can develop under an Al layer when it is subsequently deposited on the oxide-covered structure. During definition of the Al interconnection line by chemical etching, any small opening between the Al and SiO_2 layers is enhanced at the crossing point, forming a void in the Al line. This thins the line and can affect the integrated circuit reliability.

Voids.—Very often, voids in the Al lines were observed to form only on one side of the polysilicon stripe. This phenomena is shown in Fig. 4A. This preferential void formation could not be ascribed to step profiles alone because no process-related asymmetries were observed, for example, in the polysilicon etching and doping procedures, or with the gas flow direction during CVD SiO_2 deposition. Even when extreme step profiles were intentionally produced, voids still formed preferentially. Thus it became apparent that the step profile was not the prime contributor to void formation. Subsequently, it was experimentally verified that the Al source position relative to the stripe position was responsible for the preferential void formation.

Al evaporation in vacuum.—Figures 4A and 4B show the location of voids for the Al flux perpendicular to and parallel to the polysilicon stripes, respectively. The Al flux direction is indicated by arrows in the photographs. Figure 4A shows voids occurring on the downstream side of the polysilicon stripes. This was a consistent observation for the vacuum evaporation case when Al flux lines were essentially perpendicular to the stripes. The perpendicular flux case shown in Fig. 4A gave voids that were large, more uniform in size, and preferentially located on one side of the stripes. In comparison, the parallel flux case shown in Fig. 4B gave voids that were smaller, more variable in size, and located randomly on either side of the polysilicon stripes. These observations were consistent irrespective of Al film thickness.

It is proposed that in both cases the void location, relative size, and size uniformity are related to the degree of shadowing produced by either the stripe itself, or by protrusions along the irregular edge of the stripe. Consistent with this hypothesis is the observation that gross shadowing effects by the line itself produce large, uniform, and preferentially oriented voids, while more random shadowing effects due to line edge irregularities produce voids of variable size and uniformity, at nonpreferential locations. The SEM photographs of Fig. 5A and 5B show cross-sectional views of voids corresponding to perpendicular and parallel Al fluxes, respectively.

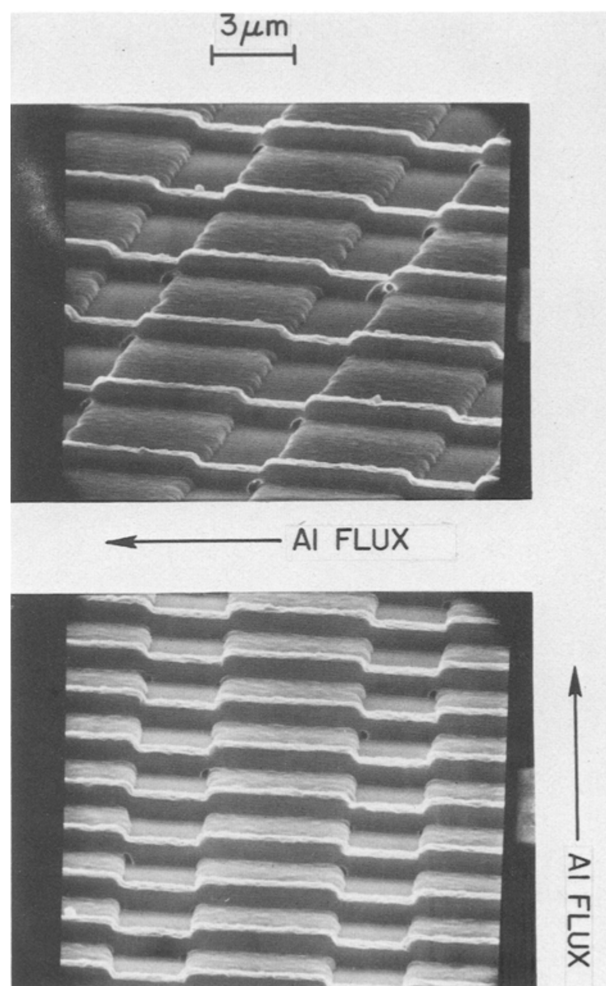

Fig. 4. Location of voids in Al lines for Al flux perpendicular (A, top) and parallel (B, bottom) to the polysilicon stripes.

Al evaporation in argon.—In an effort to obtain void-free Al step coverage even over severely recessed step profiles, Al evaporations were performed in Ar with background pressures of 0.1 to 10.0 milliTorr. The use of the Ar atmosphere gave excellent step coverage even with severe step profiles. A possible mechanism for the improved coverage might be that through molecular collisions the Ar atoms reduce the mean-free path and provide a more random direction to the depositing Al atoms. Figure 6 shows a 3500Å polysilicon step covered with 4000Å of CVD SiO_2 and crossed by a 1500Å thick Al line evaporated in a 6 milliTorr Ar atmosphere. Similar void-free coverage was obtained for Al films up to 8000Å. In addition, a variety of combinations of Al thicknesses and step profiles were examined and in all cases the Al coverage over the step exactly followed the step profile without exhibiting any of the void formation observed with vacuum evaporations.

Listed in Table I are the deposition rate and resistivity for the Al films deposited in Ar. Increasing the Ar pressure decreases the Al deposition rate and

Table I

Ar pressure (milliTorr)	Deposition rate (Å/min)	Resistivity ($\mu\Omega$-cm)
0.5	3100	8.1
2	2000	8.0
4	900	5.4
6	400	3.5

Downloaded on 2014-05-01 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

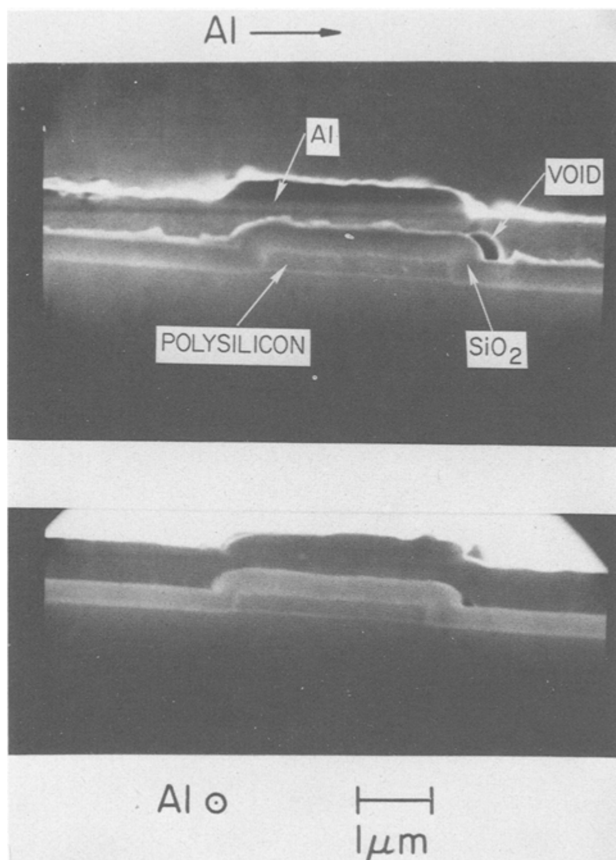

Fig. 5. SEM photographs of cross-sectional views of voids for Al flux perpendicular (A, top) and parallel (B, bottom) to polysilicon stripes.

the resistivity of the Al film. An acceptable balance of these factors was achieved at an Ar background pressure of about 4 to 6 milliTorr. For this pressure range, the Al resistivity is close to that reported for bulk aluminum at room temperature which is 2.82 $\mu\Omega$-cm. The resistivity values obtained at lower argon pressures (0.5-2 milliTorr) are higher. The cause of this is not yet understood.

Summary

In this study, the formation and structure of voids in Al interconnection lines crossing oxide-covered polysilicon steps were examined as functions of the deposition or growth of the insulating SiO_2 layer between the Al and polysilicon layers, and the deposition and delineation of the Al interconnection pattern. The size, uniformity, and location of voids is strongly dependent on the relative alignment between the incident Al flux and the polysilicon stripes. The edge profile was a lesser factor, while the CVD SiO_2 gas flow direction was insignificant to void formation. The addition of Ar gas at a pressure of about 4-6 milliTorr to the Al evaporation chamber resulted in excellent step coverage and eliminated the Al void formation, even in the case of severely undercut step profiles, without serious degradation of the Al resistivity.

Acknowledgments

We wish to express our thanks to C. M. Osburn and E. Bassous for helpful suggestions concerning the experiments. The technical assistance of H. Lazzari, A. Cramer, J. Kucza, E. Petrillo, and M. Smyth is greatly appreciated.

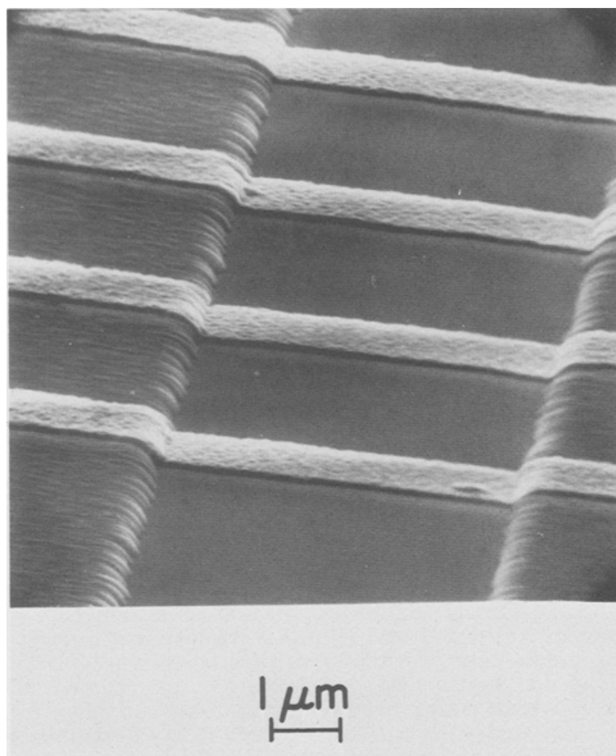

Fig. 6. 1000Å thick Al line crossing a 3500Å thick polysilicon step covered with 4000Å of CVD SiO_2: Al evaporated at 6 milliTorr Ar pressure.

Manuscript submitted Oct. 13, 1978; revised manuscript received Feb. 13, 1979. This was Paper 141 presented at the Dallas, Texas, Meeting of the Society, Oct. 5-9, 1975.

Any discussion of this paper will appear in a Discussion Section to be published in the June 1980 JOURNAL. All discussions for the June 1980 Discussion Section should be submitted by Feb. 1, 1980.

Publication costs of this article were assisted by IBM.

REFERENCES

1. D. L. Fresh and J. W. Adolphsen, Proc. 12th IEEE Reliab. Phys. Symp., pp. 118-130, Las Vegas, Apr. 2-4 (1974).
2. T. Yanagawa and I. Takekoshi, *IEEE Trans. Electron Dev.*, **ED-17**, 964 (1970).
3. I. Matsushina, T. Enomoto, and H. Fukuwatari, Paper 92 presented at the Electrochemical Society Meeting, Chicago, Illinois, May 13-18, 1973.
4. C. G. Peattie, J. D. Adams, S. L. Carrell, T. D. George, and M. H. Valek, *Proc. IEEE*, **62**, 149 (1974).
5. G. E. Moore, U.S. Patent 3,825,442 (1974).
6. R. A. Moline, R. R. Buckley, S. E. Hoszko, and A. U. MacRae, *IEEE Trans. Electron Dev.*, **ED-20**, 840 (1973).
7. G. L. Kuhn, Paper 334 presented at the Electrochemical Society Meeting, Atlanta, Georgia, Oct. 9-14, 1977.
8. I. A. Blech, D. B. Fraser, and S. E. Haszko, *J. Vac. Sci. Technol.*, **15**, 1 (1978).
9. J. T. Clemens, R. H. Doklan, and J. J. Nolen, IEEE Internat. Electron Dev. Meeting Tech. Digest, p. 299, Wash., D.C. (1975).
10. R. H. Dennard, F. H. Gaensslen, H-N. Yu, V. L. Rideout, E. Bassous, and A. LeBlanc, *IEEE J. Solid-State Circuits*, **SC-9**, No. 5, 256 (1974).

Downloaded on 2014-05-01 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).