Chapter1

Introduction

Copper metallization was an important topic in silicon IC technology since IBM announced its success in silicon very-large scale integration (VLSI) processes [1–3]. Nevertheless, there are some problems to use copper as interconnect metal, such as high oxidation rate , lack of anisotropic etching capability , ease of corrosion, and the diffusion of copper is very fast when it contact with GaAs directly without any diffusion barrier, such as in the silicon case[4]. However, the advantages of copper metallization for Si VLSI include lower resistivity and higher electromigration resistance.

Even though the use of copper as a metallization metal has become very popular in the Si devices, the use of copper as a metallization metal for GaAs is quite few. In these literatures, Ta and TaN had been discussed as diffusion barrier for copper metallization. Traditionally, GaAs FETs, MMICs , HEMTs and HBTs use gold as the metal for transmission lines and ground plane metallization. The gold used in transmission lines and ground planes are usually plated to 2μm -3μm. The use of copper as the metallization metal has the following advantages over gold: lower resist, higher thermal conductivity, and lower cost. So if we replace gold with copper as the interconnect metal in HBTs, the transmission speed will increase because of the reduction of contact resistance, and the cost of manufacturing will also be reduced. So the use of copper for metallization metal of GaAs is a very attractive topic.

However, for HBT devices, the use of copper need a suitable diffusion barrier which is compatible with HBT process to prevent copper diffusion into GaAs , and the diffusion barrier should have the following characteristics:

1. Low interaction between Cu and contact metal
2. Good adhesion on adjacent material
3. Planarization process compatible(CMP)
4. Thermal expansion coefficient compatible
5. Good conductivity
6. Good thermal conductor

The characteristics of Cu and Au are shown in Table 1-1

In this work, we will replace gold with copper as the interconnect material in the InGaP-GaAS HBTs while Mo (or Cr) was used as the diffusion barrier. The goal of this study is to find a reliable diffusion barrier for copper metallization of InGaP-GaAs devices in order to reduce the production cost of the GaAs devices and to provide comparable or even better thermal and electrical conductivities for the interconnects. Finally, Cr film was deposited on the copper to prevent copper surface from oxidation. After metal deposition, the samples were annealed at high temperature to investigate the thermal stability of the film.

The choice of suitable diffusion barrier material, deposition method and the copper layer are the major challenges for the integration of copper metallization. The barrier layer should be as thin as possible so that it would not affect the interconnect resistance while still acting as a good barrier against Cu diffusion.

Chapter2

Paper review

2.1 Ohmic Contact

2.1.1 Requirement of ohmic contact

The ohmic contact should have:

1. Linear I-V characteristic with a resistance as small as possible:

According to the scaling rule, the size of the device become shrinking for better performance. The specific contact resistivity should decrease in order to get the same contact resistance. So the reduction of the device size provides the motivation for ohmic contact materials with lower contact resistance.

2. Thermally stable:

In order to be viable alternative to the Si technology, the GaAs devices fabrication process should be compatible to Si as much as possible.

Besides, a smooth surface, strong adhesion, shallow horizontal and verticle diffusion depth, and low metal sheet resistance are required for GaAs integrated circuits. The requirement of ohmic contact is illustrated in Fig-2.1.

2.1.2 Current transport mechanism of ohmic contact

When a metal contacts with a semiconductor, the conduction and the valence bands bend to make the Fermi levels in the metal and the

semiconductor equal. The mechanism of current transport is influenced by the doping concentration in semiconductor and the temperature.

The current density(J) between contact metal and semiconductor is:

$$J \fallingdotseq \exp(-q\Phi_b/E_{00})$$

Which

- $\Phi_b = \Phi_m - \chi$
- $E_{00}=(qh/4\pi)*(N/\varepsilon m^*)^{1/2}$
- ε :dielectric constant
- N: doping concentration
- m*:effective electron mass
- χ :electron affinity

From the equation, it indicate that the current density increace when we increase the doping concentration because of the width of potential barrier decrease.

2.1.3 Limits of doping level in GaAs

For n-type GaAs, the column VI elements are desirable for donors in III-V compound semiconductors. Higher doping levels are more easily achievable in p-type than in n-type GaAs. Because of dopants which are not amphoteric are typically used and DX centers are associated with donors only. Therefore the ohmic contact to p-type GaAs fabricated by high doping levels often lead to satisfactory values of the contact resistance.

2.1.4 Guildeline for low resistance ohmic contact formation

Typically, a low resistance ohmic contact needs:

1. A semiconductor is heavily doped with carriers.
2. Low energy barrier between the metal/semiconductor interface.

The conventional ohmic contact preparation technique involves deposition of the contact metals onto the cleaned GaAs substrate and annealing the contacts at elevated temperature to form intermediate semiconductor layer at the metal/GaAs interface, as shown in Fig-2.2. We will get low ohmic contacts when the intermediate semiconductor layer with low energy barrier or high carrier density is formed between the metals and the semiconductor after heat-treatment. This fabrication process are called 'deposition and anneal ohmic contact'.

This ohmic contact fabrication technique needs a relatively simple fabrication system and has excellent reproducibility. Thus, this technique is suitable for manufacturing devices and used in a wide variety of GaAs devices.

However, the big disadvantage for this technique is that the process parameters are not easily found, such as the contact metals, thickness of each metal layer, annealing time and temperature, diffusion coefficients, stress, surface energy, etc.

2.1.5 Patterning of the ohmic metal

The patterning of the ohmic metal depends on the photolithography process. Although the lithography techniques are mature in silicon industry, the lithography process in GaAs processing is quite different. There are two basic metal patterning processes: one is the metal etch mask process typically used in silicon process, and the other is the lift-off

process commonly used in GaAs industry. This is because GaAs substrate will be attacked by many metal etchants, and aluminum, which can be easily etched in relatively innocuous etchant and can also be easily etched by dry etch techniques, is used by silicon processing as the metallization metal. Meanwhile, GaAs uses AuGeNi as Ohmic metal and TiPtAu as Schottky metal. These systems cannot be easily etched by a simple solution or dry etch techniques. In this study, lift-off process was also used for the Ohmic metallization processes.

Karl Suss MJB3 contact aligner with xenon-mercury lamps was used as the photolithography equipment for the patterning of Ohmic metals. Xenon-mercury lamp emits ultraviolet (UV) light with the wavelength in the 220-240 nm range. Photoresist, AZ-5214E was used as the resists for the lift-off process.

The photoresist was coated on the substrate firstly and then baked at hot plate at 90 °C for 60 seconds. The resist is then exposed by UV light source. Because of using image reversion, the resists formed lift off profile after exposure and development. HCl-based solution was used as the pre-metallization cleaning solution to remove the native oxide of the GaAs surface before Ohmic metallization. The Ohmic metals used were Pd/Ge/Mo(or Cr)/Cu. After metal deposition, the resist was lifted off and Ohmic metals were formed at the desired areas.

The most common method of forming Ohmic contacts on n-type GaAs is to apply an appropriate metallization scheme to the heavily doped GaAs followed by annealing process. During the annealing process, one of the constituent metals diffuses into the wafer and dopes the cap GaAs layer heavily. Many kinds of alloying systems for n-type ohmic

contacts have been studied in literature. In this study, PdGe alloys were used to form the Ohmic contacts.

The Ohmic metals deposited, from the bottom to the top, were Pd, germanium, diffusion barrier metal (Mo or Cr) and copper. In the study, germanium atoms diffused into the GaAs and heavily doped GaAs during the thermal annealing process. After the PdGeMo(or Cr)Cu metallization, the contact resistance was measured by using transmission line model (TLM). The optimized conditions for thermal alloying is 350°C for 10min by furnace method.

2.2 Diffusion barrier

Many suitable diffusion barrier materials, such as Ta[6-12] , Ta_2N[5,6,13] , TiN[14,15], W[11,16] , WN_X[16,17] , and amorphous Ta-Si-N[9,18] have been reported.

The choice of multilayer thin films needs to consider the following properties: the electrical resistivity, mechanical stress, chemical inertness, thermal stability, film deposition techniques, and easiness of film patterning [19].

Refractory metal is a good choice as the diffusion barrier material because of its high melting point. Its solubility in copper is very low even though at high temperatures. However, the sheet resistance of copper increases rapidly at 400 ℃ annealing when using a single refractory metal as the diffusion barrier, like Cu/Ti/Si, Cu/Ta/Si, and Cu/W/Si. We know the copper atoms diffuse into silicon and forms copper-silicide. The diffusion barrier layer forms polycrystalline structure. It has grain

boundaries. The grain boundaries provide fast diffusion paths for the copper because the grain boundaries has high diffusion coefficient. Copper diffuses through the grain boundaries of the diffusion barrier layer easily into the Si junction region even at low annealing temperatures and causes the device failure. Refractory metal nitrides such as TiN, TaN and WNx have been investigated due to their better thermal stabilities, good adhesion, and low resistivities. Therefore, these transition metal nitrides, which have high melting points, relatively high thermal stability, chemical inertness, and low electrical resistivity, would not form metallic compounds with copper. Some of the results of the investigations of the refractory metals and refractory metal nitrides as the diffusion barriers for silicon are listed in Table 2-1 [20-28].

The thermal stabilities of these barrier layers with Cu are summarized in Table 2-1. These barrier layers include TiW, TiN, Ta, TaN, Ta-Si-N and WNx. Most barrier materials are stable as diffusion barrier up to 550°C. The temperature is high enough for current metallization processes.

Here, we will discuss about the diffusion barrier materials. The Pd/Ge/Au and Ti/Pt/Au systems are widely used in n-type and p-type ohmic GaAs based HBT. Now we will replace gold with copper, and using Mo (or Cr) as diffusion barrier metal between copper and the ohmic contact metal because of copper is a rapid diffuser. Using Mo (or Cr) as diffusion barrier should ensure the success of Cu metallization of GaAs. Mo has high melting point, and Cr is a good diffusion barrier for Cu. Both of them have low resistivity. According to the phase diagram, Mo and Cr have no compounds with copper. Mo and Cr form compounds

with ohmic contact metal (Pd, Ge) at elevated temperature.

In this investigation, the contact resistance and the thermal stability of Cu/Mo/Ge/Pd/GaAs and Cu/Cr/Ge/Pd/GaAs structures will be discussed, we also will report the electrical performances of the copper metallization InGaP-GaAs HBTs.

Chapter3

Experiment procedures

Our experiments can be divided into two parts. Firstly, the Pd/Ge/Mo(Cr)/Cu ohmic contact was analyzed by XRD, AES, SEM, and TEM.

Secondly, the copper multilayer is applied on InGaP/GaAs HBTs. In this chapter, the methods of material analysis and electrical characteristics measurement are described.

3.1 Material Study of Diffusion Barrier

This part investigates the thermal stability of the contact resistance and analyzes the materials when we use Pd/Ge/Mo/Cu and Pd/Ge/Cr/Cu as ohmic contact in GaAs.

The doped GaAs epi-layer was grown by MOCVD on GaAs substrate. After the transmission line method (TLM) pattern (shown in Fig-3.1) transfer to the samples by photolithography, the ohmic metal, [Pd(50nm) / Ge(125nm)], was deposited by electron beam evaporation. Before evaporation, the substrate was cleaned by HCl: H_2O=1:10 for 1min. The Mo (40nm) barrier was deposited by sputtering (in Ar gas), while Cr(40nm) barrier deposited by electron beam evaporation. Then copper (150nm) was deposited on both substrates by electron beam evaporation. A Cr (15nm) layer was deposited on the surface of the Cu to avoid the copper oxidation.

After the substrates were prepared, the substrates were annealed in

the furnace in nitrogen ambient. The following were the methods of material analysis:

1. Specific contact resistivity after different annealing temperature:
   We found the proper temperature of the best ohmic contact resistivity.
2. Specific contact resistivity at different annealing time:
   The stability of the diffusion barrier metals (Mo,Cr) were evaluate at different annealing temperature and time.
3. X-ray Diffraction Analysis (XRD)
   The structures of the thin film were characterized by Siemens D5000 Diffractometer. The grazing incident angle is 1° with 0.4^{o} /min scanning rate and 0.02^{o} step.
4. Sheet Resistance
   The sheet resistances of the samples were measured by four-point probe (Napson model RT-7).
5. Auger Electron Spectroscopy
   The diffusion behavior of ohmic structure after annealing was analyzed by AES (Auger electron spectroscopy). The AES is based on the use of primary electrons with typical energies between 3 and 30 kev. It focuses and scans the primary electron beam in the nanometer and micrometer range analyzing the top-most layer.
6. Field Emission Scanning Electron Microscopy
   The surface morphology of the sample was detected by FE-SEM (Hitachi S-4000)
7. Transmission Electron Microscopy (TEM)
   TEM analysis was used to identify the phases and interface structures after annealing.

3.2 Device Fabrication and Device Electric Characteristics

After material analysis, the copper multilayer is applied on InGaP/GaAs HBTs.

3.2.1 HBT process

Pd/Ge/Mo/Cu/Cr and Au/Ge/Ni/Au ohmic contact in InGaP/GaA HBTs will be fabricated, and the process can be express as follows:

1. Wafer cleaning:

   The wafers were immersed in ACE and IPA separately to remove the contaminants from the wafer surface, then they were blown to dry by nitrogen gas.

2. Emitter Mesa, Collector Mesa, and Isolation:

   The device was fabricated by standard triple mesa process. The GaAs layer was etched by etchant composed of phosphoric acid, hydrogen peroxide, and D.I. water. The InGaP layer was etched by etchant composed of phosphoric acid and hydrogen chloride acid. After etching process, the device was rinsed by D.I water and blown to dry by nitrogen gas.

3. Emitter、Collector ans Base Metal:

   The metallization metals were difined by AZ-5214E photo resist. After the metallization, the lift off process was used to remove the metals we do not need. The emitter and collector ohmic contacts were Pd (50nm)/Ge (125nm)/Diffusion barrier (40nm)/Cu(150nm). We deposited a thin Cr (15nm) layer on the top of Cu to prevent

Cu oxidation.

The base metals we deposit were Ti(20nm)/Pt(60nm)/Au(150nm), like the traditional p-type contact metal.

3.2.2 DC Characteristics Measurement

The current-voltage (I-V) characteristics of HBT device were measured by HP4142B. During the measuring the I-V curves, there are three probes contacted onto the pads of emitter, base and collector. The DC characteristics of the HBT devices were measured under common emitter condition.

We will compared the electric characteristics (e.g. I-V characteristics, current gain and Gummel plots) of the devices which have Pd/Ge/Mo/Cu/Cr or Au/Ge/Ni/Au ohmic contact.

Chapter4

Results and Discussion

This chapter will discuss the electrical characteristic and materials analysis results of the new n-type ohmic contact metal structures used in this study. The thermal stability of Mo or Cr diffusion barrier is discussed based on the results of AES, XRD, sheet resistance and TEM profile studies. Besides, the DC measurement results of the devices manufactured using these new ohmic contacts are also shown in this chapter.

4.1 Analysis of the Contact Materials

4.1.1 Specific contact resistivity after different temperature annealing

The different annealing temperatures to obtain the lowest ohmic contact resistance are studied. Based on this data, other material characteristics were studied.

From F-4.1, when annealed at 350˚C for 10 minutes, the ohmic contacts with Mo or Cr as the diffusion barriers had the lowest specific contact resistance.

4.1.2 Thermal Stability Test for Ohmic Contact to n+GaAs

After obtaining the lowest ohmic contact resistance, the thermal stability of the Pd/Ge/Mo(Cr)/Cu structures were studied. From F-4.2, it

can be seen that the contact resistance of the ohmic structure with Mo diffusion barrier was stable up to 300°C annealing for 20 hours, while the contact resistance of the ohmic contact with Cr diffusion barrier changed after 300°C annealing for 20 hours.

4.1.3 Auger Electron Spectroscopy Analysis

Fig-4.3(a)~(f) show the AES profiles of the n+GaAs/Pd/Ge/Mo/Cu/Cr and n+GaAs/Pd/Ge/Mo/Cu/Cr samples after different temperature annealing.

Fig-4.3(a) and (b) show the sample annealed at 350˚C for 10 minutes, it is the optimum temperature to obtain the lowest contact resistance. Both figures show that Mo and Cr diffusion barriers were stable under this annealing condition.

Fig-4.3(c) and (d) show the sample annealed at 300°C for 1 hour following 350°C thermal treatment for 10 minutes. Comparing (c) with (d), it can be found that Mo diffusion barrier was stable, while there was Cr diffusion into Pd/Ge layer than Mo. It indicates that the ohmic contact with Mo diffusion barrier was stable up to 300°C annealing for 20 hours, while the ohmic contact with Cr diffusion barrier changed after 300°C 20 hours annealing.

Fig-4.3(e) and (f) show the sample annealed at 400°C for 30 minutes following 350°C for 10 minutes thermal treatment. It shows that both diffusion barriers failed after 400°C annealing for 30 minutes.

4.1.4 SEM Image

Fig-4.4(a)~(f) show the SEM surface morphology of the samples after annealing at 300°C, 350°C, and 400°C for 30 minutes respectively.

Fig-4.4(a)~(c) show the samples with Cr diffusion barrier, (d)~(f) show the samples with Mo diffusion barrier. From the results of the SEM photograph, the surfaces were almost unchanged after annealing at temperature up to 350°C, but after 400°C annealing, the surface roughness increased.

4.1.5 TEM Image

Fig-4.5(a) ~ (d) show the TEM profiles of the n+GaAs/Pd/Ge/Mo/Cu/Cr and n+GaAs/Pd/Ge/Mo/Cu/Cr samples annealed at 300°C for 1 hour following 350°C 10minutes thermal treatment.

Figure (a) and (b) show the TEM image of the contact with Mo barrier, it indicates that Mo is a good diffusion barrier and there was no interdiffusion between Cu and Pd/Ge. Figure (b) shows the high resolution image, it can be found that the ohmic contact metal, Pd/Ge layer become PdGe alloy and amorphous Ge after the thermal treatment.

Figure (c) and (d) show the TEM image of the contact with Cr barrier, it shows that Cr diffusion barrier failed after annealing at Cr diffused into Pd/Ge layer.

4.1.6 Sheet Resistance

Fig-4.6 shows the changes of sheet resistance after annealing at different temperatures for 30 minutes.

For contact with Mo barrier, the resistance dropped a little after

300-350°C annealing, it may be caused by the decrease of the defect density.

For contacts with Cr barrier, the resistance increased a little after 300-350 ^{o}C annealing, it may be caused by the reaction between different metal layers. The sheet resistance was quite stable for annealing temperature up to 350 ^{o}C.

After 400°C annealing, the sheet resistance increased, it may be attributed to the reaction between the metal layers.

4.1.7 X-ray Diffraction Analysis

Fig-4.7(a) and (b) show the XRD diffraction patterns of the contact with Mo and Cr diffusion barriers. It shows that both diffusion barriers failed after 400 ^{o}C annealing. It can be seen from the diffraction patterns, which some Cu-metal compound peaks appeared. Comparing the results with AES results, it is evident that the Cu atoms have penetrated through the diffusion barrier and mixed with the ohmic contact metal and the GaAs layer. The result is in consistent with the AES profile and sheet resistance results we observed.

4.2 Device Electrical Tests Results

Fig-4.9(a) shows the comparison of the HBTs with Cu metallization ohmic contact and traditional Au based ohmic contacts, both devices showed similar knee voltage and offset voltage. The current gain for Cu metallization HBT was 95 and for tradition Au metallized HBT was 93.

Fig-4.9(b) shows the comparison of the Gummel plot of the HBTs with Cu metallization ohmic contact and traditional Au based contacts,

the characteristics of the Gummel plot of these two HBTs are quite similar.

In order to study the thermal stability of the Cu metallization ohmic contact HBT, the samples were annealed at 250 ^{o}C for 24 hours. Fig-4.9(c) shows the common emitter I-V curves of the HBT with Pd/Ge/Mo/Cu ohmic contact before and after annealing at 250 ^{o}C for 24 hours. As can be seen, there was no additional degradation of the knee voltage after the thermal annealing.

Material	Resisivity (m-Ω•cm)	Thermal Conductivity (cal/cm sec ºC)	Melting point (ºC)	Prices (US$/Kg)
Cu	**1.69**	**0.94**	**1083**	**~2.1**
Au	**2.4**	**0.7**	**1063**	**~11400**

Table 1-1 Comparison of Copper and Gold as the metallization metal

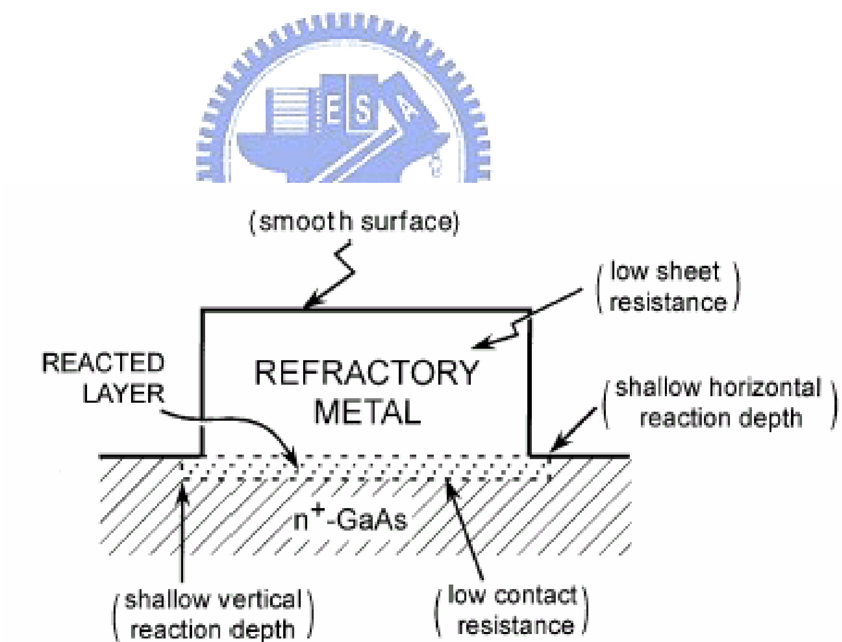


Fig-2.1 Schematics of the requirement for forming good ohmic contacts

Sample	Barrier Stability	Deposition Notes	Reference
Si/TiW (100 nm)/Cu	725 °C, 30 sec.	*In-situ* Cu on TiW	[29]
Si/TiW (100 nm)/Cu	775 °C, 30 sec.	Air between Cu and TiW	
Si/TiNx (50 nm)/Cu	600 °C, 1 hr.	Sputtering	[30]
Si/TiN (50 nm)/Cu	550 °C, 1 hr.	CVD	[31]
Si/TiN (50 nm)/Cu	650 °C, 1 hr.	Plasma treated CVD	
Si/Ta (60 nm)/Cu	600 °C, 1 hr.	Sputtering	[32]
Si/Ta (50 nm)/Cu	550 °C, 30 min.	Sputtering	[33]
Si/Ta2N (50 nm)/Cu	> 650 °C, 30 min.	Sputtering	
Si/TaN (100 nm)/Cu	750 °C, 1 hr.	Sputtering	[34]
Si/TiSi2(30nm)/Ta–Si–N (80 nm) /Cu	900 °C, 30 min.	Sputtering	[35]
Si/W (25 nm)/Cu	650 °C, 30 min.	Sputtering	[36]
Si/W2N (25 nm)/Cu	790 °C, 30 min.	Sputtering	
Si/WN (25 nm)/Cu	500 °C, 30 min.	Sputtering	
Si/WNx (20 nm)/Cu	> 550 °C, 30 min.	PECVD	[37]

Table 2-1 Summary of the thermal stability of the barrier layers used in Si industry

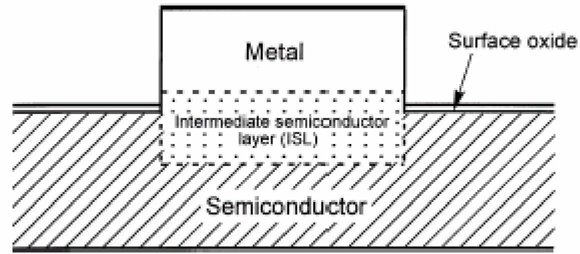


Fig-2.2 Cross-section of the metal/semiconductor interface with intermediate semiconductor layer

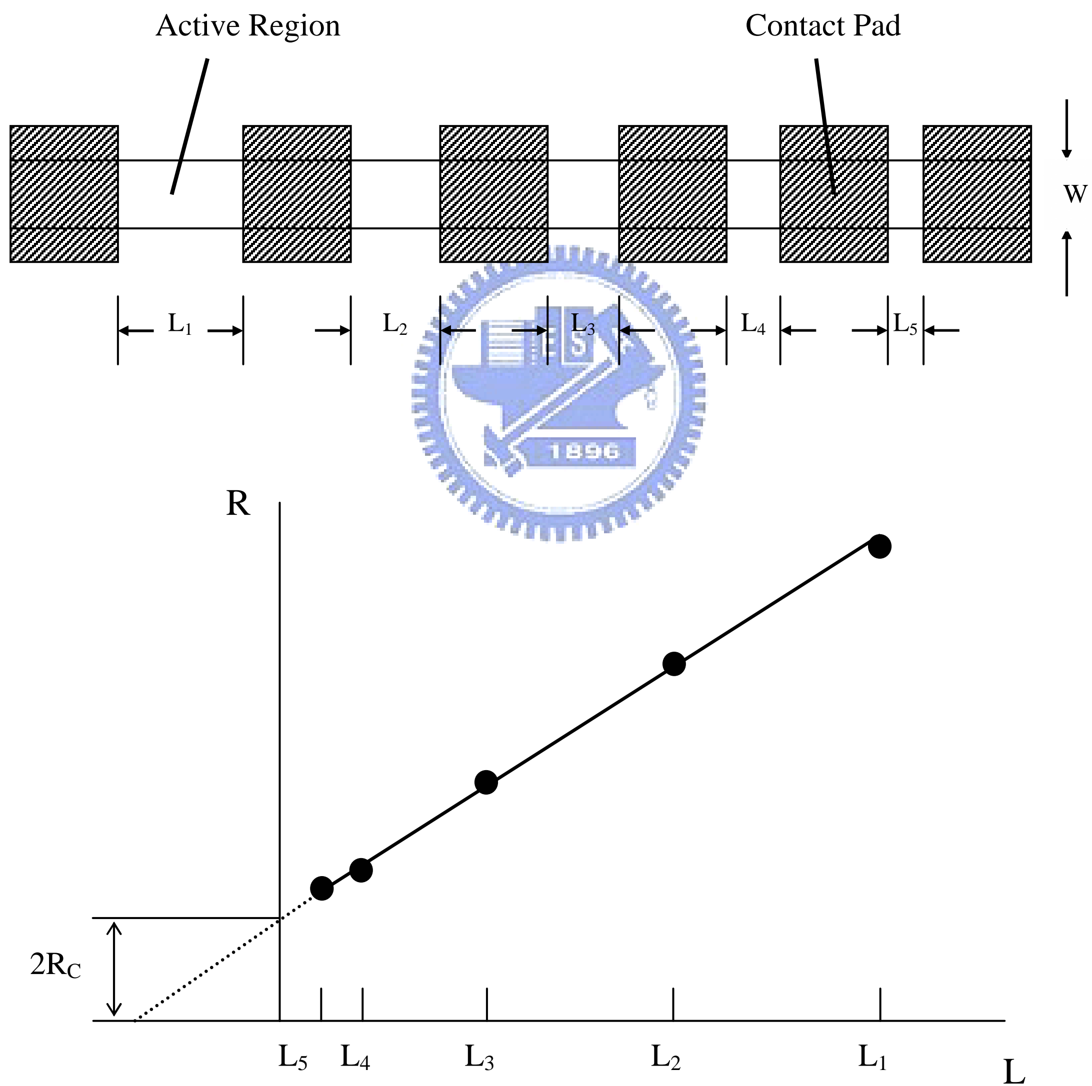


Fig-3.1 The transmission line method (TLM).
(a) TLM patterns. (b) TLM measurement method.

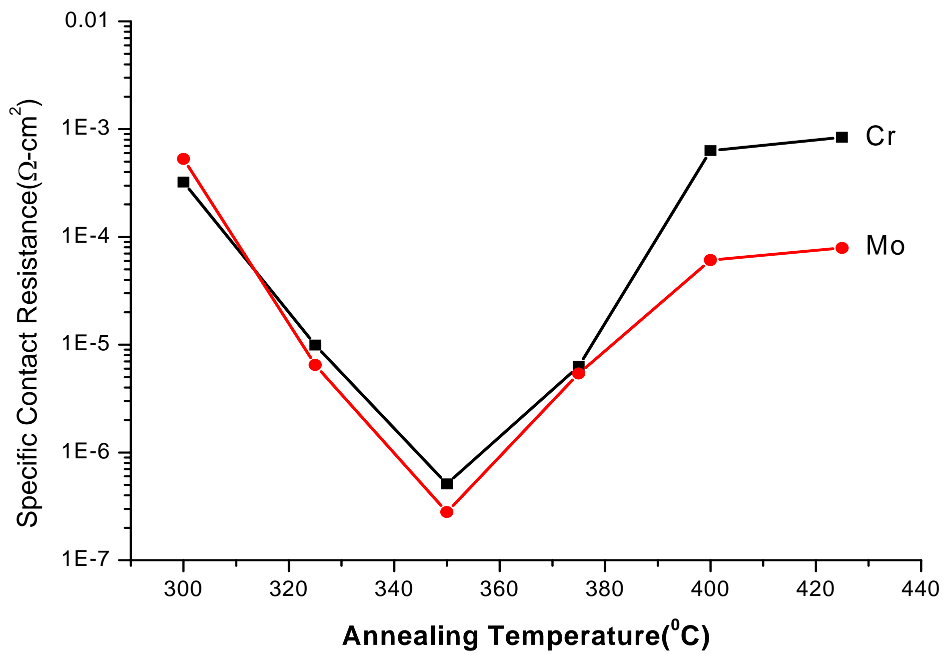


Fig-4.1 Specific contacts vs annealing temperature for contacts furnace annealed for 10 minutes at each temperature

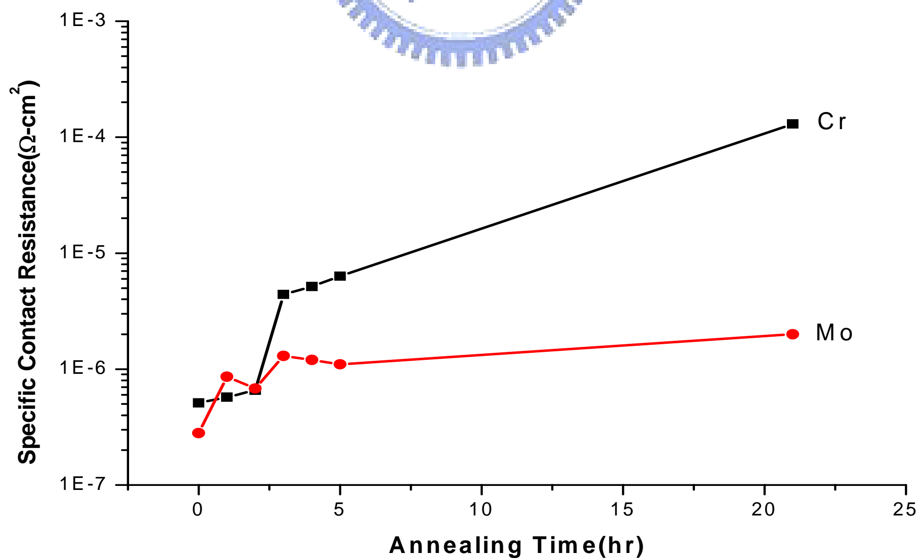


Fig-4.2 Contact resistance vs furnace thermal annealing time at $300^{O}C$

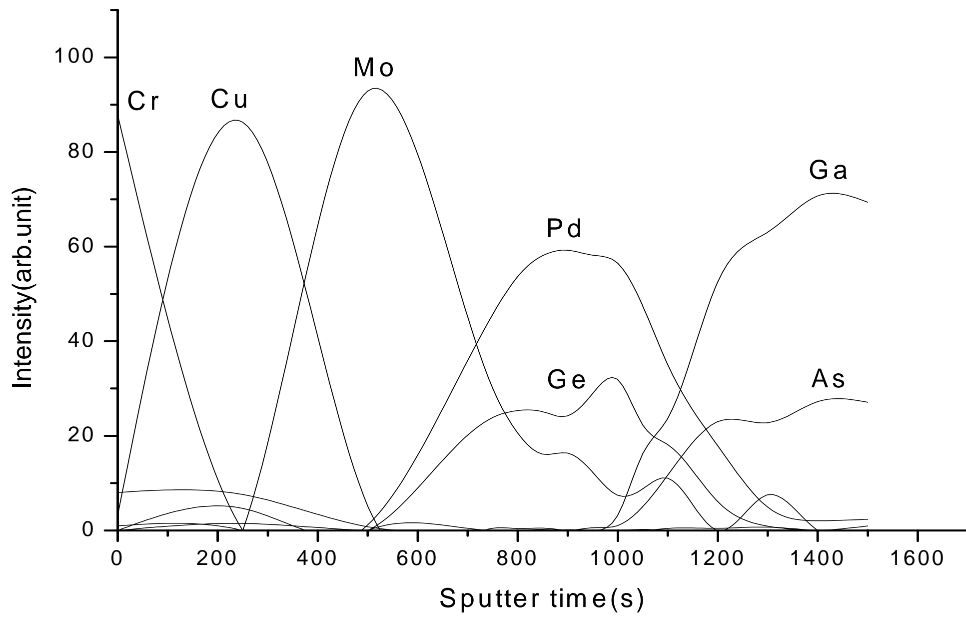


Fig-4.3(a)Ohmic contact with Mo diffusion barrier after 350°C 10min annealing

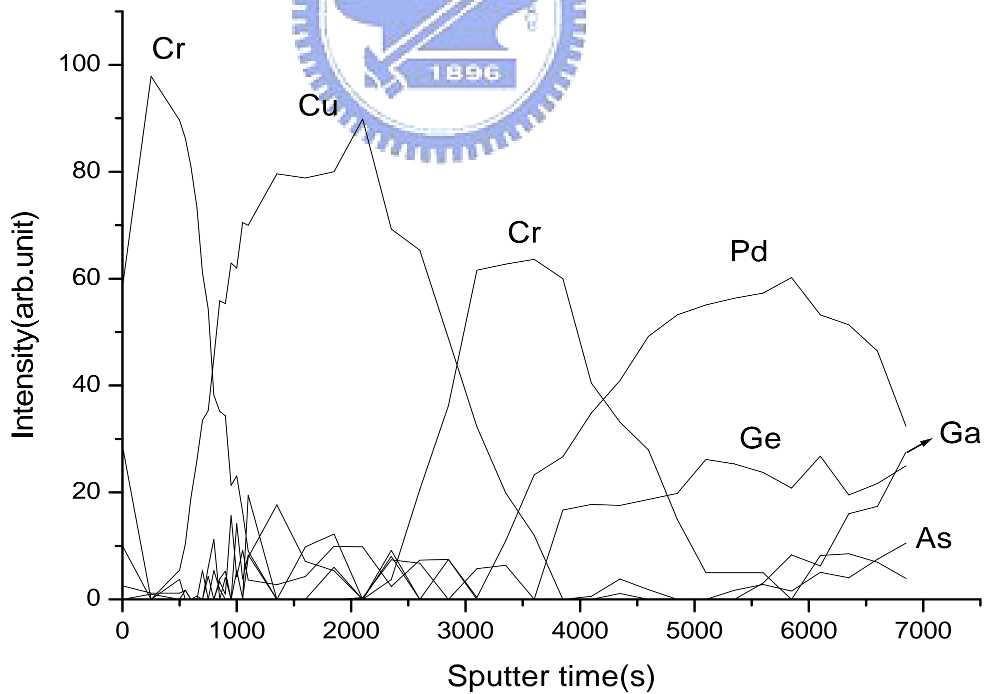


Fig-4.3(b) Ohmic contact with Cr diffusion barrier after 350°C 10min annealing

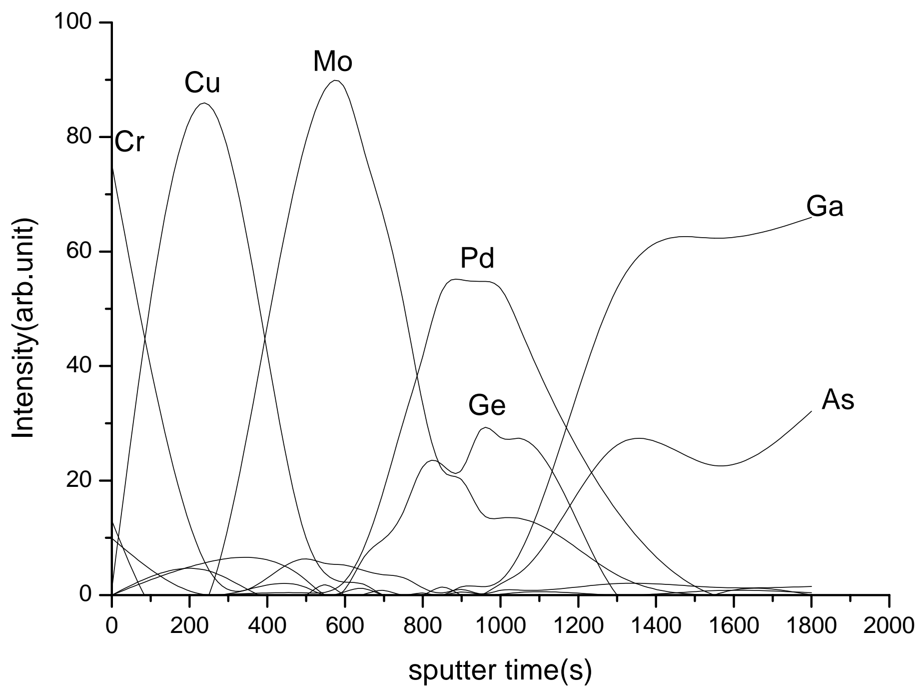


Fig-4.3(c) Ohmic contact with Mo diffusion barrier annealed at 300°C for 1hr following 350°C 10min thermal treatment

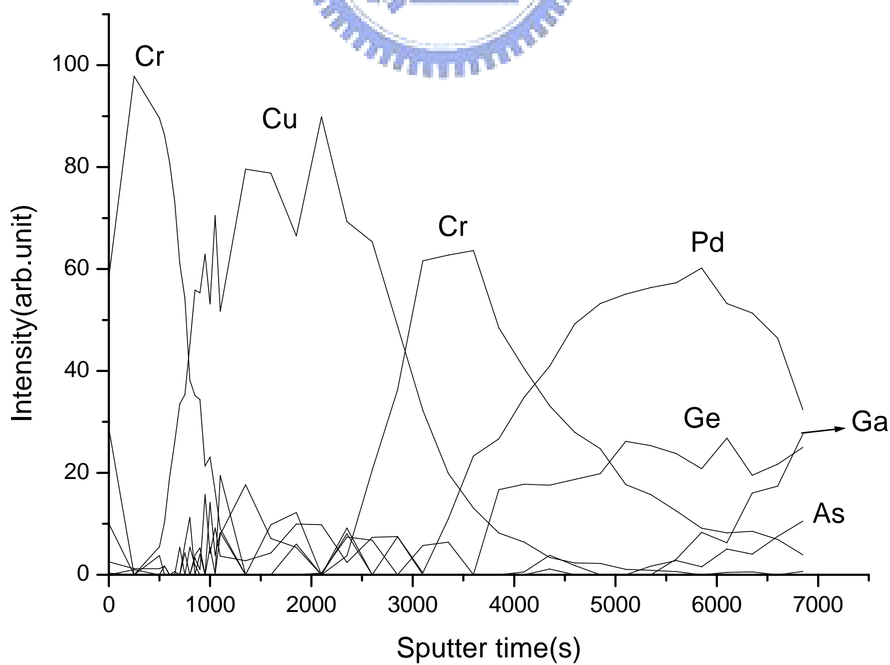
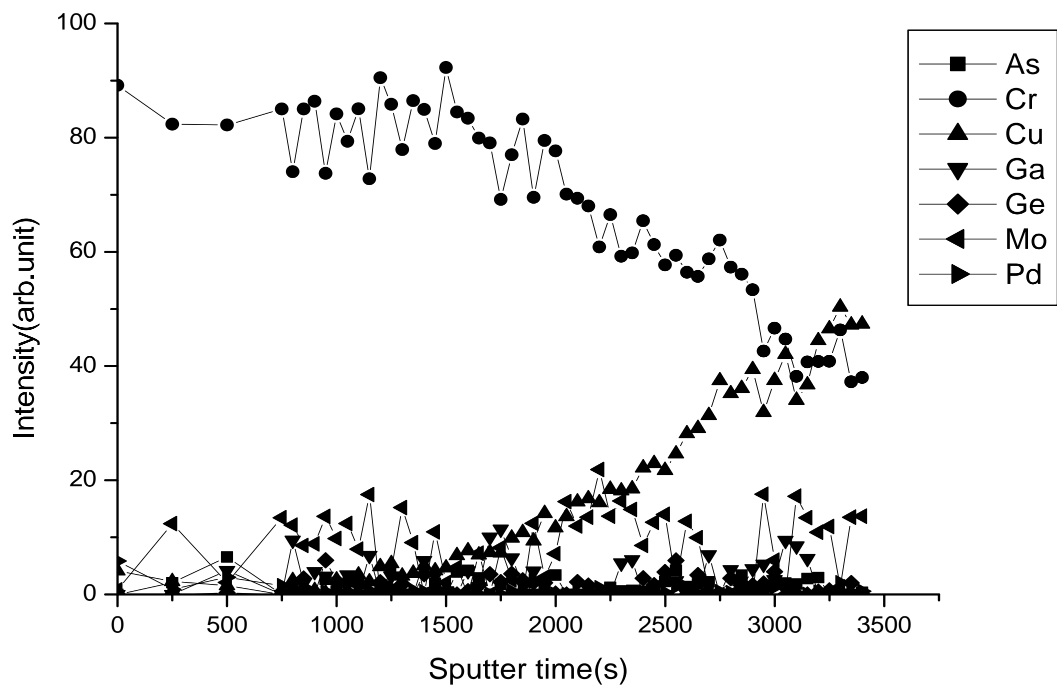


Fig4-3(d) Ohmic contact with Cr diffusion barrier annealed at 300°C for 1hr following 350°C 10min thermal treatment



1896

Fig-4.3(e) Ohmic contact with Mo diffusion barrier after 400°C 30min annealing

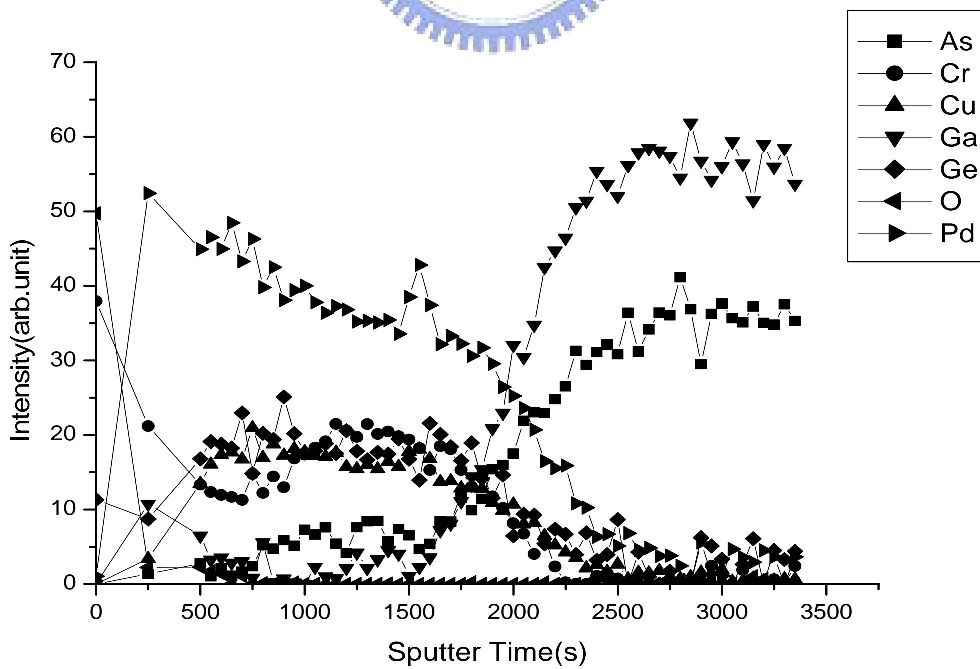


Fig-4.3(f) Ohmic contact with Cr diffusion barrier after 400°C 30min

annealing

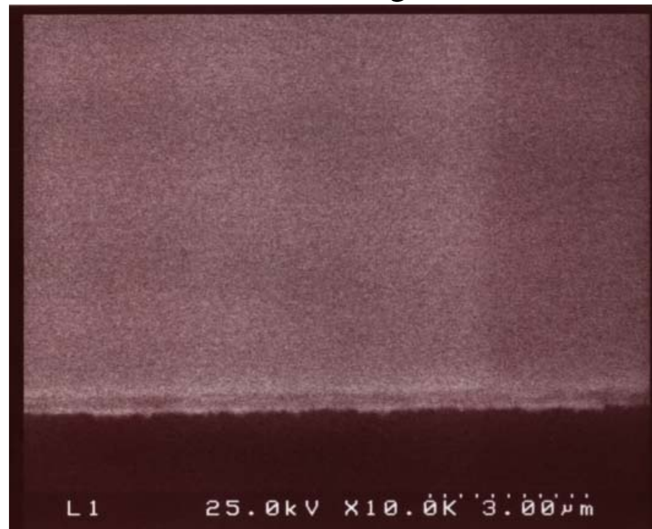


Fig-4.4 (a)Sample with Cr barrier after 300°C annealing for 30 minutes

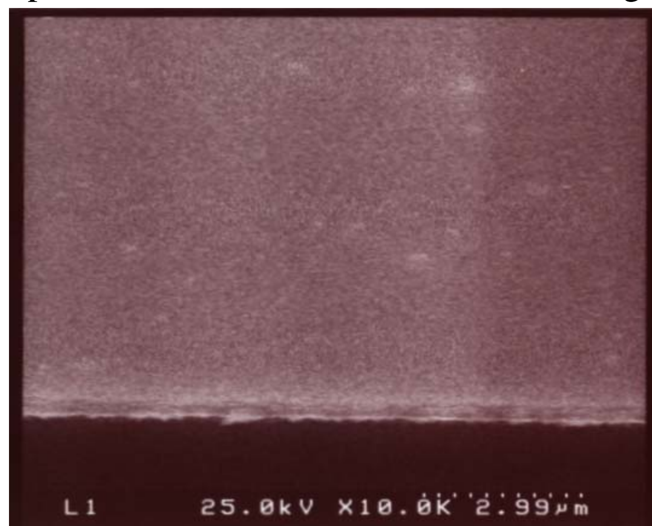


Fig-4.4(b) Sample with Cr barrier after 350°C annealing for 30 minutes

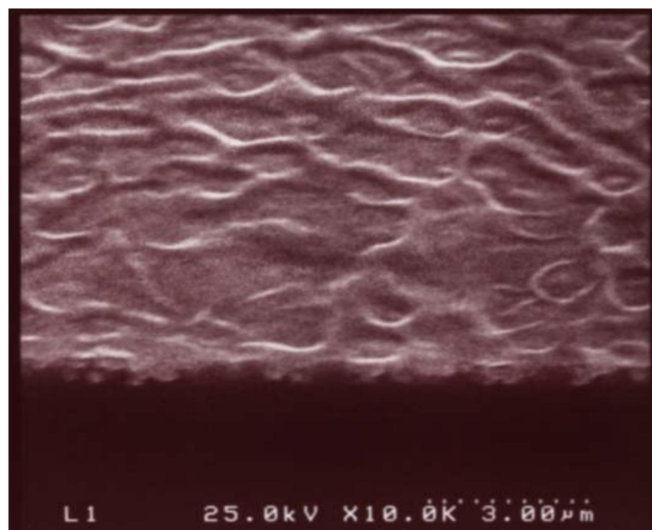


Fig-4.4(c) Sample with Cr barrier after 400°C annealing for 30 minutes

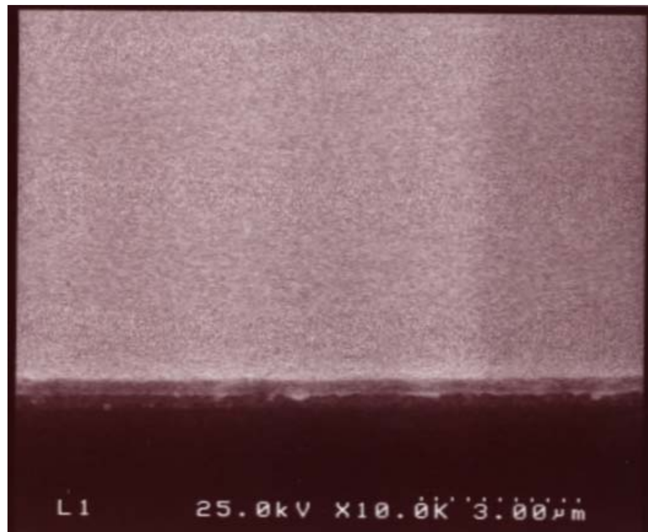


Fig-4.4(d) Sample with Mo barrier after 300°C annealing for 30 minutes

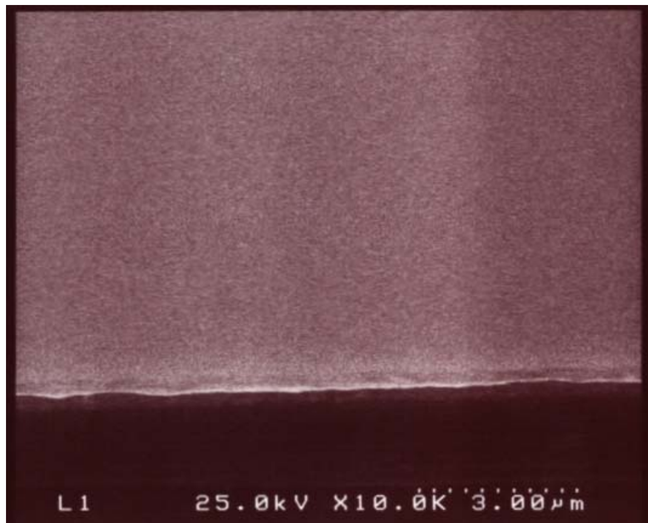


Fig-4.4(e) Sample with Mo barrier after 350°C annealing for 30 minutes

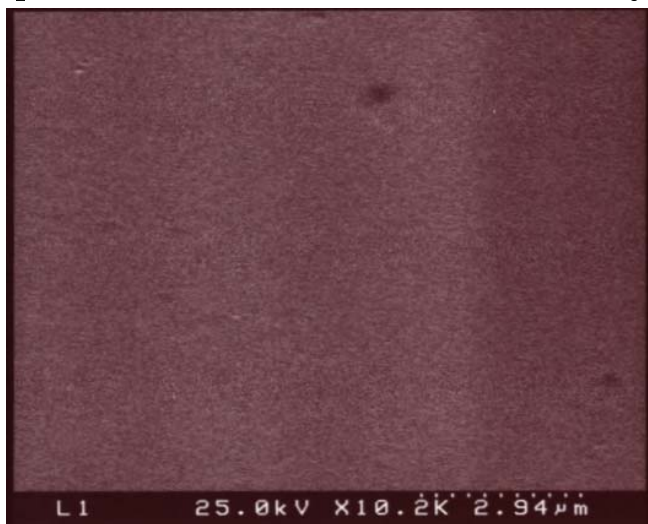


Fig-4.4(f) Sample with Mo barrier after 400°C annealing for 30 minutes

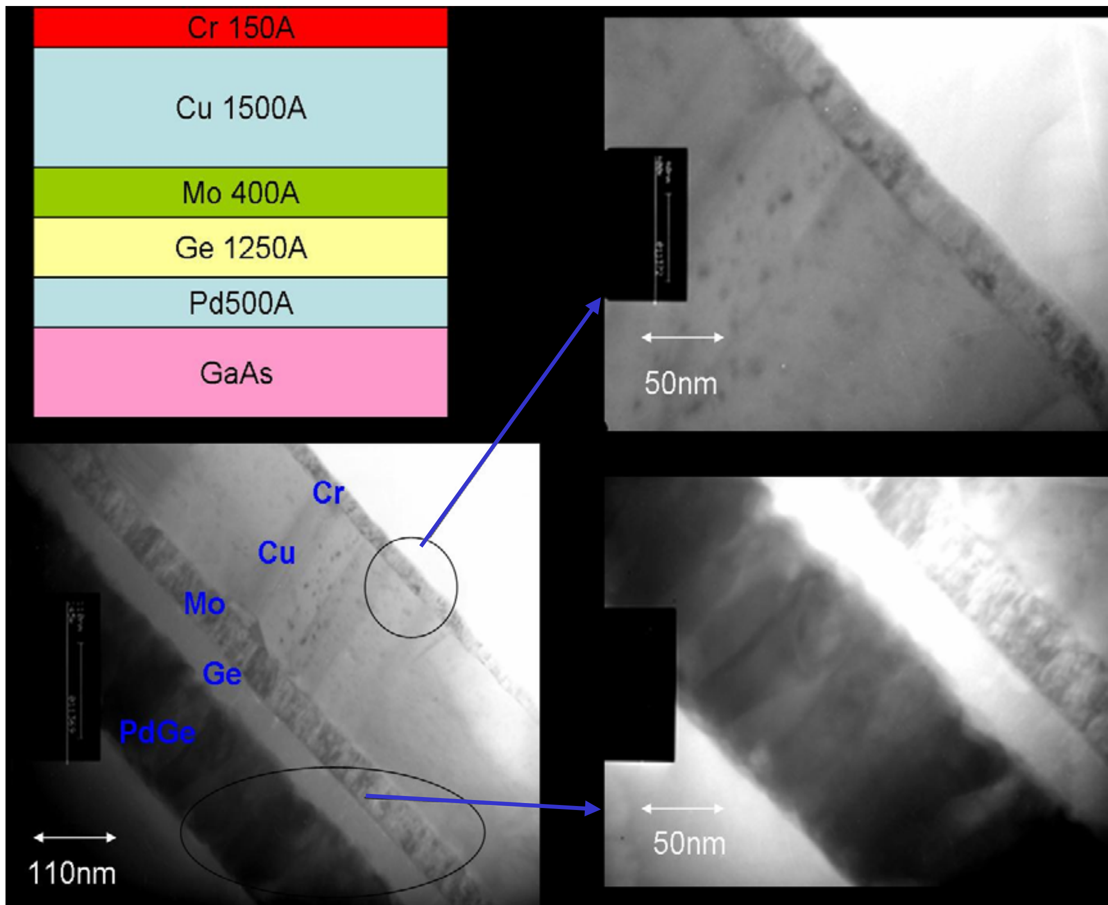


Fig-4.5(a) TEM Image of Mo barrier at 350^0C10min+300^0C1hr

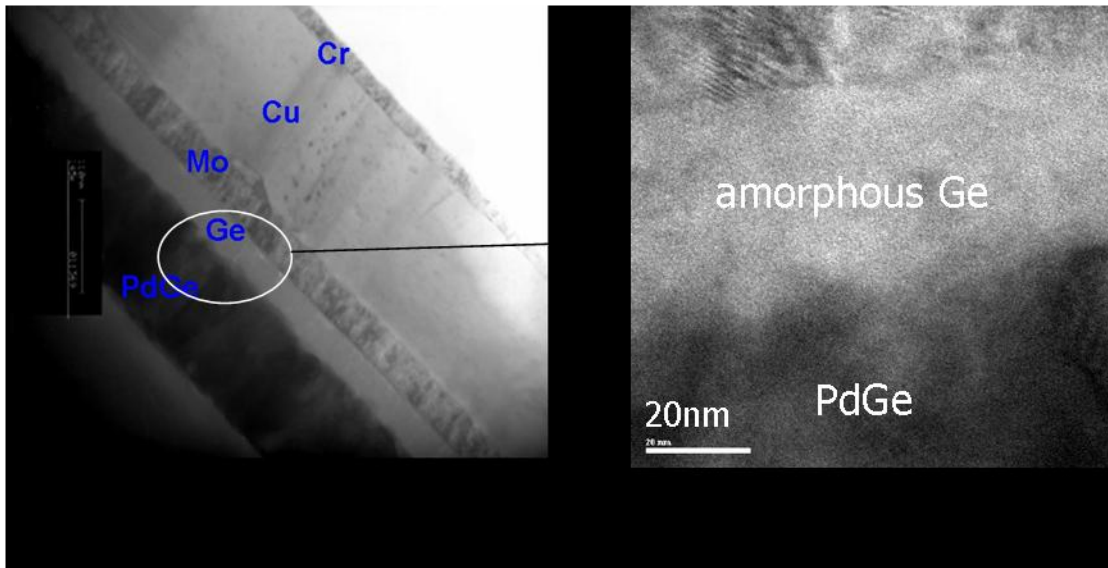


Fig-4.5(b) TEM Image of Mo barrier at 350^0C10min+300^0C1hr (High resolution)

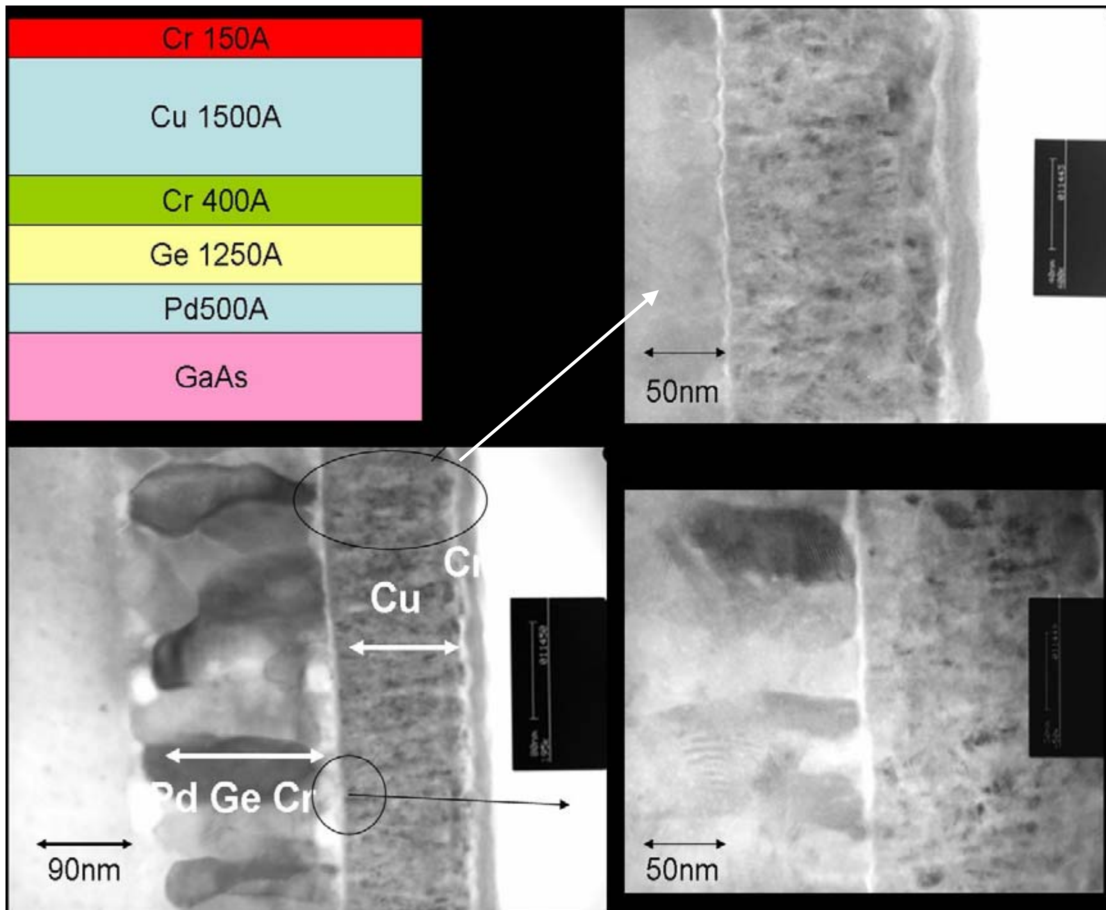


Fig-4.5(c) TEM Image of Cr barrier at 350^0C10min+300^0C1hr

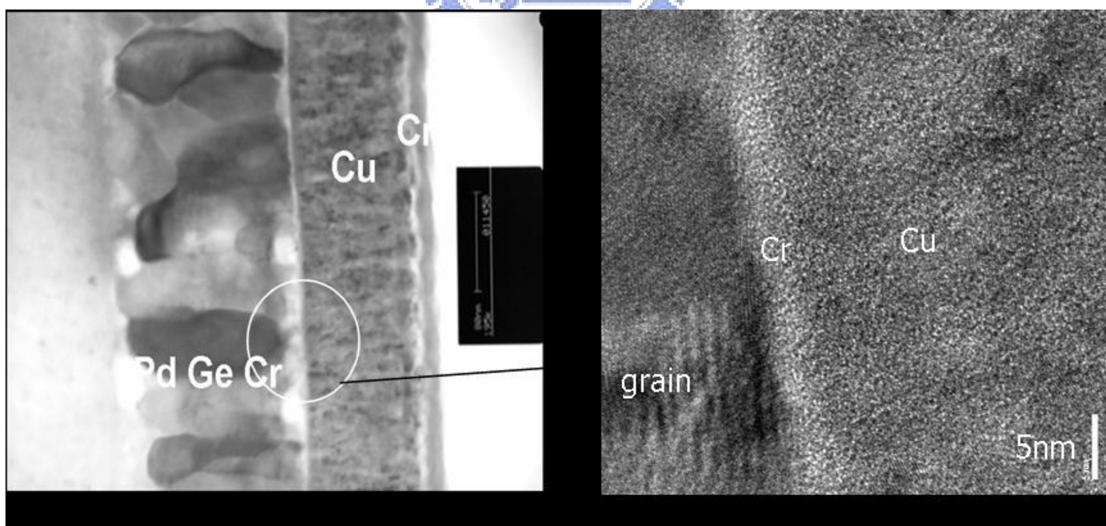
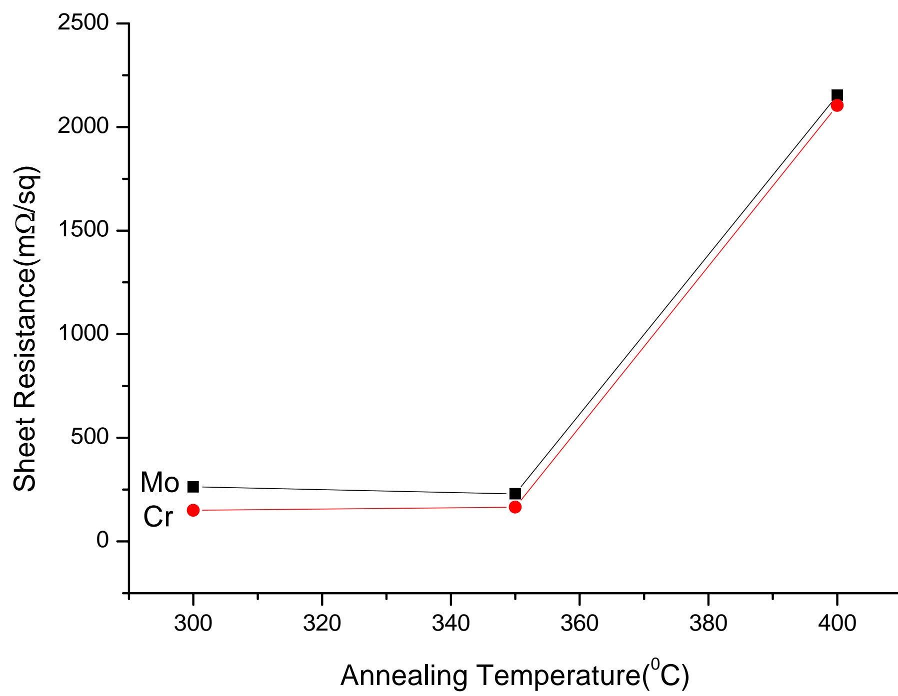


Fig-4.5(d) TEM Image of Cr barrier at 350^0C10min+300^0C1hr (High resolution)



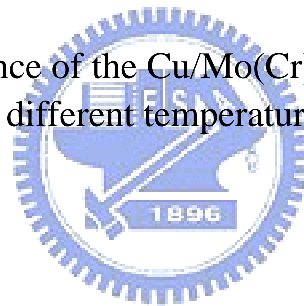


Fig-4.6 Sheet Resistance of the Cu/Mo(Cr)/Ge/Pd/GaAs Structure annealed at different temperatures for 30 min

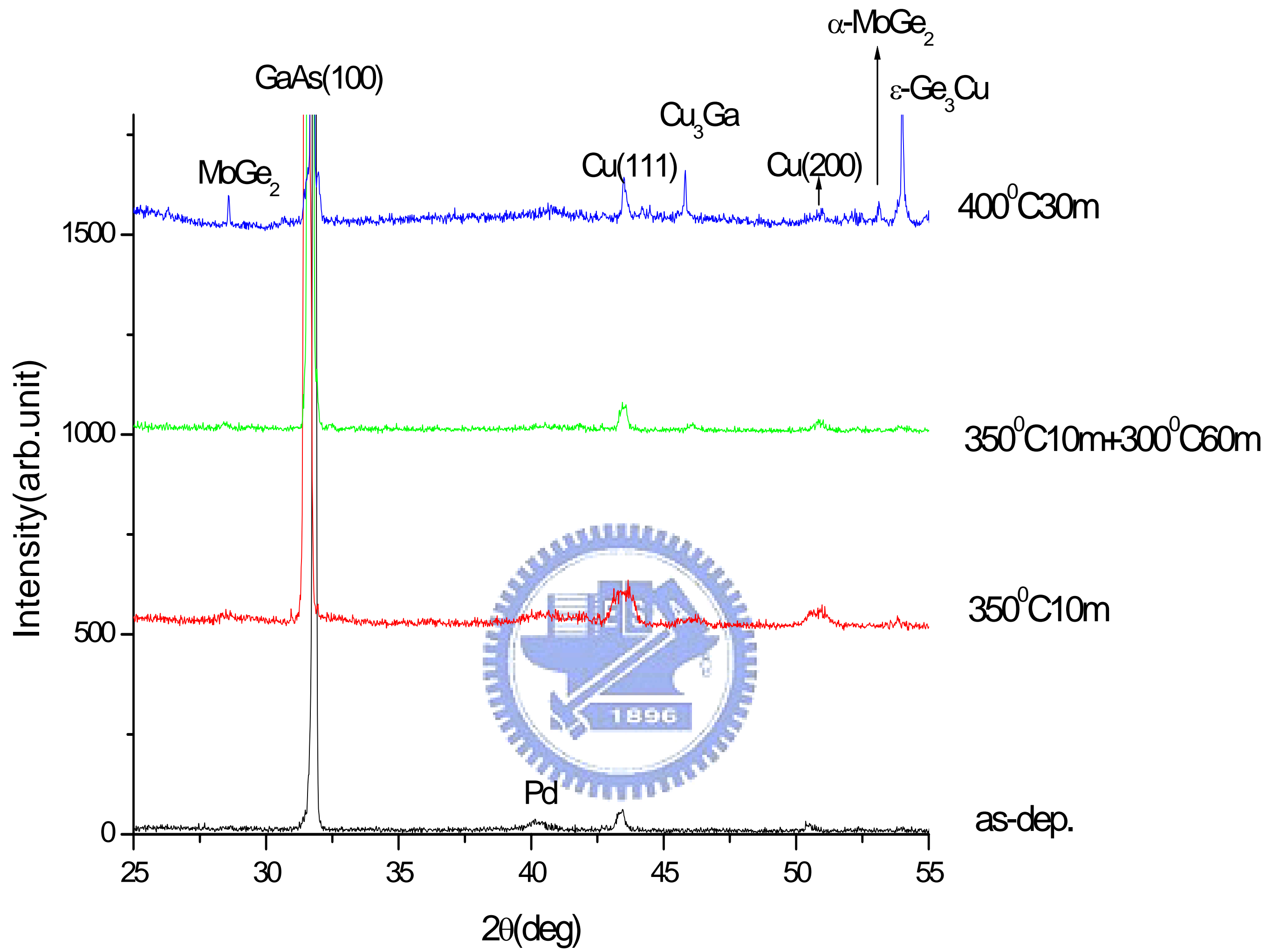


Fig-4.7(a) XRD results of the Cu/Mo/Ge/Pd/GaAs structure

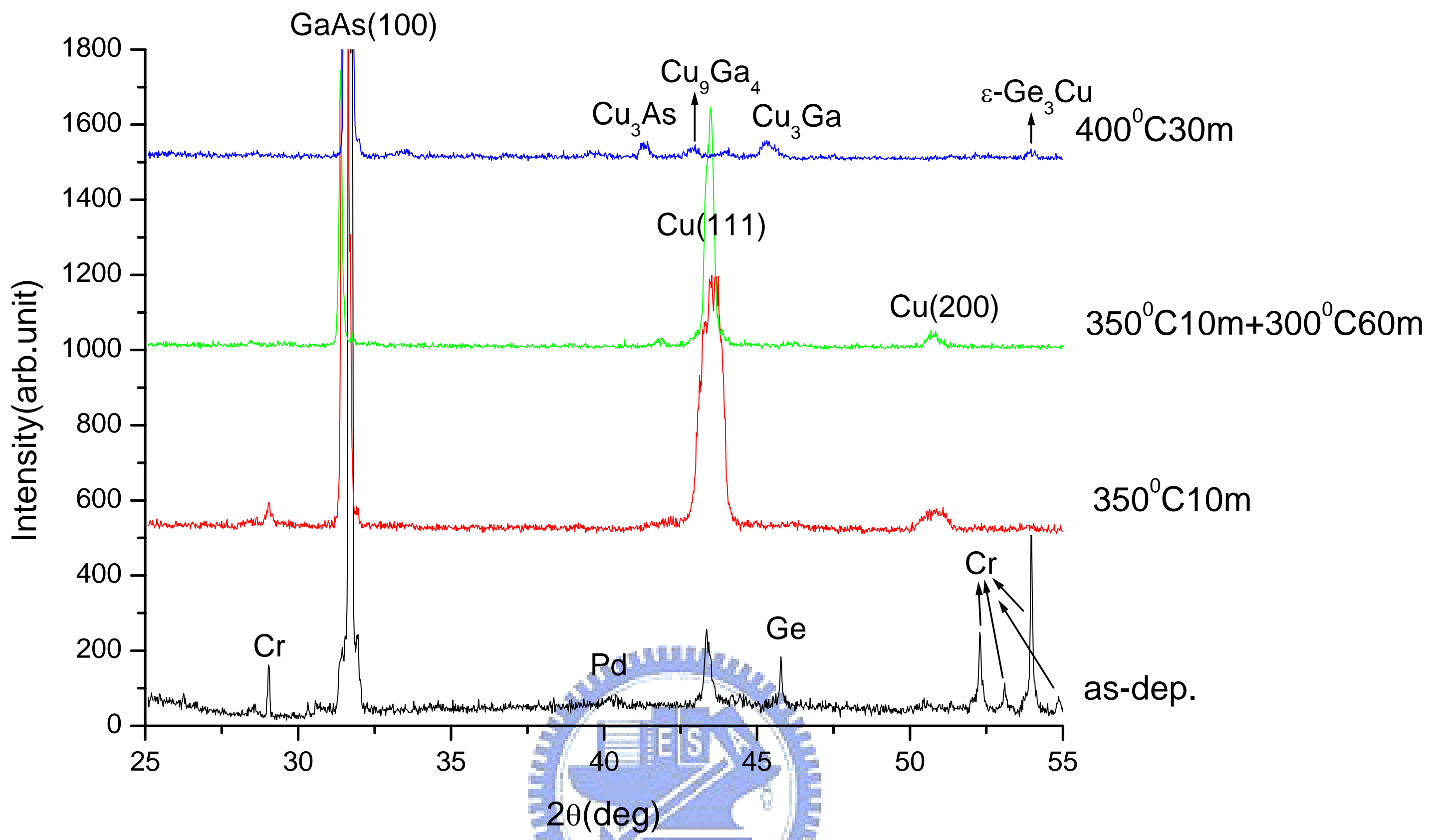
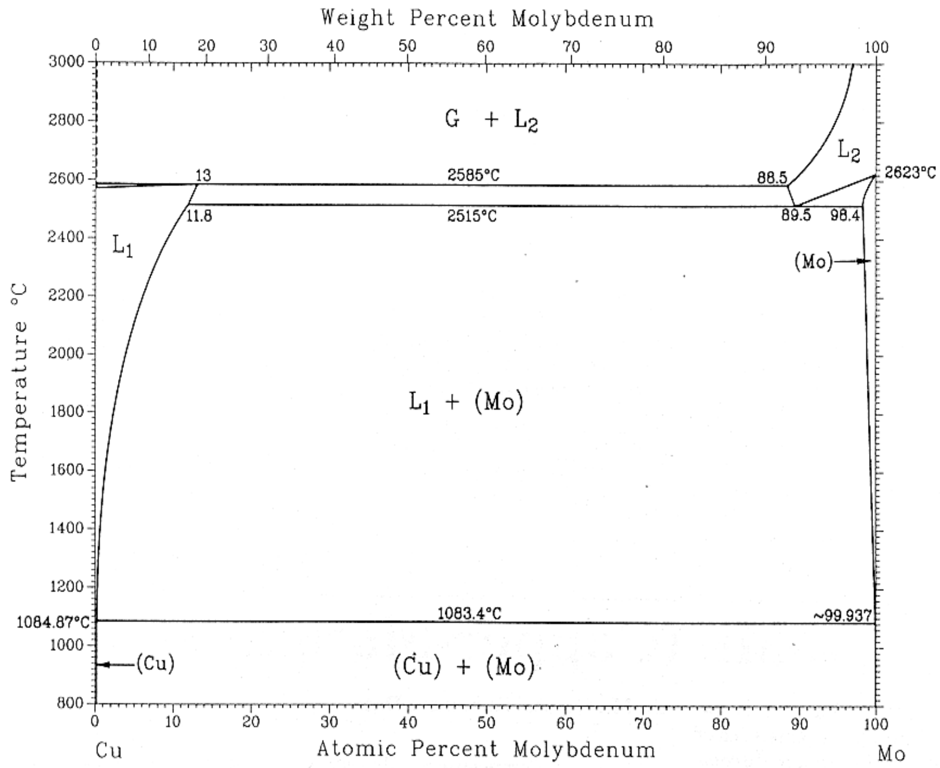
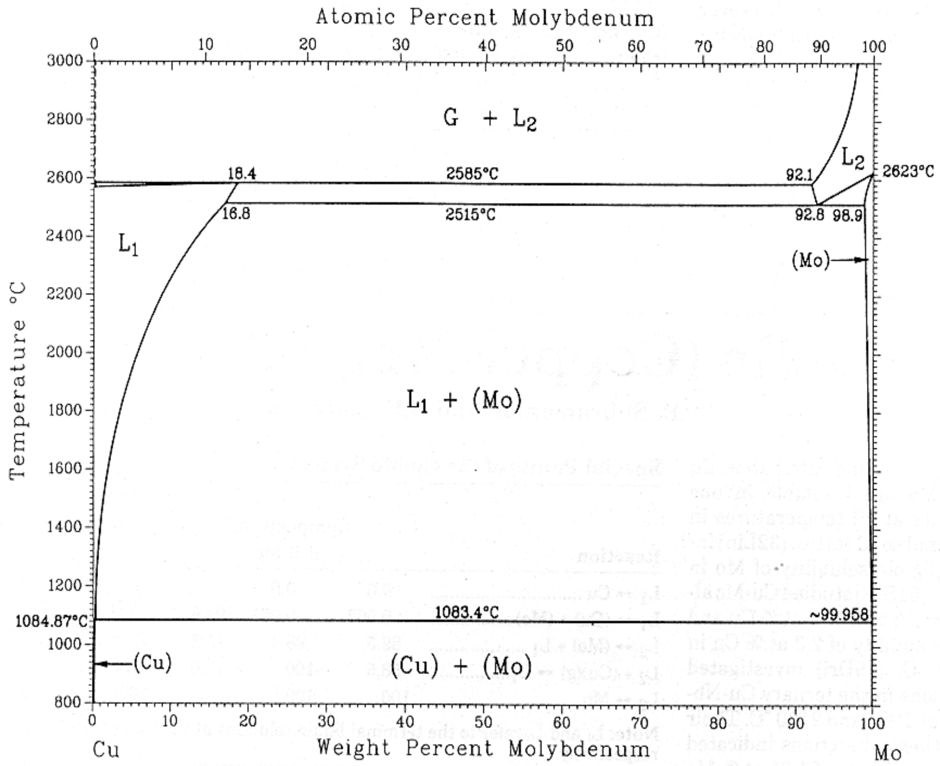


Fig-4.7(b) XRD Results of the Cu/Cr/Ge/Pd/GaAs Structure

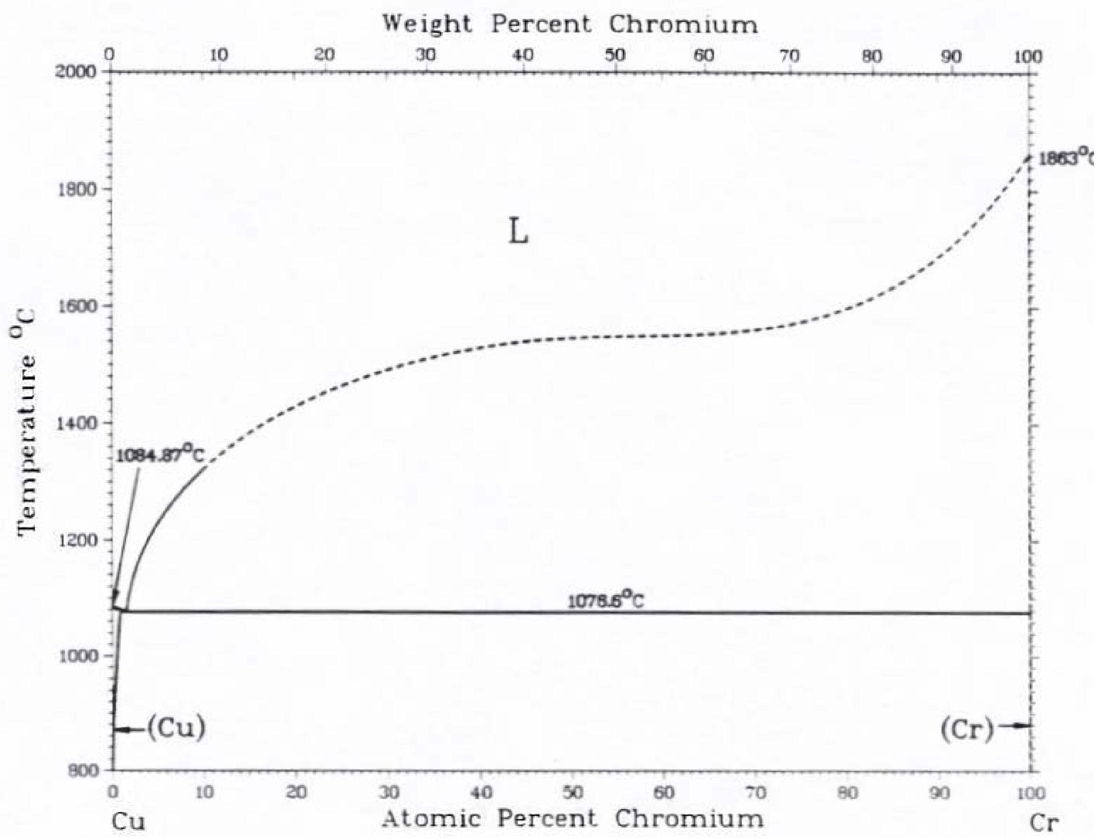
Cu-Mo Phase Diagram





P.R. Subramanian and D.E. Laughlin, 1990

Fig-4.8(a) Cu/Mo phase diagram. [38]



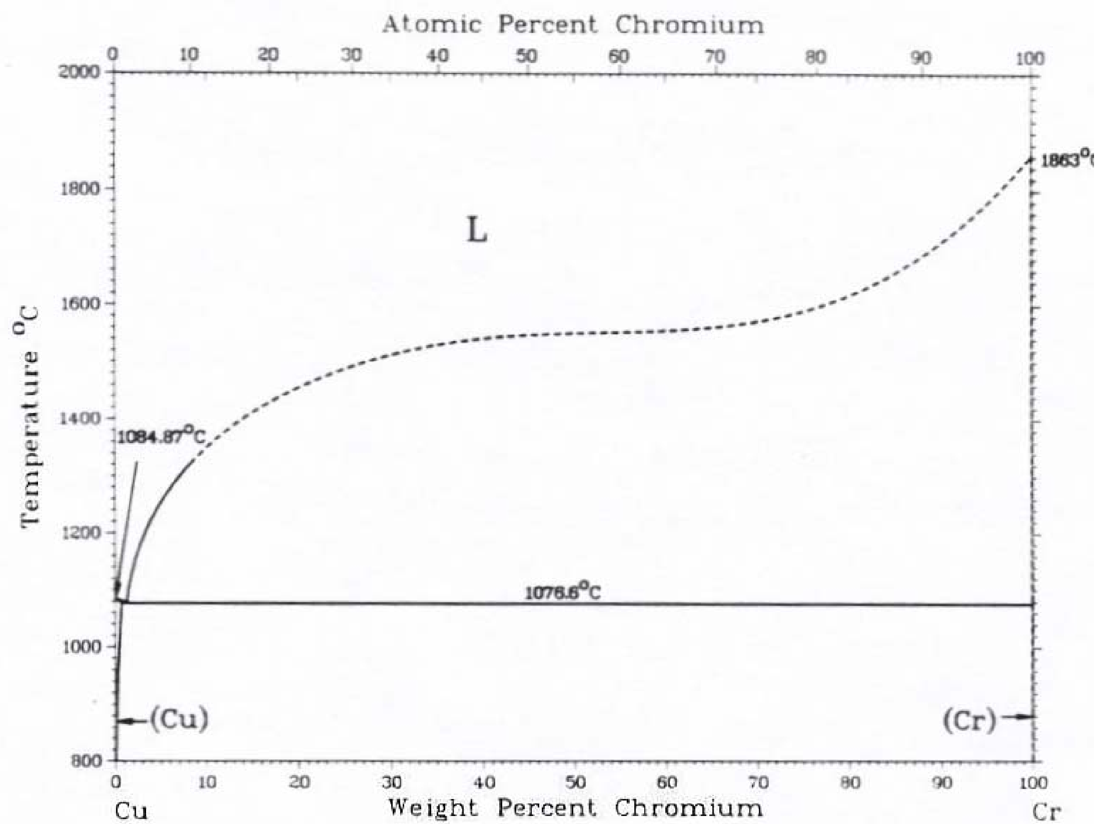
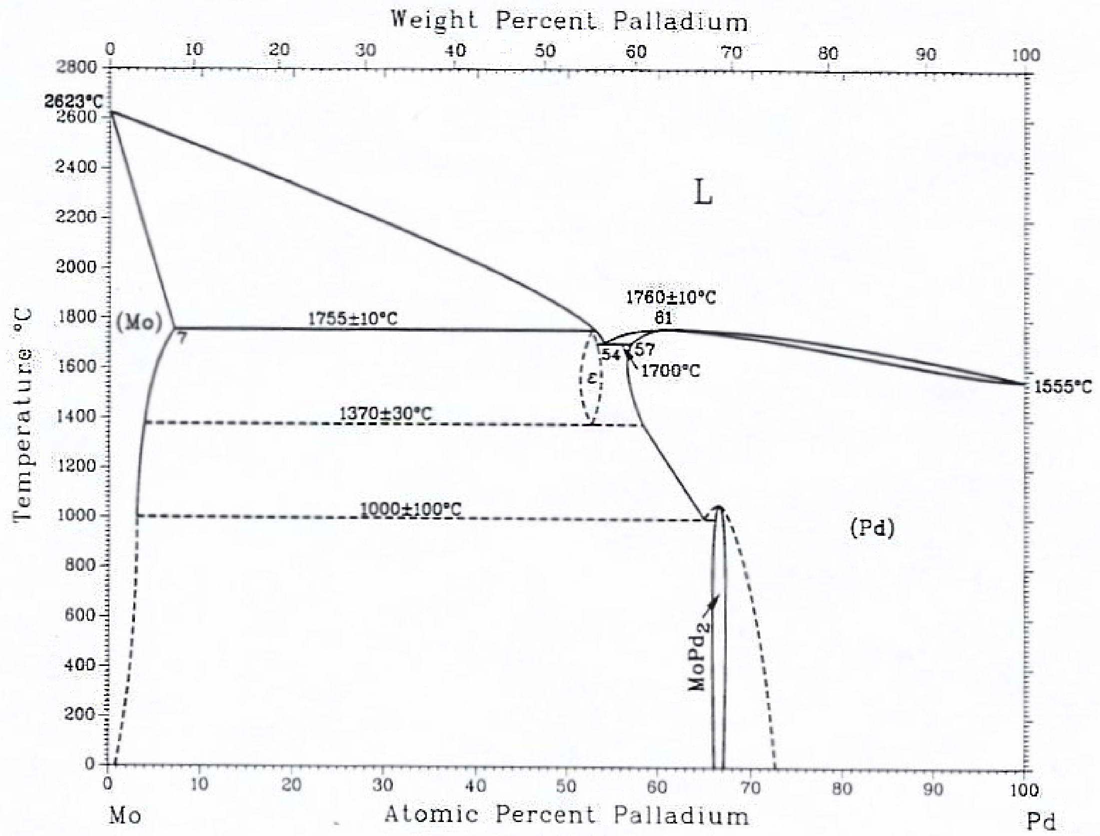


Fig-4.8(b) Cu/Cr phase diagram. [38]



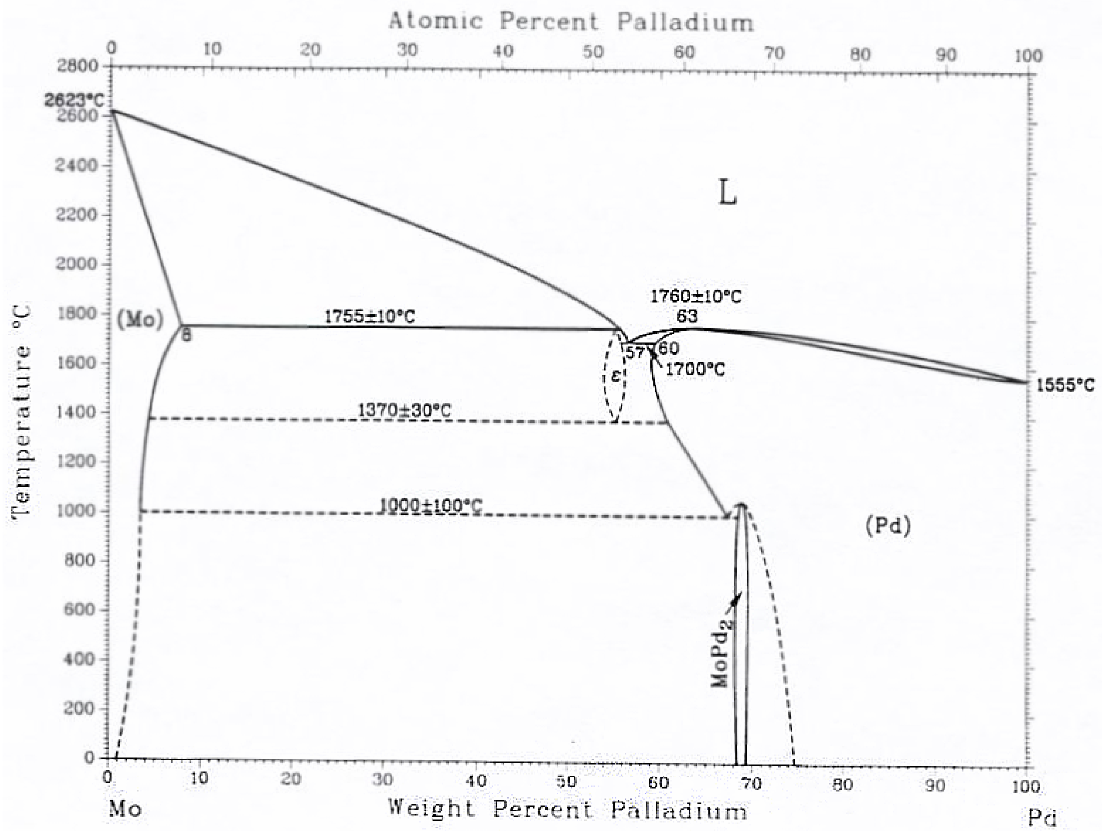
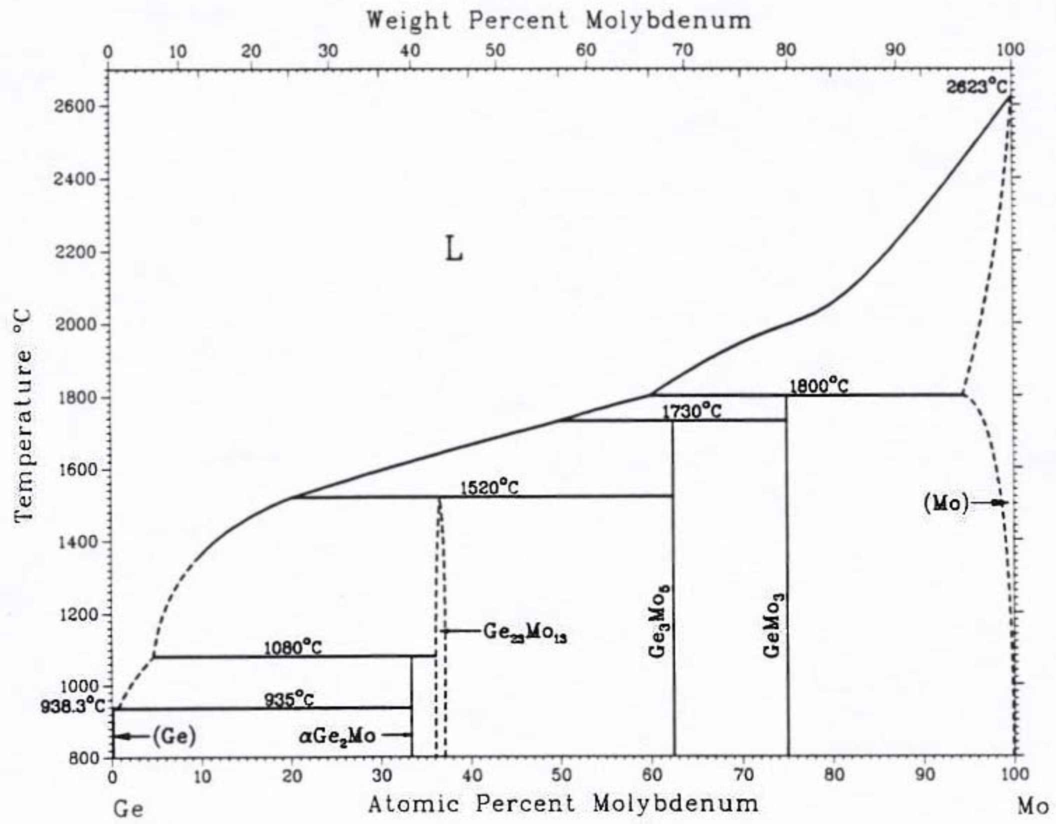


Fig-4.8(c) Mo/Pd phase diagram. [38]



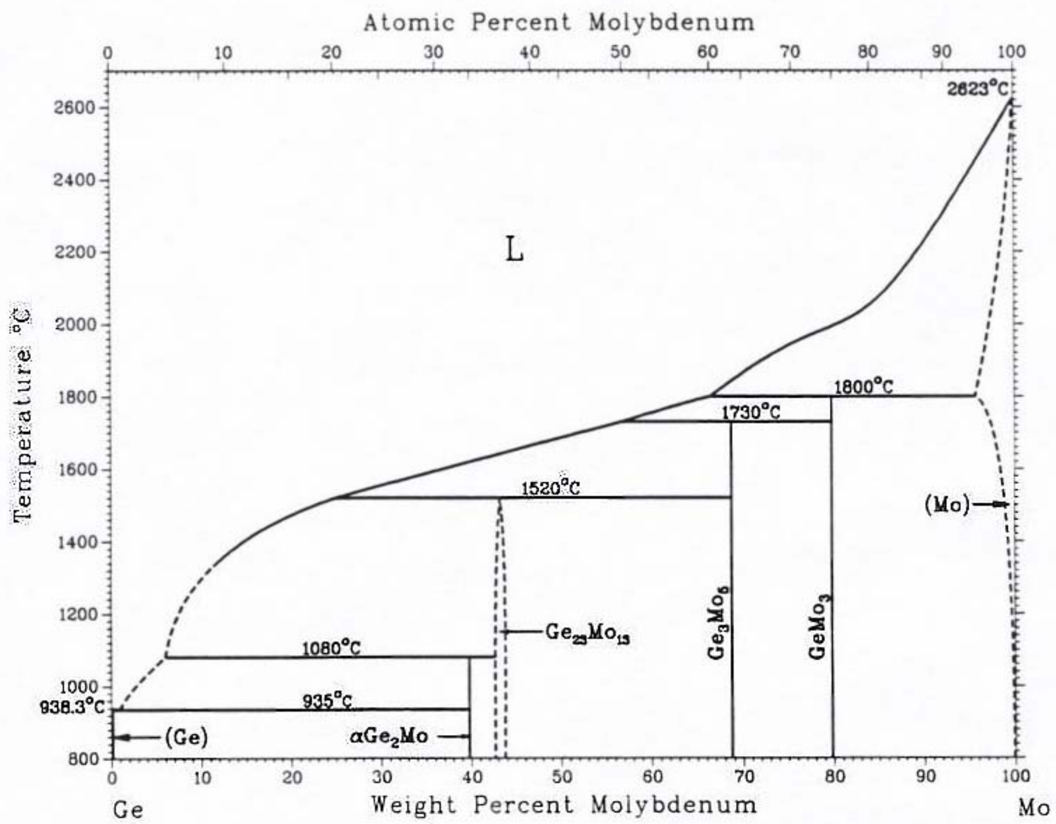
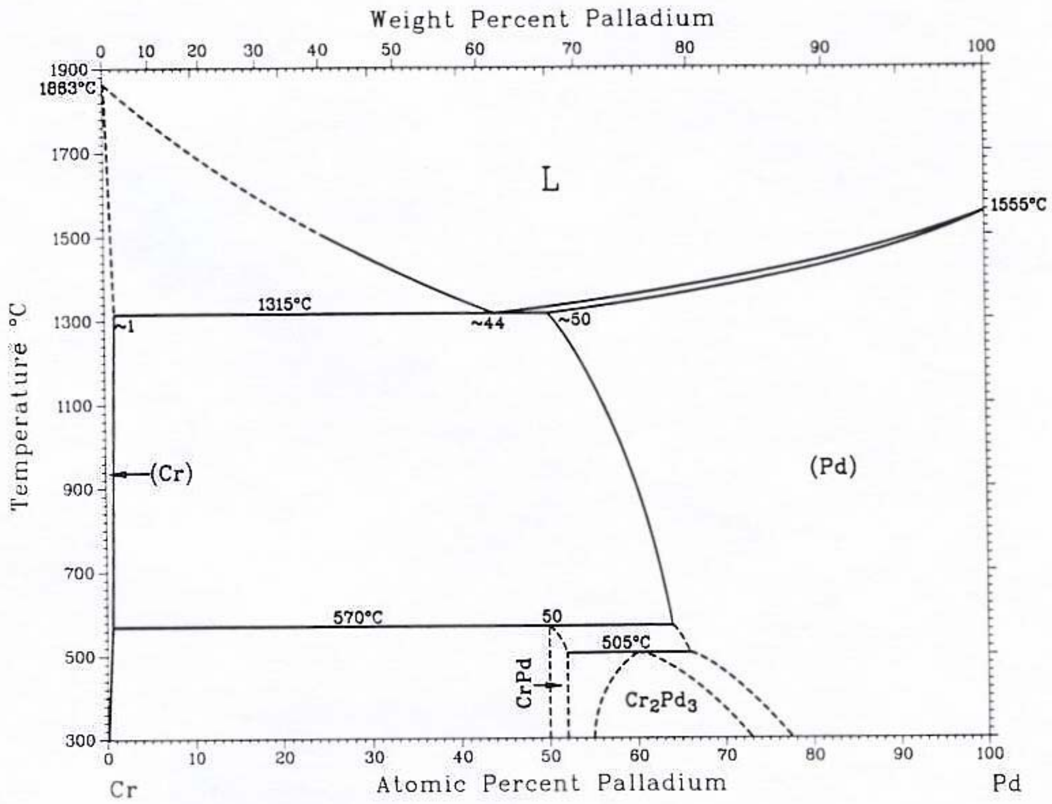


Fig-4.8(d) Mo/Ge phase diagram. [38]



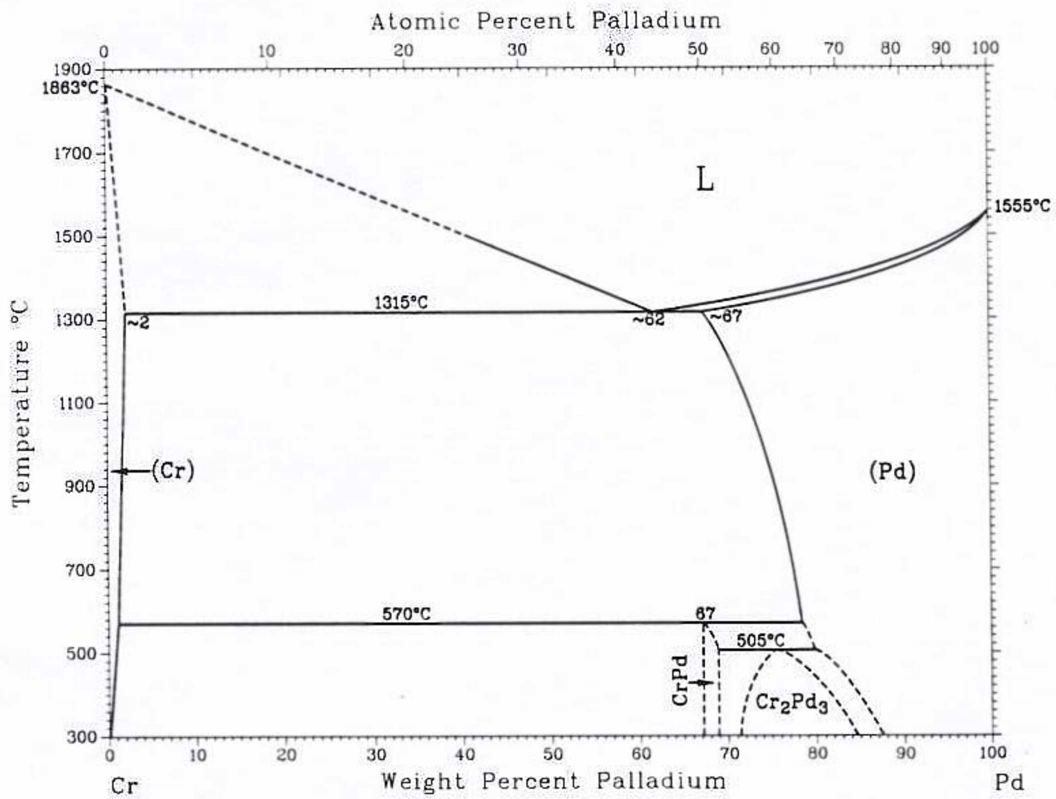
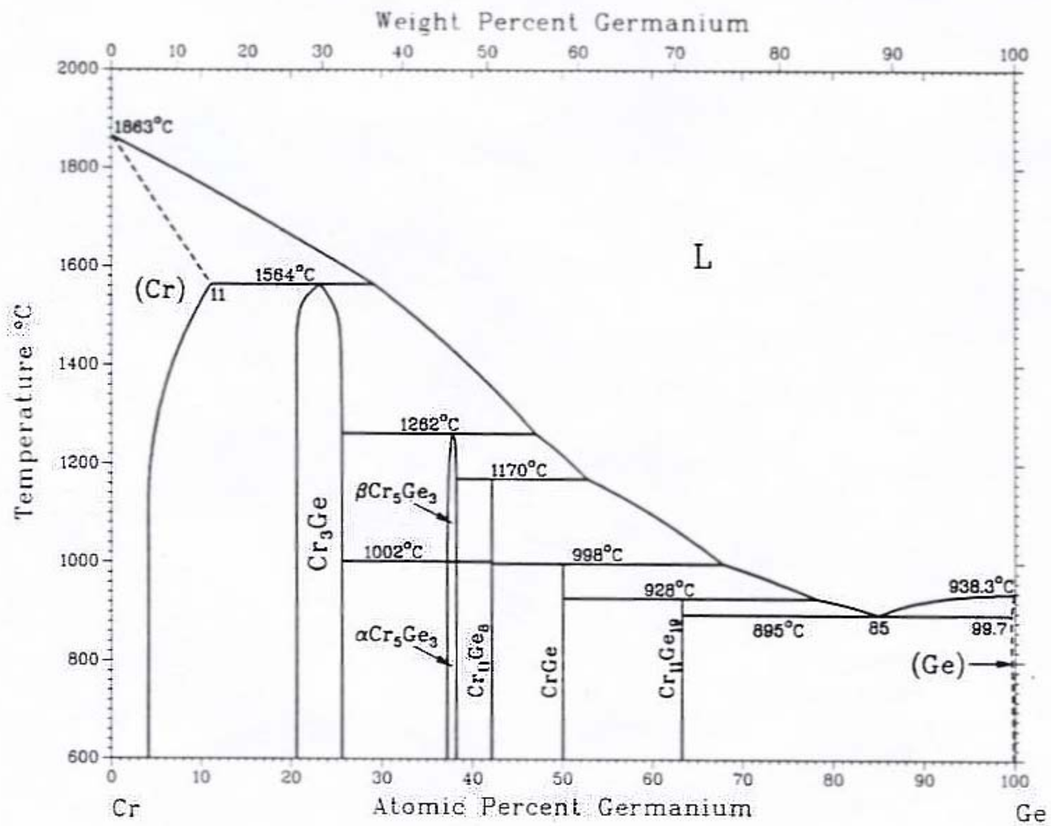


Fig-4.8(e) Cr/Pd phase diagram. [38]



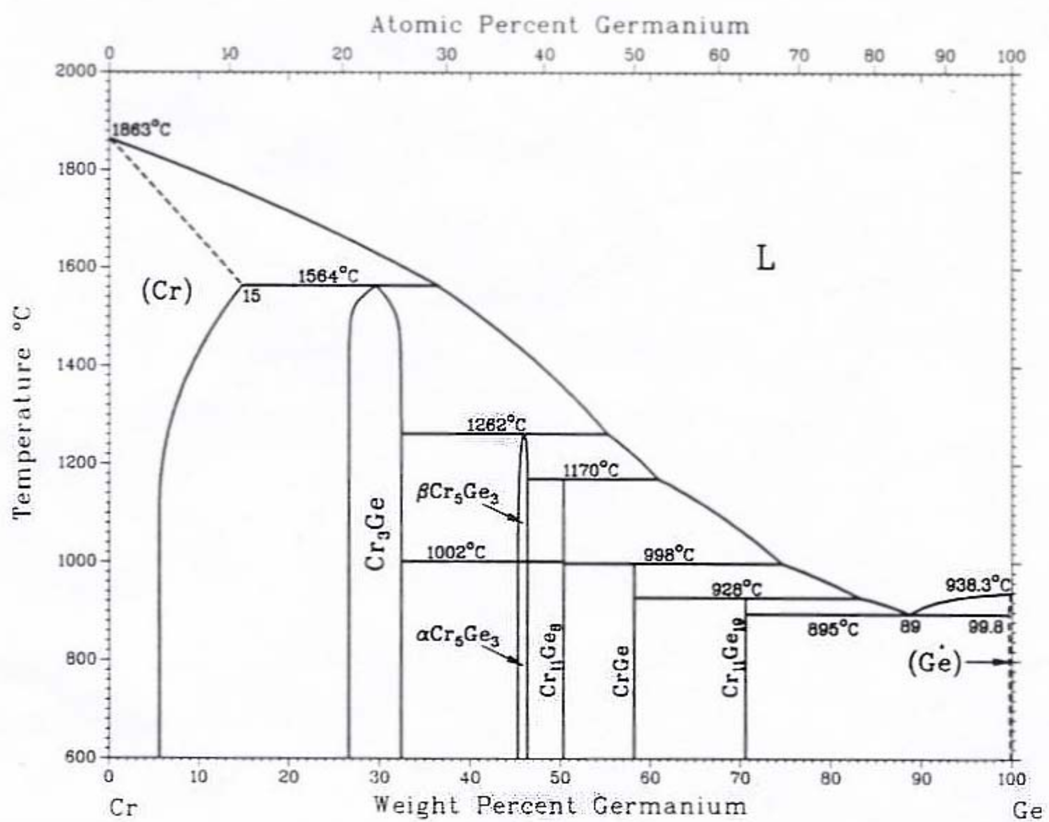


Fig-4.8(f) Cr/Pd phase diagram. [38]

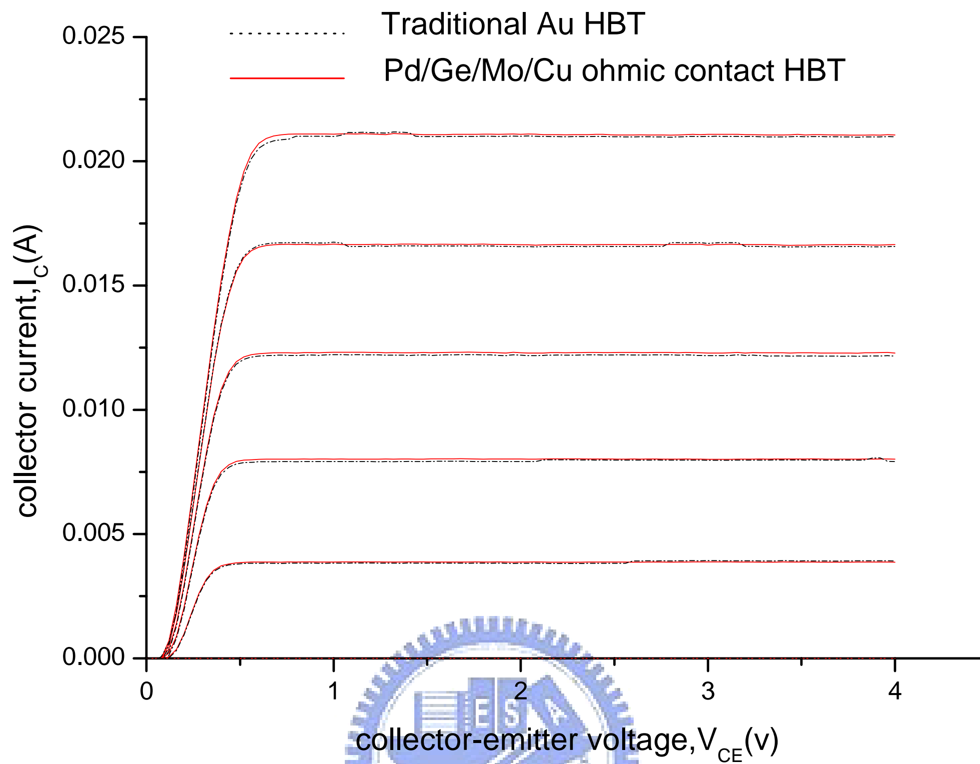


Fig-4.9(a) Common emitters I-V curve

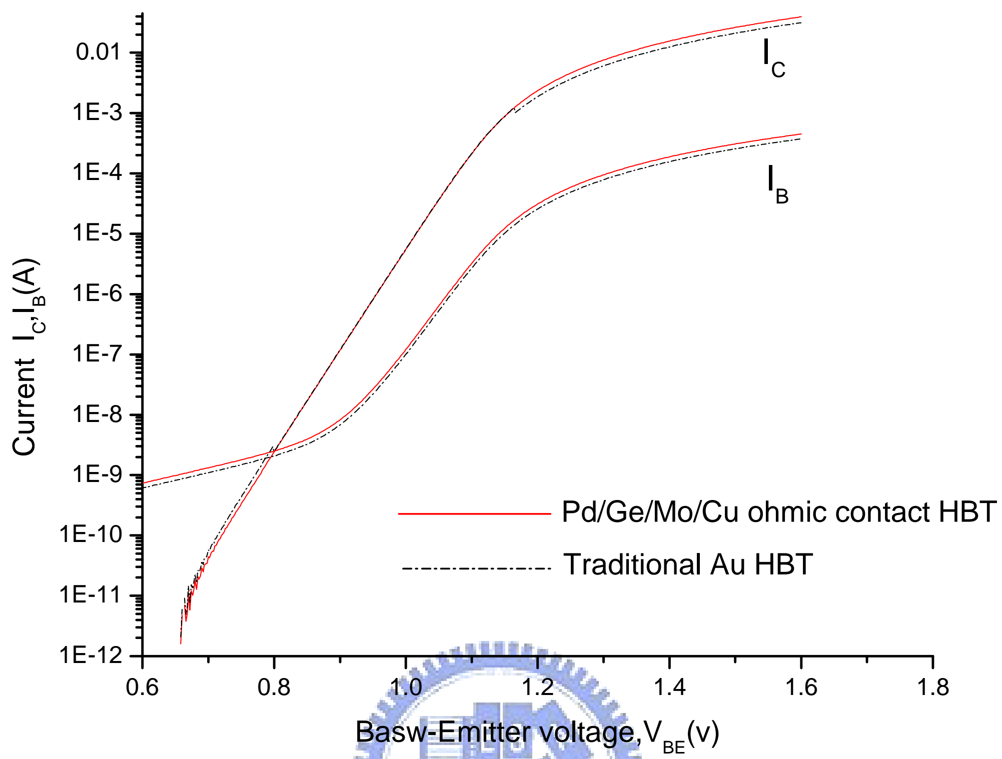


Fig-4.9(b) Gummel plot

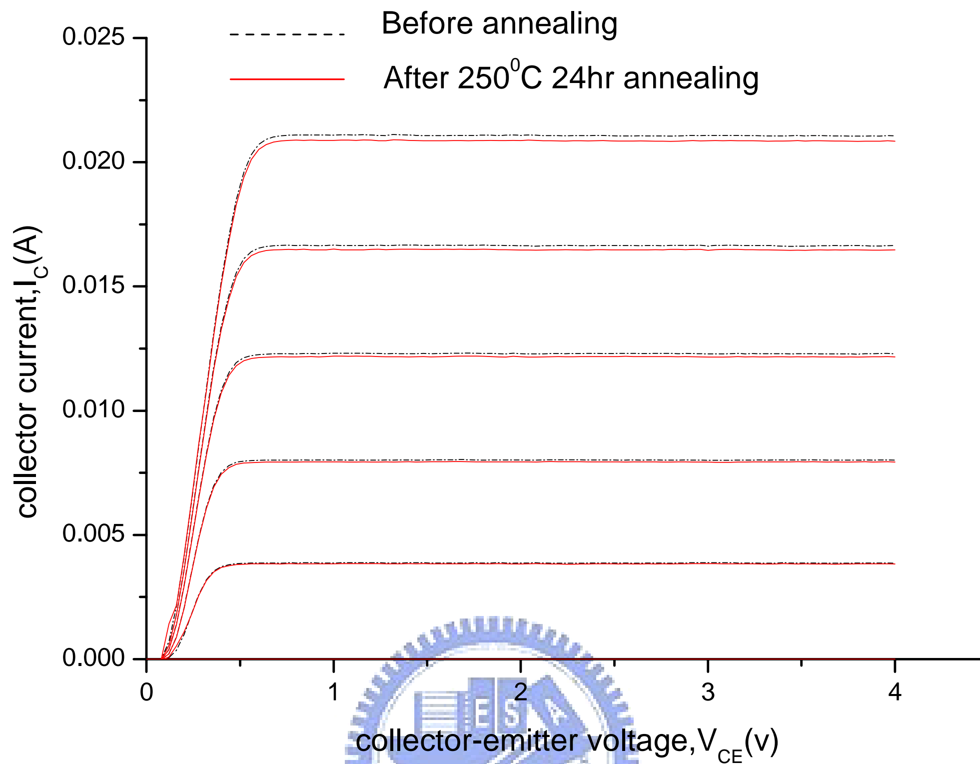


Fig-4.9(c) Common emitters I-V curve

Chapter 5

Conclusion

The Pd/Ge/Mo(Cr)/Cu ohmic structure showed the lowest contact resistance after 350 °C annealing for 10 minutes. In thermal stability test, the contact resistance with Mo diffusion barrier was stable up to 300°C annealing for 20 hours, while the contact resistance of the contact with Cr as the diffusion barrier changes drastically after 300 °C 20 hours annealing. Both of these two structures failed after 400 °C annealing for 30 minutes. This phenomenon can be explained by material analysis.

Copper metallized ohmic contact with Mo as the diffusion barrier was successfully applied to the InGaP/GaAs HBTs, and the results of the device electrical characteristics were comparable to the tradition Au metallized HBT. In thermal stability test, the Pd/Ge/Mo/Cu ohmic contact device with SiO_2 passivation showed very little degradation after 250 ^{o}C annealing for 24 hours. InGap/GaAs HBT with Pd/Ge/Mo/Cu as the n-type ohmic contact metals was also successful fabricated and demonstrated in this study.

REFERENCES

[1] K. Holloway and P. M. Fryer, “Tantalum as a diffusion barrier between copper and silicon,” *Appl. Phys. Lett.*, vol. 57, no. 17, pp. 1736–1738, Oct. 22, 1990.

[2] D. Gupta, “Diffusion in several materials relevant to Cu interconnection technology,” *Mater. Chem. Phys.*, vol. 41, pp. 199–205, 1995.

[3] D. J. Kim and Y. T. Kim, “Nanostructured Ta-Si-N diffusion barriers for Cu metallization,” *J. Appl. Phys.*, vol. 82, no. 10, pp. 4847–4851,Nov.15, 1997.

[4] E.R.Weber, “Transition metals in silicon,” Appl. Phys.A, Solid Surf.,vol. 1,pp. 1-22,1983

[5] Y.K Lee and Khin Maung Latt, *Material Sci. in Semiconductor Processing,* 3, 179(2000).

[6] K. Holloway, P.M. Fryer and C. Cabral, *J. Appl. Phys.,* 71, 5433(1992).

[7] P. Catania, J.P. Doyle, and J. J. Cuomo, *J. Vac. Sci. Technol.* A, 10,3318(1992).

[8] C. A. Chang, *J. Appl. Phys*.,67,7348(1990).

[9] E. Kolawa, J.S. Chen and J.S.Reid, *J. Appl. Phys*.,70,1369(1991).

[10] J. O. Olowolafe and C. J. Mogab, *Thin Solid Films*, 277, 377(1993)

[11] H. Ono, T. Nakano and T. Ohta, *Appl. Phys. Lett*.,64,1511(1994)

[12] T. Laurila, K. Zeng, J.K. Kivilahti, J. Molarius and I. Suni, *Thin Solid Films*, 373, 64(2000)

[13] M. Stavrev, C. Wenzel, A. Möller and K. Drescher, *Appl. Surf. Sci.*,91,257(1995)

[14] S.-Q. Wang, Ivo Raaijmakers and B. J. Brown, *J. Appl. Phys*.,68,5176(1990)

[15] Dong-Jin Kim, Young-Bae Jong and Myoung-Bok Lee, *Thin Solid Films*, 372,276(2000)

[16] Masak Uekubo, T. Oku, K. Nii and M. Murakami, *Thin Solid Films,* 286, 170(1996)

[17] S. C. Sun, M. H. Tasi, *Symposium on VLSI Technology Digest of Technology Papers,* 46(1996)

[18] Dong Joon Kim and Yong Tae Kim, *J. Appl. Phys*.,82,4847(1997)

[19] Paul Werbaneth, Zia Hasan, Paritosh Rajora, and Mark Rousey-Seidel, (Tegal Corporation), "The Reactive Ion Etching of Au on GaAs Substrates in a High Density Plasma Etch Reactor", *The International Conference on Compound Semiconductor Manufacturing Technology,* Gaasmantech On-line Digest, (12), 1999, pp. 1-4

[20] S.-Q. Wang, S. Suthar, C. Hoeflich, and B. J. Burrow, *J. of Appl. Phys.* **73** (5), 1993,pp.2301–2321

[21] J. O. Olowolafe, J. Li, J. W. Mayer, and E. G. Colgan, *Appl. Phys. Lett.* **58** (5), 1991, pp.469–471

[22] D.-H. Kim, S.-L. Cho, K.-B. Kim, J. J. Kim, J. W. Park, and J. J. Kim, *Appl. Phys. Lett.* **69** (27), 1996, pp.4182–4184

[23] H. Ono, T. Nakano, and T. Ohta, *Appl. Phys. Lett.* **64** (12),1994, pp.1511–1513.

[24] K. Holloway, P. M. Fryer, C. Cabral, Jr., J. M. E. Harper, P. J.

Bailey, and K. H. Kelleher, *J. Appl. Phys.* **71** (11), 1992, pp.5433–5443

[25] M. Takeyama, A. Noya, T. Sase, A. Ohta, and K. Sasaki, *J. of Vacuum Science & Technology B (Microelectronics and Nanometer Structures)* **14** (2), 1996, pp.674–678

[26] E. Kolawa, J. S. Chen, J. S. Reid, P. J. Pokela, and M.-A. Nicolet, *J. of Appl. Phys.* **70** (3), 1991, pp.1369–1373

[27] T. Oku, M. uekubo, E. Kawakami, K. Nii, T. Nakano, T. Ohta, and M. Murakami, in 1995, *IEEE VMIC Conf.*, pp. 182–185.

[28] J. P. Lu, Q. Z. Hong, W. Y. Hsu, G. A. Dixit, V. Cordasco, S. W. Russell, J. D. Lutttner, R. H. Havemann, L. K. Magel, and H. L. Tsai, *in Advanced Metallization and Interconnect Systems for ULSI Applications* (Oct. 1997).

[29] S.-Q. Wang, S. Suthar, C. Hoeflich, and B. J. Burrow, *J. of Appl. Phys.* **73** (5), 1993,pp.2301–2321

[30] J. O. Olowolafe, J. Li, J. W. Mayer, and E. G. Colgan, *Appl. Phys. Lett.* **58** (5), 1991, pp.469–471

[31] D.-H. Kim, S.-L. Cho, K.-B. Kim, J. J. Kim, J. W. Park, and J. J. Kim, *Appl. Phys. Lett.* **69** (27), 1996, pp.4182–4184

[32] H. Ono, T. Nakano, and T. Ohta, *Appl. Phys. Lett.* **64** (12),1994, pp.1511–1513.

[33] K. Holloway, P. M. Fryer, C. Cabral, Jr., J. M. E. Harper, P. J. Bailey, and K. H. Kelleher, *J. Appl. Phys.* **71** (11), 1992, pp.5433–5443

[34] M. Takeyama, A. Noya, T. Sase, A. Ohta, and K. Sasaki, *J. of Vacuum Science & Technology B (Microelectronics and Nanometer*

Structures) **14** (2), 1996, pp.674–678

[35] E. Kolawa, J. S. Chen, J. S. Reid, P. J. Pokela, and M.-A. Nicolet, *J. of Appl. Phys.* **70** (3), 1991, pp.1369–1373

[36] T. Oku, M. uekubo, E. Kawakami, K. Nii, T. Nakano, T. Ohta, and M. Murakami, in 1995, *IEEE VMIC Conf.*, pp. 182–185.

[37] J. P. Lu, Q. Z. Hong, W. Y. Hsu, G. A. Dixit, V. Cordasco, S. W. Russell, J. D. Lutttner, R. H. Havemann, L. K. Magel, and H. L. Tsai, *in Advanced Metallization and Interconnect Systems for ULSI Applications* (Oct. 1997).

[38] Massalski T. B., and Thaddeus B.: '*Binary phase diagrams*', Metals Park, Ohio, 1986.