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On Reducing Test Power and Test Volume by Selective Pattern Compression Schemes

Chia-Yi Lin, Hsiu-Chuan Lin, and Hung-Ming Chen

***Abstract*—In modern chip designs, test strategies are becoming one of the most important issues due to the increase of the test cost, among them we focus on the large test power dissipation and large test data volume. In this paper, we develop a methodology to suppress the test power to avoid chip failures caused by large test power, and our methodology is also effective in reducing the test data volume and shift-in power. The proposed schemes and techniques are based on the selective test pattern compression, they can reduce considerable shift-in power by skipping the switching signal passing through long scan chains. The experimental results with ISCAS89 circuits demonstrate that our methodology can achieve significant improvement in the reduction of shift-in power and test data volume. Our approach also supports multiple scan chains.**

***Index Terms*—Compression, DFT, low power, scan chain, test data volume.**

I. Introduction

The rapid increase of chip design technology leads a dramatic growth of scan cells. It makes the large scale chip designs require larger test data volume and longer scan chains. In order to reduce the test data volume, researchers are actively pursuing new solutions to test data compression. On the other hand, the large number of scan cells may generate a huge number of switching activities in the test mode, which may never have been generated in the normal mode [1], [2]. The peak and average power resulting from those extraordinary switching activities in the test mode may cause the chip malfunction and decrease its reliability [2], [3], which implies another yield and cost loss. Unfortunately, an effective test data compression scheme may not necessarily be an effective power minimization scheme. For example, the linear feedback shift register (LFSR) reseeding approach [4] utilizes the random-fill property for don't care (X) bits to achieve high encoding efficiency while introducing many switching activities. Since LFSR reseeding technique provides many transitions, [30] uses reseeding and mask technique to achieve low power test. Therefore, to develop a test compression scheme targeting both high compression ratio and large test power reduction is an important goal in test area.

A. Previous Works

Many proposed approaches are dealing with test power reduction. [13] applies Minimum Transition Fill (MT-fill) technique to achieve low test power, and this method minimizes the transitions in one scan chain. [33] considers the successive test pattern to fill the X bits in test pattern, this approach can also reduce test power. In addition, [7], [12] apply reorder techniques to reduce the test power by minimizing the transition count among the test data. Moreover, [7]–[9], [16], [27] use multiple-scan-chain technique to reduce test power or test time. The architecture in [8] can shutdown or enable a partial range of the sub scan chains, which reduces both peak power and total power consumption. [9], [20] use decoders to decode the pre-encoded test data, providing reduction on power and test data volume. [28], [29] manipulate the embedded deterministic testing (EDT) structure and patterns to achieve low power test.

On the other hand, test data volume can be reduced by compression techniques. It is another way to solve the test data problems, and it sometimes provides low power testing. Due to the necessity of test volume reduction, various techniques have been developed. For example, statistical and Huffman encoding in [5], [6], [15] are used for test volume and test application time reduction. [5] uses 4-bit blocks and encodes test patterns to Huffman code by calculating the pattern frequency. [6] uses run-length (technique in [18]) encoding and Huffman encoding technique to compress data. The basis of run-length encoding lies in encoding a long data string by counting the number of repeated characters or patterns. Nine-code encoding technique is applied in [14] to compress test data. It uses 9 code words to encode data. There are some methods which use structure and memory base scheme to encode test data. In reconfigurable switch structure, [24] applies fewer bits to reconfigurable switch block. [23] provides an inverter-interconnect based decompression network to decode the test data. Broadcast approach in [22], [26] uses broadcaster to distribute few control bits and generates large number of bits to internal scan chains. The Multi-layer Data Copy (MDC) scheme's method in [25] duplicates the test data inside the chip. [21], [31] uses dictionary based method with memory to encode test data.

For unification solutions, [11], [14] use finite state machine (FSM) mechanism and various kinds of data compression techniques to reduce scan power, test data volume, and test time. [10] modifies run length and combines resource partition to achieve low power and small test data volume. [11] also combines Golomb coding (technique in [19]) to deal with the power and volume issues.

B. The Proposed Schemes

In order to deal with the shift-in power and test data volume problems, we define the decoders with fixed (F) or variable (V) input (I) and output (O). We can have 4 choices: FIFO, FIVO, VIFO, VIVO. However, the FIFO scheme has less flexbility than VIFO in the input, which may cause some unnecessay input bits on the decoders. Since FIFO will reduce the compression effiency, we will not implement the FIFO scheme. The other scheme which we will not implement is the VIVO scheme since it needs some constraint to reduce the complexity in implementation. We implement the FIVO scheme which is a pseudo VIVO scheme. In fact, we define the maximum fan-out as constraint in the FIVO scheme. If the number of output bits is larger than the defined maximum fan-out number, we will reduce the input number bits and the input number becomes variable. After the preliminary analysis, we choose fixed output (VIFO) and fixed input (FIVO) schemes to be implemented in this work. Our methodology consists of 3 steps: define the solution scheme, deal with the complex and simple patterns seperately, and adjust the final solution. With this methodology, these two schemes present different behaviors. The compressed scan units of the VIFO scheme have fixed number of output bits but variable number of input bits. The compressed scan units of the FIVO scheme have fixed number of input bits but variable number of output bits.

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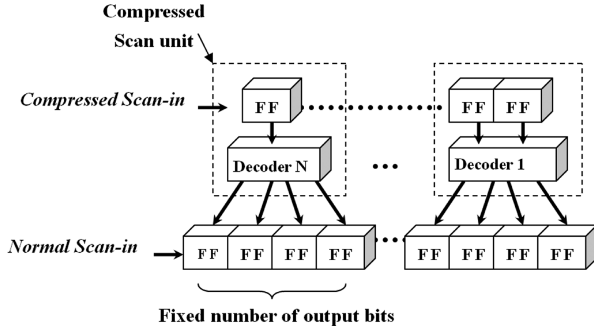

Fig. 1. Compressed scan unit and decoders structure in our fixed output scan chain architecture. The number of scan cells inside compressed scan unit depends on the optimization stage shown in Section III.

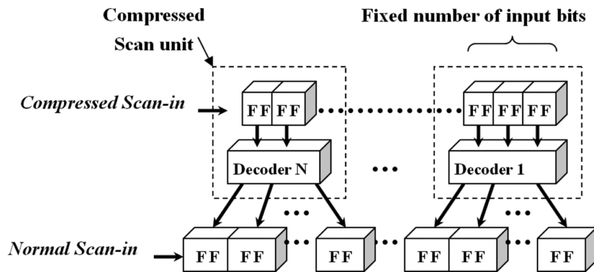

Fig. 2. Our FIVO scan chain architecture including compressed scan units. A compressed scan unit is provided with n-bit decoder ($n = 3$ in this illustration), which maps to several number of scan cells in normal scan chain. The last scan unit may not be equal to n in some cases.

The rest of this paper is organized as follows. We describe the concept and the difference between these two schemes in Section II. Sections III and IV express the detail optimization methodology of these two schemes. The experimental results of these two schemes are shown in Section V. We conclude this paper in Section VI. The preliminary version of this paper can be found in [27].

II. Selective Pattern Compression for Power and Test Data Reduction

We have proposed two schemes using compression techniques to reduce test data and power. Each of the proposed schemes applies its optimization flow to achieve low power and small test data volume respectively. The proposed selective scan chain architectures are shown in Fig. 1 and Fig. 2. We intend to divid all of the test patterns into two groups: first group of test patterns is used for compressed scan chain (CSC), the shift-in patterns are compressed form; second group of test patterns is used in normal scan chain (NSC), the shift-in patterns are not compressed. In this architecture, CSC uses the first group of test patterns which has more X bits to manipulate. X bit ratio is the ratio of the X in a single pattern length (SPL). In this paper, we use X bit omit ratio as an indicator to separate the test patterns: if X bit ratio of a test pattern is smaller than X bit omit ratio, the pattern belongs to NSC group. Otherwise the test pattern belongs to CSC group.

Compressed patterns need special decoders to decode them and the decoders of these two schemes are different. The fixed-output-bit version is shown in Fig. 1. Its decoders have fixed number of bits for output. Fig. 1 is the 1 unit-to-4 scan cells structure. Each compressed scan unit handles four output bits. The number of scan cells inside compressed scan unit depends on the optimization stage described in Section III.

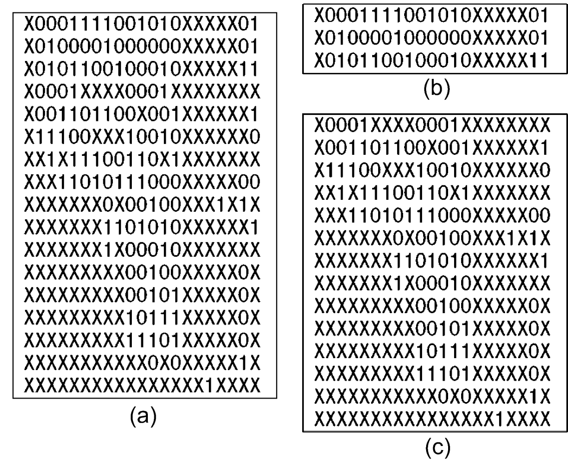

Fig. 3. Pattern selection stage example. This case uses 0.3 as X-bit omit ratio to select the test pattern. (a) Is original test pattern set which has 17 test patterns. (b) Is selected patterns for NSC. (c) Is selected patterns for CSC.

Another scheme has a fixed number of bits in the input. It means that the decoders of this scheme has a fixed number of input bits but the decoder's output bit number is variable. For example, Fig. 2 shows 3-bit decoder structure with original scan chain and compressed scan chain. It provides 2^3 conditions of coding results. Each condition provides decoding results to the normal scan cell as test data. The number of scan cells in each condition depends on the optimization stage shown in Section IV.

These schemes can be applied to multiple scan chains structure, which provide very low power consumption. Using multiple scan structure can skip many unnecessary transitions in long scan chain.

III. VIFO Scheme Optimization Method

This section will introduce the optimization methodology on test data and power in VIFO scheme. The methodology consists of scan chain partition and three stages. Scan chain partition is to divide the original single scan chain to multiple scan chains. The three stages are pattern selection, pattern compression, and power optimization. The test patterns in the same partition will be processed via the following three stages. The first stage is pattern selection: it sets the X bit omit ratio in order to select the pattern for CSC. The second stage is pattern compression: it merges the test patterns in the same segment of test sets. The third stage is power optimization stage. In this stage, it uses shorter pattern length and applies greedy search to find the smaller power consumption code in CSC segment by segment. Each X bit omit ratio provides one result for test data volume and power consumption.

A. Pattern Selection Stage

This stage separates the test patterns into two groups by X bit omit ratio. If test pattern's X bit ratio is smaller than given X bit omit ratio, this test pattern will belong to the NSC group, or it will belong to CSC. SPL_{new} is the CSC test data length that comes from compressed scan unit (Fig. 1). Total original test size in equation (1) $Original_test_size_{total} = Pattern_number_{org} \times SPL_{org}$ and total new test size in equation (2) $New_test_size_{total} = NSC_pattern_number \times SPL_{org} + CSC_pattern_number \times SPL_{new}$ are used to calculate the test data volume in this paper.

The example is shown in Fig. 3. There are 17 patterns in the original test pattern set (Fig. 3(a)). If we set X bit omit ratio as 0.3. We can get 3 patterns in NSC test data set (Fig. 3(b)) and 14 patterns in CSC test data set (Fig. 3(c)).

0	0000	1011	0000	0100	1000	1
1	0001	0000	0100	1000	0101	0
2	0111	1110	0110	0000		
3		1010	1110	1100		
4			0001			
5			1010			
6			0101			
7			0111			

(a)

0	3	0	3	1	1
1	0	0	0	1	0
2	1	1	1	1	1
2	2	2	3	1	1
2	3	3	2	0	1
2	3	4	2	1	1
2	0	5	1	1	0
2	0	0	1	1	1
2	3	4	2	0	1
2	3	4	0	0	1
2	3	6	3	0	1
2	3	7	0	0	1
2	3	5	2	1	1
2	3	7	3	0	1

(b)

01000101010
11010100011
00101001110
00110111010
00001110100
00001010110
00011101111
00010101110
00001010100
00001010000
00000001000
00000010000
00001100110
00000011000

(c)

Original Test Data	X000	1XXX	X000	1XXX	XXXX	X
Test Data in NSC	0000	1010	0000	1100	0101	0
Mapping Code	0	3	0	3	1	1
Test data in CSC	01	00	010	10	1	0

(d)

Fig. 4. VIFO scheme with a 4-bit encoding case in pattern compression stage. (a) is the compressed test pattern. (b) shows the index number of each segment. (c) shows the new test data results and the mapping code comes from (b). (d) shows one test pattern transformation from original test data to new test data.

B. Pattern Compression Stage

When the test patterns for CSC are determined, we use these patterns in compression stage. In this stage, we attempt to shrink coding size as small as possible. We use 4 bits as fixed output size to introduce the process. If the original test data length is 21 bits, we divide it to 6 segments. The compression procedure starts to compress test patterns from the first segment to the sixth segment. The next step merges patterns in each segment. For instance, this step will merge pattern XX11 and 1XX1 to pattern 1X11. We define TNC as the total number of compression results. If we get $TNC \leq 2$, number of cells in compressed scan unit (CSU) is set to 1. This means we can use 1 input bit to control all of the test patterns in output. If we get $2 < TNC \leq 4$, number of cells in CSU is set to 2. While we get TNC bigger than 8, we will not encode the segment. Fig. 4(a) is the compression result and the patterns come from the CSC test data set in Fig. 3(c). Fig. 4(a) shows the compression result and all Xs are replaced by 0 on compressed data after the compression process. Each compressed pattern is given a number as index. Through the compression procedure, the first and second segment of compressed test data in Fig. 4(a) both need 2 bits to encode the whole segment. The third segment needs 3 bits to encode since the TNC in this segment is 8.

C. Power Optimization Stage

After the pattern compression stage, this subsection introduces the power optimization method to minimize the shift-in power in CSC. We apply greedy search method to find the lower power coding, because we set the bit before first bit of each pattern to 0. This stage maps new encoded data to the compressed pattern index. We use the example in Fig. 4(b) to explain this mapping. The first segment of Fig. 4(b) has 3 different compressed codes. The mapping code and index number can be found in Fig. 4(a). By finding all of the possible codes from the first segment to the last segment, we can get the final encoding result for CSC. The result is shown in Fig. 4(c). This stage calculates the smallest transition mapping from the first segment. The permutation of 3 bits, with 8 new encoded data, is 40320(8!). The optimization method tries to find all the permutations from the first segment to the last segment, and decides the fewest switching power encoding. The encoding result becomes new encoded data.

The first pattern in Fig. 4(b) shows that 030311 is the index number of the test pattern. This pattern maps to test result 000010100000110001010 and new test pattern 01000101010. The first 4 bits of the test result is 0000. It comes from the mapping number 0 in Fig. 4(b) and first segment of pattern 0000 in Fig. 4(a). The 5th to 8th bit of the test result is 1010. It comes from the mapping number 3 in the second column of Fig. 4(b) and the second column of pattern 1010 in Fig. 4(a). At last, we can get the test result 000010100000110001010. The new test result for CSC shows in Fig. 4(c). The new test result comes from the power optimization process. Each row in Fig. 4(c) will be shifted into CSC. Fig. 4(d) integrates a pattern result of each previous described stage.

IV. FIVO Scheme Optimization Method

This section will introduce the FIVO scheme optimization methodology. The methodology is similar to the previous scheme. If we apply multiple scan chain technique, it consists of scan chain partition and three stages and different partitions go through these three steps independently. Otherwise it consists of three stages. The three stages are pattern selection, pattern compression, and power optimization. Pattern selection is the same with previous scheme. We will reference from the previous one (Section III-A). Techniques in pattern compression and power optimization are different. We will focus on these two stages in this section. Similarly, all of the test patterns in the same partition go through these three stages.

Pattern selection method of FIVO scheme is the same with VIFO scheme. Test patterns for CSC are compressed by the pattern compression stage. This stage contains merging, extending, and maximizing steps.

We use an example when $n = 3$ to illustrate the procedure of this stage. The compression procedure starts to compress test patterns with 3 bits segment from the first bit of the CSC test pattern set. Each 3-bit decoder provides 8 different codes. Each code represents one compressed pattern which is merged from original test data. For instance, this step will merge pattern X11 and XX1 to pattern X11. Moreover, XX11, X111, 0111 will be merged to code 0111 in the same segment. If the total number of compression results is smaller then 8, it extends the segment to 4 bits. Until the total number of compression results is maximum but smaller than 8 or equal to 8, the results are encoded to 3 bits in CSC. Next, it starts to encode another 3 bits. At last, it may have 2 bits or 1 bit decoder at the end. If the number of compression results is 3 or 4, the results will be encoded to 2 bits. If the compression results equal to 1 or 2, the results will be encoded to 1 bit. We also limit the maximum number of one decoder output to 256. If the output number of a decoder achieves 256, we will finish processing this segment and the input number of this segment's encoder may fewer than 3. Finally, we also can use 4-bit or 5-bit decoder that provides 16 or 32 different codes.

To be more specific, a realistic case is provided in this paragraph. This example shows 14 test patterns in CSC. The compression pattern number will equal or smaller then original pattern number after the merging step. Fig. 5(a) shows the compression results and all Xs after the compression are replaced by 0. Each compressed pattern is given a number as index. Through the compression procedure, the first segment of compressed test data in Fig. 5(a) applies 3 bits (6 codes) to encode 11 bits data.

In order to minimize the shift-in power with n-bit based encoding, the greedy search method are applied in each segment to find the lower power coding. Assume the initial state of the scan chain is 0, it will obtain the optimal solution $(n = 3)$ and heuristically good solution $(n > 3)$ after pattern selection and pattern compression stages. This stage maps new encoded data to the compressed pattern. The first column of Fig. 5(a) needs 6 different compressed codes to map. In Fig. 5(a), (b), (c), test result 00001000000 maps to 0 and 0 maps to new test pattern 110 in the first row first column of Fig. 5(b), (c). The CSC shift-in data will be 110 and the decoder will produce 00001000000 to NSC.

In this stage, we calculate the smallest transition mapping from first segment. The permutation of 3 bits, with 8 new encoded data, is

0	00001000000	0010010001
1	00011011000	0100000010
2	01110000010	0000000000
3	00101110011	1000001010
4	00011010111	0100000001
5	00000001101	1000000000
6		1010000000
7		1110000000

(a)

0	4
1	0
2	1
3	0
4	2
0	3
5	4
1	4
1	5
1	6
2	7
4	6
5	1
5	0

(b)

110	001
111	101
100	010
011	101
001	100
110	011
000	001
111	001
111	111
111	110
100	000
001	110
000	010
000	101

(c)

Original Test Data	X0001XXXX00	01XXXXXXXX
Test Data in NSC	00001000000	0100000001
Mapping Code	0	4
Test data in CSC	110	001

(d)

Fig. 5. FIVO scheme with a 3-bit encoding case in pattern compression stage. (a) Is the compressed test pattern of each segment. (b) Shows the index number of each segment. (c) Shows the new test data results and the mapping codes come from (b). (d) Shows one test pattern transformation from original test data to new test data.

TABLE I
VIFO SCHEME EXPERIMENTAL RESULTS IN TEST PATTERN REDUCTION AND POWER REDUCTION USING MINTEST SET(ISCAS'89 BENCHMARKS)

Circuit	Orig. SPL	Orig. vol.	New test vol.	Orig. power	New shift-in power
s5378	214	23754	13401	396508	252392
s9234	247	39273	23535	647634	377319
s13207	700	165200	62843	1898650	1005255
s15850	611	76986	36836	1754458	995196
s35932	1763	28208	15778	653390	268537
s38417	1664	164736	88968	11723227	6306253
s38584	1464	199104	101520	11733372	7938510

40320(8!). The optimization method tries to find all the permutations from the first segment to the last segment, and decides the fewest switch power encoding. The encoding results become new encoded data. Since the permutations of 4 and 5 bits encoded data are very large, the computation time of optimization stage will be very long. Only to optimize the partial encoded data is recommended. The first row in Fig. 5(b) shows that 04 is the index number of the test pattern. This pattern maps to test result 000010000000100000001 and new test pattern 110001. The test result can be get from Fig. 5(a) by index. In this example, the index code 0 in the first column of Fig. 5(a) maps to 0000100000 and maps to 110 in Fig. 5(c). The index code 4 in the second column of Fig. 5(a) maps to 0100000001 and maps to 001 in Fig. 5(c). We also can perceive that all of the index codes 0 in the first column of Fig. 5(b) are maps to 110.

With the mapping method, we can get the CSC shift-in codes. Each row in Fig. 5(c) will be shifted into CSC. Fig. 5(c) is the power optimization result codes. We can observe that the compressed patterns are encoded to fewer bits of data. Fig. 5(d) shows a new test pattern (on the bottom), which is generated from original test pattern, to the compressed data mapping index, then to the compressed data in CSC. We can get the decoded results for NSC from Fig. 5(a).

V. EXPERIMENTAL RESULTS

This experimental result section contains three subsections. The first subsection provides the experimental results of the VIFO scheme. The second subsection provides the experimental results of FIVO scheme. The third subsection provides the limitation of the proposed FIVO schemes. All of our experimental results use ISCAS'89 circuits. We also can integrate the method in [8] to have multiple scan chains and partition them to more sub scan chains, which provides lower power for large SoC designs than one long scan chain [27].[1]

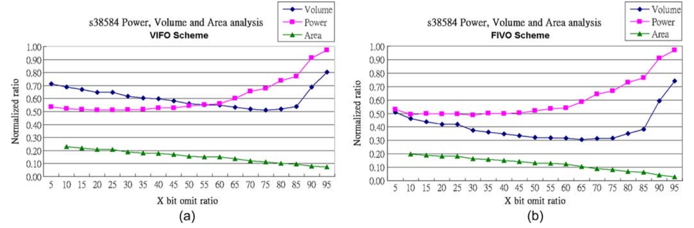

Fig. 6. (a) 4-bit VIFO scheme experimental results using one scan chain architecture with different omit ratio. New total test size is normalized to original test size. Power consumption is normalized to power of all X bits filled with 0. This shows that the scheme provides both power and volume reduction. (b) 3-bit FIVO scheme experimental results using one scan chain architecture with different omit ratio. The normalization parameters of (a) and (b) are the same.

TABLE II
FIVO SCHEME EXPERIMENTAL RESULTS IN TEST PATTERN REDUCTION AND POWER REDUCTION USING MINTEST SET(ISCAS'89 BENCHMARKS)

Circuit	Orig. SPL	Orig. vol.	New test vol.	Orig. power	New shift-in power
s5378	214	23754	8830	396508	228202
s9234	247	39273	17607	647634	370290
s13207	700	165200	32048	1898650	929472
s15850	611	76986	22266	1754458	861100
s35932	1763	28208	10798	653390	246093
s38417	1664	164736	62179	11723227	5315026
s38584	1464	199104	61064	11733372	6859668

A. Experimental Results of VIFO Scheme

We use 4 bits output scan unit as our experimental architecture which is shown in Fig. 1. The experimental results are shown in Table I and Fig. 6(a). Table I shows that different circuits need different X bit omit ratios to obtain the lowest test power. The caculation of total power consumption consists of shift in power in CSC, NSC, and transfer power from CSC and NSC. Using 55% as X bit omit rate in benchmark s38584, we can get 55% power and 55% test data volume. In Fig. 6(a), we observe that both power and data volume reduction are 45% at X bit omit ratio 55%. All of the results in Table I and Fig. 6(a) are normalized with the data of all X bits filled with 0. This technique achieves small test data size in each circuit and it has some power reduction percentage in these experimental results.

B. Experimental Results of FIVO Scheme

In our experimental results, different test data sets and circuits have different ratios to meet the lowest power and smallest test data volume. Fig. 6(b) shows the FIVO scheme result of circuit s38584. Users can apply X bit omit ratio to obtain the best power or the best compression. Fig. 6(b) shows the FIVO scheme result provides the lowest power about 49% at 30% X bit omit ratio in circuit s38584. It uses 130 of total 136 patterns in CSC. The smallest test data volume is about 31% at 65% X bit omit rate, and it uses 116 of 136 patterns in CSC. We can observe that the FIVO scheme provides better power and area results than VIFO scheme from Fig. 6(a) and (b). Table II shows the best volume size results in each bench circuit.

Table III shows the Mintest set compression results. Although previous works have smaller volume than ours in some circuits, our 5 bits FIVO scheme still provides good compression results in these circuits.

[1]This paper only deals with shift-in power. The power estimation method is weight transitions metric (WTM) from [13].

TABLE III
EXPERIMENTAL RESULTS ON TEST DATA VOLUME USING MINTEST SET

Circuit	Mintest set	FDR [17]	ARL [10]	MDC [25]	Dictionary [32]	SDI [33]	FIVO (3-bit)	FIVO (4-bit)	FIVO (5-bit)
s5378	23754	12346	11694	10416	6345	X	8830	7388	4962
s9234	39273	22152	21612	17794	11498	X	17607	13676	10288
s13207	165200	30880	32648	15596	8517	9708	26151	20448	9992
s15850	76986	2600	26306	22384	13873	10726	22266	17199	10074
s38417	164736	93466	64976	62914	62939	36864	62179	44952	27093
s38584	199104	77812	77372	57428	53287	27555	61064	46215	27667

We implement the program with C and compile these programs with gcc version 3.4.5. The programs run on the server with Intel(R) Xeon(R) 5160 3.00 GHz CPU and 32 GB memory. We check 40320(8!) cases in FIVO (3-bit) scheme. However, the permutations of 4 and 5 bits encoded data are very large, we only optimize partial of the encoded data at the optimization stage to achieve low power results.

VI. CONCLUSION

In this paper, we propose two schemes with related encoding methodology to reduce test power consumption and shrink test data volume. Experimental results of fixed input version show this scheme achieves better reduction rate of test data volume. We also compare the FIVO scheme with previous works, the results provide relatively small test data size. In addition, we implement the decoders in FIVO scheme and observe that we can get a feasible X bit omit ratio as tradeoff between volume, power, and area overhead. With acceptable hardware overhead, our approach is practical and can be applied in modern chip DFT designs.

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