鎳金屬誘發非晶矽薄膜側向結晶

－成長機制與低溫複晶矽薄膜電晶體效能之研究

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摘要

在本論文中，主要的研究是鎳金屬誘發非晶矽薄膜側向結晶。其中，探討拉伸應力對於鎳金屬誘發非晶矽薄膜側向結晶成長機制之影響以及利用鎳金屬壓印誘發結晶方法來製作低溫複晶矽薄膜電晶體。並結合鎳金屬誘發非晶矽薄膜側向結晶與準分子雷射退火來製作高效能低溫複晶矽薄膜電晶體。此外，為了解決對於鎳金屬誘發複晶矽薄膜來說，非常重要的鎳金屬殘留問題，因而發展出有效的吸鎳方法來降低鎳金屬誘發複晶矽薄膜中的鎳金屬殘留。

首先，鎳金屬誘發非晶矽薄膜側向結晶過程包括三個階段: (1)$NiSi_2$ 金屬矽化物之生成，(2)在 $NiSi_2$ 金屬矽化物生成結晶矽之核，(3)藉由金屬矽化物 $NiSi_2$ 之移動來產生非晶矽薄膜結晶與結晶成長。有相關報告指出，拉伸應力會縮短鎳金屬誘發非晶矽薄膜側向結晶的潛伏時間。然而，其詳細的

機制並不清楚。在本實驗中，利用一簡單的彎曲設備來研究拉伸應力對鎳金屬誘發非晶矽薄膜側向結晶之影響。基於實驗結果發現，拉伸應力並不會影響 $NiSi_2$ 金屬矽化物與結晶矽核之生成，但是，會影響結晶矽之成長。並發現壓應力並不影響鎳金屬誘發非晶矽薄膜側向結晶之速率。

鎳金屬壓印誘發結晶法比傳統鎳金屬誘發非晶矽薄膜側向結晶法存在著許多更好的特性。在本實驗中，利用<111>與<112>不同成長方向之針狀結晶來製作低溫複晶矽薄膜電晶體。<111>成長方向之針狀結晶是利用傳統鎳金屬誘發非晶矽薄膜側向結晶來製作，而<112>成長方向之針狀結晶是利用鎳金屬壓印誘發結晶方法來製作。結果發現，<112>成長方向之薄膜電晶體在元件電特性優於<111>成長方向之薄膜電晶體，有 2.6 倍高的電子遷移率，4 倍高的開/關電流比與 2.4 倍低的漏電流。

雖然，可以利用鎳金屬壓印誘發結晶之方法來製作元件特性較佳，均勻性較好之低溫複晶矽薄膜電晶體。但是，在複晶矽針狀結晶間仍然存在著許多的缺陷與未結晶區域，這些缺陷會使元件的特性劣化。結合準分子雷射與鎳金屬壓印誘發結晶薄膜，來降低缺陷密度。並比較其薄膜電晶體之特性，當雷射能量在 345 mJ/cm^2 時，晶粒大小從 50 奈米增加到 250 奈米。結合準分子雷射退火之電晶體，由於有較大的晶粒與較少的晶粒間之缺陷，其電子遷移率為 413 cm^2/Vs，開/關電流比為 4.24×10^6，遠優於純粹壓印結晶之電晶體。

最後，發展出兩種吸鎳的方法，來降低鎳金屬誘發側向結晶複晶矽薄膜中的鎳金屬殘留。第一，利用厚度為 100 奈米的非晶矽薄膜來當作吸鎳層，與厚度為 30 奈米的氮化矽來當做蝕刻停止層，在溫度為 550°C 下進行退火 90 小時來降低鎳金屬殘留。第二，利用鍍覆非晶矽薄膜之吸鎳基板與鎳金屬誘發結晶之複晶矽薄膜接合並進行退火。其複晶矽薄膜中的鎳金屬殘留可以被大大的降低。

Ni-Metal Induced Lateral Crystallization of Amorphous Silicon

— *Growth Mechanism and LTPS TFTs Device Performance*

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Abstract

In this thesis, Ni-metal induced lateral crystallization (NILC) of amorphous silicon (α-Si) has been studied. The influence of tensile stress on the growth mechanism of NILC is investigated. Furthermore, we fabricate the LTPS TFTs by Ni-metal imprint-induced crystallization method. Combine NILC and excimer laser annealing (ELA) method to produce high-performance LTPS TFTs. Moreover, in order to solve this issue of NILC poly-Si film, we develop an effective gettering method to reduce the Ni-metal impurity contamination of the NILC poly-Si films.

Initially, three stages have been identified in the NILC process: (1) the formation of $NiSi_2$ precipitates, (2) the nucleation of crystalline Si (c-Si) on $NiSi_2$ precipitates, and (3) the subsequent migration of $NiSi_2$ precipitates and growth of c-Si. It has been reported that the incubation time could be reduced by tensile stress. However, the detail has still not been

clarified. In this study, a simple bending fixture was used to investigate the effects of tensile stress on the growth of NILC. Base on the results of this study, it was found that tensile stress did not enhance $NiSi_2$ formation and c-Si nucleation stages, but enhanced the c-Si growth stage. It was also found that compressive stress did not change NILC rate.

The Ni-metal imprint-induced crystallization method exhibited many superior characteristic over traditional NILC method. In this study, for the LTPS TFTs fabricated using <111> and <112> needle grains have been investigated. They were fabricated by traditional NILC and Ni–metal imprint-induced crystallization method. It is found that the performance of 112-TFT was far superior to that of 111-TFT. The device transfer characteristics of 112-TFT include 2.6-fold-higher field-effect mobility (μ_{FE}), 4-fold-higher on/off current ratio ($I_{ON}/_{OFF}$), and 2.4-fold-lower leakage current (I_{OFF}) compared with those of the 111-TFT.

The improved performance and good uniformity LTPS TFTs have been fabricated using Ni-metal imprint-induced crystallization method. However, the polycrystalline silicon film contained many intra-grain defects with some un-crystallized regions between poly-Si needle grains. These defects degrade the transfer characteristics of TFT devices, including the field effect mobility (μ_{FE}) and the leakage current. In this study, combine the excimer laser crystallization method to reduce the defect density. To compare the performance of IMPRINT

and IMPRINT-ELA TFT, upon increasing the laser energy to 345 mJ/cm^2, the grain size increased from 50 to 250 nm and the performance of IMPRINT-ELA-TFT was found to be far superior to that of IMPRINT-TFT due to larger grains and fewer intra-grain defects of the IMPRINT-ELA poly-Si film than that of the IMPRINT poly-Si film. The mobility of the IMPRINT-ELA-TFT was 413 cm^2/Vs, which was 31.7 times higher than that of the IMPRINT-TFT. The on/off current ratio of the IMPRINT-ELA-TFT was 4.24 $\times 10^6$, which was 2 orders magnitude higher than that of the IMPRINT-TFT.

Finally, develop two gettering methods to reduce the Ni contamination within the NILC poly-Si film. First, using α-Si films with a thickness of 100 nm as a Ni-gettering layer, silicon-nitride (SiN_x) films with a thickness of 30 nm as the etching stop layers and annealed at 550°C for 90 h to reduce the Ni-metal impurity within the NILC poly-Si film. Second, an α-Si-coated wafers used as Ni-gettering substrates then bonding the gettering substrate and NILC poly-Si film together. The Ni-metal impurity within the NILC poly-Si film was greatly reduced.

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Chapter 1 Introduction

1-1 Overview of Thin-Film Transistors (TFTs)

Thin-film field-effect transistors (TFTs) utilize the modulation of conductivity of a semiconductor film by the voltage of an insulated gate. In contrast with the metal-oxide semiconductor field-effect transistor (MOSFET) the TFTs can be made using thin films of either amorphous or polycrystalline semiconductors. As the TFTs do not require single crystal semiconductor material, it can be fabricated on a variety of insulating substrates. The major application for the TFTs at present is in active matrix flat panel displays (AMFPD). A circuit diagram of an active matrix liquid crystal display is shown in Fig. 1-1. Each pixel consists of a capacitor with liquid crystal material as the dielectric (C_{LC}), storage capacitor (C_S) and a switching transistor. TFTs are turned on by applying a voltage to single row (scan line). Then, the signal is transferred to the capacitor (pixel) from the data line. The liquid crystal material rotates the polarization of light to a degree, which depends on the applied electric field. The intensity of transmitted light is thus determined by the signal applied to the data line. When the gate voltage is returned to zero, the signal remains on the capacitor for a time determined

by the leakage current (I_{lk}) of the TFTs. The leakage current should be low enough so grayscale levels can be maintained over the frame refresh time.

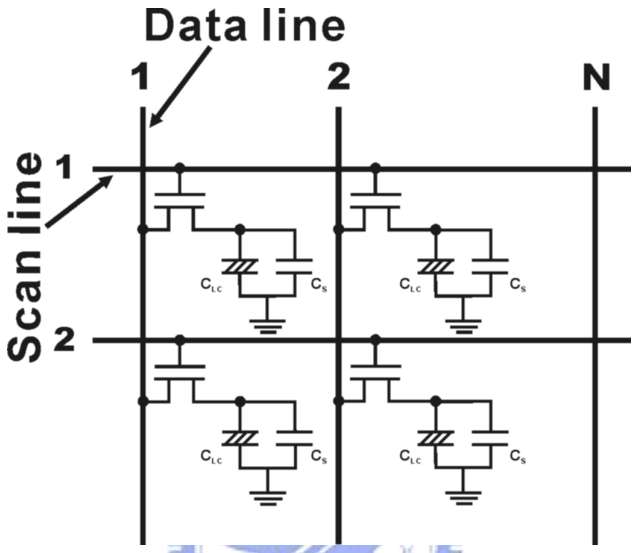

Fig. 1-1 Circuit diagram of an active matrix liquid crystal display (AMLCD).

Thin-film transistors is a fundamental component of AMFPD; therefore, to investigate the TFTs is very important for the development of flat panel display technology.

1-1-1 Amorphous Silicon (α-Si) TFTs

Compare to the conventional cathode ray tube (CRT) display, the flat panel display has light weight and small volume. Among many productive flat panel display, the active matrix liquid crystal display (AMLCD) have widely use in many applications, such as laptop and desktop monitor. Today, the α-Si TFT-LCDs have dominated the large area flat panel display market. The TFT-LCDs have become the standard component of laptop, desktop monitor and digital camera.

Active matrix liquid crystal display fabricated on α-Si TFTs is the most usual technique, due to the advantages such as low temperature process (<350℃), [1.1,1.2] suitable for large area, non-expensive glass substrate and lower leakage current, that is enabling for pixel switching. Nevertheless, the α-Si TFTs exhibited poor field-effect carrier mobility (typically μ_{FE}< 1 cm^2/V-s) and smaller on current. This is due to the poor electrical performance of the α-Si TFTs. To achieve the needed current flow for the grayscale of the frame, the dimension of α-Si TFTs device was increased. Resolution of the display will be decreased resulted from the large α-Si TFTs. The high-resolution TFT-LCD needs new solution to improve the mobility of TFTs. The poly-Si TFTs technology is one of the potential methods to achieve the requirement of high-resolution TFT LCD. And the poor field-effect carrier mobility can be overcome easily using the poly-Si films as the active layer of the TFTs.

1-1-2 Low-Temperature Polycrystalline Silicon (LTPS) TFTs

In 1980, high temperature polycrystalline silicon TFTs had been introduced.[1.3] They used chemical-vapor deposited poly-Si to achieve good carrier mobility and electrical characteristics. With mobility around 50 cm^2/V-s, these high temperature poly-Si TFTs were employed gate insulator SiO_2 grown thermally at 1050°C. This approach requires a high strain temperature substrate such as quartz, incompatible with the commercially available large area non-expensive glass substrate.

Recently, many researchers have developed various techniques for crystallization of α-Si at low temperature (below 600°C), and then transformation it to poly-Si; the motivation for pushing up the mobility to be able to integrate drive circuitry [1.4,1.5] as well as providing pixel TFTs and more compatible with the glass substrate. In fact, the field effect mobility of poly-Si TFTs is significantly higher than that of α-Si about two orders of magnitudes. The higher drive current allows small TFTs dimension to be used as the pixel switching elements, resulting in higher aperture ratio and lower parasitic gate-line capacitance for improved display performance. [1.6]

Unlike MOSFETs, where the active layer is part of the substrate, in the case of TFTs the active layer needs to be separately formed on the host substrate. The crystallization method affect the microstructure quality of the resulting poly-Si film, which means that the performance of poly-Si TFT will be affected by the selection of techniques for the

crystallization of Si films.

A various techniques have been investigated for crystallization of α-Si at low temperature such as: (1) solid phase crystallization (SPC) (2) excimer laser Annealing (ELA) (3) Ni-metal induced/Ni-metal induced lateral crystallization (NIC/NILC). In the following section, we will review the crystallization method that the above-mentioned.

1-2 Low-Temperature Polycrystalline Silicon (LTPS) Crystallization Method

Crystallization of α-Si films has been considered as the most important process step in the fabrication of LTPS TFTs. The quality of crystallized poly-Si films is quite sensitive to the performance of poly-Si TFT. In poly-Si films, most defects are generated at the grain boundaries. Enlarging the grain size can promote the quality of poly-Si, as deposited poly-Si generally exhibits small grain size. In general, the poly-Si crystallized from α-Si usually has larger grain size than that of as-deposited poly-Si. Historically, solid phase crystallization [1.7] was the first technology to produce poly-Si films for display applications, followed by laser crystallization. The ultimate goal of the LTPS technology is to integrate the pixel-driving circuits on the display substrate. Fig. 1-2 shows the anticipated evolution of poly-Si technology development and its impact on the degree of on-panel integration.[1.8]

Year	2004	2006	2008	2010
SOP Generation	1st	2nd	3rd	4th
Display Resolution	300ppi	400ppi		
Power Supply	12V	3-5V	1.5-3V	1.5V
TFT Mobility	200-300 $cm^2V^{-1}s^{-1}$	300-500 $cm^2V^{-1}s^{-1}$	500 $cm^2V^{-1}s^{-1}$	
Design Rule	3μm	1.5μm	0.8μm	0.5μm
Logic Frequency	~3MHz	10MHz	20-50MHz	50-100MHz
Key Process Crystallization Gate Insulator Patterning	CGSi	Advanced CGSi Thin GI Fine Patterning	Texture-control CGSi Ultra-thin GI Sub-μm Patterning	
Monolithic Integration	Digital Driver	Timing Geneator Photo Sensor Amplifier	Display controller Image processor LN Amplifier	ULC Driver RF Capability Advanced MPU

Fig. 1-2 Roadmap of poly-Si TFT technology.

1-2-1 Solid Phase Crystallization (SPC) Method

Deposited α-Si thin films were transformed to poly-Si using SPC method has obtained better TFT device electrical performance [1.9] than as-deposited poly-Si films. For the SPC method, α-Si films are crystallized in a furnace at temperature about 600°C for duration time (about 24 h). The polycrystalline grains are generally in oval-shaped, and large defect density exists in poly-Si films. Amorphous Si is a thermodynamically meta-stable phase possessing a driving force for transformation to polycrystalline phase given a sufficient energy to overcome the initial energy barrier.

A key factor affecting crystallization is the nucleation rate in the α-Si films. The nucleation rate is strongly influenced by the selected deposition method and condition. [1.10,1.11] The structural order/disorder in the α-Si films affects the films to form stable nuclei. Higher disorder structure increases the energy barrier required to form the Si nuclei; this concept has been used in the past to increase the grain size of poly-Si films. Ideally, a small number of fast-growing nuclei are needed to maximize the grain size. However, the reality of the situation is that the probability that additional nucleation events will occur within the volume separating growing nuclei increases geometrically with the separation distance.

1-2-2 Excimer Laser Annealing (ELA) Method

Excimer laser annealing is suitable for fabrication of LTPS TFTs on large area glass substrate. Development of the ELA method has provided poly-Si material with high quality than SPC method. This is attributed to the melt-induced poly-Si growth. For the crystallization process, the laser is irradiated at the α-Si and the silicon is heated above 1200°C. However, only sustained for a very short time; therefore, it will not damage the glass substrate. Moreover, as shown in Fig. 1-3, there are two major transformation regimes (occurring at low and high laser energy, respectively) and one minor transformation regime in between (that so-called superlateral growth, or SLG).[1.12,1.13] The low laser energy regime describes a situation where the incident laser is sufficient to induce melting of the silicon films, but it is low enough that a continuous layer of silicon at the maximum extent of melting. For this reason, this regime is referred to as the partial melting regime. The high laser energy regime corresponds to a situation that the laser energy is sufficiently high to completely melt the silicon film; this regime is also referred to as complete melting regime. In addition to these two regimes, a third regime has been found to exist within a very narrow experimental window in between the two main regimes. Despite the small extent of this region, it is nonetheless one with great technological significance, because the poly-Si films within the regime feature large-grained polycrystalline microstructures.[1.14] The stable grain size of ELA poly-Si films is typically limited to 0.3~0.6 μm. Larger grain size is possible within the

SLG window, but this regime is intrinsically unstable.

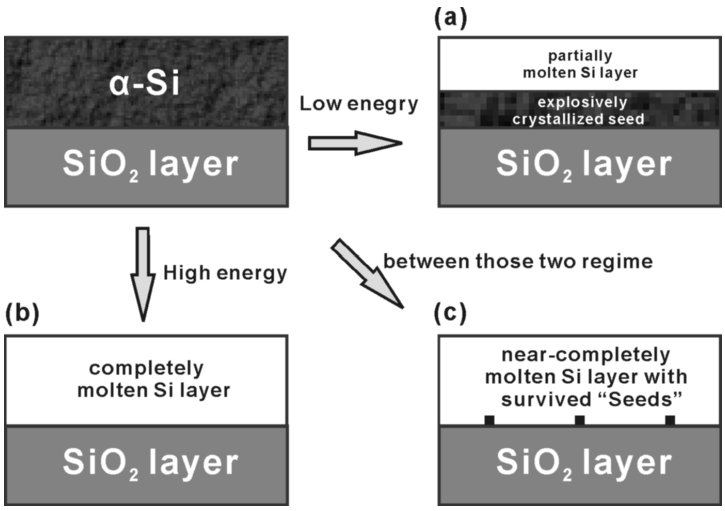

Fig. 1-3 Illustration of transformation scenarios during the ELA process. Correspond to (a) partial melting, (b) completely melting and (c) near-completely melting of the initial Si film.

The surface roughness in ELA poly-Si films is localized at the planes and point of congruence of grain boundaries. The mechanism for the formation of roughness is well understood and is attributed to the specific density difference between molten Si (2.53 g cm^{-3}) and solid Si (2.30 g cm^{-3}). In other words, as the molten Si solidifies, it simultaneously expands. Solidification starts from neighboring seed areas, and the last region to solidify is the volume at the vicinity of the two colliding lateral fronts. As that happens, the generated solid Si can only expand upward, as shown in Fig. 1-4, thus generating the ridge associated with the formation of the grain boundary at the location.

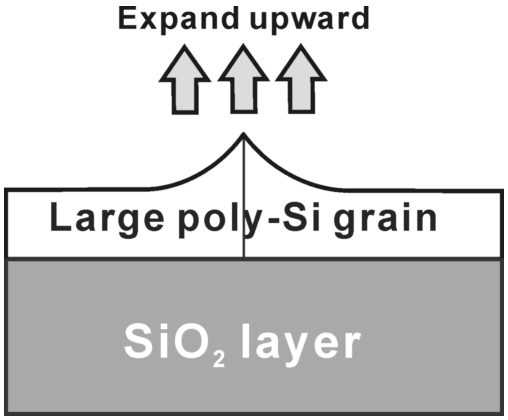

Fig. 1-4 Solidification of the molten Si film. Resulting in the higher surface roughness.

Although the highest quality poly-Si films were fabricated by ELA method, the poor grain size uniformity and high roughness ELA poly-Si films degraded the performance of TFT.[1.15]

1-2-3 Ni-Metal Induced Crystallization (NIC) / Ni-Metal Induced Lateral Crystallization (NILC) Method

Solid phase crystallization of α-Si needed a high temperature and longer annealing time for furnace annealing process. In the NIC/NILC method,[1.16~1.19] the annealing time and temperature could be reduced, and the grain size of NILC poly-Si films uniformly over large area could be obtained. In 2000, Sharp Corp. and SEL (Semiconductor Energy Lab.) propose the CGSi (Continuous Grain Silicon) technique to fabricate the 60 inch HDTV rear

projector.[1.20] When thin Ni is deposited on α-Si and annealed, Ni disilicide ($NiSi_2$) forms.[1.21] The nickel disilicide is cubic with CaF_2 structure and has a very close lattice parameter match to c-Si (-0.4%), the lattice constant of $NiSi_2$, 5.406A, is nearly equal to that of Si, 5.430A. The disilicide is actually the species that mediates the transformation of α-Si to c-Si. As shown in Fig. 1-5, the c-Si formed below the Ni-pad is called NIC and the lateral growth is called NILC.

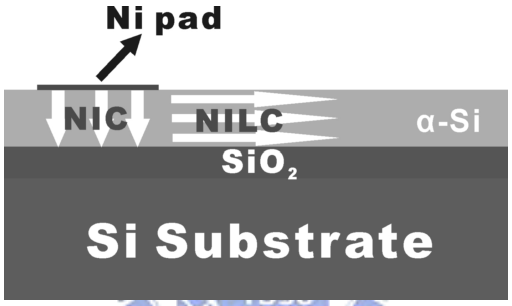

Fig. 1-5 Schematic illustration of the Ni-metal induced Crystallization (NIC) and Ni-metal induced lateral crystallization (NILC).

The silicide mediate growth of silicon occurs in three stages. In the first stage, precipitation and growth of $NiSi_2$ occur in the temperature range of 325~400°C. In the second phase, crystalline Si nucleates on one or more the eight {111} faces of the octahedral $NiSi_2$, as shown in Fig. 1-6. Finally, in the third phase, c-Si growth proceeds with a $NiSi_2$ precipitate at the planar advancing growth front.

As shown in Fig. 1-6, for <110>-oriented precipitates, four of the {111} planes exhibit surface normal within the planes of the film, which makes extensive growth possible. On the other hand, the <100>- and <111>-oriented precipitates exhibits {111} planes normal that intersect the upper and lower surface of α-Si films.

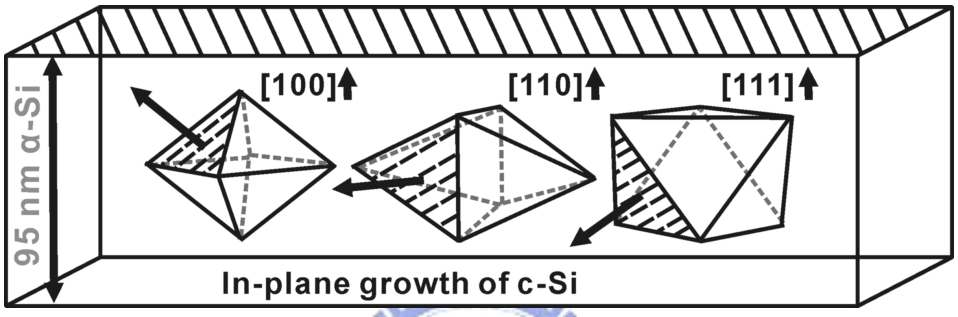

Fig. 1-6 Schematic representation of favorable precipitate orientations for long-range growth of epitaxial Si within the plane of the α-Si.

The driving force for the migration of $NiSi_2$ precipitates is reduction in the free energy associated with the transformation of meta-stable α-Si to stable c-Si. An equilibrium free-energy diagram is provided for explanation, as shown in Fig. 1-7.[1.21] It is well known that the α-Si has a higher free energy than c-Si. In the case of Ni silicide mediated crystallization, the free energy difference between Ni and Si atoms at the $NiSi_2$/α-Si and $NiSi_2$/c-Si interface acts as the driving force for Ni diffusion.[1.21] The free energy of the Ni atom is lower at the $NiSi_2$/α-Si interface than at the $NiSi_2$/c-Si interface, whereas the free

energy of the Si atom is lower at the $NiSi_2$/c-Si interface. Therefore, with the dissociative model,[1.21] the $NiSi_2$ layer dissociates to provide free Si for epitaxial growth of c-Si at the c-Si/$NiSi_2$ interface by the diffusion of Ni atoms. The Ni atoms diffuse to α-Si following by formation of a fresh $NiSi_2$/α-Si interface. Repetition of this process results in migration of $NiSi_2$ precipitates through α-Si and growth of needlelike Si. Fig. 1-8 shows a schematic representation of a possible growth process incorporating the formation of intermediate thin layer of c-Si on the leading edge of migrating $NiSi_2$ precipitate.[1.21] As a result of this growth mechanism, NILC poly-Si films demonstrate a needlelike microstructure, with each needle grain attribute to c-Si growth from an individual disilicide precipitate.

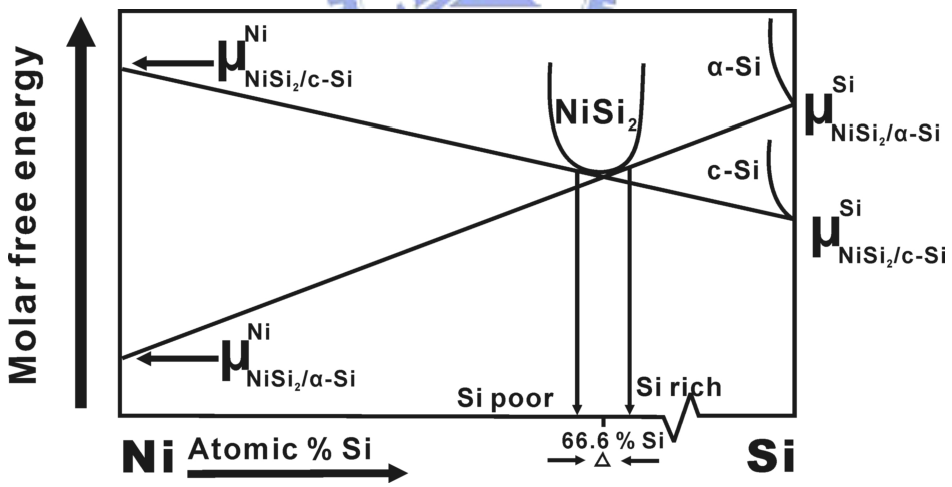

Fig. 1-7 Schematic equilibrium molar free-energy diagram for $NiSi_2$ in contact with α-Si.

In addition to Ni, other metals have been investigated as far as their effectiveness in

enhancing Si crystal growth. These include Au[1.22], Al[1.23] and Sb[1.24] which form eutectic with Si, and Pd[1.25,1.26], which form silicide with Si.

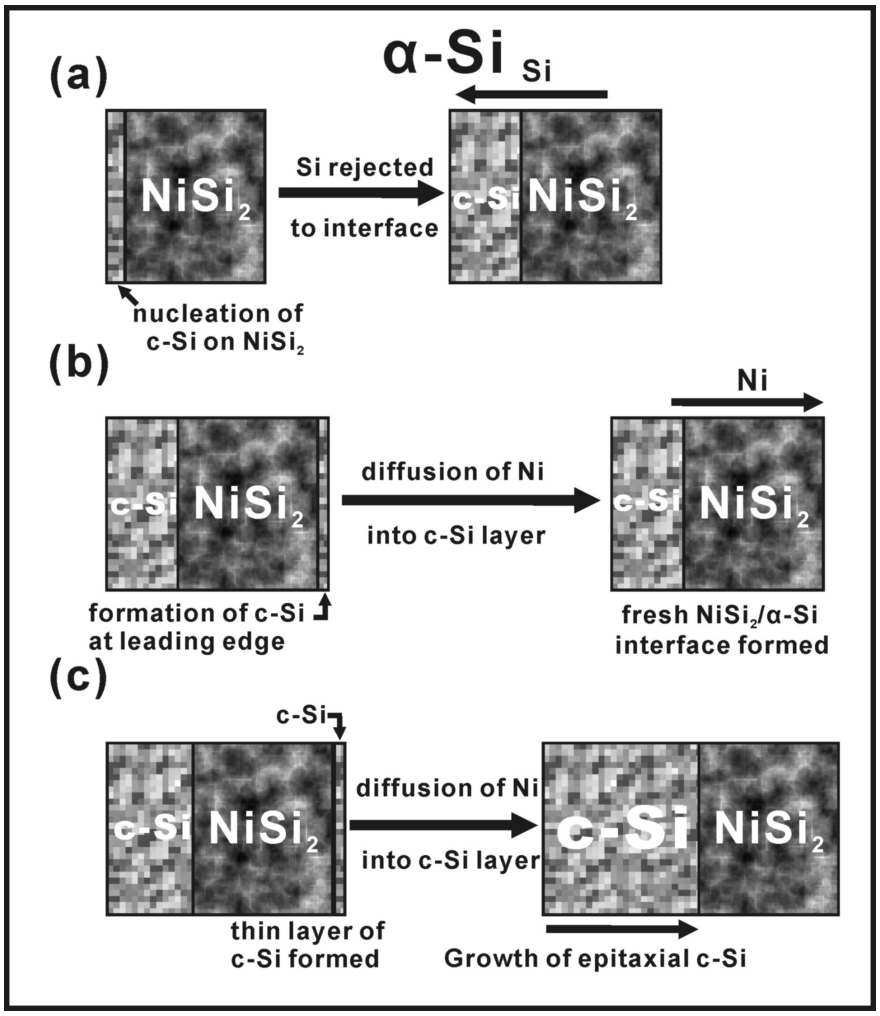

Fig. 1-8 Schematic representation of a possible growth mechanism involoving the formation of a thin layer of c-Si at the $NiSi_2$/α-Si interface.

As a result, Ni remains the undisputed metal of choice for silicide-assisted crystallization. It should be noted that traces of $NiSi_2$ also remain within the c-Si that is left behind after the growth phase. This would have presented an insurmountable obstacle had it not been for the existence of an efficient gettering process.[1.27,1.28] This process utilizes the implantation of phosphorous, followed by low-temperature annealing to generate electrically inactive compounds. Previous studies have demonstrated the effectiveness of the gettering process in removing the remaining silicide in the film after Si crystallization.[1.20,1.29] In practice, the necessity to maintain a low processing temperature poses certain limitations on the quality of the poly-Si microstructure. One way to boost the poly-Si quality is by combining NILC with laser annealing process [1.30,1.31] to produce high quality and good uniformity poly-Si films to realize the system-on-panel technology.[1.8,1.32-1.33]

In this thesis, we will focus on the Ni-metal induced lateral crystallization method. To discuss the growth mechanism of NILC and utilized Ni-metal imprint induced crystallization method[1.34] to fabricate the LTPS TFT. Moreover, to produce high performance LTPS TFTs by combined Ni-metal imprint and ELA method. And develop a simple method to getter the nickel impurity within the NILC polycrystalline silicon films.

1-3 Electrical Characteristics of Ni-Metal Induced Lateral Crystallization (NILC) Thin Film Transistors

The NILC method has some advantages over other crystallization methods such as: lower equipment cost, better uniformity than ELA method, and lower thermal budget than SPC method. However, several intrinsic growth characteristics of NILC method always resulted in poor TFT performance, such as higher leakage current (I_{lk}) and poor electrical stability due to large defect (trap state) density in NIC/NILC interface and NILC/NILC grain boundary and high Ni metal contamination.[1.35~1.39] Fig. 1-9 illustrates the leakage current model using band diagrams,[1.40-1.42] the first situation in Fig. 1-9 (a) is described only the thermal activation of an electron from the valence band to the conduction band. The second situation in Fig. 1-9 (b), the leakage current is induced by the trap or surface state in the band gap. With increase the drain bias, the activation energy of leakage current decreases, which suggests that the high field in the drain depletion region has reduced the barrier that the electron must overcome. This situation comprises two steps: the first step is the thermal activation of an electron from the valence band to a trap state (E_t) in the band gap, and the second step is electron tunneling through this reduced barrier to the conduction band. As such, the dominant leakage current mechanism is thermionic field emission. The third situation in Fig. 1-9 (c) is induced under strong electric field, in which the dominant leakage current mechanism is pure tunneling. With the increase of the electric field, the tunneling length decreases. The presence

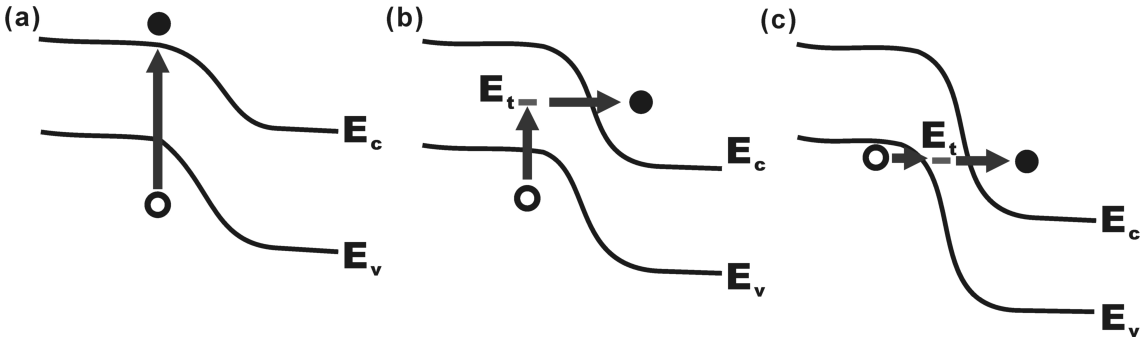

Fig. 1-9 The band diagram for the leakage current model. (a) Case of weak electric field. (b) Case of medium electric field. (c) Case of strong electric field.

of the trap state in the band gap assists the process by shorting the effective tunneling length of the electron. In addition, the trap state in the band gap plays an important role in the leakage current model. In the traditional MOSFET, those situations do not occur easily because the trap state is low. This causes different leakage current between MOSFET and TFTs.

Moreover, the Ni contamination of the NILC poly-Si films can degrade the minority carrier life time and increase the leakage current. The leakage current is proportional to the impurity concentration. [1.43,1.44]

In order to solve the above problems, the post-annealing treatment [1.30,1.45-1.47] was

proposed to reduce the NILC/NILC grain boundary defect density. Moreover, gettering process [1.20,1.29] was proposed to reduce the Ni-metal contamination within the NILC poly-Si films. In the following, we will discuss the effects of grain boundary and Ni-metal impurity on the electrical performance of NILC TFTs.

1-4 Motivation and Thesis Organization

In this thesis, the major research subject is Ni-metal induced lateral crystallization of amorphous silicon, which involved of the tensile stress effects on the NILC growth mechanism. It has been reported that the Ni-metal imprint method introduced a tensile stress, while the crystallization process and the incubation time could be reduced by tensile stress. However, the detail of the tensile stress effects on the growth mechanism of NILC has still not been clarified. In addition, in this study, we chose the Ni-metal imprint-induced crystallization method due to it exhibited many superior characteristics over traditional NILC method, such as: higher growth rate, better crystallization quality and less branch needle-like grain microstructure. But, between the NILC/NILC needle-like gains contained many un-crystallized region; these intra-grain defects can degrade the device performance. Therefore, combine NILC and ELA method to gather the advantages of each method, producing the high performance TFTs device. Finally, the most important issue for the NILC poly-Si film is the Ni-impurity contamination. To develop a simple gettering method for reduced the Ni-impurity within the NILC poly-Si films.

In chapter 2, the influence of tensile stress on the growth of NILC of α-Si was investigated by using a simple bending fixture. Before the growth of needlelike poly-Si grains, there must be an incubation period, which included (1) the formation of $NiSi_2$ and (2) the nucleation of c-Si on $NiSi_2$. It has been reported that the incubation time could be reduced by tensile stress.

However, the detail of the tensile stress effects on the growth mechanism of NILC has still not been clarified. The principal goal of this research, therefore, was to develop a series of two-step annealing processes to study the effects of tensile stress on these three stages of NILC growth.

In chapter 3, using the Ni-metal imprint method to crystallized α-Si and fabricated the TFTs device. For traditional NILC method, Crystalline Si nucleates on {111} faces of $NiSi_2$. The crystallization of needlelike Si grains proceeds via the migration of nickel silicides through α-Si. The orientation of needle grain is <111>. Unfortunately, the NILC poly-Si film has intra-grain defects and some un-crystallized regions between poly-Si grains. In this chapter, these defects were reduced by Ni-metal imprint induced crystallization method. In Ni-metal imprint method, a thin Ni metal layer was deposited on the imprint mold. The mold and α-Si film were then pressed together and annealed at 550°C. The orientation of Ni-metal imprint needle grains is <112>, which differed from that of NILC needle grains <111>. Therefore, the principal goal of this chapter has been to investigate the performances of TFTs fabricated by <112> and <111> needle grains.

In chapter 4, among various crystallization technologies, excimer laser crystallization (ELA) and Ni-metal induced lateral crystallization have shown to be most two promising techniques to produce high quality poly-Si thin films at low temperature. There are still some problems about those two methods, especially for LTPS TFTs applications. In this study, combining the

Ni-metal imprint and ELA method, to produce high quality poly-Si films with good uniformity and reduced the intra-grain defect density within the NILC poly-Si films using excimer laser for post-crystallization to improve the electrical characteristics.

Some intrinsic growth characteristics of NILC technique can degrade the performance of TFTs device._As mention in the last chapter, the intra-grain defects can be reduced using post-crystallization technique. Besides, the reduction of Ni contamination within the NILC poly-Si films is also a very important issue. Therefore, in chapter 5, two gettering methods have been utilized to reduce the Ni impurity within the NILC poly-Si film. Those two gettering process are uncomplicated, one is using a SiNx/α-Si and the other is using α-Si/Si substrate as the gettering material. Use the un-doped silicon layer to prevent other impurity contamination and more compatible for the TFTs fabrication process.

Finally, conclusions as well as the recommendation for the further research are given in Chapter 6.

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Chapter 2 Effects of Tensile Stress on Growth of Ni-Metal Induced Lateral Crystallization of Amorphous Silicon

2-1 Growth Mechanism of Ni-Metal Induced Lateral Crystallization (NILC)

Three stages have been identified in the NILC process: (1) the formation of $NiSi_2$ precipitates, (2) the nucleation of crystalline silicon (c-Si) on $NiSi_2$ precipitates, and (3) the subsequent migration of $NiSi_2$ precipitates and growth of c-Si.[2.1,2.2] The first stage, the formation of $NiSi_2$ precipitates, is a diffusion-controlled process. When a precipitate nucleates, nickel depletion occurs around the precipitate. As for stages (2) and (3), the nucleation and growth of c-Si, they are mediated by $NiSi_2$ precipitates. Crystalline Si nucleates on one or more of the eight {111} faces of octahedral $NiSi_2$. The crystallization of needlelike Si grains proceeds via the migration of nickel silicides through α-Si.

The driving force for the migration of $NiSi_2$ precipitates is reduction in the free energy associated with the transformation of meta-stable α-Si to stable c-Si. An equilibrium free-energy diagram is provided for explanation, as shown in Fig. 2-1.[2.2] It is well known

that the α-Si has a higher free energy than c-Si. In the case of Ni silicide mediated crystallization, the free energy difference between Ni and Si atoms at the $NiSi_2$/α-Si and $NiSi_2$/c-Si interface acts as the driving force for Ni diffusion.[2.2] The free energy of the Ni atom is lower at the $NiSi_2$/α-Si interface than at the $NiSi_2$/c-Si interface, whereas the free energy of the Si atom is lower at the $NiSi_2$/c-Si interface. Therefore, with the dissociative model,[2.2] the $NiSi_2$ layer dissociates to provide free Si for epitaxial growth of c-Si at the c-Si/$NiSi_2$ interface by the diffusion of Ni atoms. The Ni atoms diffuse to α-Si following by formation of a fresh $NiSi_2$/α-Si interface. Repetition of this process results in migration of $NiSi_2$ precipitates through α-Si and growth of needlelike Si.

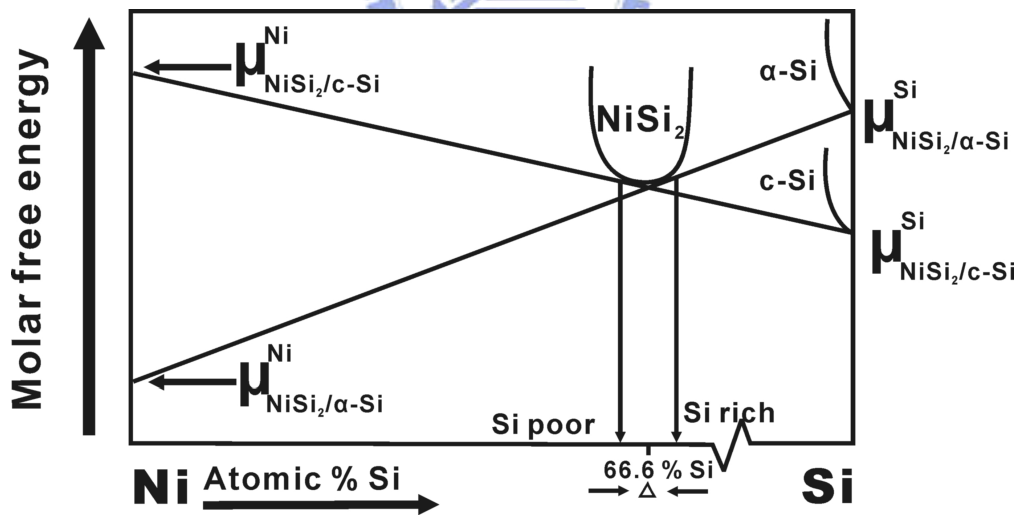

Fig. 2-1 Schematic equilibrium molar free-energy diagram for $NiSi_2$ in contact with α-Si.

Before the growth of needlelike poly-Si grains, there must be an incubation period, which included (1) the formation of $NiSi_2$ and (2) the nucleation of c-Si on $NiSi_2$. It has been reported that the incubation time could be reduced by tensile stress.[2.3] However, the detail of the tensile stress effects on the growth mechanism of NILC has still not been clarified. The principal goal of this research, therefore, was to develop a series of two-step annealing processes to study the effects of tensile stress on these three stages of NILC growth.

2-2 Experimental Procedure

2-2-1 Features of the Bending Fixture

In this study, the tensile stress on the silicon film was introduced to the sample using a stainless bending fixture as shown in Fig. 2-2 (a). It is a simple equipment, without any vacuum or pumping system like the previous study.[2.4,2.5] The tensile stress was characterized by laser Raman spectroscopy on the basis of the extra shift of a Raman frequency. Since the Raman peak of α-Si was too broad and too weak to measure the difference, a single-crystal Si(100) sample was used to measure the peak shift. The Raman shift for a bended Si substrate (519.9 cm^{-1}) was smaller than that for a stress-free Si substrate (520.437 cm^{-1}). The stress in a bended Si substrate estimated from an extra peak shift was 241 MPa.[2.6] The actual stress, however, could not be determined because both the Si substrate and the Si film undergo plastic deformation at elevated temperatures. These samples were

designated as ‘‘BENDED’’. For the purpose of comparison, other samples were also annealed under the same conditions but without tensile stress. They were labeled as ‘‘UNBENDED’’. For the purpose of comparison, as shown in Fig. 2-2 (b), when the sample was turned upside down, a compressive stress was introduced to the Si film.

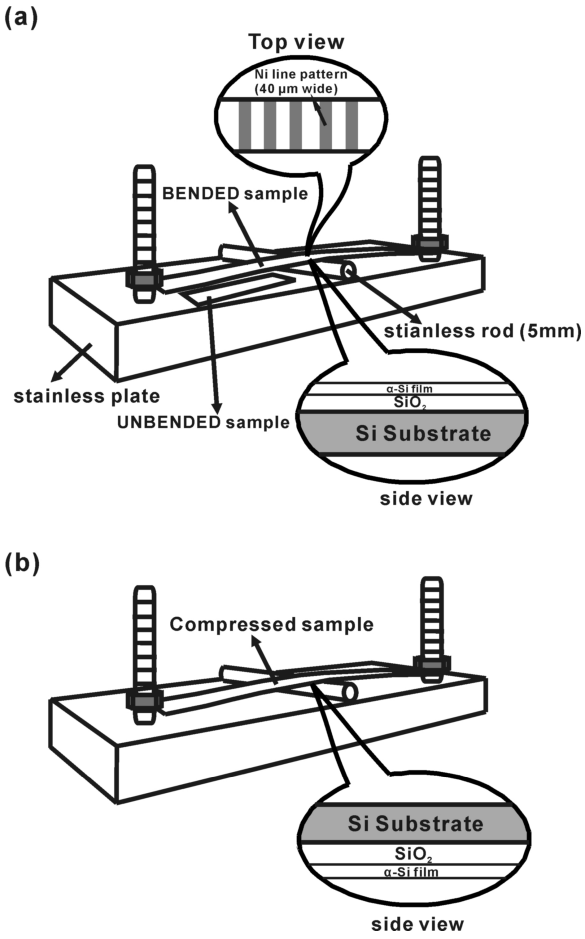

Fig. 2-2 Schematic illustration of stainless bending fixture, (a) BENDED (tensile) sample and UNBENDED sample, and (b) compressed sample. The side view shows the sample structure and the top view the location of the Ni line pattern.

2-2-2 Preparation for the Bending Sample

As shown in Fig. 2-3, silicon (100) wafers were used as the substrates in this study. Wet oxide films of 500 nm thickness were grown using a H_2/O_2 mixture at a substrate temperature of 1050°C. Silane-based α-Si films with a thickness of 100 nm were then deposited using a low-pressure chemical vapor deposition (LPCVD) system at 550°C. The photoresist was then patterned to form the desired Ni features, and a 10-nm-thick Ni film was deposited on α-Si by the sputtering method. After samples were dipped into acetone and ultrasonic bath for 5 min, Ni deposited on the photoresist was removed together with the photoresist. The wafers were then cut into 1×9 cm^2 samples and placed on the bending fixture; the samples were subsequently annealed at 550°C.

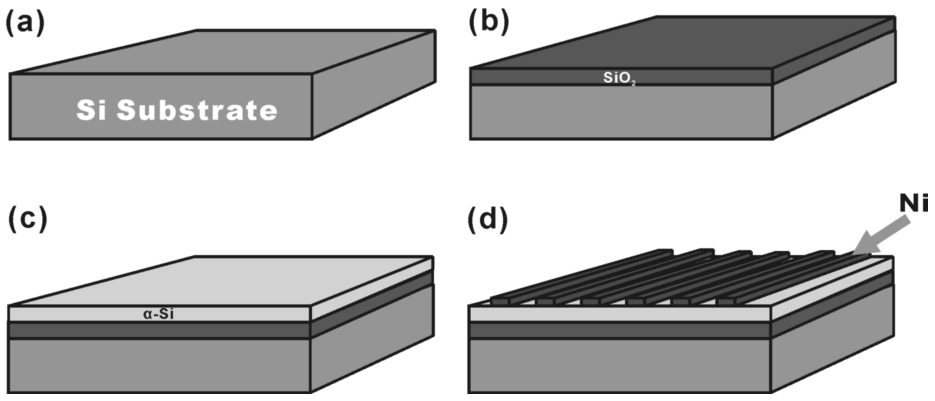

Fig. 2-3 Flow chart of the sample preparation.

2-3 Results and Discussion

2-3-1 OM and SEM Analysis

Figure 2-4 (a) shows the NILC poly-Si induced by 40-μm-wide Ni lines after 6 h of annealing. The light region at the periphery of the Ni lines was the poly-Si area. After dipping in the Secco solution,[2.7] the samples were examined by SEM. A typical SEM image of the NILC front region is shown in Fig. 2-4 (b). The morphologies of UNBENDED samples were similar to those of BENDED (tensile) samples. The only difference was that the NILC length of BENDED samples was 26 μm, which was longer than that of UNBENDED samples, 22 μm. The tensile stress did increase NILC rate.

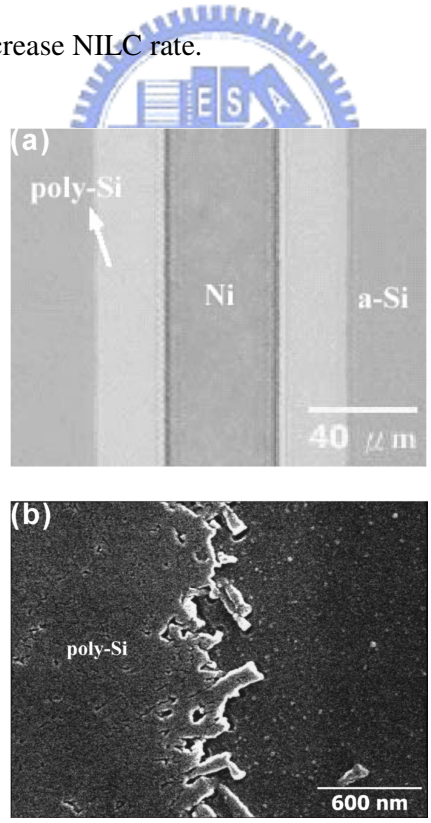

Fig. 2-4 (a) Optical microscopy image of BENDED sample annealed at 550°C for 6 h. (b) SEM image of NILC front region of BENDED sample annealed at 550°C for 6 h.

However, the NILC crystal length of BENDED samples was dependent on the position of Ni lines. As shown in Fig. 2-5, the NILC length was 26 μm for the Ni lines located at the center of the Si substrate, while it decreased to 22 μm for the Ni lines located near the edge of the Si substrate. This is because, with our stainless fixture, most of the bending force is applied on the center of the samples. Not much stress is applied near the edge of the Si substrate. Therefore, NILC length near the edge of the Si substrate did not increase.

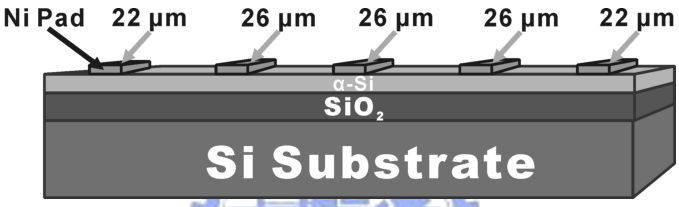

Fig. 2-5 Illustration of the NILC growth length (BENDED sample) related to the position of Ni lines.

The NILC length of BENDED samples was also dependent on the direction of the Ni lines. As shown in the Fig. 2-6, the induced NILC length of Ni lines parallel to the bending direction (26 μm) was longer than that of Ni lines perpendicular to the bending direction (22 μm), which was equal to the UNBENDED sample. This is because in the pure bending, the stress perpendicular to the bending direction is equal to zero.[2.8]

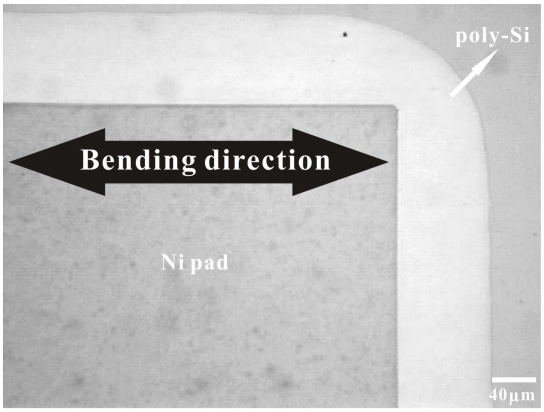

Fig. 2-6 Optical microscopy (OM) image of the NILC growth length (BENDED sample) related to the direction between Ni line and bending direction.

2-3-2 A Series Two-Step for NILC

As mentioned previously, the NILC growth mechanism involved three stages. The enhancement of NILC length observed in our BENDED (tensile) samples might have resulted from two mechanisms: (1) reduction in NILC incubation time (included $NiSi_2$ formation and c-Si nucleation stages) and/or (2) increase in c-Si growth rate. In order to test the effects of tensile stress on those three stages of the NILC growth mechanisms, a series of two-step annealing processes were used in this work. The details of these processes are listed in Table I. Samples were first annealed under either an UNBENDED or a BENDED condition for 6 h. Each set of samples was then annealed again either in an UNBENDED or a BENDED condition for another 6 h. They were labeled as ‘‘UNBENDED–UNBENDED’’, ‘‘UNBENDED–BENDED’’, ‘‘BENDED–UNBENDED’’ and ‘‘BENDED–BENDED’’.

Table I Summary of two-step annealing processes for NILC of α-Si.

	Annealing condition (NILC length)	Total NILC length (μm)
UNBENDED-UNBENDED	U 6h (22μm)+U 6h (22μm)	44
UNBENDED-BENDED	U 6h (22μm)+B 6h (26μm)	48
BENDED-UNBENDED	B 6h (26μm)+U 6h (22μm)	48
BENDED-BENDED	B 6h (26μm)+B 6h (22μm)	48

As shown in Table I, in the first UNBENDED annealing step, the NILC lengths of both UNBENDED–UNBENDED and UNBENDED–BENDED samples were the same. Then samples were annealed again under either an UNBENDED or a BENDED condition for another 6 h. In the second annealing step, the extra NILC length of the UNBENDED–BENDED sample was 26 μm, which was longer than that of the UNBENDED–UNBENDED sample (22 μm). In this annealing step, there was no need for $NiSi_2$ formation and c-Si nucleation; NILC growth rate was only dependent on c-Si growth rate. Therefore, the tensile stress in the second step must have increased c-Si growth rate, which increased NILC growth length.

However, in the second annealing step of BENDED–UNBENDED and BENDED–BENDED samples, the extra NILC lengths of both samples were the same, 22 μm. As described in the previous section, if there had been any tensile stress, c-Si growth rate should have increased. Thus, the absence of c-Si growth rate increase indicated that during the second BENDED annealing step, no tensile stress was applied on the BENDED–BENDED

sample. The decrease in tensile stress is not surprising since the yield stress of Si is only about 100 MPa at 550°C,[2.9] which is much less than the applied stress 241 MPa. The effective tensile stress on the Si film vanished due to plastic deformation. This plastic deformation was confirmed by the observation of the samples after the first BENDED annealing step as shown in Fig. 2-7. It means that the effective tensile stress in the second BENDED annealing step for BENDED–BENDED samples (applied using the bending fixture) on the Si film vanished.

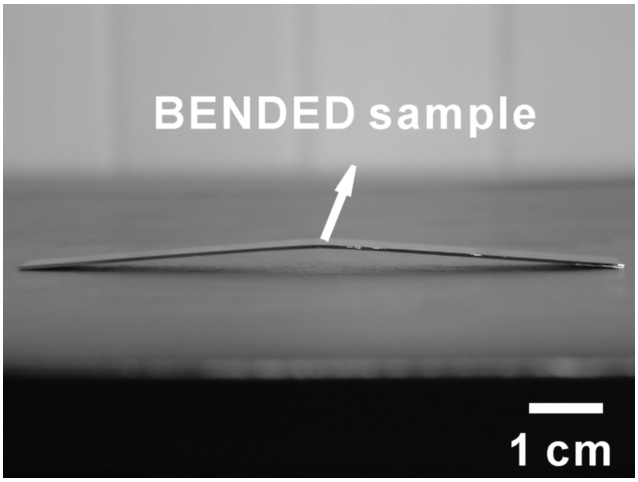

Fig. 2-7 Photograph of bended sample annealed at 550°C for 6 h. The sample was bent due to plastic deformation.

Figure 2-7 also shows that most of the plastic deformation occurred at the center of the Si substrate, and little deformation occurred at the edge of the substrate. That is, not much stress was applied near the edge of the Si substrate. This behavior is consistent with our previous

observation of various NILC lengths in different positions on the Si substrate. The induced NILC length near the edge of the bended Si substrate did not increase.

In order to study the effects of annealing time on the NILC growth mechanisms, the NILC lengths of the UNBENDED and BENDED samples are plotted as a function of annealing time in Fig. 2-8.

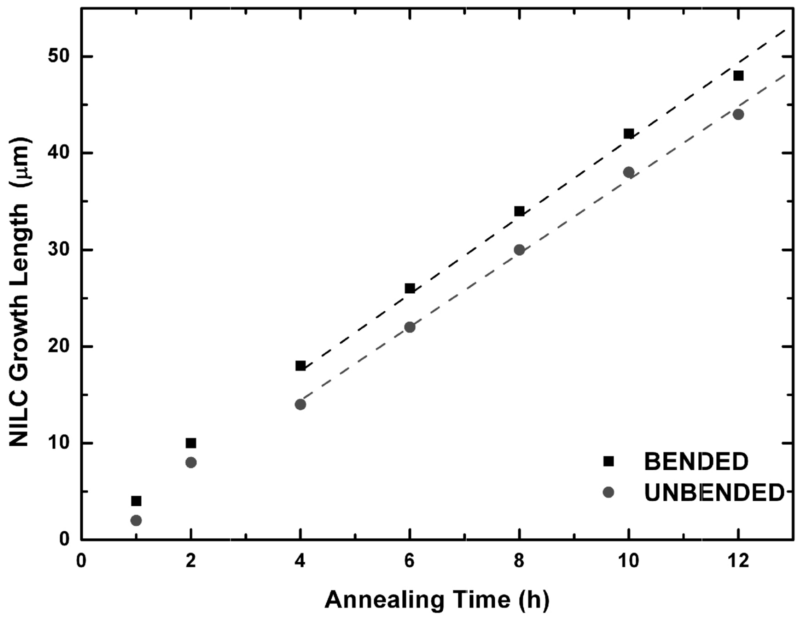

Fig. 2-8 NILC growth length as function of annealing time.

It was found that the lateral growth lengths of BENDED samples were always higher than those of UNBENDED samples. The NILC length difference between the BENDED and UNBENDED samples increased with annealing time. However, when the annealing time exceeded 4 h, the NILC length difference between these two samples was constant (4 μm).

However, the slope of the curve shown in Fig. 2-8 could be used to estimate NILC rate as a function of annealing time. It clearly shows that the growth rates (slope) of the UNBENDED and BENDED samples are the same when the annealing time exceeds 4 h. As mentioned previously, tensile stress would increase c-Si growth rate, and the effective tensile stress would vanish due to plastic deformation. These observations clearly showed that the effective tensile stress on the BENDED sample vanished when the annealing time exceeded 4 h.

2-3-3 Mechanism for the Effects of Tensile Stress on the Growth of NILC

From this observation, the increase in c-Si growth rate caused by tensile stress is considered as follows. It has been reported that the growth of NILC is governed by the migration of $NiSi_2$ precipitates through α-Si as illustrated in Fig. 2-9 (a),[2.2,2.10,2.11] Hayzelden and Batstone[2.2] suggested that the driving force behind NILC is that the chemical potential of Ni is lower at the $NiSi_2$/α-Si interface, whereas the chemical potential of Si atoms is lower at the $NiSi_2$/c-Si interface. In order to decrease free energy, the Ni atoms should move toward a-Si and they in turn react with α-Si to form new $NiSi_2$. The remaining Si atoms attach to the $NiSi_2$ template to form c-Si because their chemical potential is lower at the $NiSi_2$/c-Si interface. Hayzelden and Batstone[2.2] also showed that growth velocity is

inversely proportional to $NiSi_2$ thickness, which agrees with diffusion-limited growth. In other words, the growth of NILC is governed by Ni diffusivity in $NiSi_2$. The diffusivity in materials can be affected by tensile stress.[2.12] As illustrated in Fig. 2-9 (b), when a Ni atom diffuses through $NiSi_2$, the Ni atom must pass through a non-equilibrium position, which distorts considerably the positions of adjacent atoms and form an activated complex. This distortion will have an energy cost, so the energy will have a maximum as the atom moves from one site to another as shown in Fig. 2-9 (c). With the increase in tensile stress, we believe that the space between atoms may change and the maximum energy required forming the activated complex decreases. These changes might be the reason why in our BENDED sample, Ni diffusivity in $NiSi_2$ increased, which resulted in an enhancement of c-Si growth. For the purpose of comparison, as shown in Fig. 2-2 (b), a compressed α-Si film was also heated under the same conditions to investigate the effect of compressive stress on NILC growth. It was found that the NILC length of the compressed α-Si film was equal to that of the UNBENDED (stress free) sample. In other words, the compressive stress did not change (suppress) NILC growth rate. It is well known that the density of α-Si is similar to that of c-Si.[2.13] With such a high atomic density, the applied compressive stress might not change much of the space between atoms and it is suggested that the applied compressive stress might not change Ni diffusivity in $NiSi_2$.

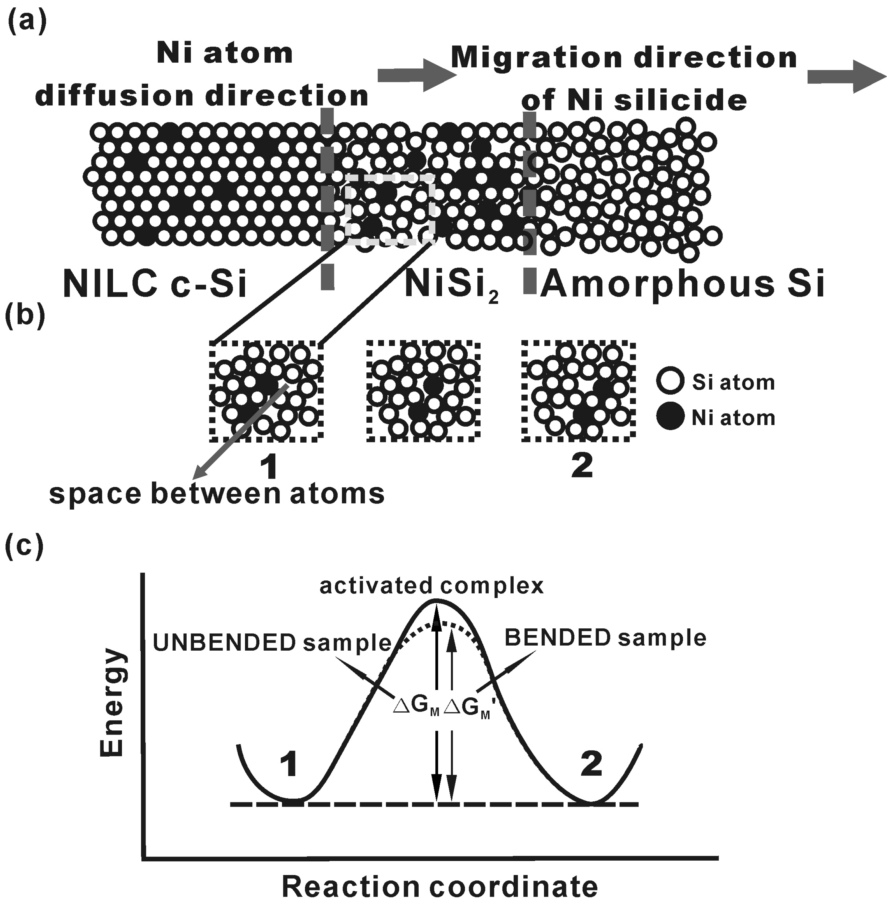

Fig. 2-9 NILC poly-Si formation mechanism. (a) shows that Ni atoms and $NiSi_2$ diffuse/migrate to the a-Si region. (b) shows the schematic illustration of the atomic jump process. (c) shows the schematic illustration of free energy as a function of reaction coordinate as an atom moves from one site to another. In this case the reaction coordinate corresponds to the distance along the path connecting the sites.

2-4 Summary

The effects of tensile stress on the growth of Ni–metal induced lateral crystallization (NILC) of α-Si were investigated. This was accomplished by annealing samples in a bending fixture. It was found that tensile stress did not affect the morphologies of needlelike Si grains, but enhanced the NILC growth rate. A series of two-step annealing processes were introduced to study the effects of tensile stress on three stages of the NILC process: (1) $NiSi_2$ formation, (2) c-Si nucleation and (3) c-Si growth. It was found that tensile stress did not enhance $NiSi_2$ formation and c-Si nucleation stages, but enhanced the c-Si growth stage.

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Chapter 3 Performance of NILC Thin Film Transistors with <111> and <112> Needle Grains

3-1 Different Method for Ni-Metal Induced Lateral Crystallization of Amorphous Silicon

Three stages have been identified in the NILC process: (1) the formation of $NiSi_2$ precipitates, (2) the nucleation of crystalline silicon (c-Si) on $NiSi_2$ precipitates, and (3) the subsequent migration of $NiSi_2$ precipitates and growth of c-Si.

As shown in Fig. 3-1, for the conventional NILC method, a thin Ni-metal film was selectively deposited on the top of α-Si and then annealed at temperature below 600°C, subsequently. The poly-Si forming below the metal film is called “NIC”, and that forming outside the metal coverage is called “NILC”. The first stage, the formation of $NiSi_2$ precipitates, is a diffusion-controlled process. As for stages (2) and (3), the nucleation and growth of c-Si, they are mediated by $NiSi_2$ precipitates. Crystalline Si nucleates on {111} faces. The crystallization of needlelike Si grains proceeds via the migration of nickel silicides through α-Si. The orientation of the needlelike Si grains is <111>. Unfortunately, the NILC

poly-Si film has intra-grain defects and some un-crystallized regions between poly-Si grains.

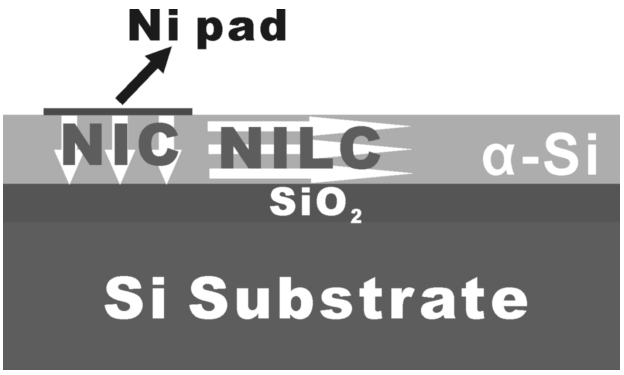

Fig. 3-1 Schematic illustration of the Ni-metal induced Crystallization (NIC) and Ni-metal induced lateral crystallization (NILC).

In this study, these defects were reduced by Ni-metal imprint-induced crystallization.[3.1-3.3] As shown in Fig. 3-2, for the Ni-metal imprint-induced crystallization, a thin Ni metal layer was deposited on the imprint mold. The mold and α-Si film were then pressed together and annealed at 550°C. The orientation of the Ni-metal imprint needlelike Si grains is <112>, which differs from that of the NILC needlelike Si grains, <111>. Therefore, the principal goal of this research has been to investigate the performances of TFTs fabricated using <112> and <111> needlelike Si grains. As shown in Table I, two kinds of TFT were used in this study. Samples designated "111-TFT" were TFTs fabricated by traditional NILC, whose poly-Si grain growth direction is <111>, whereas samples designated "112-TFT" were fabricated by Ni-metal imprint method, whose growth direction is <112>.

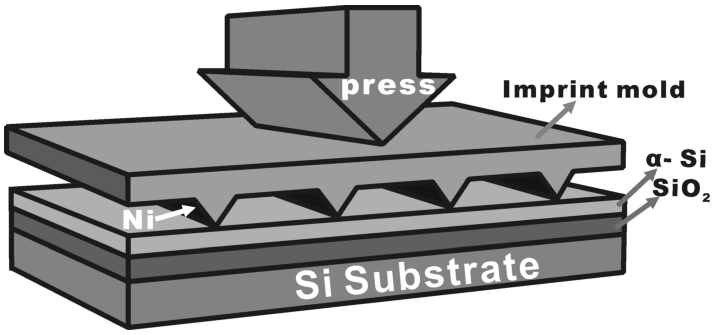

Fig. 3-2 Schematic illustration of Ni-metal imprint method.

Table I Specifications and fabrication methods of 111-TFT and 112-TFT.

	Fabrication method
111- TFT	Traditional NILC
112- TFT	Ni-metal imprint-induced crystallization

3-2 Experimental Procedure

In this study, for fabrication of both TFTs, the basic process of 112-TFT were the same as those of fabricating 111-TFT. Silicon (100) wafers were used as the substrates. Wet oxide films of 500 nm thickness were grown using a H_2/O_2 mixture at a substrate temperature of 1050°C. Silane-based α-Si films with a thickness of 100 nm were then deposited using a low-pressure chemical vapor deposition (LPCVD) system at 550°C.

3-2-1 Preparation of the of the Imprint Mold

Figure 3-3 shows the imprint mold fabrication process flow. Silicon (100)-orientation wafers were used to fabricate the imprint mold. Wet oxide films of 500 nm thickness were grown using a H_2/O_2 mixture at a substrate temperature of 1050°C to serve as hard mask for wet etching. The wet oxide layer was patterned in stripe shape by photolithography and removed using buffer-oxide etching (BOE) solution. Then, the molds were prepared by wet chemical etching using potassium hydroxide (45 wt%) solution at 70°C.[3.4,3.5] Figure 3-4 shows the SEM image of imprint mold.

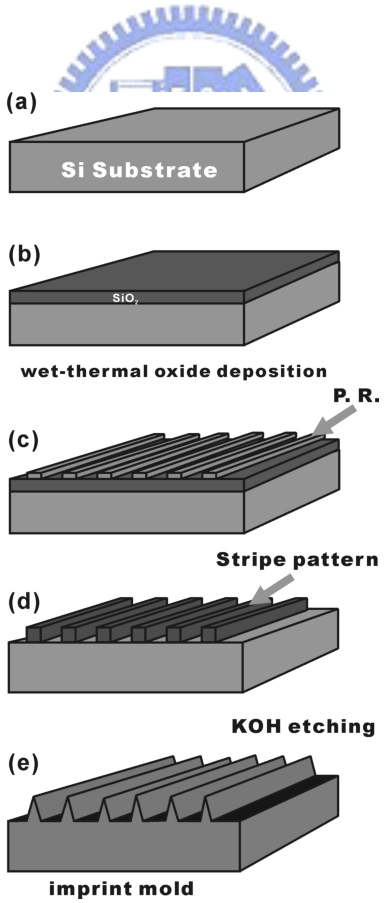

Fig. 3-3 Imprint mold preparation process flow.

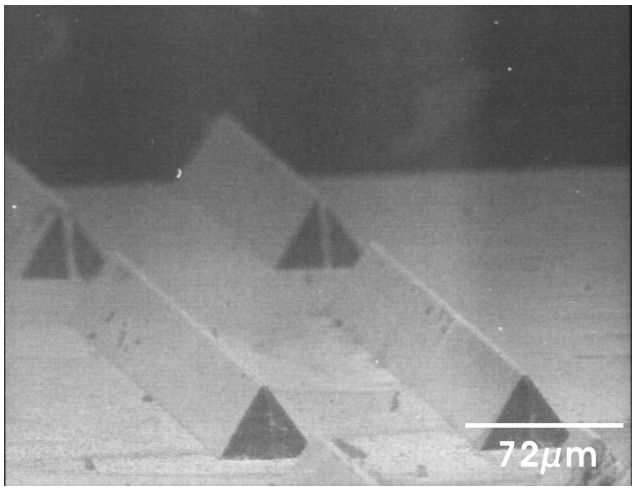

Fig. 3-4 SEM image of imprint mold.

3-2-2 Fabrication of 111-TFTs and 112-TFTs

For the fabrication of 111-poly-Si, a 2-nm-thick Ni film was selectively deposited on the top of α-Si film, which was followed by crystallization at 550°C. The fabrication of 112-poly-Si is illustrated in Fig. 3-2. A 2-nm-thick Ni film was then deposited on the imprint mold. The imprint mold and α-Si film were then pressed in a differential thermal expansion apparatus,[3.6] which was followed by annealing at 550°C for 24 h in argon ambient. An OM image of 112-poly-Si is shown in Fig. 3-5; the light region is the poly-Si area. The grain growth is very uniform at each imprint site.

The TFTs were then fabricated by defining the active areas on these two poly-Si films. Channels of TFTs were parallel to the longitudinal grain boundaries. A 100-nm-thick SiO_2

film, as a gate insulator, was deposited using plasma-enhanced chemical vapor deposition (PECVD). Subsequently, 150 nm poly-Si as a gate electrode was deposited using high-density plasma chemical vapor deposition (HDP-CVD). After the gate was defined, self-aligned 35 keV phosphorus ions at the dosage of 5×10^{15} ions/cm^2 were implanted to form a source/drain and a gate. The implanted dopants were activated by thermal annealing at 600°C for 24 h. Finally, a 500-nm-thick SiO_2 film was deposited using PECVD to serve as a passivation layer. Contact holes were opened through the oxide layer, 500 nm of aluminum (Al) was then deposited as the interconnection, and hydrogen plasma treatment was applied after the TFT devices were fabricated.

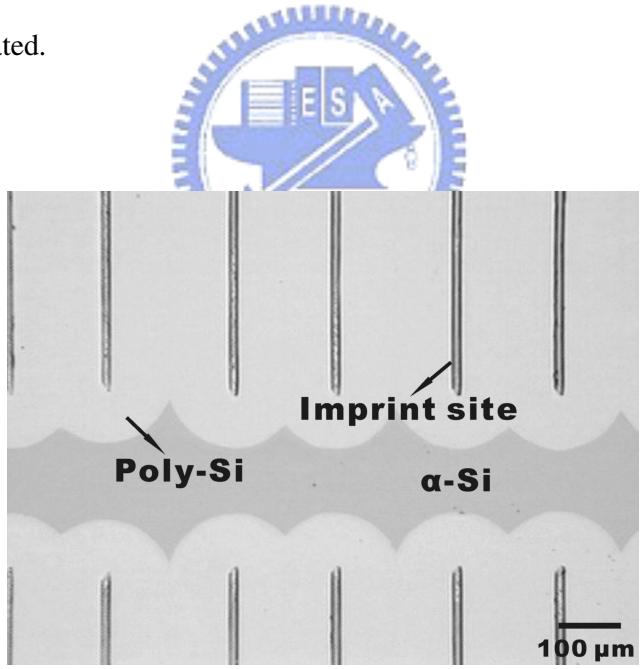

Fig. 3-5 Optical microscopy image of 112-poly-Si annealed at 550°C for 24 h.

3-3 Results and Discussion

3-3-1 Scanning Electron Microscopy (SEM) and Transmission Electron Microscopy (TEM) Analysis

Figure 3-6 shows SEM and TEM images of 111-poly-Si. Not all the α-Si film was transformed to c-Si. Some regions between the needlelike Si grains remained un-crystallized. Lots of branch grains were found. The growth direction of the needlelike Si grains was <111> and as shown in Fig. 3-7, the growth rate was about 4.6 μm/h.

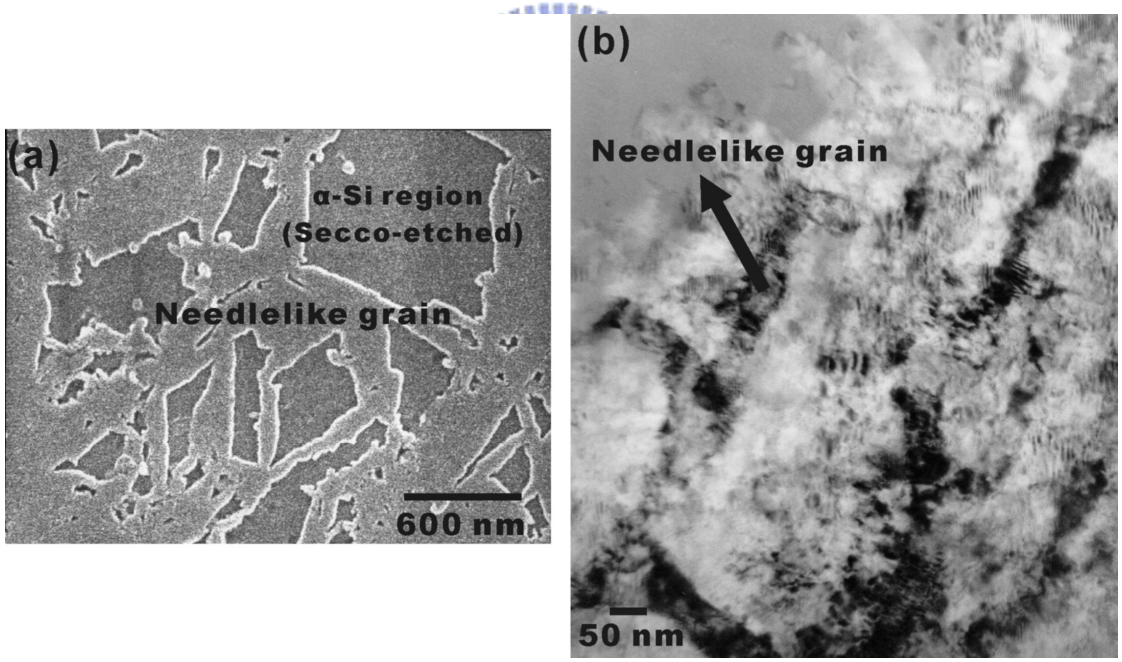

Fig. 3-6 (a) SEM image of Secco-etched 111-poly-Si film and (b) TEM image of 111-poly-Si film.

SEM and TEM images of 112-poly-Si are shown in Fig. 3-8. The diffraction pattern of the grains reveals that the grain orientation (perpendicular to the film plane) is <111> and the growth direction (parallel to the film plane) of the needlelike grains is <112>. Most of the grains were parallel to each other. Compared with 111-poly-Si, 112-poly-Si had fewer branch grains and a smaller un-crystallized α-Si region, which had been etched away using Secco solution. The growth rate (Fig. 3-7) of 112-poly-Si was about 5.3 μm/h, which was higher than that of 111-poly-Si.

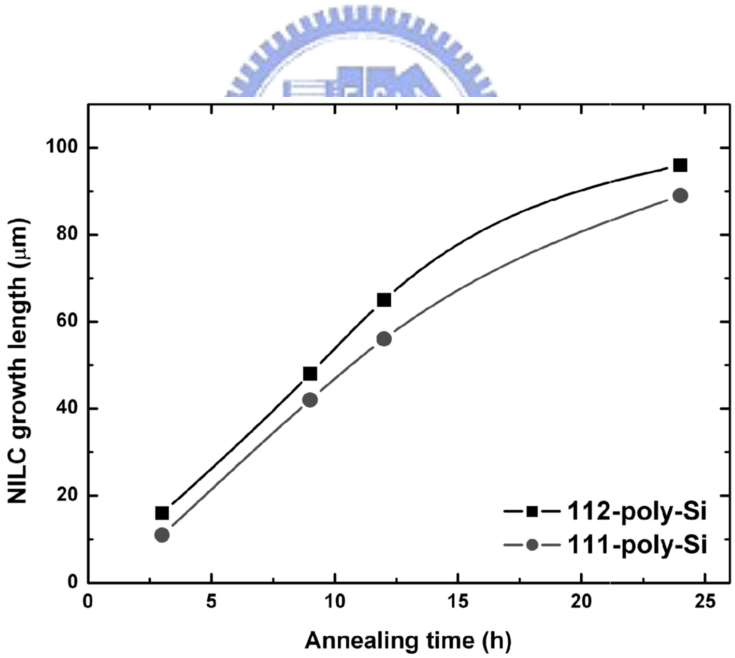

Fig. 3-7 NILC growth length as a function of annealing time. For different crystallization method involved of 112-poly-Si and 111-poly-Si.

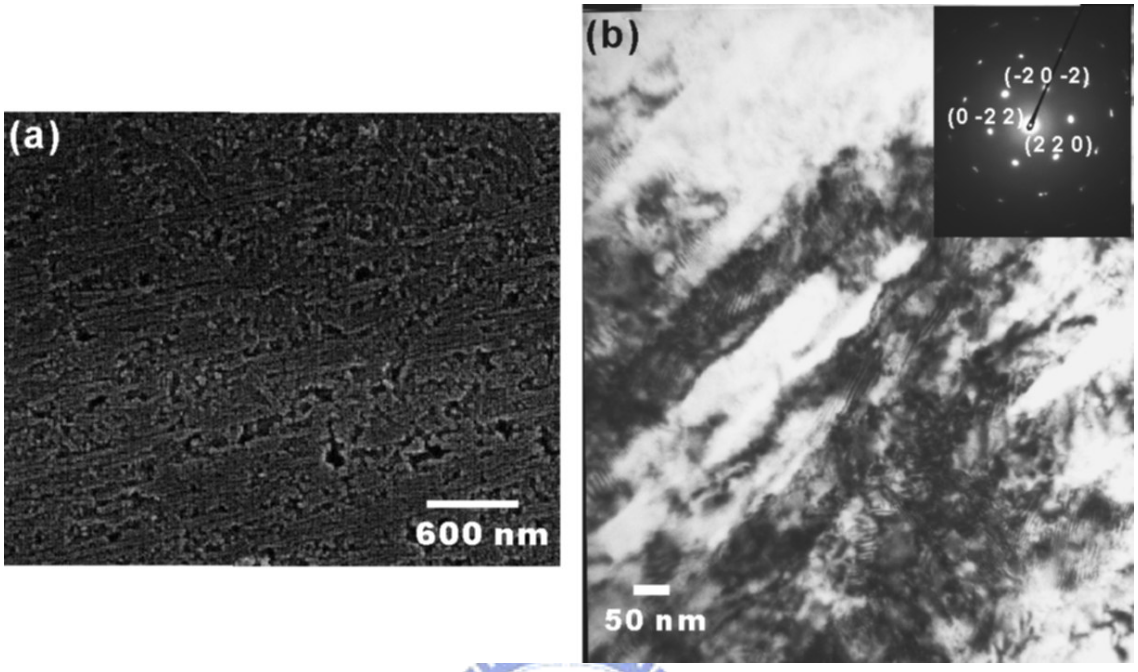

Fig. 3-8 (a) SEM image of Secco-etched 112-poly-Si film and (b) TEM image of 112-poly-Si film. Compared with 111-poly-Si, 112-poly-Si had fewer branch grains and less un-crystallized α-Si. The preferred direction of needlelike Si grains was <112>, which differed from that of 111-poly-Si grains, <111>.

The different poly-Si growth mechanisms used should be the main cause of the different results. In 111-poly-Si grains, the α-Si directly under the Ni layer was completely crystallized to very small grain sizes (15–20 nm) due to the NIC mechanism.[3.7,3.8] At the edges of the Ni layer, Ni silicide nodules moved laterally into the α-Si region and induced the crystallization of α-Si. As for the 112-poly-Si, the Si crystallization mechanism was also

mediated by $NiSi_2$ precipitates, which were found in front of the 112-needle grains. However, as shown in Fig. 3-9, there was no need for the formation of NIC grains. Therefore, the 112-poly-Si had a faster growth rate than 111-poly-Si.

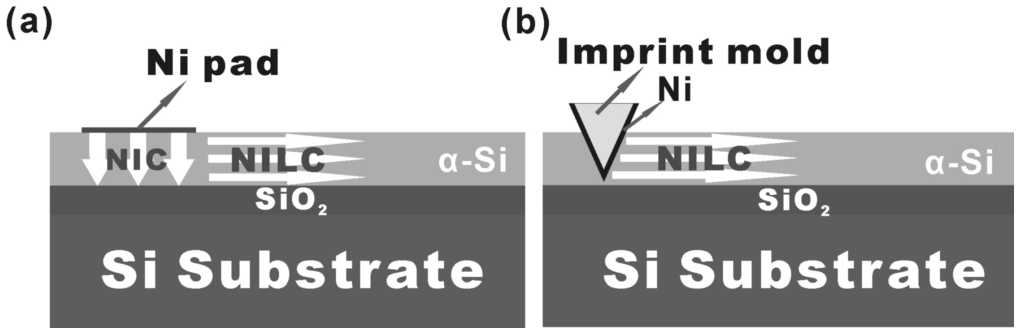

Fig. 3-9 Schematic illustration of growth mechanisms of (a) 111-poly-Si and (b) 112-poly-Si grains.

When samples were annealed at 550ºC, numerous Ni silicides were formed on the faces of the imprint-stripe patterns. These silicide nodules moved into the α-Si region and any α-Si along the path was crystallized. Therefore, as shown in Fig. 3-8, a small un-crystallized α-Si was left. Thus, the growth of branch grains was suppressed by neighbor major needlelike grains. These extra constraints of the NILC growth mechanism might be the reason why the growth direction of our Ni-metal imprint needlelike Si grains as <112>.

3-3-2 Electrical Characteristics of 111-TFTs and 112-TFTs

Figure 3-10 and Table II show the transfer characteristics (I_{DS}-V_{GS} curve) of 111-TFT and 112-TFT. The performance of 112-TFT was far superior to that of 111-TFT. Compared with 111-TFT, the field-effect mobility (μ_{FE}) was higher by a factor of 2.6, 44 compared with 117 cm^2/V-s, the on/off current ratio (I_{ON}/I_{OFF}) by a factor of 4, 2.29×10^5 compared with 9.23×10^5, the leakage current (I_{OFF}) was lower, 13 compared with 5.47 pA/μm.

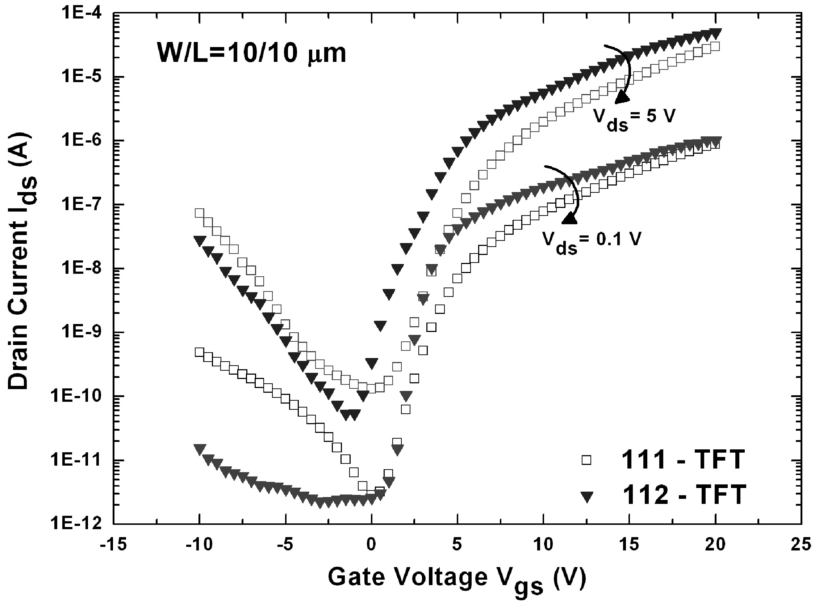

Fig. 3-10 Typical I_{DS}-V_{GS} transfer characteristic of 111-TFT and 112-TFT.

Table II Device characteristics of 111-TFT and 112-TFT.

W/L=10/10	111 - TFT	112 - TFT
Mobility(cm^2/V-s)	44	117
on/off current ratio (10^5)	2.29	9.23
Minimum leakage current /channel width(pA/μm)	13	5.47
Subthreshold slope (V/dec)	0.56	0.33
Threshold voltage (V)	3.36	2.54

As mentioned earlier, some α-Si regions remained among the poly-Si grains. These regions trap charge carriers and constitute potential barriers to the flow of carriers. The presence of these potential barriers and additional scattering at the boundaries degrade mobility.[3.9,3.10] As shown in Figs. 3 and 4, 112-poly-Si had less α-Si than 111-poly-Si. Therefore, 112-TFT had a higher μ_{FE}, a higher I_{ON}/I_{OFF}, a smaller subthreshold slope (S.S) and a lower threshold voltage (V_{th}) than 111-TFT.

Besides the effect of α-Si regions, the orientation of grain boundaries also affects the performance of TFTs. Chao *et al.*[3.11] found that NILC-TFT (111-TFT) exhibits enhanced performance compared with SPC-TFT. This was because that SPC poly-Si had a columnar grain structure with grain boundaries randomly oriented with respect to the direction of drain current (I_D).[3.10] These grain boundaries trapped charge carriers and built up potential barriers to the flow of carriers. The presence of these grain boundaries degraded μ_{FE}, S and V_{th}. These degradations could be reduced by using 111-poly-Si because many of its

longitudinal grains and their boundaries were parallel to I_d and hence impeded carrier flow less than SPC. In this study, as illustrated in Fig. 3-11, the arrangement of 112-poly-Si grains was even better than that of 111-poly-Si grains. All 112-poly-Si grains and their boundaries were parallel to each other with the exception of those that had very few branch grains between them. Therefore, the performance of 112-TFT was far superior to that of 111-TFT.

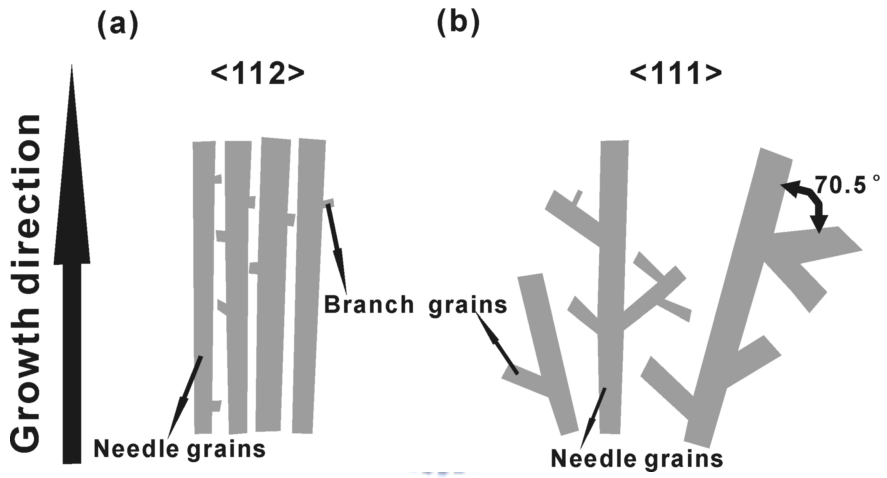

Fig. 3-11 Schematic illustration of growth of needle grains: (a) 112–poly-Si and (b) 111-poly-Si grains. All 112-poly-Si grains were parallel to each other with the exception of very few branch grains between them.

3-4 Summary

TFTs fabricated using <111> and <112> needlelike Si grains were investigated. 111-poly-Si grains were fabricated by NILC, whereas 112-poly-Si grains were fabricated by Ni-metal imprint-induced crystallization. It is found the performance of 112-TFT was far superior to that of 111-TFT. Compared with 111-TFT, the field-effect mobility (μ_{FE}) was higher by a factor of 2.6, 44 compared with 117 cm^2/V-s, and the on/off current ratio (I_{ON}/I_{OFF}) was higher by a factor of 4, 2.29×10^5 compared with 9.23×10^5 and the leakage current (I_{OFF}) was lower, 13 compared with 5.47 pA/μm. These improvements are realized 112-poly-Si has fewer branch grains and less un-crystallized α-Si than 111-poly-Si. Also, all 112-poly-Si grains and their boundaries were parallel to each other with the exception of very few branch grains between them.

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crystallization of nickel-implanted amorphous silicon thin films." J. Appl. Phys., vol. 73, pp. 8279-8289, 1993.

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Chapter 4 Comparison of LTPS TFTs Made by IMPRINT and IMPRINT-ELA Methods

4-1 The Conception of the Post Laser Treatment

The improved performance and good uniformity LTPS TFTs have been fabricated using NILC method. However, the polycrystalline silicon film are existed many NILC/NILC intra-grain defects with some un-crystallized regions between poly-Si needle grains. These defects degrade the transfer characteristics of TFT devices, including the field effect mobility (μ_{FE}) and the leakage current.[4.1-4.5] As mentioned in chapter 3, the Ni-metal imprint induced crystallization method [4.6-4.8] has many better characteristics than the traditional NILC method, including fewer branch grains and a higher grain growth rate. However, some α-Si regions are present between needle grains. As a result, in order to reduce the defect density in the poly-Si, another post annealing process seems to be required.

A high temperature (>900°C) annealing [4.9] using conventional furnace seems not compatible with low strain temperature glass substrate. As mentioned in chapter 1, the excellent electrical characteristic LTPS TFTs fabricated using ELA method suffer from poor uniformity of device performance. This is due to the narrow process window of laser

annealing.

Obviously, a high quality poly-Si films with large grains can be produced by a combination of NILC and ELA method. To gather the advantages of both crystallization methods produced high performance and good uniformity LTPS TFTs. In this study, the NILC poly-Si films was crystallized using Ni-metal imprint induced crystallization method, followed by excimer laser annealing to reduce the defect density.

4-2 Experimental Procedure

4-2-1 Fabrication of the IMPRINT-ELA Polycrystalline Silicon Films

Two types of poly-Si films were investigated in this study. Samples were designated as follows: (1) “IMPRINT” was a poly-Si film fabricated with Ni-metal imprint method, while (2) “IMPRINT-ELA” utilized the same imprint method with an additional ELA process. The imprint process is shown in Fig. 4-1 (a).

P-type (100) silicon wafers were used to fabricate imprint mold and α-Si/SiO_2/Si wafer. The imprint mold was prepared by wet chemical etching using potassium hydroxide (45wt %) solution at 70°C, the same process has been described in chapter 3. Figure 4-1(b) shows the SEM image of an imprint mold. A 2-nm-thick Ni was then deposited on the imprint mold by sputtering. As for theα-Si/SiO_2/Si, a 500 nm-thick wet thermal oxide layer was grown on the

Si wafer, and then a 100 nm silane-based α-Si film was deposited using a low-pressure chemical vapor deposition (LPCVD) system. The deposition pressure and temperature were 100 mTorr and 550°C, respectively.

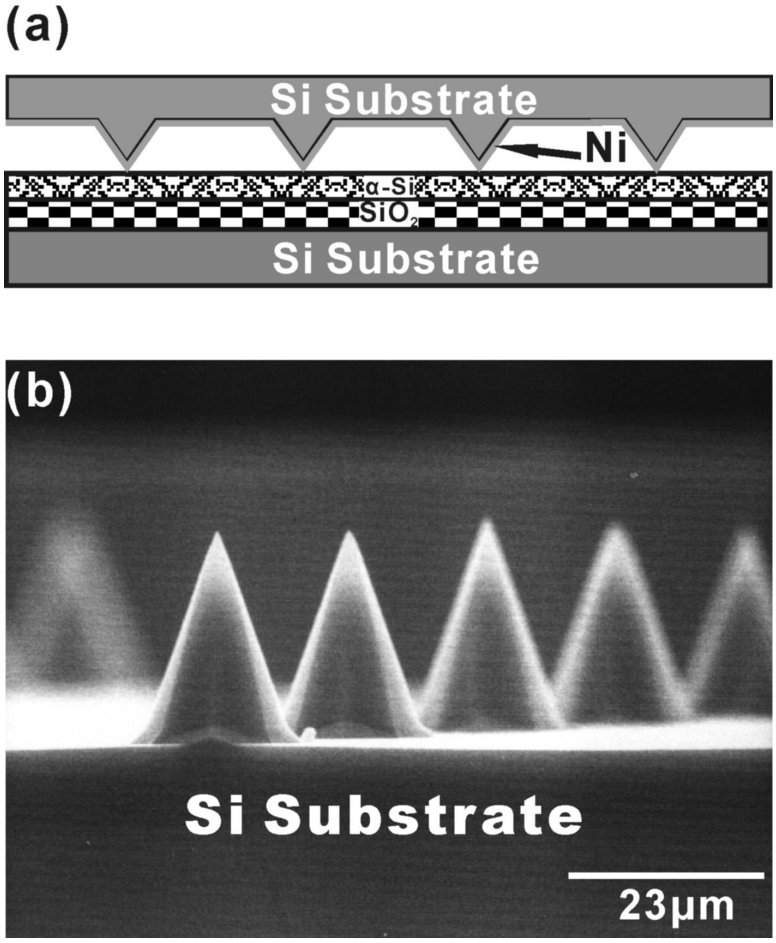

Fig. 4-1 (a) The Schematic illustration of Ni-imprint method. (b) SEM image of imprint mold.

Imprint mold and α-Si/SiO_2/Si wafer were pressed in a differential thermal expansion coefficient apparatus, made of stainless steel, molybdenum and highly pure graphite.[4.10] To fabricate the IMPRINT poly-Si, the sample stack was first clamped at room temperature and a minimal compressive load was applied; it was then annealed at 550°C for 24 h. After the sample stack was separated, as shown in Fig. 4-2, the IMPRINT poly-Si films were irradiated by a KrF excimer laser (Lambda Physik LPX-210i, λ~248 nm) at room temperature with the N_2 flow rate of 50 sccm at a pressure of 800 mtorr to fabricate the IMPRINT-ELA poly-Si films. The laser beam spot size of 1.8×23.1 mm was scanned with a 95% overlap from pulse to pulse and its repetition rate was maintained at 20 Hz. The principle setup of excimer laser crystallization system is shown in Fig. 4-3.

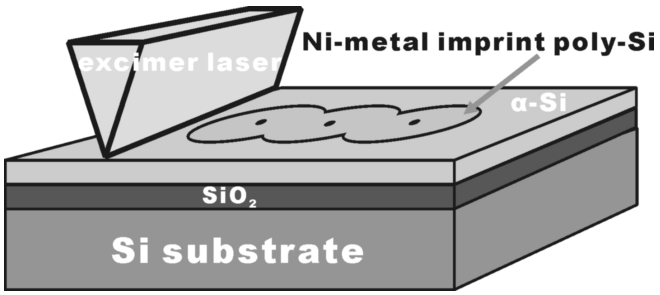

Fig. 4-2 Illustration of the Ni-metal imprint poly-Si with post excimer laser treatment process.

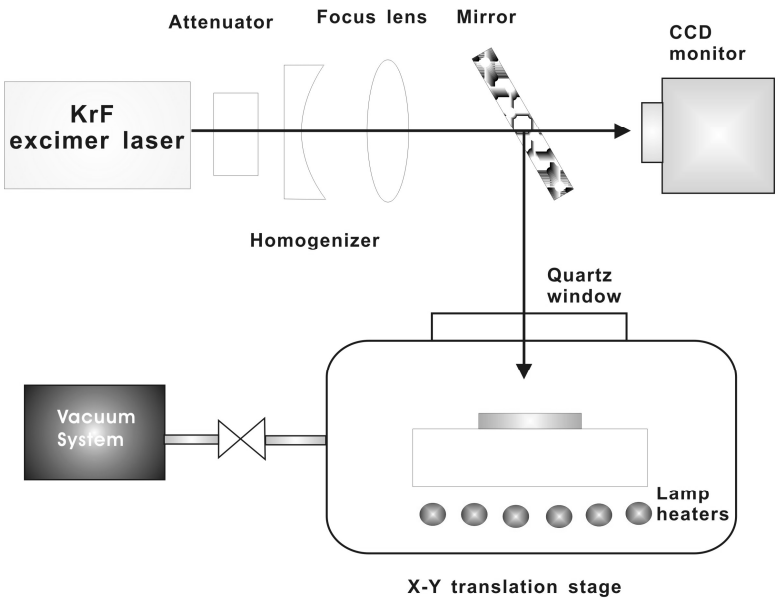

Fig. 4-3 Setup of excimer laser annealing system.

4-2-2 Fabrication of the IMPRINT-ELA TFTs

As shown in Fig. 4-4, TFTs were fabricated by patterning the Si islands as active areas on the IMPRINT and IMPRINT-ELA poly-Si films. A 100nm-thick tetraethylorthosilicate/O_2 oxide layer was deposited as the gate insulator by plasma-enhanced chemical vapor deposition (PECVD). Then, a 150nm-thick poly-Si film was deposited for gate electrodes by high-density plasma chemical vapor deposition (HDP-CVD) at 350°C. After defining the gate, self-aligned 35keV phosphorus ions were implanted at a dose of 5×10^{15} ions/cm^2 to form the source/drain and gate. The implanted dopants were activated by thermal annealing at 600°C

for 24h. A 500nm-thick SiO_2 film was deposited by PECVD to serve as a passivation layer. Contact holes were opened through the oxide layer, and 500nm of aluminum (Al) was deposited as the interconnection. In this study, the device characteristics were all intrinsic, without any hydrogen plasma treatment.

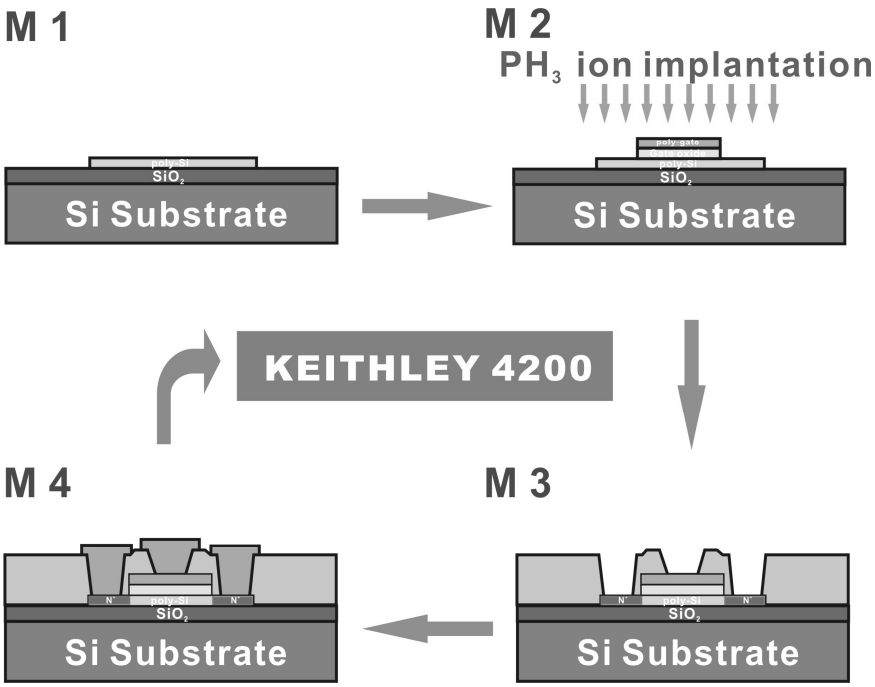

Fig. 4-4 Flow chart of TFT device fabrication process.

4-3 Results and Discussion

4-3-1 Microstructure Analysis of Polycrystalline Films

Figure 4-5 (a) shows an SEM image of the Secco-etched IMPRINT poly-Si grains.

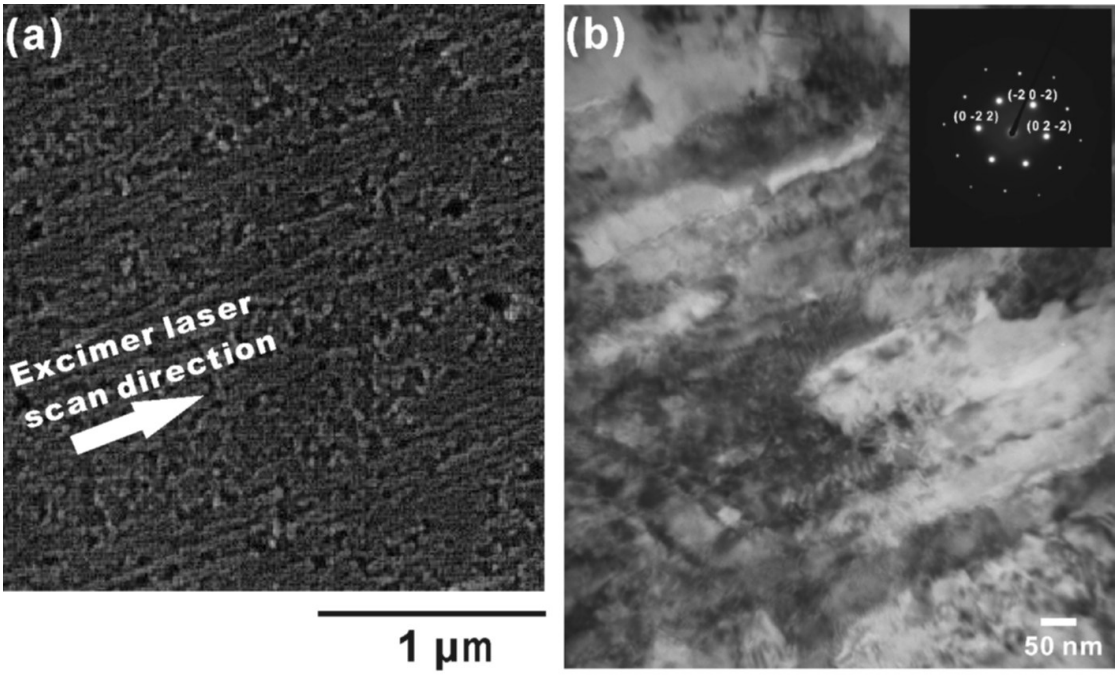

Fig. 4-5 (a) The SEM image of Secco-etched Ni-imprint poly-Si film. The needle grains were parallel to each other. (b) The TEM image and the corresponding diffraction pattern of the Ni-imprint poly-Si.

Most of the grains were parallel to each other. Only few branch grains were observed. The width of the needlelike grains was around 50nm. Among these grains remained some un-crystallized α-Si regions, which had been etched away. The TEM bright field image and

the diffraction pattern of the Ni-imprint Si grains are shown in Fig. 4-5 (b). It reveals the IMPRINT grains with <111> orientation (perpendicular to the substrate).

This result was the same as that of other imprint methods.[4.7-4.8] This orientation, however, was different from that of conventional NILC poly-Si orientation, <110>.[4.11] The diffraction pattern also reveals that the growth direction of the needlelike IMPRINT grains was along the <112>, which differed from that of conventional NILC Si grains, <111>.[4.11] These difference between the orientations of the needlelike grains influenced the growth of poly-Si; it might be the reason why only a few branch grains were found in IMPRINT films.

To fabricate IMPRINT-ELA poly-Si films, IMPRINT films were then irradiated using an excimer laser. The scan direction of the laser was parallel to the crystallization direction of needlelike poly-Si grains, <112>, as illustrated in Fig. 4-5. The laser energy density varied from 225 to 430 mJ/cm^2. The grain size as a function of laser energy density is shown in Fig. 4-6 (a). As the laser energy reached 345 mJ/cm^2, the width of the grains increased markedly from 50nm to 250nm, as presented in Fig. 4-6 (b). Similar results have been reported by Hu *et al*.[4.12] who converted an α-Si film to poly-Si using NILC method. After the NILC poly-Si film was annealed using an excimer laser (ELA), they found that most of the α-Si and small Si grains were molten when the laser energy was between 230mJ/cm^2 and 265mJ/cm^2. However, the large grains were only molten partially and served as the nuclei for predetermined to grow. The width of these grains markedly increased to 600nm due to the

geometrical coalescence of Si needle grains. Geometrical coalescence can be simply described as an encounter of grains whose relative orientations are similar during the grain growth. The grain boundary between grains disappears, resulting in the sudden development of a much larger grain.[4.13] This coalescence is an important phenomenon for grains having a strong preferred orientation. Since our IMPRINT needlelike grains had a strong preferred orientation <112>, it was favorable for the geometrical coalescence to occur.

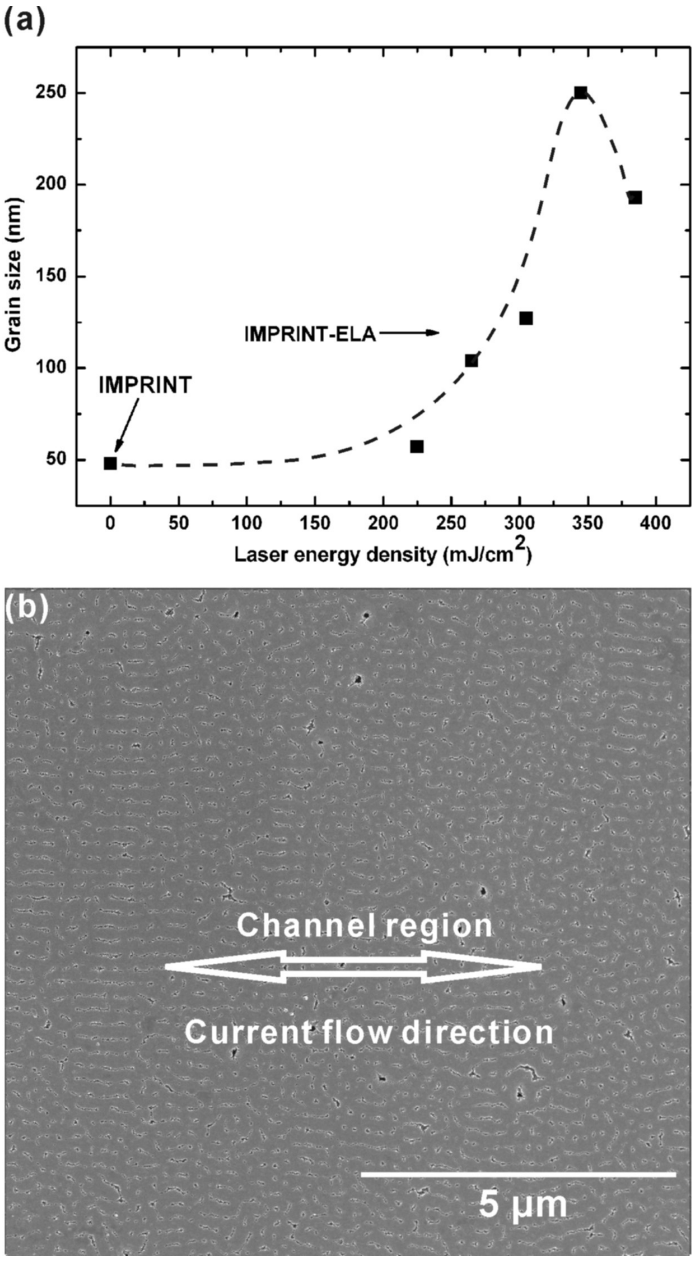

Fig. 4-6 (a) Grain size versus laser energy density. (b) The SEM image of Secco-etched IMPRINT-ELA poly-Si film.

However, the IMPRINT-ELA sample herein has smaller grains than the geometrically coalesced sample of Hu *et al.*, and requires a higher laser energy density. We believe that

these variations are caused mainly by the differences between the film thicknesses and the preferred orientations of the needle grains. In this case, the film thickness of the IMPRINT-ELA sample was 100 nm, which exceeded that of the NILC-ELA sample (50 nm) of Hu *et al*. The preferred orientation of the needle grains of the IMPRINT-ELA film was along <112>, whereas that in the NILC-ELA film was along <111>.

4-3-2 Electrical Characteristic of IMPRINT and IMPRINT-ELA TFTs

The performance of TFT devices was also used to examine the quality of poly-Si films, as shown in Fig. 4-7 and Table I. The subthreshold slope and field effect mobility was extracted from the maximum transconductance in the linear region at a drain bias (V_{DS}) of 0.1 V. The I_{ON}/I_{OFF} current ratio was defined at V_{DS} = 5 V. It was found that the field effect electron mobility (μ_{FE}) of the IMPRINT-ELA-TFT was 413 cm^2/V-s, which was 31.7 times higher than that of the IMPRINT-TFT. The I_{ON}/I_{OFF} current ratio of the IMPRINT-ELA-TFT was 4.24×10^6, which was greater by two orders of magnitude than that of the IMPRINT-TFT. The threshold voltage of IMPRINT-ELA-TFT was 0.848 V, which was less than that of the IMPRINT-TFT, 1.9 V.

As mentioned earlier, some α-Si regions remained among the IMPRINT poly-Si grains. These regions (boundaries) trap charge carriers and constitute potential barriers to the flow of

carriers. The presence of the potential barriers and the additional scattering at the boundaries degrade the mobility.[4.4]

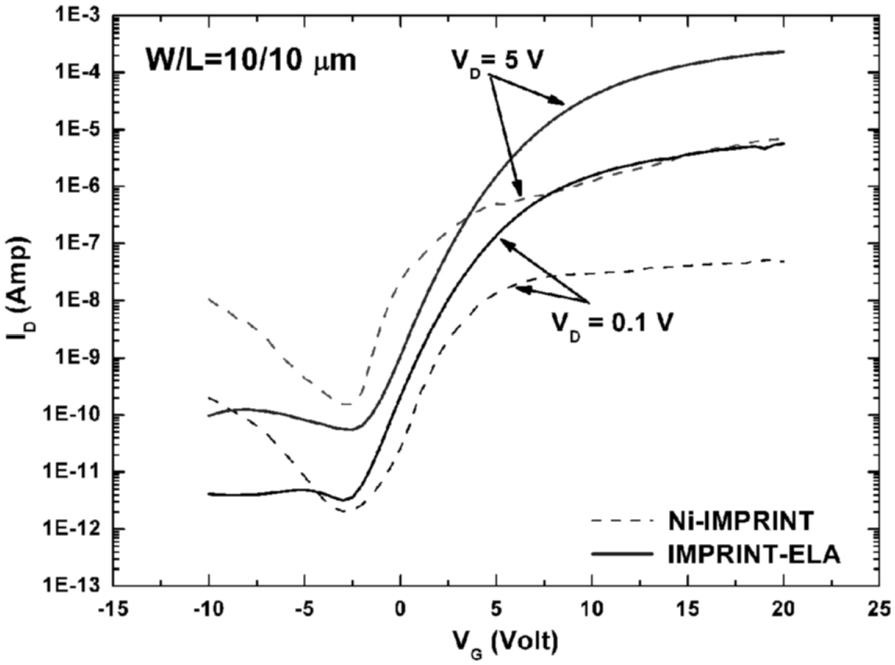

Fig. 4-7 The Transfer characteristics of IMPRINT-TFT and IMPRINT-ELA-TFT with a laser energy density of 345 mJ/cm^2.

IMPRINT-ELA-TFTs do not have these problems because, as presented in Fig. 3(b), most of the geometrical coalescence grains and their boundaries are parallel to the drain current (I_{DS}), reducing the impedance to carrier flow and, thereby, reducing the threshold voltage and greatly increasing the mobility. The higher I_{ON}/I_{OFF} current ratio of the IMPRINT-ELA-TFT than the IMPRINT-TFT was also attributed to the larger grains and the fewer intra-grain

defects. However, this geometrical coalescence grain growth resulted in a significant increase in surface roughness. The root mean square surface (rms) roughness of IMPRINT-ELA surface (4.334 nm) was much greater than that of IMPRINT surface (0.544 nm). Since the subthreshold slope increased with the surface roughness,[4.14] the subthreshold slope of IMPRINT-ELA-TFT was higher than that of IMPRINT-TFT.

Table I Summary of device characteristics of IMPRINT-TFT and IMPRINT-ELA-TFT with a laser energy density of 345 mJ/cm^2.

W/L=10/10	Ni-IMPRINT	IMPRINT-ELA
Mobility(cm^2/V-s) at V_{DS}= 0.1v	13	413
on/off current ratio at V_{DS}= 5V	4.5x 10^4	4.24x 10^6
Minimum leakage current /channel width(pA/μm) at V_{DS}= 5V	15.4	5.47
Subthreshold slope (V/dec) at V_{DS}= 0.1V	0.597	0.678
Threshold voltage (V) at V_{DS}= 0.1V	1.9	0.848

The existence of grain boundaries and intra-grain trap states are also responsible for the increase in leakage current of TFTs. At high V_{DS}, the leakage current is dominated by trap sites-associated field emission current.[4.15,4.16] As shown in Fig. 4, at V_{GS}= -10V and V_{DS}= 5V, the leakage current of the IMPRINT-TFT approaches 10^{-8}A, which is 100 times greater

than that of the IMPRINT-ELA-TFT. The leakage current of the IMPRINT-ELA-TFT is less sensitive to the gate voltage because the density of defect state is lower than that of the IMPRINT-TFT. At low V_{DS}, the leakage current of the IMPRINT-ELA-TFT is also less sensitive to the gate voltage. However, at V_{GS} around -2.5V, the leakage current of IMPRINT-ELA-TFT is higher than that of IMPRINT-TFT. This is because, at low V_{DS}, the leakage current is limited by the channel resistance, which is sensitive to the height of potential barrier associated to the trap sites. With a reduction in the trap sites of IMPRINT-ELA-TFT, the channel resistance was reduced resulting in the increase in leakage current.[4.3]

4-4 Summary

High-performance LTPS TFT fabricated by IMPRINT-ELA was investigated. In this process, amorphous silicon was first transformed to poly-Si using a Ni-imprint method at 550°C for 24 h, and then annealed using a KrF excimer laser. Most IMPRINT Si grains were parallel to each other. The preferred orientation of needle grains (parallel to the film) was <112>, which differed from that of the conventional NILC Si grains <111>. Laser annealing at an energy density of 345 mJ/cm^2 greatly increased the width of the needle grains from 50nm to 250nm by geometrical coalescence. IMPRINT-ELA-TFT markedly outperformed the IMPRINT-TFT because the IMPRINT-ELA poly-Si film had larger grains and fewer

intra-grain defects than the IMPRINT poly-Si film. The IMPRINT-ELA-TFT has a lower threshold voltage, and a higher I_{ON}/I_{OFF} current ratio than the IMPRINT-TFT. The mobility of IMPRINT-ELA-TFT was 413 $cm^2/V\text{-}s$, which was 31.7 times higher than that of the IMPRINT-TFT. The on/off current ratio of the IMPRINT-ELA-TFT was 4.24×10^6, which was higher by two orders magnitude than that of the IMPRINT-TFT.

Reference:

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Chapter 5 Gettering of Nickel from NILC Polycrystalline Silicon Films

5-1 The Conception of the Gettering Method

Transition metals (e.g. Ni, Cu, Pd…..) are common impurities in silicon originating from the crystal growth and subsequently integrated circuits (IC) fabrication steps. The metal contamination can degrade the minority carrier lifetime and device performance, and increase the junction leakage current.[5.1-5.3]

Gettering is defined as the process of removing device-degrading impurities from the active layer regions, which is an important ingredient for enhancing the performance and the yield of device manufacturing. In general, the mechanism by which gettering removes impurities from device regions may be described by the following steps: (1) the impurities to be gettered are released into solid solution from whatever precipitate they're in; (2) they undergo diffusion through the silicon; (3) they are trapped by defects such as dislocations or precipitates in an area away from device regions.

There are two general classifications of gettering, namely, extrinsic, and intrinsic. Extrinsic gettering refers to gettering that employs external means to create the damage or

stress in the silicon lattice in such a way that extended defects needed for trapping impurities are formed. These chemically reactive trapping sites are usually located at the wafer backside.

Several methods have been used to accomplish external gettering. For instance, the introduction of mechanical damage by abrasion, grooving, or sandblasting can produce stresses at the backside of a wafer, which when annealed create dislocations that tend to relieve these stresses. These locations can then serve as gettering sites. The main drawback of this method, of course, is its tendency to initiate and propagate wafer backside microcracks that may compromise the mechanical strength of the wafer.

Diffusing phosphorus [5.4,5.5] into the wafer backside is another technique used for external gettering. Phosphorus diffusion into silicon results in phosphorus vacancies or dislocations that serve as trapping sites for impurity atoms, such as gold. Another effect of P diffusion is the creation of Si-P precipitates, which have been shown to be capable of removing Ni impurities through interactions between Si self-interstitials and Ni atoms, nucleating $NiSi_2$ particles in the process.

Introduction of damage by laser is another external gettering method.[5.8-5.10] Scanning a laser beam across the wafer surface induce damage that is very similar to mechanical damage, with the exception that the laser damage is “cleaner”. Laser subjects the irradiated areas to thermal shock, forming dislocation nests that serve as gettering sites.

Ion bombardment to produce wafer backside damage is another method for external gettering, [5.11-5.13] this time using high-energy ions to induce the necessary stress within the lattices of the wafer backside. Deposition of a poly-Si layer on the wafer backside has also been used for external gettering. Poly-Si layers introduce grain boundaries and lattice disorder that can act as traps for mobile impurities.

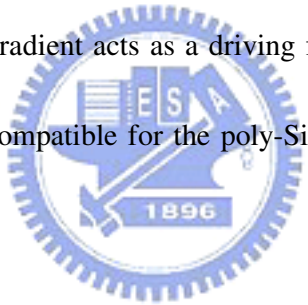
Intrinsic gettering refers to gettering that involves impurity trapping sites created by precipitating supersaturated oxygen out of the silicon wafer.[5.14-5.16] The precipitation of supersaturated oxygen creates clusters that continuously grow, introducing stress to the wafer as this happens.

As mentioned previously, the method of ion implantation to produce nano cavities as a gettering site is too complicate and needed high temperature annealing (>900°C) which not suited to the LTPS TFTs manufacturing process. For the method of diffusion of P atoms into silicon region, the phosphorous will also contaminate the active region.

5-2 Gettering of Nickel within the NILC Polycrystalline Silicon Films Using α-Si Films

5-2-1 Introduction

In this study, we have used an α-Si layer as the gettering material and a silicon-nitride (SiN_x) layer as the diffusion and etching stop layer to accomplish the gettering process. Using the α-Si as the gettering material in order to prevent the other elements contamination and relied on the concentration gradient acts as a driving force for transport of Ni through the SiN_x to the α-Si, it is more compatible for the poly-Si TFTs fabrication and large area application.



5-2-2 Experimental Procedure

Two types of poly-Si films were investigated in this study. Samples were designated as follows: (1) “NILC poly-Si” was a poly-Si film fabricated with traditional NILC methods, while (2) “GETR poly-Si" utilized the same traditional NILC method with an additional Ni-gettering process.

Figure 5-1 shows the basic NILC fabrication process of both poly-Si films began with four-inch Si (100) wafer substrates where wet thermal oxide films of 500nm were grown

using a H_2/O_2 mixture and substrate temperature of 1050°C. Silane-based α-Si films with thicknesses of 100 nm were deposited using low-pressure chemical vapor deposition (LPCVD) at 550°C and 100 mTorr. The photoresist was patterned to form the desired Ni lines, and a 2-nm-thick Ni film was deposited on the α-Si using an e-gun. Afterward, samples were dipped into acetone and ultrasonic bath for 5 min to remove the photoresist. The samples were subsequently annealed at 550°C for 24 h to form the NILC poly-Si film. Then, to form islands of poly-Si regions on the wafers using photolithography process and reactive-ion etch (RIE) system.

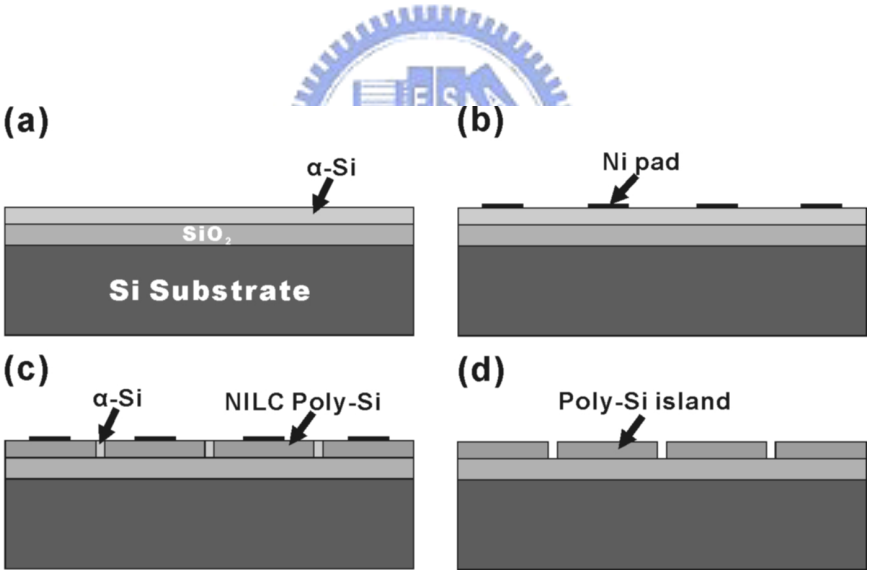


Fig. 5-1 Schematic illustration of basic NILC fabrication process of both poly-Si films. (a) is the α-Si / SiO_2. (b) is the 2 nm Ni thin film deposited on the top of α-Si. (c) is the α-Si coated with Ni pads to form the NILC poly-Si. (d) is the NILC poly-Si islands.

To form the GETR poly-Si film, a 30 nm SiN_x layer was capped on the top of NILC poly-Si film, and then 100-nm-thick α-Si was deposited on the top of SiN_x film, as shown in Fig. 5-2.

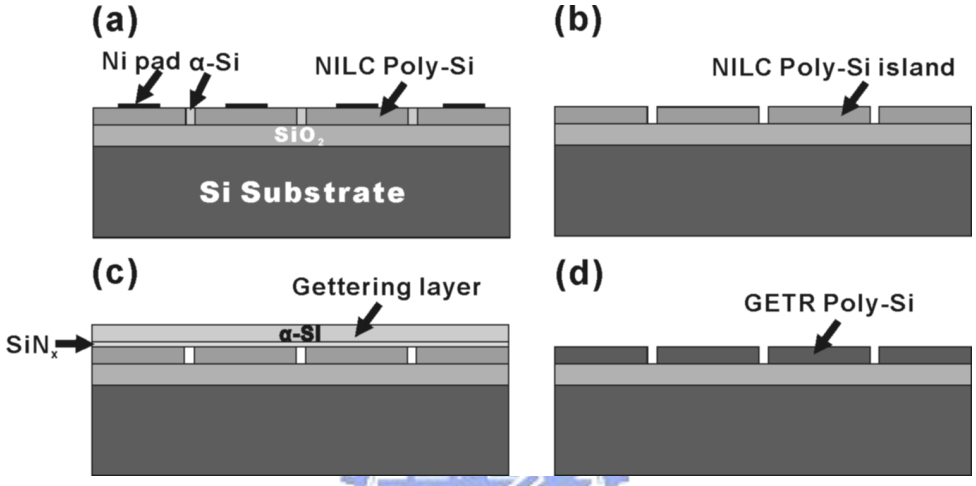


Fig. 5-2 Schematic illustration of the gettering process. (a) is the α-Si coated with Ni pads to form the NILC poly-Si. (b) is the NILC poly-Si islands. (c) is the NILC poly-Si coated with etching stop layer (SiN_x) and gettering layer (α-Si). They were then annealed at 550 °C for 90 h to carry out the gettering process. (d) is the GETR poly-Si (after removed the SiN_x and α-Si layers).

The top α-Si layer served as a gettering layer, while the middle SiN_x layer was used as an etching stop layer. Since these processes are compatible with traditional IC processes, α-Si / SiN_x layers seems to be a promising method to reduce the Ni impurities within the NILC

poly-Si film.

Samples were then annealed at 550°C for 90 h with the goal of removed the unwanted Ni metal within the poly-Si film. Following the annealing process, the top Si gettering layer was removed using the HNA chemical etching solution ($HF:HNO_3:CH_3COOH$=6:20:7), and the SiN_x layer was removed using buffer-oxide etching (BOE) solution. For the purpose of comparison, NILC poly-Si (without α-Si / SiN_x layer) was also annealed under the same condition (550°C for 90 h).

5-2-3 Results and Discussion

Figure 5-3 (a) shows the optical microscope (OM) image of samples after annealing at 550°C for 24 h. The light region at the periphery of the Ni lines outlined the poly-Si area. The α-Si and Ni silicide were etched away with Secco etching solution [5.17] and examined by a scanning electron microscope (SEM). It was found that the NILC poly-Si was composed of needlelike Si grains, as shown in Figs. 5-3 (b). TEM was also used to investigate the NILC poly-Si film. As shown in Fig. 5-3 (c), the Si film was composed of needlelike Si grains.

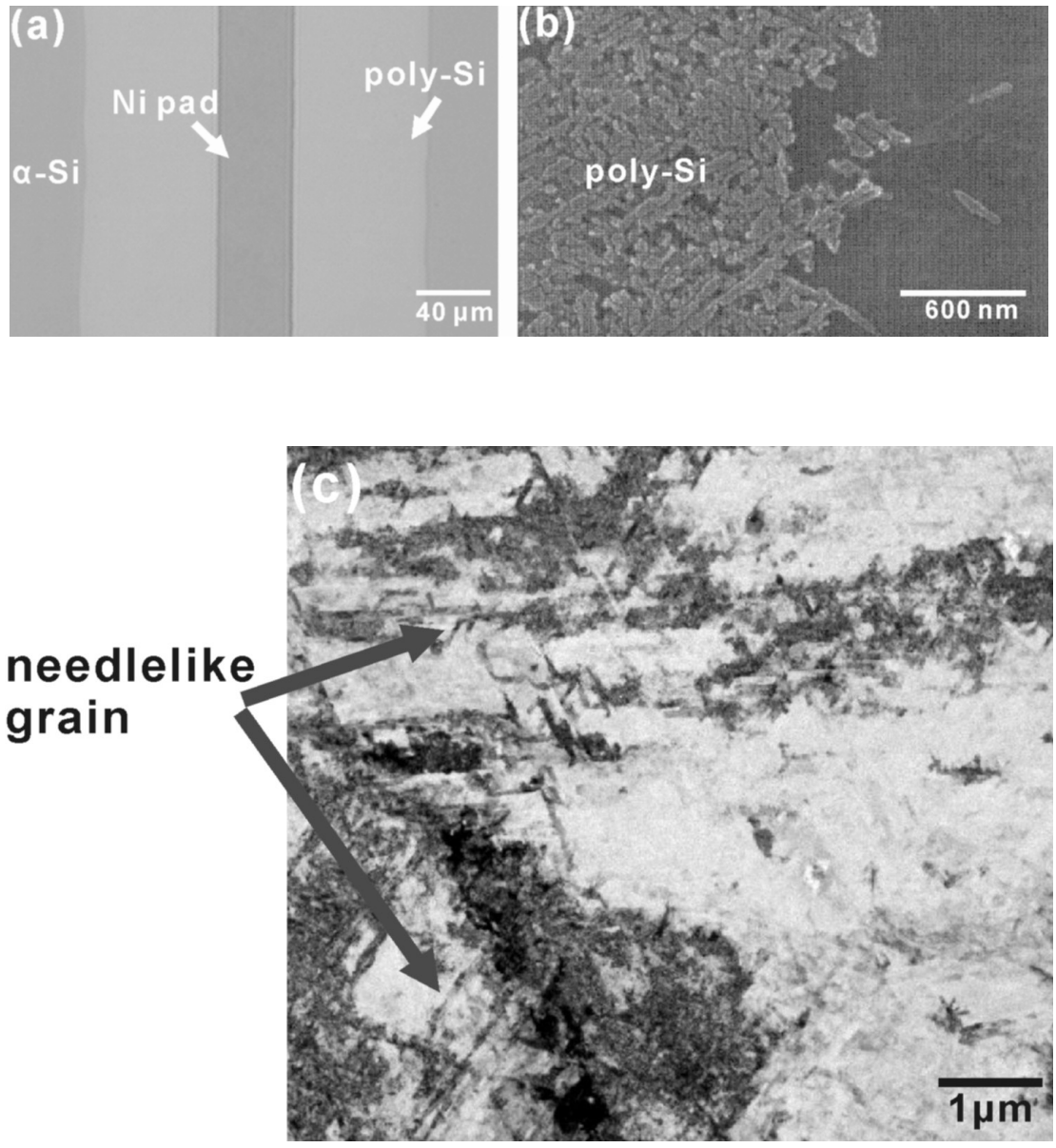


Fig. 5-3 (a) is OM image of sample after annealing at 550°C for 24 h. (b) is SEM image of NILC poly-Si front region (after Secco etching). (c) is TEM image of NILC poly-Si grains.

For the purpose to verify the results of gettering process, the samples both of NILC poly-Si and GETR poly-Si were dipped into a silicide-etching solution (HNO_3:NH_4F:H_2O=4:1:50), which only removed the nickel silicide (not the α-Si), numerous holes were observed at the boundaries where two poly-Si fronts intersected, as shown in Fig. 5-4.

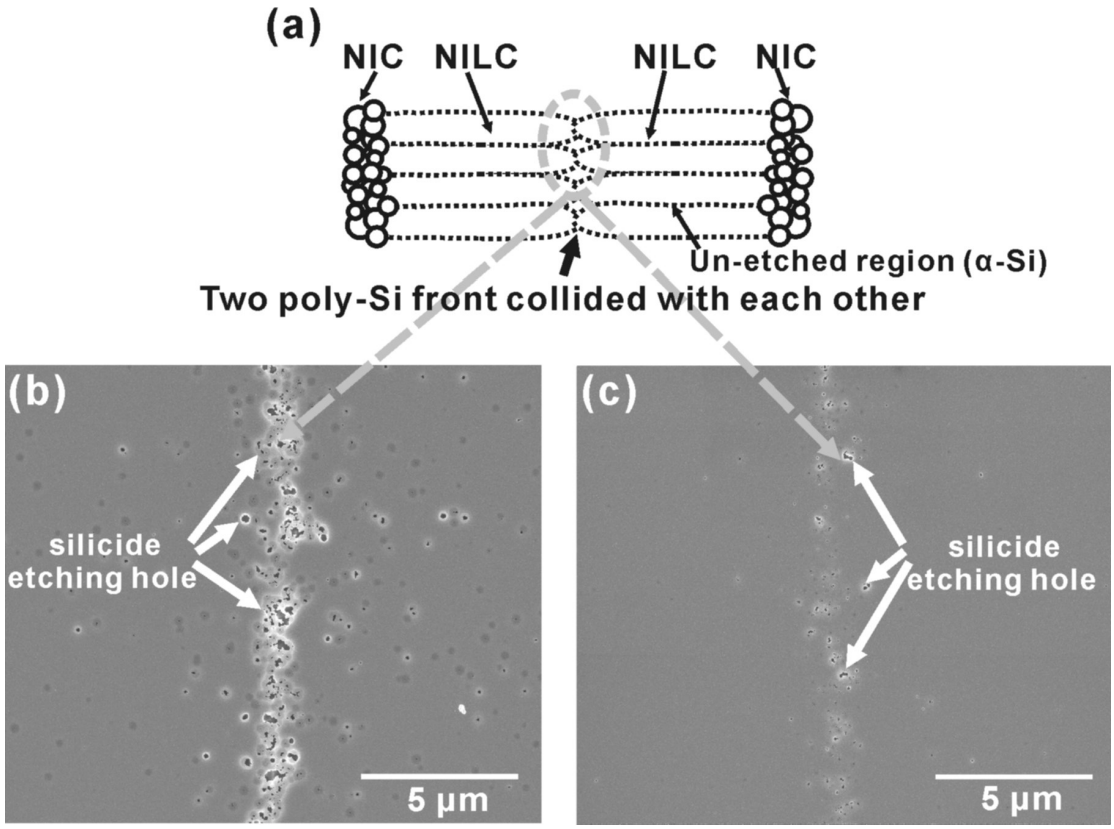


Fig. 5-4 (a) Schematic illustration of the silicide-etching holes at the boundaries where two poly-Si fronts intersected. SEM image of these etching holes were shown on (b) and (c). (b) is the NILC poly-Si. (c) is the GETR poly-Si.

These holes were residues of the Ni silicides that had been etched away by the silicide-etching solution. Ni contamination in the NILC poly-Si film should be reduced, especially in the grain boundaries, since they induce trap charge carriers and build up potential barriers to the flow of carriers. These silicide-etching holes in Fig. 5-4 (b) were quite sensitive to the reduction of Ni residue in the NILC poly-Si, and were therefore ideal for elucidating the "Ni gettering" phenomenon observed. After the gettering process, fewer silicide-etching holes were found on the GETR poly-Si, as shown in Fig. 5-4 (c). This indicates that a substantial number of Ni atoms diffused into the α-Si / SiN_x layers.

The Ni-gettering layer (α-Si) was also used to investigate the Ni-gettering phenomenon. Figure 5-5 (a) shows the OM images of the Ni-gettering layer after the gettering process. The light region was the NILC poly-Si; the dark region was the α-Si. The nature of the poly-Si grains was verified using SEM (Fig. 5-5 (b)). This illustrates that the in-diffusion of Ni atoms from the NILC poly-Si to the Ni-gettering substrate caused the α-Si to transfer to the poly-Si grains by NILC mechanism.

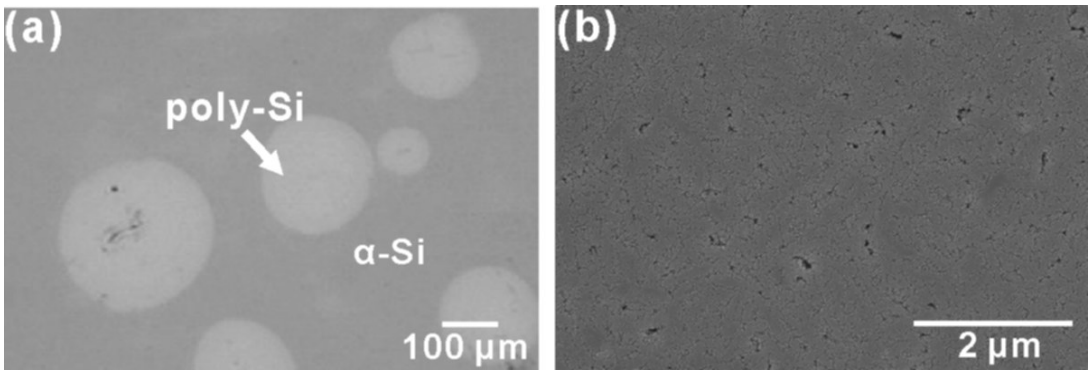


Fig. 5-5 (a) OM and (b) SEM images (after Secco etching) of the gettering layer (Si film).

A model based on diffusion of Ni is proposed, where the concentration gradient acts as a driving force for transport of Ni from the NILC poly-Si to the α-Si / SiN_x layers. During the gettering process, Ni atoms were allowed to transverse through the SiN_x layer. The diffusion time can be estimated by the following equation:

$$\sqrt{Dt} = l$$

where D is the Ni diffusivity in the the SiN_x and equates to 2.64×10^{-17} cm^2/s at 550°C,[5.18] whereas, l is the thickness of SiN_x layer (=30nm). Therefore, in this gettering process, the Ni atoms need about 90 h to pass through the SiN_x layer. The time required is too long. However, without this SiN_x layer, the Ni-gettering layer cannot be selectively removed alone due to the identical material between NILC poly-Si and gettering layer. The SiN_x served as an etching stop layer. Fortunately, we also found the gettering efficiency increased with the increase of the thickness of gettering layer (α-Si) and the annealing temperature, and increased with the

decrease of the thickness of SiN_x, as expected from the kinetic nature of the diffusion process.

Figure 5-6 shows the secondary-ion mass spectrometry (SIMS) depth profile of Ni atom within the poly-Si film (50 nm) for GETR poly-Si (dash line) and NIC poly-Si (solid line). As shown in the depth profile, the Ni concentration within the poly-Si film has been reduced half one order magnitude after the gettering process.

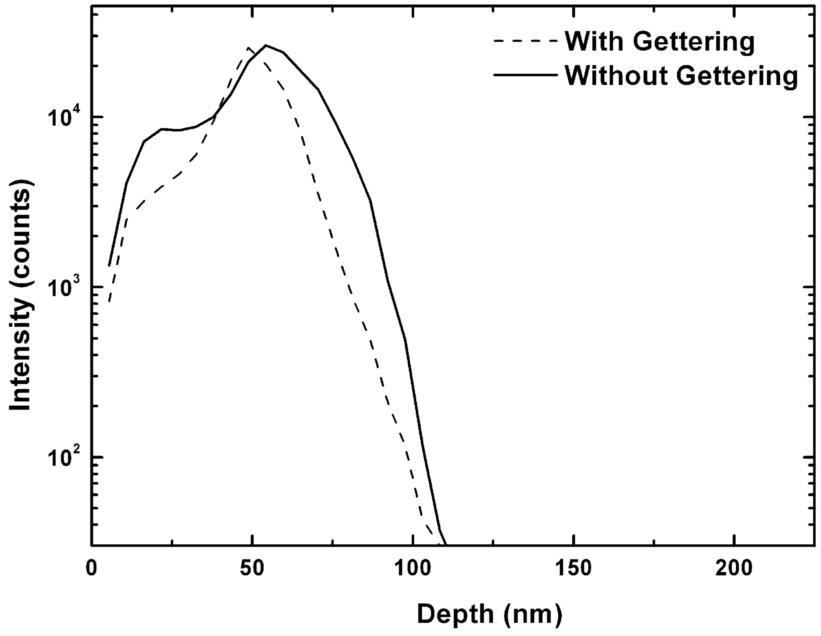


Fig. 5-6 SIMS depth profile of nickel in the poly-Si film. The dash line is the GETR POLY; the real line is the NIC POLY, respectively.

5-2-4 Summary

An investigation of the relationship between Ni-gettering layers (α-Si / SiN_x films) and Ni-metal impurity within the NILC poly-Si film has led to the development of a simple, effective, Ni-gettering process for large area NILC poly-Si films. To form the GETR poly-Si film, a SiN_x layer was capped on the top of NILC poly-Si film, and then α-Si layer was deposited on the top of SiN_x film. The SiN_x layer was used as an etching stop layer, while the α-Si layer served as a gettering layer. It was found that the silicide-etching holes at the NILC poly-Si grain boundaries were greatly reduced after samples were annealed at 550°C for 90 h. This is because the concentration gradient acts as a driving force for transport of Ni from the NILC poly-Si through the SiN_x layer to the α-Si layer. It was also found that the gettering layer (α-Si) was transferred to the poly-Si by NILC mechanism. The NILC fraction in the gettering layer increased with the increase of the annealing time and temperature, and with the decrease of the thickness of SiN_x, as expected from the kinetic nature of the diffusion process.

5-3 Gettering of Nickel from NILC Polycrystalline Silicon Films Using a Gettering Substrate

5-3-1 Introduction

In this study, an α-Si-coated Si wafer and an α-Si-coated quartz wafer were utilized as Ni-gettering substrates. Through a specialized wafer-bonding technique, the Ni concentration inside the NILC poly-Si film was significantly reduced.

5-3-2 Experimental Procedure

Two types of poly-Si films were investigated in this study. Samples were designated as follows: (1) “NILC POLY” a poly-Si film fabricated by traditional NILC methods, while (2) “GETR POLY", a poly-Si film fabricated by the same traditional NILC method with an additional Ni-gettering process. The basic NILC fabrication process of both poly-Si films began with four-inch Si (100) wafer substrates where wet oxide films of 500 nm were grown using a H_2/O_2 mixture and substrate temperature of 1050°C. Silane-based α-Si films with thicknesses of 100 nm were deposited using low-pressure chemical vapor deposition (LPCVD) at 550°C and 100 mTorr. The photoresist was patterned to form the desired Ni lines, and a 2-nm-thick Ni film was deposited on the α-Si using an e-gun. Afterward, samples were

dipped into acetone and ultrasonic bath to remove the photoresist. The samples were subsequently annealed at 550°C for 12 h to form the NILC poly-Si film. To reduce the Ni contamination, the un-reacted Ni metal was removed by chemical etching. A lift-off process using photoresist was employed to form islands of poly-Si regions on the wafers. At this point, only 20% of the poly-Si film remained on the NILC POLY sample.

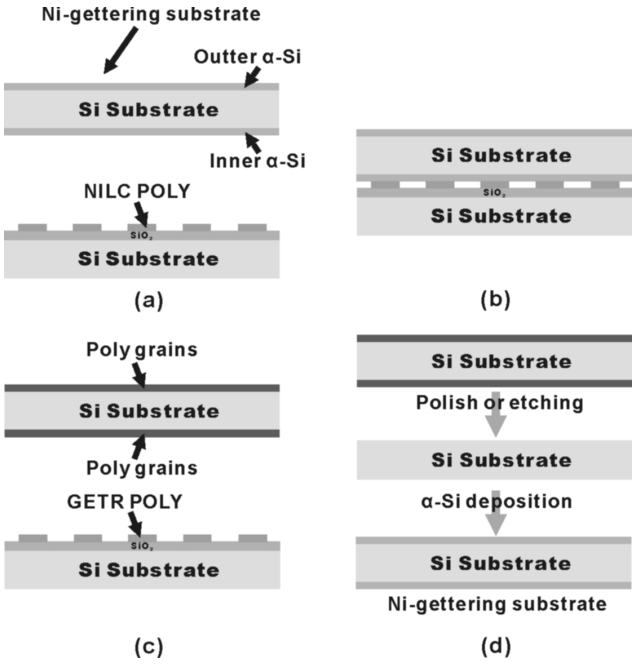


Fig. 5-7 Schematic illustration of the gettering process. (a) is the NILC POLY and the Ni-gettering substrate coated with α-Si films. (b) is the NILC POLY bonded to the Ni-gettering substrate. They were then annealed at 550 °C for12 h to carry out the gettering process. (c) is to separate two substrates. (d) is the Ni-gettering substrate recycled process. The Si-films on the surface of the gettering substrate was polished or etched away. Again, α-Si films were deposited onto the wafers as Ni-gettering substrate.

As for the Ni-gettering substrate, 100-nm-thick α-Si films were directly deposited onto both sides (inner and outer sides) of the Si substrate, as shown in Fig. 5-7.

To form the GETR POLY film, the NILC POLY film was bonded to the Ni-gettering substrate, and then annealed at 550°C for an extra 12 h. Following the gettering process, the Ni-gettering substrate was removed. As shown in Fig. 5-7, the Ni-gettering substrate was recycled by polishing or etching away the α-Si films on the surface of the gettering substrate.

5-3-3 Results and Discussion

Figure 5-8 (a) shows the optical microscope (OM) image of the poly-Si grains induced by the Ni lines. The light region at the periphery of the Ni lines outlined the poly-Si area. The α-Si and Ni silicide were etched away with Secco etching solution and examined by a scanning electron microscope (SEM).

It was found that the NILC was composed of needle-like Si grains, as shown in Fig. 5-8 (b). If the samples were dipped into a silicide-etching solution (HNO_3:NH_4F:H_2O=4:1:50), numerous holes were observed at the NIC areas and at the boundaries where two poly-Si fronts intersected, as seen in Fig. 5-9 (a).

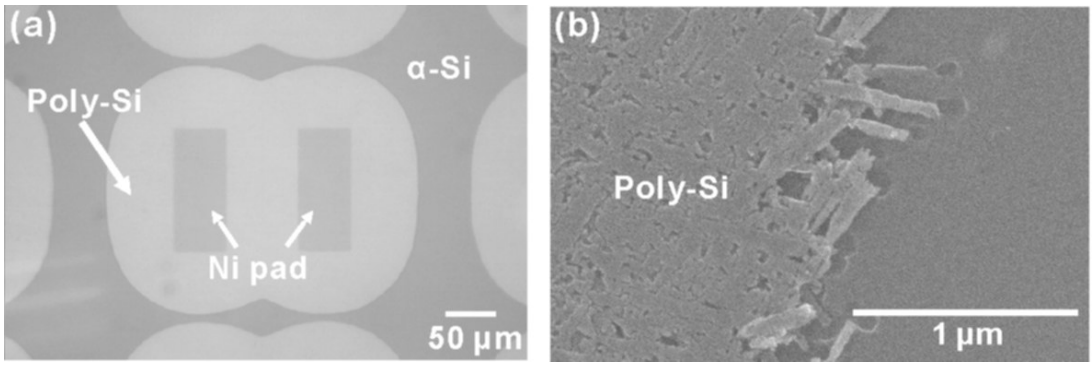


Fig. 5-8 (a) is OM image of the NILC POLY film. (b) is SEM image of NILC poly-Si front region (after Secco etching).

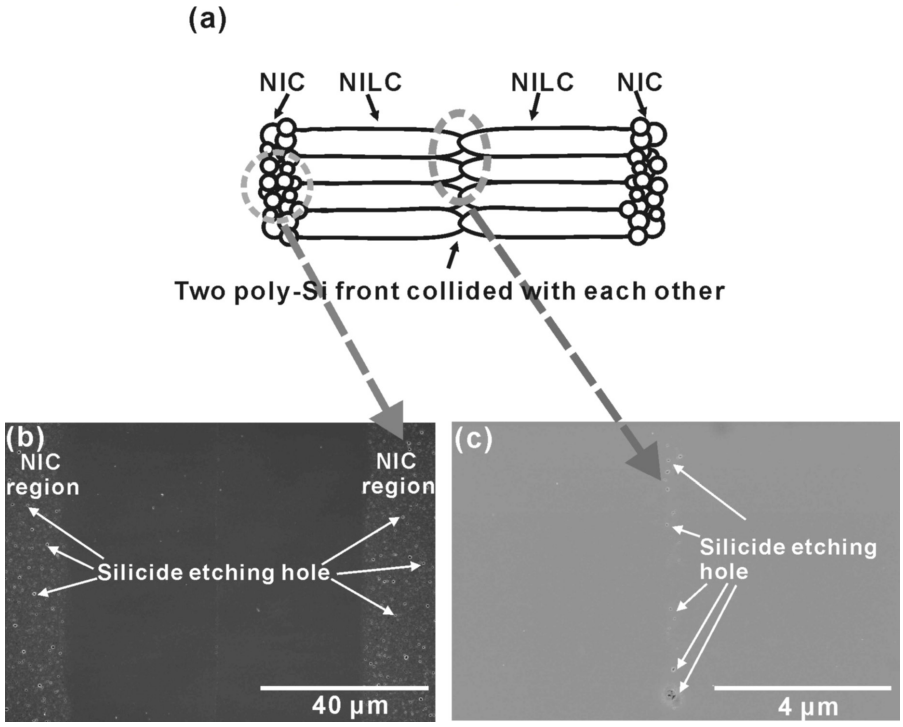


Fig. 5-9 (a) Schematic illustration of the silicide-etching holes on the NIC areas and grain boundaries of the NILC POLY film. SEM image of these etching holes were shown on (b) and (c), respectively.

These holes were residues of the Ni silicides that had been etched away by the silicide-etching solution. Ni contamination in the NILC POLY film should be reduced, especially in the NIC areas and grain boundaries, since they induce trap-charge carriers and build up potential barriers to the flow of carriers. These silicide-etching holes in Fig. 5-9 were quite sensitive to the reduction of Ni residue in the NILC POLY, and were therefore ideal for elucidating the "Ni gettering" phenomenon observed. After the gettering process, no silicide-etching holes were found on the GETR POLY with the exception of very few etching holes in the NIC areas. This indicates that a substantial number of Ni atoms had diffused into the Ni-gettering substrate.

Secondary-ion mass spectroscopy (SIMS) was also employed to measure the reduction of Ni residues in the NILC region of poly-Si films. As shown in Fig. 5-10, the Ni concentration in the GETR POLY film has been reduced to 1/10 compared with that in the NILC POLY films. This also demonstrates successful out-diffusion of Ni atoms to the Ni-gettering substrate.

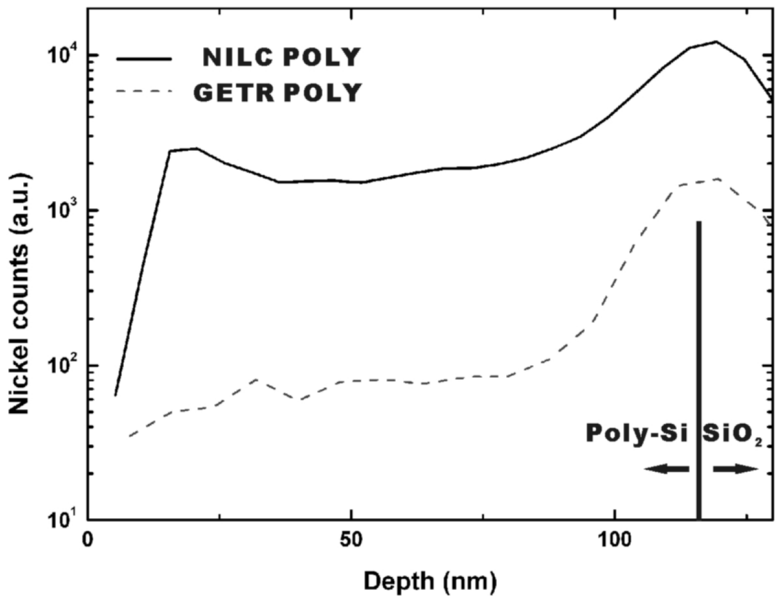


Fig. 5-10 SIMS depth profile of nickel in the poly-Si film. The dash line is the GETR POLY; the real line is the NILC POLY, respectively.

The Ni-gettering substrate was also investigated. Figure 5-11 (a) shows the OM images of the inner-side Si film on the Ni-gettering substrate. The light region denotes α-Si; and the dark region denotes the NILC poly-Si. The nature of the poly-Si grains was verified using SEM (Fig. 5-11 (b)). This illustrates that the in-diffusion of Ni atoms from the NILC POLY to the gettering substrate caused the inner-side α-Si to transform into the poly-Si grains. The OM and SEM images of the outer-side Si film resembled those of the inner-side Si film. The only difference was that the fraction of NILC poly-Si region (determined by estimating the areas of dark (poly-Si) region vs. total area on the optical microscope micrograph) on the outer-side poly-Si film was 90%, which was smaller than that of the inner-side poly-Si film, 95%.

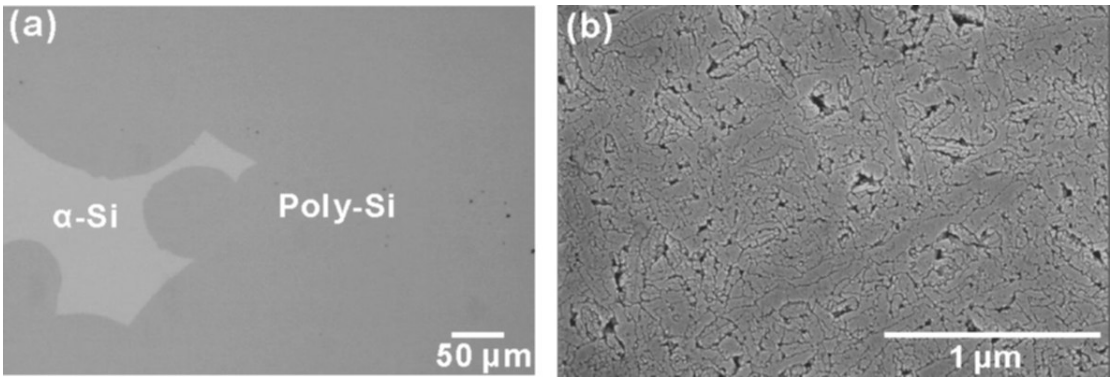


Fig. 5-11 (a) OM and (b) SEM images (after Secco etching) of the inner-side Si film on the Ni-gettering substrate.

During the gettering process, Ni atoms were diffused from the NILC POLY to the gettering substrate due to a concentration gradient. When Ni atoms reached the inner-side of the α-Si film, the α-Si was transformed to needlelike poly-Si grains as shown in Fig. 5-11. Then, during the annealing process, the Ni atoms were allowed to transverse through the Si wafer. The diffusion time can be estimated by the following equation:

$$\sqrt{Dt} = l$$

where D is the Ni diffusivity in the crystalline Si and equals to 2.67×10^{-6} cm^2/s at 550°C.[5.20] Whereas, l is the thickness of Si wafer (=500μm). Therefore, it takes only 15 min fort the Ni atoms to pass through the Si wafer. When the Ni atoms reached the outer-side α-Si films, the α-Si films were transformed into needle-like poly-Si. Since Ni

atoms could pass through the Si wafer in just 15 min. to pass through the Si wafer, most of outer-side α-Si films were transform to the poly-Si after the 12-hr gettering process.

A quartz wafer coated with α-Si was also used as a Ni-gettering substrate. We also found reduction of silicide-etching holes at the grain boundaries of the NILC POLY film, and NILC poly-Si grains formed on the inner-side Si film of the quartz wafer. However, no NILC poly-Si grains were found on the outer-side α-Si film due to the quartz diffusion barrier. This gettering process was also performed under various conditions. It was found that the gettering process becomes more efficient with increase in annealing time and α-Si thickness, which can be explained by the kinetic nature of the diffusion process.

After the gettering process, the Si-films on the surface of the gettering substrates (both the Si and quartz wafers) were polished or etched away, as shown in Fig. 5-7 (d). Again, α-Si films were deposited onto the wafers as Ni-gettering substrates. Even though some residual Ni concentration remained inside the Si wafer (the Ni solubility in the Si wafer is 1.646×10^{14} atom/cm^3 at 550°C[5.21]), the number of silicide-etching holes on subsequent NILC POLY films could still be reduced.

5-3-4 Summary

An investigation of the relationship between Ni-gettering substrates and Ni-metal impurity within the NILC poly-Si (NILC POLY) film has led to the development of a simple, effective Ni-gettering process for NILC poly-Si films. Ni-gettering substrates were fabricated by coating α-Si films on both sides of Si and quartz wafers, respectively. When the Si wafer was used as a Ni-gettering substrate, it was found that the silicide-etching holes at the NILC POLY grain boundaries were greatly reduced. The Ni concentration within the NILC POLY film was reduced to 1/10 after the Ni-gettering process. Both sides of the α-Si films were transformed into the poly-Si by NILC mechanism. The quartz wafer also achieved the reduction of silicide-etching holes on the NILC POLY film. NILC poly-Si grains were only located on the inner-side Si film of the quartz Ni-gettering substrate. No NILC poly-Si grains were found on the outer side due to the quartz diffusion barrier. These improvements increased with annealing time and α-Si thickness.

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Chapter 6 Conclusion and Future Prospects

In this dissertation, the grain growth mechanism and performance of TFTs device based on Ni-metal induced lateral crystallization (NILC) method has been studied. Moreover, combine the ELA method to reduce the intra-grain defect density of NILC poly-Si films, to produce high performance TFTs device. In the last part of this work, have using gettering method which purposed to reduce the Ni contamination within NILC poly-Si films.

In chapter 2, effects of tensile stress on the growth of Ni-metal induced lateral crystallization (NILC) of α-Si were investigated. It was found that tensile stress did not affect the morphologies of needlelike Si grains, but enhanced the NILC growth rate. A series of two-step annealing processes were introduced to study the effects of tensile stress on three stages of the NILC process. Base on the results of two-step annealing process, it was found that tensile stress did not enhance $NiSi_2$ formation and c-Si nucleation stages, but enhanced the c-Si growth stage.

In chapter 3, LTPS TFTs fabricated using <111> and <112> NILC needlelike Si grains were investigated. 111-poly-Si grains were fabricated by traditional NILC, whereas

112-poly-Si grains were fabricated by Ni-metal imprint-induced crystallization. It is found the performance of 112-TFT was far superior to that of 111-TFT. Compared with 111-TFT, the field-effect mobility (μ_{FE}) was higher by a factor of 2.6, 44 compared with 117 cm^2/V-s, and the on/off current ratio (I_{ON}/I_{OFF}) was higher by a factor of 4, 2.29×10^5 compared with 9.23×10^5 and the leakage current (I_{OFF}) was lower, 13 compared with 5.47 pA/μm. These improvements are realized 112-poly-Si has fewer branch grains and less un-crystallized α-Si than 111-poly-Si. Also, all 112-poly-Si grains and their boundaries were parallel to each other with the exception of very few branch grains between them.

In chapter 4, high-performance LTPS TFT fabricated by IMPRINT-ELA was investigated. In this process, α-Si was first transformed to poly-Si using a Ni-imprint method at 550°C for 24 h, and then annealed using a KrF excimer laser. As mention in chapter 3, most IMPRINT Si grains were parallel to each other. Laser-annealing at an energy density of 345mJ/cm^2 greatly increased the width of the needle grains from 50nm to 250nm by geometrical coalescence. IMPRINT-ELA-TFT markedly outperformed the IMPRINT-TFT because the IMPRINT-ELA poly-Si film had larger grains and fewer intra-grain defects than the IMPRINT poly-Si film. The IMPRINT-ELA-TFT has a lower threshold voltage, and a higher I_{ON}/I_{OFF} current ratio than the IMPRINT-TFT. The mobility of IMPRINT-ELA-TFT was 413 cm^2/V-s, which was 31.7 times higher than that of the IMPRINT-TFT. The on/off current ratio of the IMPRINT-ELA-TFT was 4.24×10^6, which was higher by two orders magnitude

than that of the IMPRINT-TFT.

In chapter 5, for the first section, an investigation of the relationship between Ni-gettering layers (α-Si / SiN_x films) and Ni-metal impurity within the NILC poly-Si film has led to the development of a simple, effective, Ni-gettering process for large area NILC poly-Si films. To form the GETR poly-Si film, a SiN_x layer was capped on the top of NILC poly-Si film, and then α-Si layer was deposited on the top of SiN_x film. The SiN_x layer was used as an etching stop layer, while the α-Si layer served as a gettering layer. It was found that the silicide-etching holes at the NILC poly-Si grain boundaries were greatly reduced after samples were annealed at 550°C for 90 h. This is because the concentration gradient acts as a driving force for transport of Ni from the NILC poly-Si through the SiN_x layer to the α-Si layer. It was also found that the gettering layer (α-Si) was transferred to the poly-Si by NILC mechanism. The NILC fraction in the gettering layer increased with the increase of the annealing time and temperature, and with the decrease of the thickness of SiN_x, as expected from the kinetic nature of the diffusion process.

For the second section, the relationship between Ni-gettering substrates and Ni-metal impurity within the NILC poly-Si (NILC POLY) film was investigated. Ni-gettering substrates were fabricated by coating α-Si films on both sides of Si and quartz wafers, respectively. When the Si wafer was used as a Ni-gettering substrate, it was found that the silicide-etching holes at the NILC POLY grain boundaries were greatly reduced. The Ni

concentration within the NILC POLY film was reduced to 1/10 after the Ni-gettering process. Both sides of the α-Si films were transformed into the poly-Si by NILC mechanism. The quartz wafer also achieved the reduction of silicide-etching holes on the NILC POLY film. NILC poly-Si grains were only located on the inner-side Si film of the quartz Ni-gettering substrate. No NILC poly-Si grains were found on the outer side due to the quartz diffusion barrier. These improvements increased with annealing time and α-Si thickness.

According to the results in this thesis, there are some interesting topics that are valuable for the future research:

(1) Surface roughness of the NILC-ELA or ELA poly-Si films.

The surface roughness degrades the electrical characteristics and reliability of TFTs. Therefore, to develop a smooth surface is required. Some approaches can be taken into account to reduce the surface roughness, including the decrease the cooling rate of laser crystallization process and surface planarization technique.

(2) Ni contamination within the NILC poly-Si films.

The Ni contamination within the NILC poly-Si films can degrade the performance of TFT. In this study, a silicon nitride and α-Si were used as a gettering material and annealed at 550°C for 90h. To consider the production cost and yield, must to decrease the annealing time. One of the solutions is to increase the annealing temperature but can't damage the glass substrate,

such as rapid thermal annealing technique. Another way is to search a new diffusion layer with higher diffusivity for Ni atom, to replace the silicon nitride layer.