A CMOS Mismatch Model and Scaling Effects

Shyh-Chyi Wong, Kuo-Hua Pan, and Dye-Jyun Ma

***Abstract*— In this letter, a novel single-pair mismatch model for short-channel MOS devices is developed, and scaling effects of mismatch distributions are investigated based on the model. Mismatch effect is modeled with threshold voltage, current factor, source resistance, and body factor mismatches. SPICE mismatch simulation is defined with mismatch parameters extracted from the model for accurate offset estimation in circuit simulation. Scaling effects with device size are investigated based on statistical mismatch data, and the results indicate that CMOS mismatch is induced by both local edge roughness and global variations. In addition, a $\sqrt{n}$-law model is developed for modeling gate-finger dependence of mismatch.**

I. Introduction

MATCHING property greatly influences analog circuit offset. Thus, an accurate mismatch characterization is essential for analog circuit design. Pelgrom *et al.* [1] and Lakshmikumar *et al.* [2] used a direct measurement approach for their mismatch characterization. Gregor [3] used a differential technique with short-channel effects ignored. For submicron MOS devices, short-channel effects affect mismatch properties. Bastos *et al.* [4] thus incorporated partial short-channel effects in their mismatch study.

Here, our goal is twofold: 1) to develop an accurate single-pair mismatch model which can give voltage-bias dependence to allow for accurate offset prediction, and 2) to develop a statistical (scaling analysis) model which can give device-size dependence of mismatch to ensure accurate simulation of circuit offset distribution. A single-pair mismatch model is the foundation of statistical scaling analysis.

Our single-pair mismatch model aims to extract accurate mismatch parameters, which will in turn be used for defining SPICE mismatch simulation (see Section II). The accuracy of SPICE mismatch simulation is validated with measured data, and it can thus be reliably used for circuit offset voltage prediction. The mismatch model is similar to the α-law model [8] in spirit, including major short-channel effects, and is simple for easy extraction.

Toward our second goal, we collect a high volume of mismatch data on two test patterns (cross-coupled and fingered layouts) based on the mismatch model to analyze scaling effects in terms of standard deviations of mismatch parameters. It is observed that mismatch means are comparably negligible because of properly symmetric layouts in our test patterns [1], [2]. Our results indicate that CMOS mismatch is induced by both local edge roughness (following the $(WL)^{-(3/4)}$ law) and global variations (following the $(WL)^{-(1/2)}$ law) [6]. In addition, a $\sqrt{n}$-law model is developed for modeling gate-finger dependence of mismatch.

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S.-C. Wong is with the Department of Electronics Engineering, Feng-Chia University, Taichung, Taiwan, R.O.C.

K.-H. Pan is with the Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C.

D.-J. Ma is with the Department of Electrical Engineering, National Chung-Hsing University, Taichung, Taiwan, R.O.C.

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II. A Mismatch Extraction Model

We assume that device mismatch is induced by four parameters: threshold voltage mismatch δV_t, current factor mismatch $\delta\beta$, source resistance mismatch δR_s, and body factor mismatch $\delta\sigma$. The four mismatch parameters, which induce drain-current mismatch $\delta I_d/I_d$, are decomposed into gate-bias $V_{\rm gs}$-dependent and $V_{\rm gs}$-independent terms. This is different from traditional formulation where $\delta I_d/I_d$ is assumed to be induced only by δV_t and $\delta\beta$. Geometry mismatch which is $V_{\rm gs}$-independent is attributed to $\delta\beta/\beta$, and $V_{\rm gs}$-dependence is contained in velocity saturation parameter α and source resistance mismatch δR_s, which will yield $V_{\rm gs}$-dependence in the final $\delta I_d/I_d$. This decomposition process is meant to provide a simple and physically meaningful mismatch extraction model.

Our mismatch extraction model is based on a simplified drain current formula [5], [7], which is similar to the α-law model [8] in spirit. That is

$$I_d = \beta[(V'_{\rm gs} - V_t) - 0.5(1+\sigma)V'_{\rm ds}]V_{\rm ds}$$

and

$$I_d = \frac{\beta(V'_{\rm gs} - V_t)^\alpha}{2(1+\sigma)} \tag{1}$$

for linear and saturation regions, respectively. In (1), $V'_{\rm gs} = V_{\rm gs} - I_d R_s$ and $V'_{\rm ds} = V_{\rm ds} - 2I_d R_s$ which model voltage drops on source and drain resistances, respectively. Also

$$\sigma = \frac{\sqrt{2\epsilon q N_a}}{2\sqrt{2\phi_F + |V_{\rm bs}|}C_{\rm ox}}$$

[7], $V_{\rm ds}$ is drain bias, $V_{\rm bs}$ is back bias

$$\beta = \frac{\mu W C_{\rm ox}}{L(1+\theta(V_{\rm gs} - V_t))},$$

ϵ is dielectric constant of silicon, q is unit charge, N_a is bulk doping concentration, $C_{\rm ox}$ is unit-area gate-oxide capacitance, ϕ_F is Fermi potential, μ is mobility, θ is vertical field mobility degradation factor [7], W is channel width and L is channel length. Here, short-channel effects are taken care of by using α as velocity saturation factor [7], [8] and σ as body factor parameter [7], with drain-induced barrier lowering effect being included in the threshold voltage V_t.

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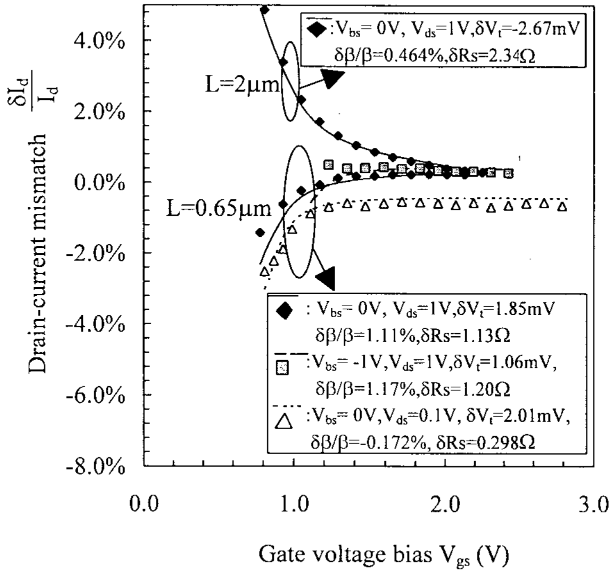

Fig. 1. Verification of voltage dependence of single-pair mismatch extraction model. Lines: HSPICE simulations; Symbols: measured data. $W = 50\,\mu$m; Model parameters for $L = 0.65\,\mu$m: $\alpha = 1.72, \beta = 7.19 \times 10^{-3}\,(A/V^2), \theta = 0.0187\,(1/V), V_t = 0.748$ V. For $L = 2\,\mu$m, $\alpha = 1.93, \beta = 2.19 \times 10^{-3}\,(A/V^2), \theta = 0.0218(1/V), V_t = 0.802$ V.

The mismatch extraction model is derived by differentiating (1) with respect to the mismatch parameters (given that $\delta\beta/\beta$ is a constant with respect to $V_{\rm gs}$). That is

$$\{1+3\beta R_s[V'_{\rm ds}+2[V'_{\rm gs}-V_t-(1+\sigma)V'_{\rm ds}]]\}\frac{\delta I_d}{I_d} = \frac{-1}{V'_{\rm gs}-V_t-\dfrac{1+\sigma}{2}V'_{\rm ds}}\delta V_t+\frac{\delta\beta}{\beta} - \{V'_{\rm ds}+2[V'_{\rm gs}-V_t-(1+\sigma)V'_{\rm ds}]\} \cdot\beta\delta R_s - \frac{V'_{\rm ds}}{2\left[V'_{\rm gs}-V_t-\dfrac{(1+\sigma)}{2}V'_{\rm ds}\right]}\delta\sigma \quad (2)$$

and

$$\left[1+\frac{\alpha\beta R_s}{2(1+\sigma)}(V'_{\rm gs}-V_t)^{\alpha-1}\frac{\delta I_d}{I_d}\right] = -\frac{\alpha}{V'_{\rm gs}-V_t}\delta V_t+\frac{\delta\beta}{\beta}-\frac{\alpha\beta}{2(1+\sigma)}(V'_{\rm gs}-V_t)^{\alpha-1} \cdot\delta R_s-\frac{\delta\sigma}{1+\sigma} \quad (3)$$

for linear and saturation regions, respectively. With (2) and (3), we can easily extract the mismatch parameters $\delta V_t, \delta\beta, \delta R_s$, and $\delta\sigma$ by solving them directly using (2) and (3) based on measurement data of $(\delta I_d/I_d, V_{\rm gs})$.

The extracted mismatch parameters are used in HSPICE for mismatch simulation as follows. Two Level-28 [9] model files are generated for a mismatch pair, with mismatch being modeled using HSPICE parameters *delvto* (for δV_t) and DXL/L (for $\delta\beta/\beta$). For δR_s and $\delta\sigma$, there are no direct corresponding HSPICE parameters, and therefore we use different HSPICE parameters RS and $K1$ in the two models to generate equivalent δR_s and $\delta\sigma$, respectively.

TABLE I
MISMATCH DISTRIBUTIONS FOR CROSS-COUPLED NMOS $E(\ )$: MEAN; $\sigma(\ )$: STANDARD DEVIATION

Device size W/L	Voltage bias V_{ds}, V_{bs} (V)	$E(\delta V_t),\sigma(\delta V_t)$(mV)	$E(\delta\beta/\beta)$, $\sigma(\delta\beta/\beta)$ (%)	$E(\delta I_d/I_d),\sigma(\delta I_d/I_d)$ @$V_{gs}=V_t+0.26$V (%)
50/0.5	2.5, 0	-0.259, 3.05	0.0634, 0.535	0.254, 1.89
50/0.8	2.5, 0	0.0795, 1.94	-0.182, 0.389	not available
50/1	2.5, 0	-0.0748, 1.51	0.0584, 0.348	not available
50/2	2.5, 0	0.172, 0.861	-0.0199, 0.297	0.0829, 0.829
50/0.5	0.1, 0	0.120, 2.98	-0.0212, 0.367	0.254, 1.850
50/2	0.1, 0	0.388, 1.114	0.0329, 0.137	-0.0894, 0.839
50/0.5	2.5, -1	-0.353, 3.41	0.0705, 0.575	-0.323, 2.05
50/2	2.5, -1	0.229, 1.06	0.0232, 0.267	0.0661, 0.929

Fig. 1 compares HPICE simulation with measured data, and shows the accuracy of our mismatch extraction model for various biases and channel lengths. This is important, since the accuracy of single-pair mismatch is the foundation of a precision circuit offset simulation. Note that considerable difference of mismatch parameters between $V_{\rm ds} = 0.1$ V and $V_{\rm ds} = 1$ V suggests that linear region mismatch parameters should not be used for most analog circuit designs. Dependence of mismatch parameters on $V_{\rm bs}$ (for $V_{\rm bs} = 0$ V and $V_{\rm bs} = -1$ V) is shown in Fig. 1 for single-pair mismatch and in Table I for standard deviations. The values of extracted mismatch parameters used in the simulation are also listed in Fig. 1 for easy reference; here $\delta\sigma$ is negligible and is thus omitted.

III. SCALING EFFECTS

Two structures are used in our mismatch study: 1) cross-coupled pair and 2) stripe pair with n fingers (see Figs. 2 and 3). Statistical mismatch data are collected from a twin-well CMOS technology with polycide gate, gate-oxide thickness of 90 Å, field oxide of 0.35 μm, and LDD with spacer of 0.2 μm. Mismatch parameters are measured and extracted using a test program based on (2) and (3) on a Hewlett-Packard-4062 machine in a class-ten environment, on 22 lots of 6-inch wafers with 24 wafers per lot produced within six months. A total of 32 dies are measured per wafer to cover sufficient intra-wafer random errors for a meaningful statistical analysis.

Means $E()$ and standard deviations $\sigma()$ of mismatch parameters for a cross-coupled NMOS pair are listed in Table I. Observe that the means are negligible compared to the standard deviations, as symmetric layouts eliminate most systematic errors in our mismatch data. Standard deviations are mainly induced by random errors, and can be used for our mismatch scaling study.

Fig. 2 shows device-size dependence of mismatch standard deviations in cross-coupled NMOS pairs, exhibiting that $\sigma(\delta V_t)$ is proportional to $(WL)^{-(3/4)}$ and $\sigma(\delta\beta/\beta)$ is proportional to $(WL)^{-(1/2)}$, with root-mean-square (RMS) errors (in log scale) of 0.0494 and 0.0465, respectively. Moreover, a 0.102 RMS error (in log scale) is calculated for a $(WL)^{-(1/2)}$ fit for $\sigma(\delta V_t)$, which is apparently not suitable. This result disagrees with the one in [2], but agrees with the general model of [6], suggesting that δV_t is caused by local-edge roughness and $\delta\beta/\beta$ by global distortions. The relatively large periphery-

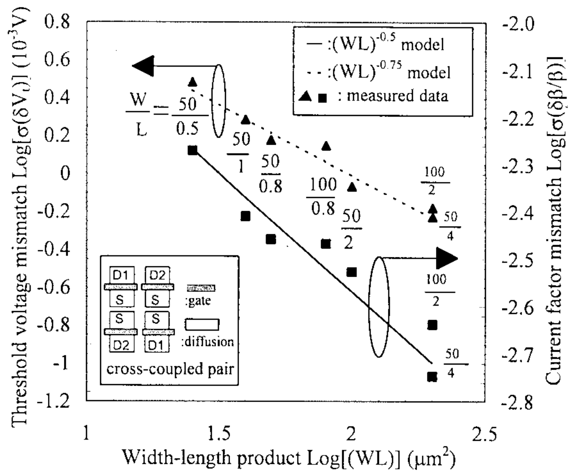

Fig. 2. Scaling of mismatch standard deviations in cross-coupled NMOS pairs. Symbols: measured data. Lines: $(WL)^{-(1/2)}$ and $(WL)^{-(3/4)}$ model. S: common source; D1, D2: drain nodes for first and second MOS in the pair. All diffusions are with identical size.

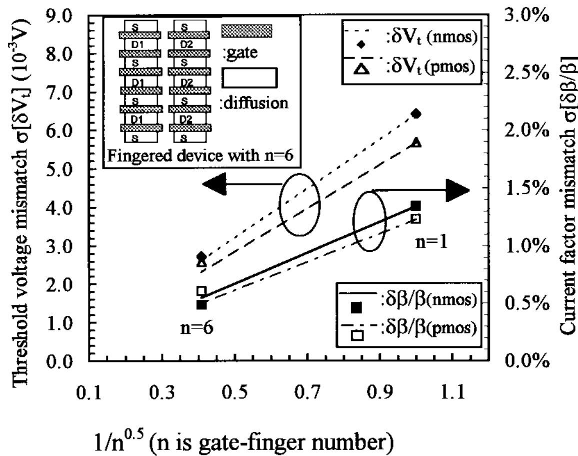

Fig. 3. $\sqrt{n}$-law model of mismatch standard deviations. Lines: model; Symbols: measured data. $L = 0.5\,\mu$m and $W = 20\,\mu$m for each finger (NMOS). S: common source; D1, D2: drain nodes for first and second MOS in the pair. All gates are placed with equal space.

to-area ratio of diffusion in the cross-coupled layout may be a cause of this significant local-edge effect.

To model gate-finger dependence, a $\sqrt{n}$-law is developed. Assume that each stripe in the matched pair has a threshold-voltage standard deviation σ_v. A pair with one finger each then has a standard deviation $\sigma_p = \sqrt{2\sigma_v^2}$ and the matched pair with n fingers each has a variance

$$\sigma_s^2 = E\left(\left(\frac{1}{n}\sum_{i=1}^{n} V_{ti} - \frac{1}{n}\sum_{j=1}^{n} V'_{tj}\right)^2\right) = \frac{\sigma_p^2}{n}$$

and this gives a standard deviation of mismatch

$$\sigma(\delta V_t)|_{n\text{-finger-pair}} = \sigma_s = \frac{\sigma_p}{\sqrt{n}} = \frac{\sigma(\delta V_t)|_{1\text{-finger-pair}}}{\sqrt{n}}. \quad (4)$$

The $\sqrt{n}$-law model, as shown in Fig. 3, agrees well with measured data. Note that this $\sqrt{n}$ model now agrees with the traditional $(WL)^{-(1/2)}$ dependence [1], [2], but differs from the previous $(WL)^{-(3/4)}$ model of threshold-voltage mismatch in cross-coupled pairs. We suggest that this deviation is due to smaller periphery-to-area ratio of diffusion-layer in the n-finger layout than that in the cross-coupled layout, resulting in negligible local-edge-roughness effect [6] and eliminating the $(WL)^{-(3/4)}$ dependence. Thus, using n fingers in fingered layout is different from using a device size of nWL in cross-coupled layout, although their overall device sizes are the same.

IV. Conclusions

An accurate single-pair mismatch model has been developed for circuit simulation, and scaling effects of mismatch distributions have been investigated. SPICE mismatch simulation has been defined based on the mismatch model, and can be used for accurate circuit offset prediction. In specific, we have obtained a new $(WL)^{-(3/4)}$ dependence result of threshold voltage mismatch in the cross-coupled pairs, and developed a $\sqrt{n}$-law model for mismatch in multifinger device pairs.

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