In Situ Doped Source/Drain for Performance Enhancement of Double-Gated Poly-Si Nanowire Transistors

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***Abstract*—A poly-Si nanowire (NW) thin-film transistor configured with the double-gated scheme was fabricated and characterized. The fabrication process features the clever use of selective plasma etching to form a rectangular NW underneath a hard mask. In this paper, we show that replacing the original ion-implanted poly-Si with *in situ* doped poly-Si for the source/drain significantly enhances the device performance, including steeper subthreshold swing (SS), larger on/off current ratio, and reduced series resistance. In particular, the SS is improved to a record-breaking low value of 73 mV/dec, which, to the best of our knowledge, is the most ideal ever reported for a poly-Si based device. The new NW transistors with such excellent switching properties are highly promising for reducing power consumption and operational voltage in practical circuit applications.**

***Index Terms*—Field-effect transistor, *in situ* doping, leakage, multiple gate, nanowire (NW), polycrystalline-Si (poly-Si).**

I. Introduction

POLYCRYSTALLINE-Si (poly-Si) thin-film transistors (TFTs), which act as an important building block in drivers of liquid crystal display (LCD), have become very attractive for future 3-D electronics integration [1]. Compared with single-crystalline Si-based microelectronics, where expensive substrates are inevitable, high- performance TFTs have emerged as a promising alternative for microelectronics employing glass and plastic substrates, where flexibility and light weight are primarily preferred [2]. It would be quite a breakthrough if poly-Si TFTs could display comparable performance to single-crystalline Si-based devices on account of its low fabrication cost. However, the fine-grained structure that is inherent in poly-Si significantly degrades the carrier mobility [3] and limits its adoption and proliferation in advanced ultra large-scale integration (ULSI) technologies. To address this intrinsic material issue, a plethora of recrystallization methods for grain enlargement have been proposed, with solid-phase crystallization (SPC) [4], metal-induced lateral crystallization (MILC) [5], and excimer laser annealing (ELA) [6] being the most commonly used. To continue the scaling trend while simultaneously improving poly-Si device characteristics, extrinsic modification, e.g., ultrathin body structures, provides an effective solution for the aforementioned problem. From a microscopic perspective, 1-D nanowire (NW) structure also offers a unique platform for physical properties not easily observed in conventional devices. The unique characteristics of large surface-to-volume ratio and high sensitivity to surface conditions have rendered NW a functional device suitable for biosensing [7] and nonvolatile memory [8] applications. Among the various methods for NW fabrication, top–down approaches avoid the misalignment and hard-to-manipulate issues that are frequently encountered in bottom–up processes and, meanwhile, are more compatible with modern CMOS process flows. Moreover, when combined with multiple-gated scheme, the fabricated device exhibits enhanced drive current and steeper subthreshold swing (SS) due to improved control of electrostatic potential in the channel, as demonstrated in various works, including FinFET [9], omega gate [10], trigate [11], and gate all around [12]. Meanwhile, CMOS-compatible performance has also been achieved using poly-Si NW devices [13], [14]. To this end, we had presented several innovative top–down approaches for forming poly-Si NWs using conventional I-line-based lithography [15]–[17]. Most recently, a selective plasma-etching technique was adopted to fabricate devices with rectangular NW channels, thus alleviating the sharp corners in previous triangular-shaped NW devices [18]. In the original fabrication process, source/drain (S/D) regions were formed by a low-energy ion implantation so that dopants were situated near the top surface to avoid compromising the gate controllability caused by inadvertent channel doping [15]. Although this method attains good gate control over NW channels, it still unavoidably leads to slight channel doping by the tail part of dopant distribution and is achieved at the expense of S/D resistance, because only a small portion of S/D is heavily doped. In addition, as reported in one of our previous studies [19], the major leakage current is identified to be the gate-induced leakage current (GIDL) that originated in the gate/drain overlap area in the structure. Because the portion of drain that is closest to the gate is only moderately doped, this approach makes band-to-band tunneling (BTBT) much easier to occur and results in severe leakage current. To alleviate this problem,

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here, we propose a modified method for fabricating devices with identical structure, except that the S/D regions are more uniformly and heavily doped by employing an *in situ* doping approach. This way, the S/D resistance and gate controllability are no longer compromised, leading to a win–win situation.

The content of this paper is arranged as follows. In Section II, the condition and results of selective plasma etching are discussed. Section III then describes process flows for devices with implanted and *in situ* doped S/D, respectively, followed by electrical characterization in Section IV. Finally, a brief conclusion is given in Section V.

II. Investigation of Selective Plasma-Etching Conditions

The main feature in this structure lies in the fact that a sub-100-nm cavity could be formed by isotropic plasma etching using a high-density plasma (HDP) etching apparatus. In this paper, a transformer-coupled plasma (TCP) reactor manufactured by Lam Research was used, which operates by inductively coupling RF power to plasma. This tool is equipped with two RF power generators. The top source RF power generates plasma and determines ion density, whereas the bottom bias RF power is responsible for controlling the ion bombardment energy. In other words, ion density and energy are independently controlled in this reactor, thus solving the inflexibility and poor efficiency of conventional capacitively coupled reactors. In contrast to the typical anisotropic RIE process in an HDP etching tool, the sub-100-nm cavity-forming technique is accomplished by turning off the bottom bias. This way, the bombarding energy of ions would be reduced to achieve high etching selectivity between poly-Si and the other layers.

The process flow of the proposed two-step n^+ poly-Si etching scheme is depicted in Fig. 1(a). A stack of layers that comprise thermal oxide/nitride/n^+ poly-Si/nitride was sequentially deposited on a 6-in Si wafer. Next, the top nitride and n^+ poly-Si stack were patterned by anisotropic etching in a TCP reactor. Fig. 1(b) displays a scanning electron microscope (SEM) picture taken after this step. It is observed that the final etching profile is anisotropic. This result is because chlorine etching mainly proceeds in an ion-induced manner; therefore, the etched profile is essentially anisotropic. Following photoresist stripping, the wafer was loaded into the same reactor for selective and isotropic n^+ poly-Si plasma etching. In this step, fluorine-containing gas SF_6 is added, along with chlorine, to increase the isotropic etching component, with the result shown in Fig. 1(c). It has been well known that poly-Si can be etched by fluorine-based etchants because of the high volatility of SiF_4 [20]. Meanwhile, F radicals are usually produced in large quantities in plasma, along with little polymer formation; therefore, the final profile will be relatively isotropic. This image indicates that fluorine addition greatly enhances the isotropic profile and demonstrates high selectivity with respect to nitride layer. This approach is quite reasonable, because in addition to rendering the motion of bombarding ions a random manner, setting the bias power to zero improves the etching selectivity of poly-Si against other materials. It is noted that this isotropic etching is performed in the same reactor as that of anisotropic etching, suggesting the compatibility and convenience of this novel procedure. To demonstrate the merit of this approach in fabricating decananometer NWs, Fig. 2 displays the lateral encroaching depth as a function of etching time as characterized by SEM, indicating that the NW dimension could flexibly be controlled. In fact, it is very hard to produce the same result

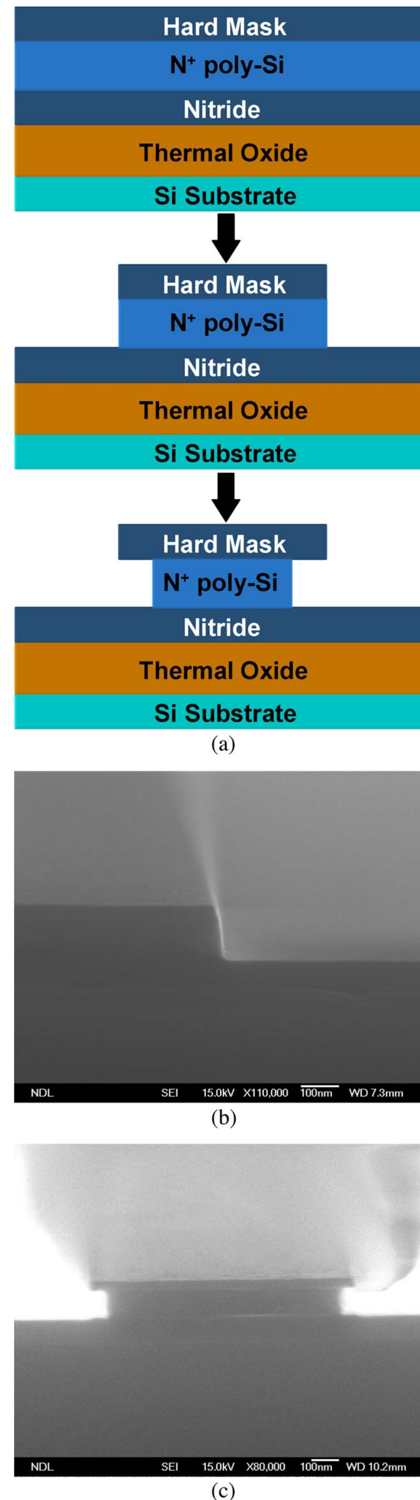

Fig. 1. (a) Test structure used for investigating selective plasma-etching conditions. Cross-sectional SEM image after plasma etching using (b) chlorine and (c) chlorine and sulfur hexafluoride gases.

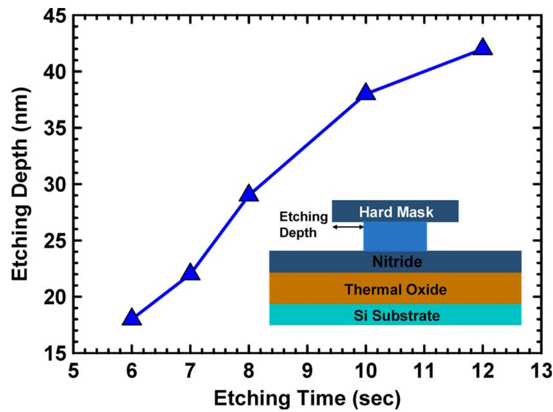

Fig. 2. Measured lateral etching depth as a function of etching time. The inset gives the definition of lateral etching depth.

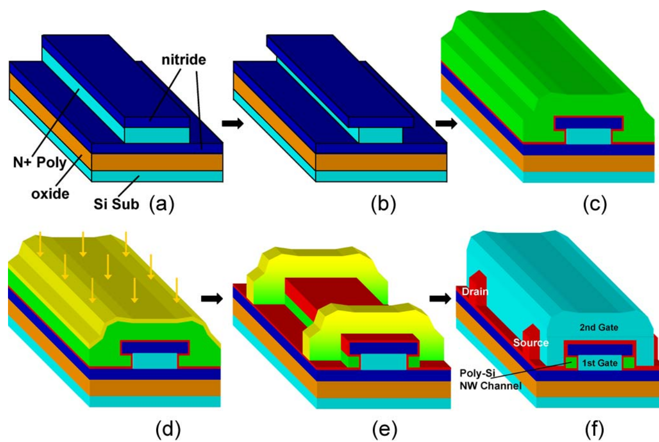

Fig. 3. Schematic process flow for the double-gated NWTFT with implanted S/D. (a) Sequential deposition of 200-nm thermal oxide, 50-nm nitride, 100-nm N^+ poly-Si, and 50-nm nitride on a 6-in Si wafer. First gate stack patterning was then performed. (b) Selective plasma etching of the first gate. (c) First gate dielectric (20-nm LPCVD TEOS oxide) and 100-nm amorphous Si-layer deposition followed by 600 °C annealing at N_2 ambient for 24 h (SPC). (d) S/D implantation with energy 15 keV and dosage 5×10^{15} cm^{-2}. (e) Simultaneous definition of NW channels and S/D regions using dry etching. (f) Second gate stack (20-nm LPCVD TEOS oxide and 100-nm N^+ poly-Si) deposition and definition.

each time for etching with duration of less than 10 s, because the condition of glow discharge is not yet stable in such a short period. However, it is believed that the proposed method will have more reproducible results, provided that the etching condition is optimized. In other words, by carefully adjusting the flow rate of source gas, RF power, and etching time, the structural parameter can be easily and reliably shrunk into the decananometer regime.

III. Device Structures and Fabrication

The devices characterized in this paper employ a double-gated configuration, where NW channels are formed underneath a nitride hard mask. In this paper, two types of devices with different S/D formation techniques are compared. For the implanted S/D type, a detailed device fabrication process was elaborated in [18] and is briefly illustrated in Fig. 3. The gradual variation of colors in the S/D regions in Fig. 3(e) highlights that the doping concentration is not uniform and decreases from the topmost surface toward the channel regions. Fig. 4 schematically illustrates the modified process for which S/D is formed by using *in situ* doping technique. The process flow is identical to that shown in Fig. 3 down to the SPC step. Then, without any photolithographic process, a spacer-like portion of poly-Si along the sidewall of the first gate, whose purpose will later be discussed, was created by carrying out a dry etching step with endpoint detection. Subsequently, *in situ* phosphorus doped poly-Si was deposited by low-pressure chemical vapor deposition (LPCVD) at 550 °C and 600 mtorr using 200 sccm PH_3 and 1 slm SiH_4, followed by S/D region patterning. This way, because there was no implantation involved and NW channels underneath the hardmask were protected by the spacer-shaped poly-Si from being exposed to PH_3 in the *in situ* doped poly-Si deposition step, the entire S/D regions were heavily doped, whereas the NWs remained unscathed (i.e., undoped). The second gate stack was then deposited and patterned to complete the device. Dopant activation was fulfilled using the thermal budget of processing steps after implantation, including the deposition of the second gate stack [20-nm LPCVD tetraethoxysilane (TEOS) oxide and 100-nm N^+ poly-Si] and 350-nm passivation LPCVD TEOS oxide, approximately amounting to 700 °C annealing for 8 h. To avoid possible dopant diffusion into NWs, we intentionally left a spacer-like poly-Si instead of directly forming rectangular NWs as shown in Fig. 3(e) so that, even if diffusion occurs, this spacer-like portion, which is part of S/D, is doped first before channel doping happens. In addition, channel doping should not be of significance, because the highest temperature of the subsequent thermal budget is merely 700 °C in TEOS oxide deposition step.

IV. Electrical Characteristics

Fig. 5 depicts a transmission electron microscope (TEM) picture of the proposed device, from which the thickness of NW (or the width of NW between the two gate dielectrics) is observed to be 22 nm. Transfer characteristics for the control device with implanted S/D are shown in Fig. 6. Channel length and gate oxide thickness are 1 μm and 20 nm, respectively. Due to the unique feature associated with two independent gates in the proposed structure, device operation can be categorized into SG-1, SG-2, and DG modes. In particular, the SG-1 and SG-2 modes refer to the scheme with the first or second gate acting as the sweeping gate, respectively, whereas the other one is grounded. Under the DG mode, two gates are connected together and serve as a single sweeping gate. It can be observed that DG operation demonstrates much enhanced performance in terms of lower threshold voltage (V_{TH}), higher ON current (I_{ON}), and steeper SS (i.e., 89 mV/dec) due to its stronger electrostatic gate controllability over channels. It has been stated in [18] that additional nongated routes would have significantly increased the series resistance of the SG-1 mode. However, the nearly symmetric transfer curves between the SG-1 and SG-2 modes indicate that this detrimental effect related to the NW thickness is dramatically reduced. Impacts of NW thickness on device performance are exhibited in Fig. 7, where devices with three different NW dimensions are compared. The size

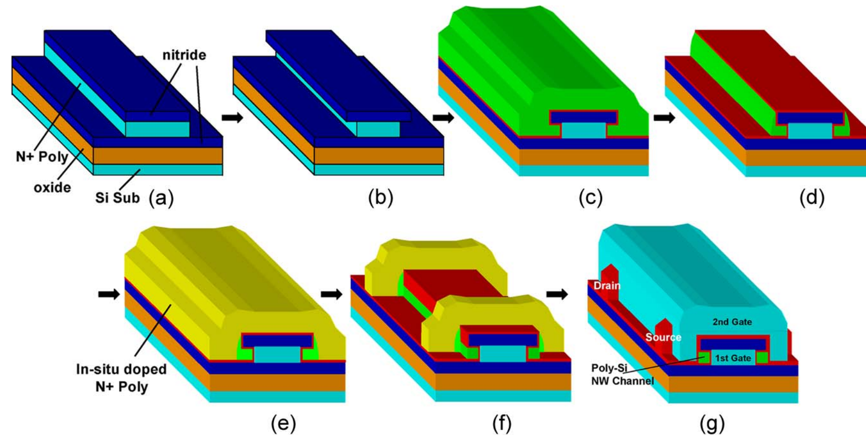

Fig. 4. Schematic process flow for the double-gated NWTFT with *in situ* doped S/D. (a) Sequential deposition of 200-nm thermal oxide, 50-nm nitride, 100-nm N^+ poly-Si, and 50-nm nitride on a 6-in Si wafer. First gate stack patterning was then performed. (b) Selective plasma etching of the first gate. (c) First gate dielectric (20-nm LPCVD TEOS oxide) and 100-nm amorphous Si-layer deposition followed by 600 °C annealing at N_2 ambient for 24 h (SPC). (d) Dry etching to form NWs underneath the hard mask and a spacer-like portion of poly-Si along the sidewall of the first gate. (e) Deposition of 100-nm *in situ* phosphorus doped poly-Si. (f) Simultaneous definition of NW channels and S/D regions using dry etching. (g) Second gate stack (20-nm LPCVD TEOS oxide and 100-nm N^+ poly-Si) deposition and definition.

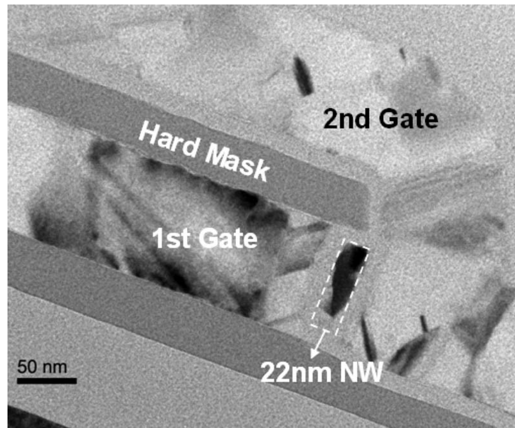

Fig. 5. TEM image of an independent double-gated transistor that shows 22-nm NW thickness.

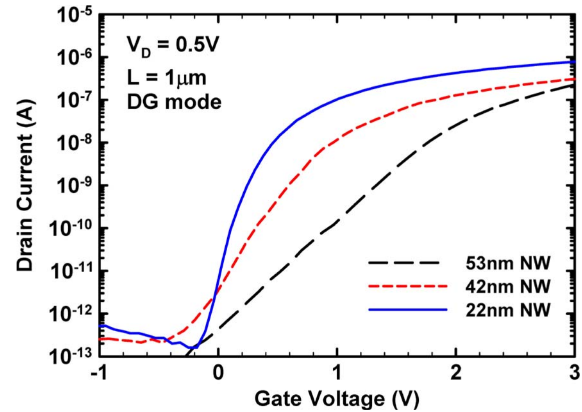

Fig. 7. Size dependency of transfer characteristics for devices with NW thickness of 53, 42, and 22 nm.

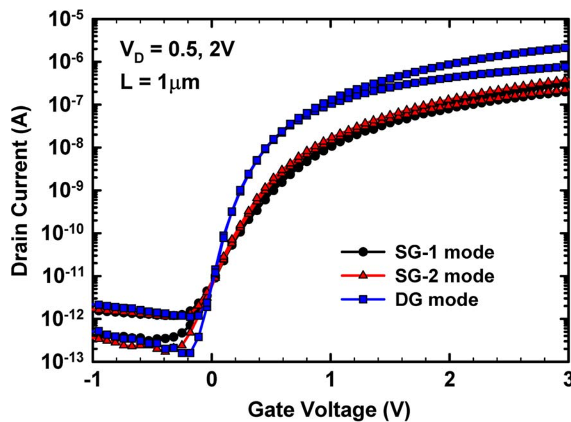

Fig. 6. Transfer characteristics of a fabricated device with implanted S/D.

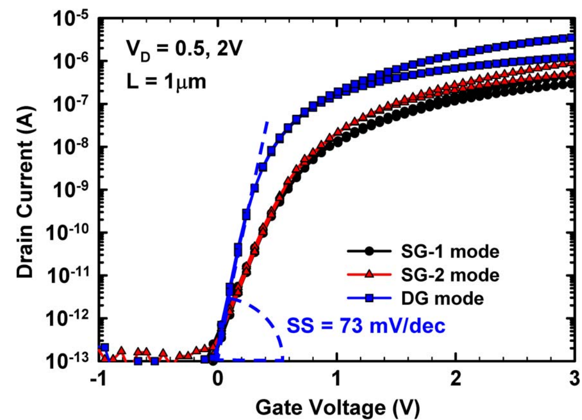

Fig. 8. Transfer characteristics of a fabricated device with *in situ* doped S/D.

dependency has been briefly discussed in [18], in which it was found that smaller NW thickness led to more improvement in DG operation. According to our recent calculation results [21], the major cause of enhanced DG performance over SG modes is its stronger grain boundary barrier modulation ability. Because reduced NW thickness enables gate coupling to a larger extent, this phenomenon manifests itself in steeper SS of DG operation, as evidenced in Fig. 7.

Fig. 8 shows the transfer characteristics of the device with *in situ* doped S/D with structural parameters nominally identical to the device characterized in Fig. 6. The ON/OFF current ratio of the DG mode at $V_D = 2$ V is more than 10^7, an order of

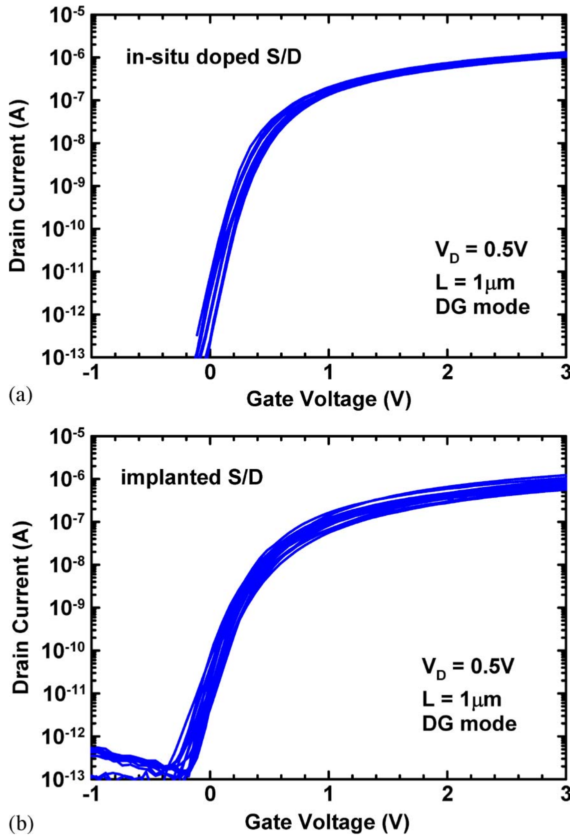

Fig. 9. Fluctuation analysis of devices with (a) *in situ* doped S/D and (b) implanted S/D.

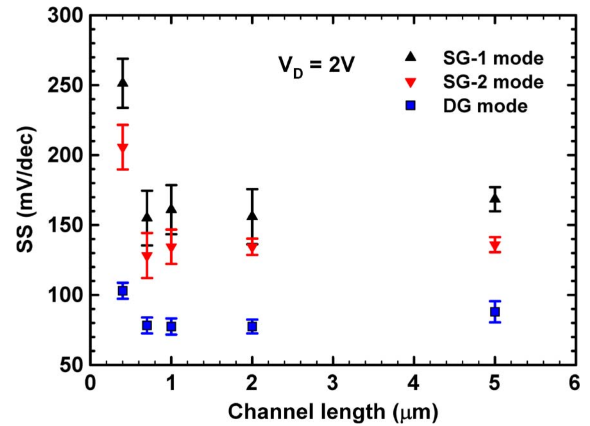

Fig. 10. SS as a function of channel length for the *in situ* doped device.

TABLE I
SUMMARY OF THE MAJOR CHARACTERISTICS OF DEVICES WITH IMPLANTED (FIG. 6) AND *In Situ* DOPED S/D (FIG. 8)

	Implanted S/D			*In-situ* doped S/D		
	SG-1	SG-2	DG	SG-1	SG-2	DG
V_{TH} (V)	0.51	0.45	0.29	0.59	0.56	0.31
SS (mV/dec)	184	171	89	153	149	73
I_{ON} (μA)	0.32	0.39	2.21	0.51	0.94	3.67
I_{OFF} (pA)	4.61	5	5.35	0.39	0.45	1.67
DIBL (mV/V)	26.6	13.3	12	18.1	12	10

V_{TH} is equal to V_G @ I_D = 10nA×W/L
V_{TH} and SS are extracted @ V_D = 2V
I_{ON} and I_{OFF} are extracted @ V_G = 3V, V_D = 2V and V_G = -2V, V_D = 2V, respectively

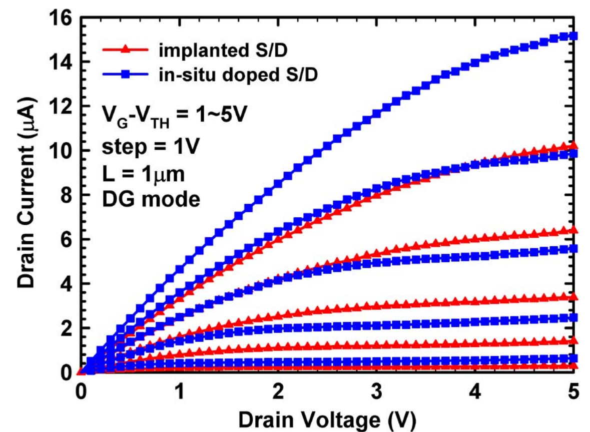

Fig. 11. Output characteristics comparison under the DG mode for devices with implanted and *in situ* doped S/D.

magnitude higher than that for the device with implanted S/D in Fig. 6. Furthermore, SS is enhanced from 89 mV/dec to 73 mV/dec under the DG mode when *in situ* doping technique is adopted. Note that, to the best of our knowledge, this result is the best value ever reported for a poly-Si based device. To prove that the aforementioned characteristics are representative of the whole picture, we have conducted fluctuation analysis in Fig. 9 by showing transfer curves of 20 devices with similar characteristics collected from a total of 29 and 26 devices for implanted and *in situ* doped types, respectively, amounting to 69% and 77% chip yield. Those not shown have either larger than 100-mV/dec SS or are simply not functional. As shown in the figure, the variation is not severe, and this result suggests the good uniformity offered by the selective plasma-etching technique. The mean value and standard deviation of $V_{\rm TH}$ at $V_D = 0.5$ V for *in situ* doped and implanted devices are 0.33 V, 35 mV and 0.31 V, 46 mV, respectively. SS distribution with respect to channel length is shown in Fig. 10 for *in situ* doped devices. Under DG operation, excellent immunity to the short-channel effect is observed, and the characterized devices demonstrate tight distribution.

Major device characteristics of both types of devices shown in Figs. 6 and 8 are summarized in Table I. The difference in $V_{\rm TH}$ between the two devices is small and within the measured fluctuation value. Aside from this, all the other device characteristics of the *in situ* doped type are superior to the implanted type. For the SS improvement, *in situ* doping avoids unintentional channel doping by ion implantation. Meanwhile, more uniform and highly activated doping concentration gives rise to larger ON/OFF current ratio due to smaller series resistance and reduced BTBT probability. This statement is further evidenced in the output characteristics shown in Fig. 11, where only those under the DG mode are displayed for clarity. At $V_G - V_{\rm TH} = V_D = 5$ V, the saturation current improvement over the implanted control device is 48%. For the SG-1 and SG-2 modes, under the same bias condition, the improvement is 107% and 5.4%, respectively (data not shown). The large

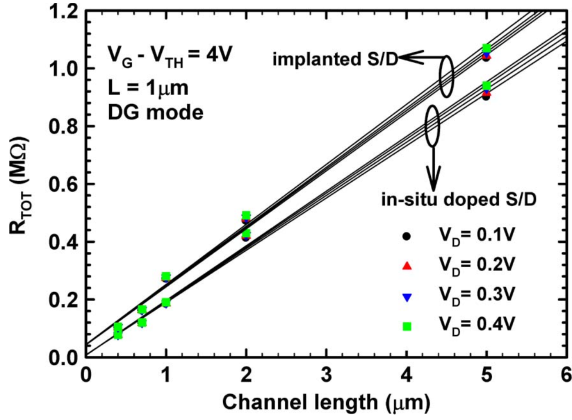

Fig. 12. Extraction of S/D series resistance showing five times reduction with the adoption of *in situ* doped S/D.

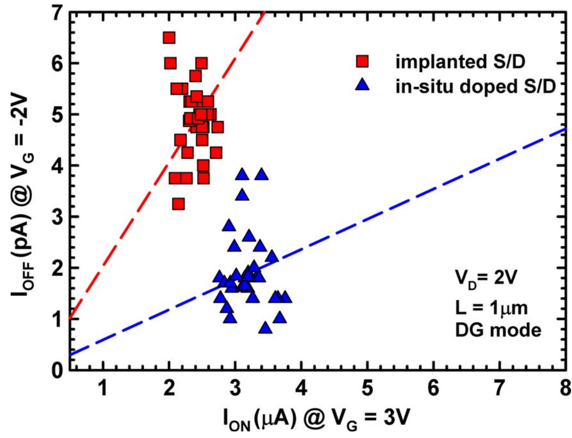

Fig. 13. $I_{\rm ON}$–$I_{\rm OFF}$ statistical analysis comparison between devices with implanted and *in situ* doped S/D.

disparity between the extent of improvement for the two SG modes is related to their different current paths from the source to the drain. If S/D is formed by ion implantation, carriers under the SG-1 mode must transport across a long distance of only moderately doped S/D before reaching the topmost portion of S/D where the resistivity is the smallest. Under the SG-2 mode, because the outer channel surface controlled by the second gate is closer to the most heavily doped S/D regions than the first gate, it is easier for carriers to reach the topmost S/D without experiencing significant series resistance. This condition explains why output current is dramatically improved for the SG-1 mode, whereas it is only slightly increased for the SG-2 mode when *in situ* doping results in S/D with lower series resistance. By using the measured output curve data, the total resistance can be plotted against channel length [22], as shown in Fig. 12. It is shown that there is approximately five times reduction in series resistance from 45 KΩ to 8.1 KΩ when S/D is formed by *in situ* doping.

For statistical analysis, the $I_{\rm ON}$–$I_{\rm OFF}$ plot is shown in Fig. 13. At a fixed $I_{\rm OFF}$ equal to 3 pA, the *in situ* doping method results in 252% $I_{\rm ON}$ improvement by increasing $I_{\rm ON}$ from 1.46 μA to 5.14 μA, suggesting the significance of S/D engineering for performance enhancement.

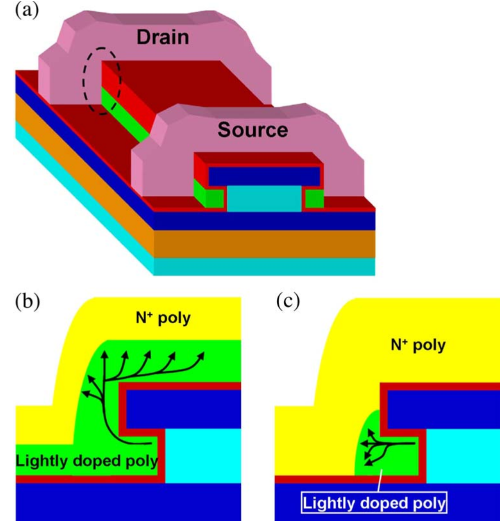

Fig. 14. (a) Schematic of the device structure before the second gate stack deposition. GIDL current conduction paths in the circled areas of (a) are depicted for (b) implanted S/D and (c) *in situ* doped S/D type devices.

The reason for the drastic GIDL current reduction with the adoption of *in situ* doped S/D is now discussed. There does not exist an absolute relationship between the GIDL current and S/D doping concentration [23]. At a given gate and drain bias, very low S/D doping concentration would lead to severe band bending at the drain/oxide interface. However, the depletion width is also large because of the low doping concentration. This condition increases the tunneling width; therefore, the BTBT probability is diminished. On the other hand, for the highly doped case, although the depletion width is extremely small, the band bending is also curbed, which corresponds to the *in situ* doped S/D scenario in this paper. Taking these factors into account, it is straightforward to understand that moderate S/D doping concentration is the most susceptible to GIDL, and this approach fits the implanted S/D type device. The GIDL current difference can be explained from another perspective in terms of the effective conduction area of leakage current in Fig. 14. To make it more lucid, Fig. 14(a) is the schematic structure before the second gate stack deposition. Fig. 14(b) and (c) shows, respectively, the major leakage current conduction paths in the gate/drain overlap regions that correspond to the circled areas in Fig. 14(a) for the implanted and *in situ* doped S/D type devices. Due to the dissimilar doping profiles, the lightly doped region, where GIDL easily occurs, is much more widespread in Fig. 14(b) than in Fig. 14(c), posing as another factor that accounts for the leakage current difference. In addition, the lightly doped areas are essentially nongated and behave as additional transport barriers, which can also explain the improvement of SS by the *in situ* doping technique.

V. Conclusion

In this paper, we have investigated the performance enhancement of a double-gated poly-Si NW transistor with *in situ* doped S/D, which can be fabricated by a simple selective plasma-etching process without resorting to sophisticated lithographic tools. Because of the elimination of ion implantation that is

likely to cause excessive dopant incorporation into the channel, the *in situ* doping technique has been shown to improve the SS down to 73mV/dec. We believe that this result is the best SS ever reported for any poly-Si channel based device. Due to the higher dopant concentration offered by the proposed method, five times reduction in series resistance is achieved compared with the control device, and leakage current that results from GIDL is substantially suppressed. The proposed NW device with excellent switching properties appears to be very promising for reducing the operational voltage and power consumption in future circuit applications.

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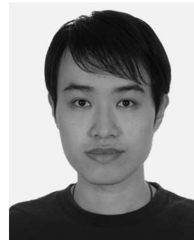

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