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Metal nanocrystals as charge storage nodes for nonvolatile memory devices

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Abstract

The memory effects of the metal nanocrystals were found to be more pronounced than those of the semiconductor nanocrystals. Various metal nanocrystals as charge storage nodes are reviewed. The memory effects have strong relationship with the work function, and the work function can be modulated by changing the metal species. By tunneling dielectrics engineering, the optimum $I_{\mathrm{G\ Write/Erase}}/I_{\mathrm{G\ Retention}}$ ratio can be obtained.
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1. Introduction

The flash memories have evolved from single device components to megabit nonvolatile memory (NVM) arrays [1]. Flash memories are easily scalable replacements for erasable programmable read only memory (EPROMs) and electrically erasable programmable read only memory (EEPROMs). Unlike EPROMs and EEPROMs, flash memory cells provide single-cell electrical program and fast simultaneous block electrical erase. Thus, a small cell size is combined with a fast in-system erase capability.

These low-power and powerful flash systems are ideal for a myriad of portable applications such as cellular phones, digital cameras, digital voice recorders, notebook computer, MP3 walkman, personal data assistants to compact smart cards, USB flash personal disc, etc. These products have been widely used and play important roles in the consumer market. They may eventually replace the ubiquitous magnetic memory media and random access memories (RAMs) in many compact electronic applications [2].

The effective flash technology compatible with the standard complementary metal-oxide-semiconductor (CMOS) device process flow presents some challenges. The bigger one is the inter-related scaling requirements for voltage and gate oxide for embedded flash devices. The aggressive scaling of gate dielectric to control deleterious short-channel effects in logic devices is intrinsically incompatible with the need to preserve minimum dielectric thickness in flash devices to maintain oxide reliability and data-retention after many write/erase cycles [3].

Furthermore, the program and erase voltages of flash devices are typically above 10 V. This is far too large for the one-volt-operation of logic CMOS devices. Erratic failure bits and increase in leakage-current when a device is stressed under high bias conditions compromise memory performance. As a result, research is moving along the following paths for embedded flash devices:

(1) scaling down the cell size of device memory;
(2) lowering voltage operation;

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(3) increasing the density of state per memory cell by using a multi-level cell.

To sustain the continuous scaling, conventional flash devices may have to undergo revolutionary changes. Novel device concepts with new physical operation principles are needed [4–8].

A memory cell is a system element that contains 1-bit of information. The standard commercial flash device is similar to the Intel EPROM Tunnel Oxide (ETOX) structure, as shown in Fig. 1(a). The basic device is a MOS-field-effect-transistor (MOSFET) with a modified gate stack structure that has a control gate (CG) and a floating gate (FG) embedded in a dielectric material such as SiO_2 [9].

Thus, flash memory cell scaling below the 0.1 μm feature size will be difficult, if channel-hot-electron (CHE) and Fowler–Nordheim (FN) injection processes are involved in the program and erase operations [3]. To circumvent these limitations, new device concepts that are more robust to leakages through oxide defects are being considered. Among the recent proposals are the silicon/oxide/nitride/oxide/silicon (SONOS), the nitride read-only memory (NROM) and the nanocrystals charge-storage nodes memories. The SONOS structure is shown in Fig. 1(b).

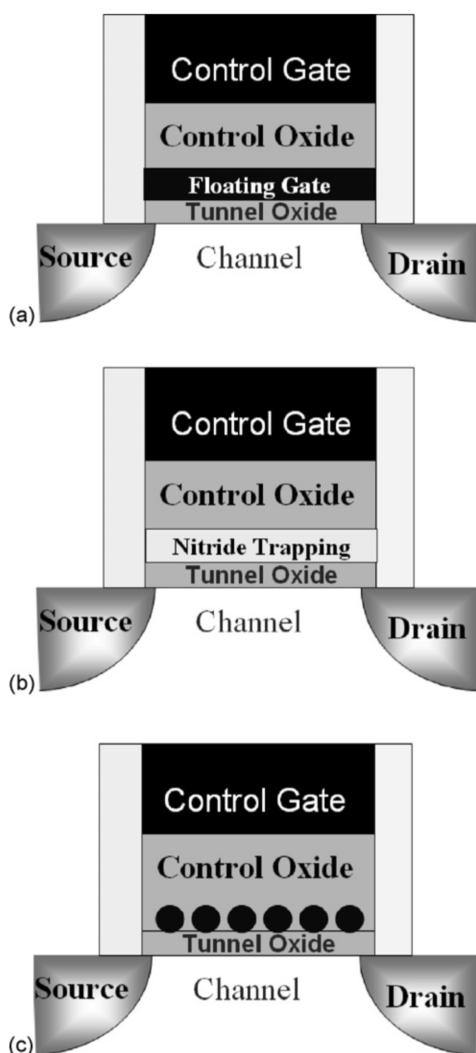

Fig. 1. The device structures of: (a) conventional nonvolatile flash, (b) SONOS stored unit nonvolatile flash, and (c) nano-dots stored unit nonvolatile flash.

These technologies replace the extended floating gate structure with a great number of charge-storage nodes in the dielectric. Unlike the extended floating gate, stored charges in isolated nodes cannot easily redistribute amongst themselves. If the storage node density is much higher than the defect density in the isolation dielectric, only a relatively small number of nodes will be drained by defects. This effectively prevents the leakage of all the stored charge out of the floating gate.

2. Nanocrystals structure

Beside the SONOS structure, Tiwari et al. first proposed flash memory with a floating gate made out of silicon nanocrystals [8]. The nanocrystals are extremely small clusters of Si atoms ranging from 5 to 10 nm in diameter. As illustrated in Fig. 1(c), the nanocrystals embedded between the tunneling and controlling dielectric. By limiting nanocrystals deposition to just one layer and adjusting the thickness of the top controlling dielectric, charge leakages to the control gate from the nanocrystals can be effectively prevented. Also, compared to the atomic-size nitride traps, electron or hole energy states are energetically deeper in the nanocrystal wells. Conceptually, the increased confinement and the reduction in leakages imply that tunneling oxide can be more aggressively scaled down. With a thin tunnel oxide, direct quantum-mechanical tunneling can be exploited as a transport mechanism for programming and erasing the charges in the nodes.

Memory-cell structure using nanocrystals as the charge storage media have received much attention as the promising candidates to replace conventional dynamic random array memory or flash memories for future high speed and low power consumer memory devices [8,10,11]. Most studies have focused on the fabrication on Si and Ge nanocrystals in metal-oxide-semiconductor (MOS) structure [12–20]. In addition, atomic-force-microscopy (AFM) was utilized to inject charges in the nanocrystals [21–23]. The use of a floating gate composed of distributed nanocrystals reduces the problems of charge loss encountered in conventional floating-gate electrically erasable programmable read-only memory devices. It allows thinner tunnel oxide and, thereby, smaller operating voltages, better endurance and retention, and faster program/erase speed [13–15].

In optimizing such devices, the ideal goal is to achieve the fast write/erase of DRAM and the long retention time of flash memories simultaneously. For this purpose, we need to create an asymmetry in charge transport through the gate dielectric to maximize the $I_{\mathrm{G\ Write/Erase}}/I_{\mathrm{G\ Retention}}$ ratio. For dielectrics engineering, by replacing the rectangular barrier with a parabolic or triangular barrier, the barrier height can be modulated by the electric field in the tunnel oxide [24]. In practice, the parabolic or triangular barrier can be simulated by stacking multiple layers of dielectrics.

Another approach is to use double-stacked storage nodes, preferably self-aligned with smaller dots at the lower stack. In

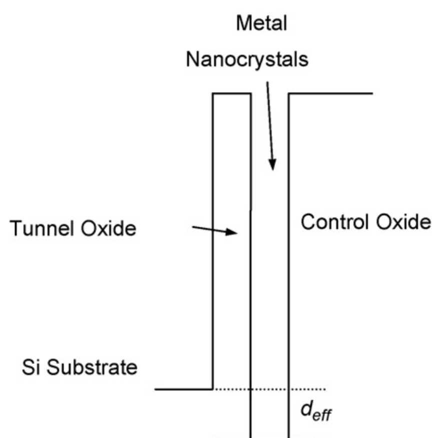

Fig. 2. Energy band diagram for embedded metal nanocrystals between control oxide and tunnel oxide.

such devices, fast write/erase can still be achieved, if sufficiently thin tunnel oxides are used below and between the two stacks. However, the retention time can be significantly improved due to the Coulomb blockade effect at the lower stack, which prevents electrons in the top stack storage nodes from tunneling back into the substrate [25].

The third approach, which is the focus of this paper, is to engineer the depth of the potential well (d_{eff}) at the storage nodes, thus creating an asymmetrical barrier between the substrate and the storage nodes, i.e., a small barrier for writing and a large barrier for retention. This can be achieved if the storage nodes are made of metal nanocrystals. The energy band diagram for embedded metal nanocrystals between control oxide and tunnel oxide is shown in Fig. 2.

In this paper, we will discuss unique features of metal nanocrystal memories in comparison with their semiconductor counterparts. The metal nanocrystal memory possesses several advantages, such as stronger coupling with the conduction channel, a wide range of available work functions, higher density of states around the Fermi level and smaller energy perturbation due to carrier confinement [26].

3. Work function engineering

The memory effects of the Ag, Au, Pt, W, Co, Ni, $NiSi_2$, $Ni_{1-x}Fe_x$, TiN and Al metal nanocrystals were investigated [26–43]. Devices with Au, Ag and Pt nanocrystals working in the F–N tunneling regime have been investigated and compared with Si nanocrystals memory devices. The memory effect will be seen when the effective potential well depth (d_{eff}) is higher. As a result, the memory effects of the Pt and Au are better than the Ag [26–29]. The work functions of various metallic materials are listed in Table 1.

For the industrial applications, the Pt and Au are precious metals that would increase the fabrication cost. Therefore, metallic materials with high work function, but not the precious metals, are more desirable. There are a number of reports on high work function materials with significant memory effects [30–43]. For example, good memory effects were found for

Table 1
Work functions of various metallic materials

Element	Work function, Φ (eV)
Au	5.10 ± 0.1
Ag	4.33 ± 0.15
Pt	5.32 ± 0.1
W	4.55 ± 0.1
Ni	4.96 ± 0.1
$NiSi_2$	4.71 ± 0.1
$CoSi_2$	4.70 ± 0.1
Al	4.24 ± 0.1
TiN	2.92 ± 0.1

devices with the W nanocrystals and the work function of W is 4.55 eV [30,31].

The W-rich tungsten silicide layer, W_5Si_3, was physically sputtered onto the tunnel oxide. The W_5Si_3 layer was capped by an amorphous-Si layer deposited also by sputtering. The stacked structure was, afterwards, dry oxidized at 900 °C to form a layer with control oxide on the top and W nanocrystals precipitated and embedded between tunnel oxide and control oxide. Fig. 3 represents a typical bright-field, cross-section TEM image. Spherical and well-separated W nanocrystals embedded in the SiO_2 layer are clearly observed. Fig. 4 shows the capacitance–voltage (*C–V*) hysteresis after bidirectional sweeps, which implies the electron charging and discharging effects of W nanocrystals embedded in SiO_2. In Fig. 4, with the voltage swept from 3 to (−4) V and back to 3 V, a significant threshold voltage shift of 0.95 V is observed. As the swept voltage is increased to 8 V or 10 V, a more pronounced *C–V* shift is observed. It is worth noting that the hysteresis is counterclockwise which is due to substrate injection from the electrons of the deep inversion layer and holes of the deep accumulation layer of Si substrate [44].

Ni, $NiSi_2$ and $CoSi_2$ nanocrystals embedded in the SiO_2 exhibiting memory effects have been formed; the cross-section TEM images and *C–V* hysteresis are shown in Figs. 5–7, respectively. The Ni nanocrystals embedded in the SiO_2 layer has been formed by rapid thermal annealing of a SiO_2/Ni/SiO_2 structure at

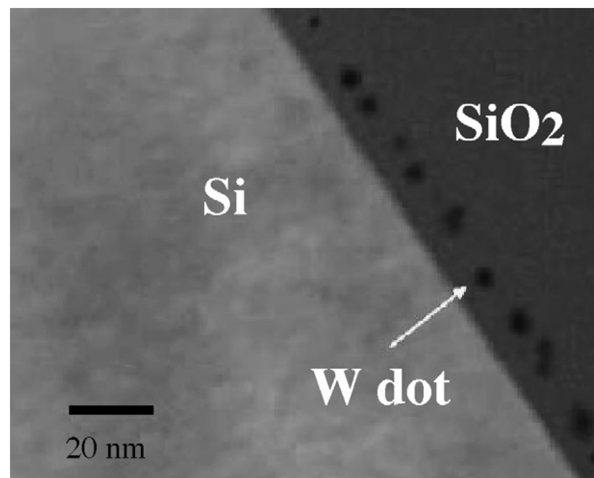

Fig. 3. Cross-section TEM image of the W nanocrystals embedded in the SiO_2.

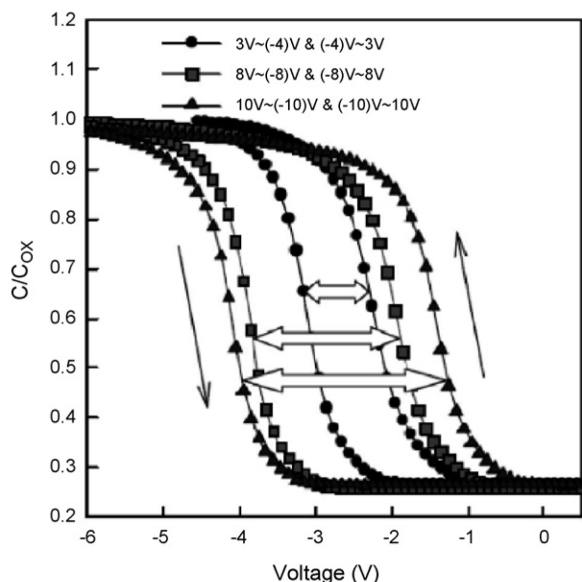

Fig. 4. The capacitance–voltage (*C–V*) hysteresis after bidirectional sweeps, which implies the electron charging and discharging effects of W nanocrystals embedded in SiO_2.

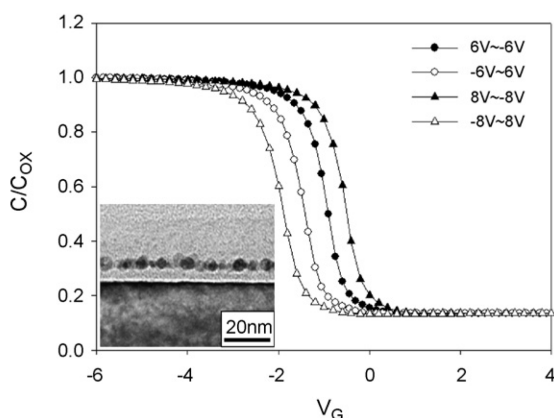

Fig. 5. The *C–V* hysteresis of Ni nanocrystals embedded in SiO_2. Inset is the cross-section TEM image. Well-separated and spherical Ni nanocrystals are seen.

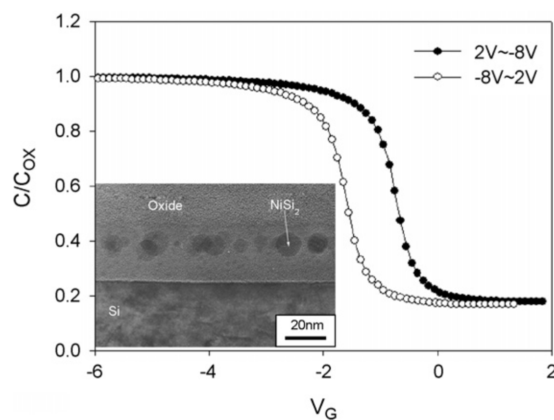

Fig. 6. The *C–V* hysteresis of $NiSi_2$ nanocrystals embedded in SiO_2. Inset is the cross-section TEM image. Well-separated and spherical $NiSi_2$ nanocrystals are seen.

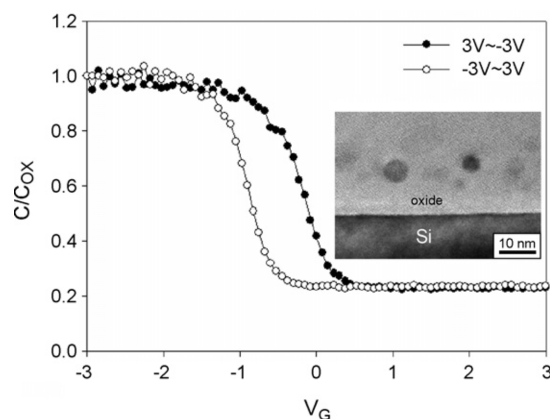

Fig. 7. The *C–V* hysteresis of $CoSi_2$ nanocrystals embedded in SiO_2. Inset is the cross-section TEM image. Well-separated and spherical $CoSi_2$ nanocrystals are seen.

400 °C. The $NiSi_2$ and $CoSi_2$ nanocrystals have been formed by thermal oxidation of an amorphous-Si/Ni/SiO_2 and amorphous-Si/Co/SiO_2 structures, respectively. The stacked structure was, afterwards, dry oxidized at 900 °C to form a layer with control oxide on the top and $NiSi_2$ or $CoSi_2$ nanocrystals precipitated and embedded between tunnel oxide and control oxide. The insets of Figs. 5–7 are the cross-section TEM images showing the well-separated and spherical Ni, $NiSi_2$ and $CoSi_2$ nanocrystals, accordingly. The mean sizes of the Ni, $NiSi_2$ and $CoSi_2$ nanocrystals are 3.7, 7.6 and 4.4 nm, respectively. The significant threshold voltage shift of 1 and 1.1 V are seen for $NiSi_2$ and $CoSi_2$ nanocrystals, correspondingly, as the charge storage nodes at low voltage operation, respectively.

Other nanocrystals as the charge storage nodes, like TiN and Al, with memory effects have also been studied [32–34]. The memory windows are sufficient to be defined as "1" and "0" by a typical sensing amplifier for a memory device. Using the metal nanocrystals to be the charge storage nodes, various dielectrics were used for the tunnel dielectric to maximize the $I_{G\ Write/Erase}/I_{G\ Retention}$ ratio. The influence of the tunneling dielectric to the memory effect is also addressed.

4. Dielectric engineering

The fabrications of the metal nanocrystals using other tunneling and capping dielectrics have attracted a great deal of interest. Nonvolatile memory with Ni nanocrystals embedded in HfO_2 has been investigated. The initial Ni layer thickness and annealing temperature were found to influence the Ni nanocrystal formation [35–37]. The size and density of the nanocrystals were found to increase and decrease with the annealing temperature, respectively.

$NiSi_2$ nanocrystals embedded in the SiO_2 layer exhibiting memory effect has been formed [38,39]. The $NiSi_2$ nanocrystals using the SiO_2 and HfO_2 for the tunneling dielectrics were also fabricated. Two sets of samples (samples A and B) were prepared. Samples A and B consist of 3-nm-thick SiO_2 and 2-nm-thick HfO_2/1-nm-thick SiO_2 as the tunneling dielectrics, respectively. The detailed conditions for the preparation of

Table 2
Detailed conditions for the preparation of samples A and B

	Samples	
	A	B
SiO_2 (nm)	1	3
HfO_2 (nm)	2	–
Ni (nm)	1.5	1.5
Si (nm)	3.5	3.5
Anneal (°C)	600	600
HfO_2 (nm)	18	18

the samples A and B are listed in Table 2. The cross-section TEM images of the $NiSi_2$ using the SiO_2 and HfO_2 tunneling dielectrics are shown in Fig. 8. One nanometer-thick SiO_2 in the samples B was used to improve the flat interface between the Si substrate and the tunneling HfO_2. The physical thickness of samples A and B are all 3 nm, but the effective oxide thickness (EOT) of the samples B is 1.5 nm, which is half of that in samples A. So the memory effect will be increased, when using the HfO_2 to replace the SiO_2 for the tunneling dielectric at the same programming voltage, as shown in Fig. 9. The memory windows of the $NiSi_2$ using SiO_2 and HfO_2 tunneling dielectrics are 1.04 and 1.38 V, respectively. The memory window of the samples with HfO_2 tunnel dielectric is larger than the samples with SiO_2 owing to the smaller voltage drop for HfO_2 tunnel dielectric with the same physical thickness. Fig. 10 shows the retention characteristics for the samples A and B. The retention characteristics were rather poor for the samples B. It is ascribed to the EOT (1.5 nm) being too thin so that the electrons can tunnel back easily. The physical thickness of HfO_2 tunnel dielectric is enough for the small operation voltage, but not adequate for the retention requirement. The tunneling probability of electron is related to the thickness and the barrier of the tunnel dielectric. Fig. 11 shows the band diagrams of $NiSi_2$ nanocrystals with SiO_2 or HfO_2 tunnel dielectrics after programming. When the device is written or programmed, the electrons directly tunnel from the Si substrate through the tunnel dielectric, and are trapped in the $NiSi_2$ nanocrystals. Without applied voltage, the band diagrams are shown as Fig. 11(a and b) for SiO_2 and HfO_2, respectively. At this stage, the electrons may tunnel back to Si substrate. The tunnel probability of electrons is strongly related to the thickness and barrier of the tunnel dielectrics without operation voltage. In the present investigation, the samples using HfO_2 appear to be inferior to the SiO_2 tunnel dielectric in the retention characteristics. But if the optimum thickness of the HfO_2 can be found, it is

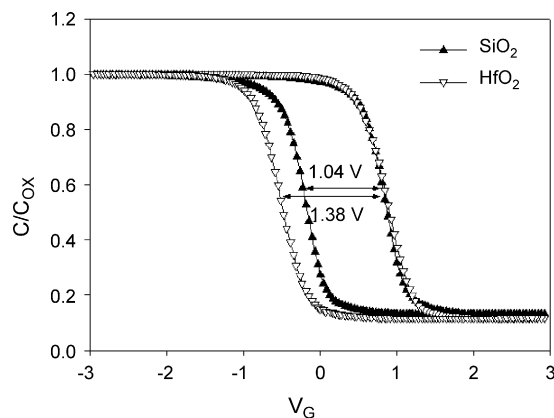

Fig. 9. The C–V hysteresis of the $NiSi_2$ using SiO_2 and HfO_2 tunneling dielectrics. The memory windows of the $NiSi_2$ using SiO_2 and HfO_2 tunneling dielectrics are 1.04 and 1.38 V, respectively.

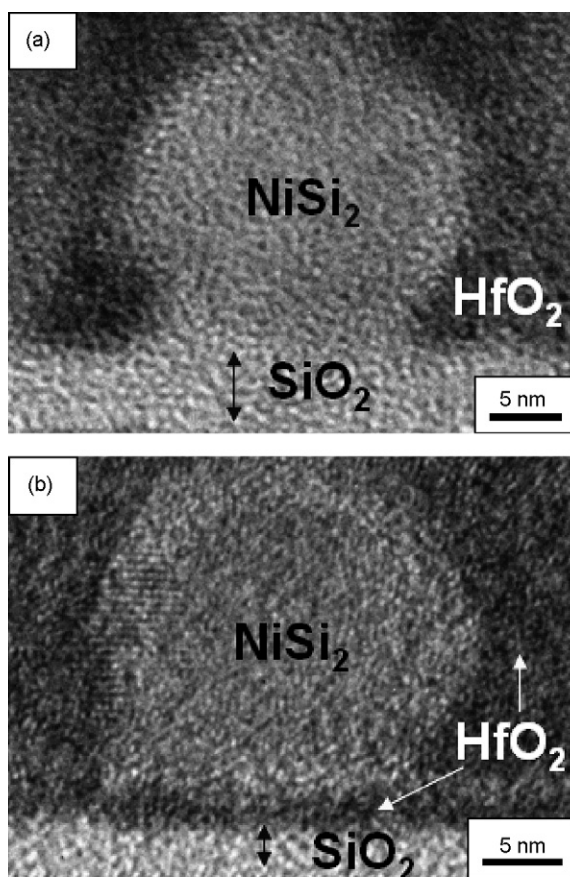

Fig. 8. (a and b) The $NiSi_2$ nanocrystals with SiO_2 and HfO_2 tunnel dielectrics, respectively.

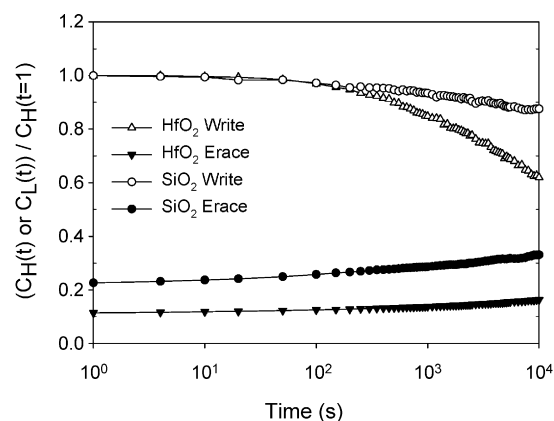

Fig. 10. The retention characteristics for the samples A and B. The retention characteristic was rather poor for the sample B. It is ascribed to the EOT (1.5 nm) is too thin so that the electrons can be tunneled back easily.

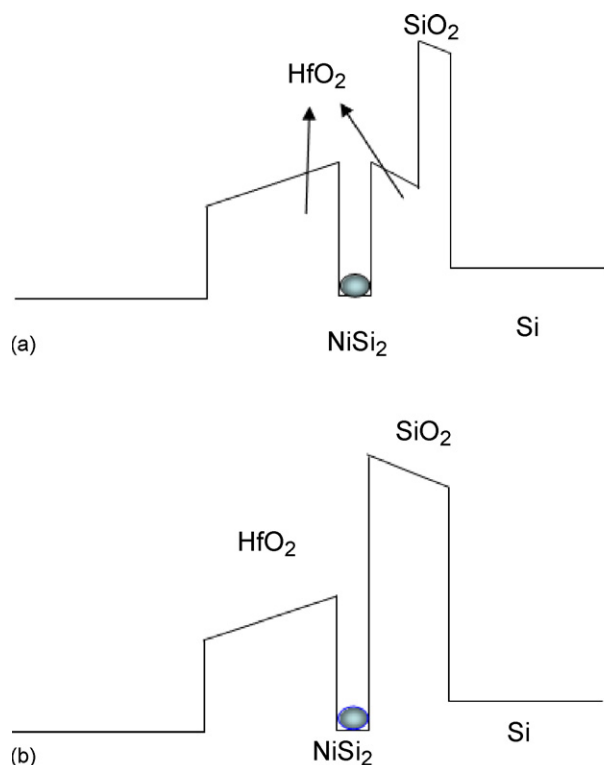

Fig. 11. The band diagrams of $NiSi_2$ nanocrystals with SiO_2 or HfO_2 tunnel dielectrics after programming.

possible that more favorable maximum $I_{G\ Write/Erase}/I_{G\ Retention}$ ratio can be obtained.

There are other dielectrics used as the tunneling dielectrics. As an example, self-assembled $Ni_{1-x}Fe_x$ nanoparticles embedded in a polyimide (PI) matrix were formed by curing $Ni_{1-x}Fe_x$ thin films with polyimide precursor layers [40]. The $Ni_{1-x}Fe_x$ nanocrystals were created inside the PI layer. The process can be conducted at relatively low temperature with the highest temperature being 400 °C.

For the various metal nanocrystals as the charge storage nodes described, the memory effects of the various metal nanocrystals are summarized in Table 3.

Table 3
Memory effects of various metal nanocrystals

Element	Tunnel dielectric	V_{th}, C–V (V)	Sweep voltage (V)
Au	SiO_2	2.3	2 to −4
Ag	SiO_2	2.1	2 to −4
Pt	SiO_2	3.8	2 to −4
W	SiO_2	0.95	3 to −4
Ni	SiO_2	0.52	6 to −6
	HfO_2	0.75	2 to −2
$NiSi_2$	SiO_2	1.04	3 to −3
	HfO_2	1.38	3 to −3
$CoSi_2$	SiO_2	1.1	3 to −3
Al	AlN	1	5 to −5
$Ni_{1-x}Fe_x$	PI	2	11 to −6
TiN	Al_2O_3	2.9	NA

5. Room temperature deposition

In addition to the metal nanocrystals fabricated by thermal annealing, there are other fabrication processes to form the metal nanocrystals. The Langmuir–Blodgett technique is a room-temperature deposition process that may be used to deposit monolayer and multilayer films of organic materials. Furthermore, this method permits the manipulation of organic molecules on the nanometer scale, thereby allowing intriguing superlattice architectures to be assembled [45]. The Langmuir–Blodgett deposition of organically passivated Au nanoparticles is reported [41]. A monolayer of these particles has been incorporated into a MIS structure.

6. Four bits per cell

Scaling down the memory device is to increase the density of the memory cell for NVM, but there is scaling limitation to all NVM technologies. Instead of scaling down NVM, one important new innovation is multi-bits per cell. Based on the 2-bits per cell metal nanocrystal memories [27], a novel quad source/drain device capable of 4-bits per cell data storage is demonstrated [43]. Along with the new device structure, a reliable parallel read scheme is also proposed and verified for 4-bit-per-cell operations.

7. Conclusions

After explosive study on the NVM in application, NVM has come of age as a mainstream memory product. Using the metal nanocrystals as the storage nodes has a great deal of advantages for the memory effects. Extensive researches on metal nanocrystals as the storage nodes for NVM have been conducted. In this paper, we review the memory effects of the Ni, $NiSi_2$, $CoSi_2$ and $NiSi_2$ with SiO_2/HfO_2 tunneling dielectrics. The memory windows of $NiSi_2$ and $CoSi_2$ nanocrystals are 1 and 1.1 V at low programming voltage, respectively. By tunneling dielectrics engineering, the optimum $I_{G\ Write/Erase}/I_{G\ Retention}$ ratio may be obtained.

Acknowledgments

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