Chapter 1

Introduction

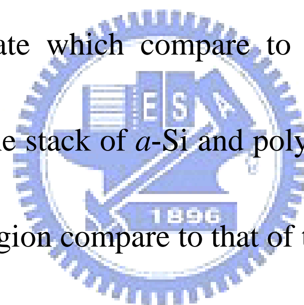
1-1 General Background

As the scaling of CMOS structure reaches its fundamental limits, the improvement of carrier mobility has been intensively studied by introducing strain in the channel region. This has been demonstrated in a strained Si devices on SiGe substrate which have been used the lattice mismatch between Si and SiGe. Theoretical calculations indicate that Si strained in biaxial tension should exhibit a higher mobility than bulk Si. The tensile strain induced quantization in the MOS inversion layer formed by the triangular potential well splits the six-fold degenerate Si conduction band minimum into a two-fold ($\triangle_2$) and a four-fold ($\triangle_4$) degenerate band. A self-consistent Schrödinger-Poisson solution was used to determine the sub-band splitting. The population of the $\triangle_2$ and $\triangle_4$ bands is then the total number of electrons in all of their respective sub-bands. The energy difference $\triangle E$ between $\triangle_2$ and $\triangle_4$ bands will determine the total relative population of the bands. Since electrons preferentially populate the $\triangle_2$ band, which is lower in energy, the electron mobility enhancement due to the stronger population primarily reflects the reduction in inter valley phonon scattering, and the reduced in-plane effective mass in this band [1-7]. However, the fabrication of the strained Si devices is more complicated, such as forming a relaxed

SiGe buffer layer. Recent studies have shown that the uniaxial strained channel from a contact etch-stop silicon nitride (SiN) layer affects the current drivability [5-6]. Depending on the deposition condition, the SiN layer which is placed directly over the transistor can generate high level internal stress that is either tensile or compressive. In general, SiN layer with tensile stress produced by thermal CVD and with compressive stress produced by PECVD. Unfortunately, uniaxial tensile strain only improves the electron mobility but degrades the hole mobility and the compressive strain is in the opposite direction. The drive currents of nMOSFETs and pMOSFETs are therefore in trade-off relationship in terms of mechanical strain. In order not to degrade either of them, Local Mechanical-Stress Control (LMC) technique has been demonstrated [7-8]. It utilized a SiN layer with high mechanical stress and selective Ge-ion implantation into the SiN layer, can improve the performance of nMOSFETs and pMOSFETs simultaneously. Ge-ion implantation which destroyed many bonds can relax the stress in SiN layer. The stress level of SiN layer decreased as the Ge-ion implantation energy is increased. However, additional Ge implantation process has to increase one more photo alignment in CMOS process. This kind of strained Si devices has many difficulties in manufacturing and increases the total cost in CMOS process. For this reason, the local strained channel (LSC) technique is proposed which provides highly tensile strained channel only in nMOSFETs by forming

compressively strained poly silicon (poly-Si) gate electrodes [9]. Compressive stress of n^+-poly gate, which is enhanced by cap high tensile SiO_2 and annealing process, derives from expansion of arsenic implanted poly-Si. On the other hand, p-channel is not strained, because boron implanted poly-Si is hardly expanded. Therefore, the improvement of current drivability of nMOSFETs without degrading the performance of pMOSFETs has been realized.

In this study, we proposed a local strained channel technique that using deposition of SiN layer with high mechanical stress and demonstrated the stack of amorphous silicon (*a*-Si) and poly-Si gate which compare to that of the single-poly-Si gate structure. It was found that, the stack of *a*-Si and poly-Si gate is estimated to increase tensile strain in the channel region compare to that of the single-poly-Si gate structure. The mechanism of the stress elevation could be as follows: before the dopant activation process, the n^+-poly gate is in amorphous phase due to the stack of *a*-Si and high dose implantation of arsenic. The re-crystallization of amorphous region during rapid thermal annealing leads to n^+-poly gate expansion, and resulting in residual compressive stress [9]. Furthermore, thermal CVD SiN-capping layer with highly tensile stress enhances compressive strain in the n^+-poly gate. Therefore, the highly compressive stress in n^+-poly gate provides high tensile strain to the channel region. We experimentally demonstrate the improvement of current drivability of nMOSFETs



with control the stress to the channel region. The drain current is improved 17% compared to that of the conventional devices. The current drivability can be enhanced by controlling the thickness of the *a*-Si stack and SiN-capping layer. We believe that the performance changes are caused by changes of the electron mobility. We also demonstrated the threshold voltage can be tunable with different thickness of the SiN layer. We found that the strain dependence of mobility enhancement will become significant by using both SiN-capping layer and stack of *a*-Si gate structures.

1-2 Thesis Organization

This dissertation is divided into four chapters as follows:

In chapter 1, a brief general background of strained Si devices is introduced to describe the various characteristics. Then we discuss recent studies in local strained channel devices and motivation of our study. The organization throughout this dissertation is described here.

In chapter 2, we report the process flow with the stack gate poly-Si and SiN-capping layer for fabricating n-channel metal oxide semiconductor field effect transistors.

In chapter 3, we demonstrate the characteristics of local strained channel devices

with the stack gate poly-Si and SiN capping layer. The improvement of electron mobility is turn out by elevating strain in the channel region. Moreover, we found that the strain dependence of mobility enhancement will become significant by using both SiN-capping layer and stack of *a*-Si gate structures. Then we discuss the important issue while we attempt to enhance carrier mobility by introducing strain in the channel region on device fabrication.

In chapter 4, we summary our experimental results and give a brief conclusion. Recommendations are also given for further study.

Chapter 2

Device fabrication

The local strained structure with the stack of *a*-Si and SiN-capping layer has been fabricated. The schematic cross section is illustrated in Fig. 2-1. After BF_2 implantation for p-well region, CVD SiO_2 for oxidation enhanced diffusion (OED) in well drive-in process. Active region alignment follows pad oxide and Si_3N_4 deposition. After Si_3N_4 etch, BF_2 implantation for the sake of channel stop. Then, field oxidation was carried out in high temperature ambient for LOCOS isolation. Two sacrificial oxide deposition followed Si_3N_4 removal process to eliminate Kooi effect. Then, threshold voltage adjustment form by arsenic implantation and phosphorus implantation was performed in order to anti-punch through. After RCA cleaning process, 2.5nm gate oxidation was carried out in vertical furnace (800°C, O_2 ambient). *a*-Si (550°C, 20-70nm) and in-situ doped n^+ poly-Si (550°C) were deposited in the same ambient followed by gate oxidation. The total thickness of poly-gate for all samples is 200nm. Then, poly-Si and *a*-Si etch followed gate alignment process. After sidewall polymer removal, wafers underwent n^+-source / drain implantation (As, 20 kev, 5E15) followed alignment process. Rapid thermal annealing was carried out in nitrogen ambient at 1050°C for 10 seconds followed p^+-substrate implantation (BF_2, 50 kev, 2.5E15). Thermal CVD SiN layer (at 780°C) with different thickness,

20-280nm, was directly deposited on the transistor and followed by TEOS (at 700°C, 350-550nm) deposition. After contact alignment, TEOS and SiN etch were carried out in the same system. This step is the key to this experiment. In the first place, we used the dry etching process to remove the upper TEOS and dipped in BOE solution to confirm that the TEOS was completely removed. Then, we used another recipe to etch the lower SiN layer in the same system. In order to protect the Si surface without plasma etching damage, SiN layer was etched in two-step. We calculated the SiN etch rate and kept 20nm after dry etching process. Then, we used H_3PO_4 solution to etch the residual SiN layer. In order to confirm the contact hole without SiN residual, an over-etching (100%) step in the wet etching process was used. After these processes, (Ti / TiN / Al / TiN) four-level metallization were carried out in PVD system and final alignment was followed this process. After the metal etching process, annealing in a H_2 / N_2 ambient at 400℃ for 30 minutes was performed in order to mend dangling bonds and reduce interface state density in oxide / Si interface.

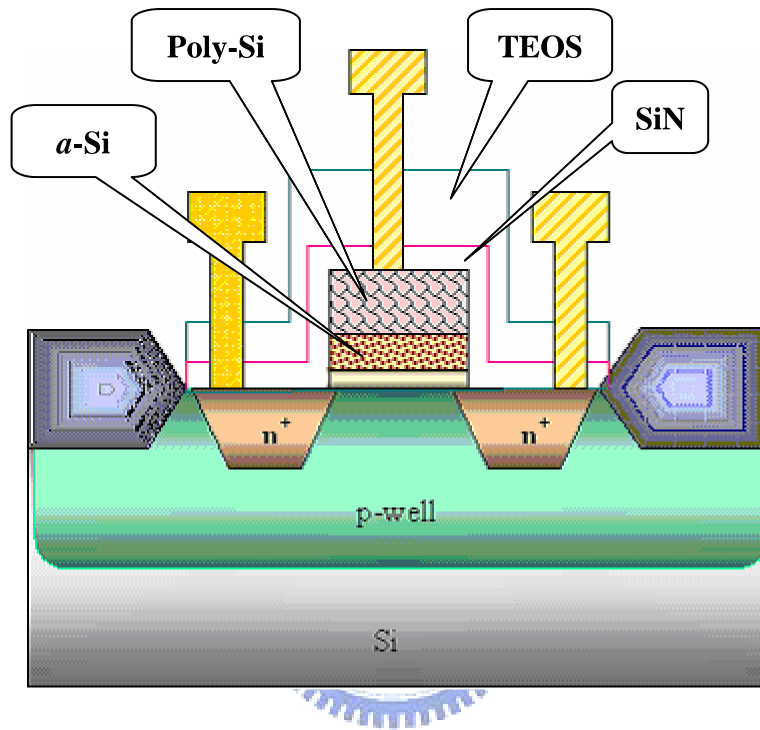


Fig. 2-1 Schematic cross section of the local strained channel nMOSFET.

Chapter 3

Results and Discussion

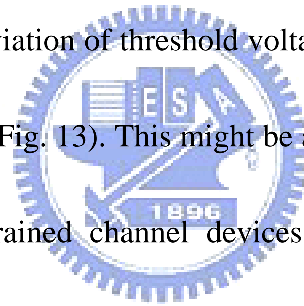
3-1 Single-poly-Si gate structure with different thickness of SiN-capping layer

nMOSFETs with four different structures of the stack of *a*-Si and four different thickness of SiN-capping layer has been fabricated as shown in Table I. In the first place, we discussed the characteristics of the single-poly-Si gate structure with different thickness of SiN layer. The dependence of I_d-V_g characteristics on different thickness of SiN layer is shown in Fig. 3-1. The improvement of the drain current is in proportion to the thickness of SiN layer. The transconductance increases with the increase of thickness of SiN layer is shown in Fig. 3-2. This result implies that the increase of electron mobility is the cause of the observed enhancement of the drain current. The mechanism could be as follows: CVD SiN layer with highly tensile stress provides compressive strain in the poly-Si gate and induces highly tensile strain to the channel region. The strain induced quantization in the inversion layer formed by the triangular potential well, splits the conduction band and increases the total relative population energy. The electron mobility enhancement due to the stronger population primarily reflects the reduction in inter valley phonon scattering, and the reduced in-plane effective mass in this band. However, if the thickness of SiN layer is not thick enough, the strain effect is not clear and obvious, even cause the performance

degradation. The pronounced enhancement of drain current with capped SiN layer is shown in Fig. 3-3. The drain current of nMOSFETs with capped 2800Å SiN layer shows 15% increased compare to that of the conventional device. The dependence of threshold voltage on different thickness of SiN layer is shown in Fig. 3-4. The threshold voltage decreases as the thickness of SiN layer is increased. This result indicates that we can tune the threshold voltage by different thickness of SiN-capping layer for other device applications. Fig. 3-5 illustrates a measured C-V profile with different thickness of SiN layer. The inversion capacitance and flat band voltage in long channel devices (10 μm) are almost the same as that of the conventional devices. However, if the threshold voltage depends on SiN thickness, we should observe the difference in C-V characteristics. To see what happens, we measured the C-V characteristics for short channel devices (5 μm). Fig. 3-6 illustrates a measured C-V profile of 5um channel length devices with different thickness of SiN layer. We observed that the flat band voltage shift increases with the increase of thickness of SiN layer. This fact means that the strain dependence of performance enhancement is only pronounced in short channel devices. Based on this result, we suspected the threshold voltage decreases with the increase of SiN thickness is due to the short channel effect. The effective channel length could be reduced during SiN deposition. The threshold voltage roll-off characteristics are illustrated in Fig. 3-7. The short

channel effect increases with the increase of thickness of SiN layer. However, even though the short channel effect is getting serious, the threshold voltage in the strained devices is still larger than the conventional device except the sample with capped 2800Å SiN layer. This maybe is due to a long processing time for deposition of thicker SiN film. However, the short channel effect is not serious in the observed results. Therefore, we believe that the improvement of current drivability is dominated by introduced tensile strain to the channel region. The dependence of junction resistance by capping SiN layer of different thickness is shown in Fig. 3-8. It shows that the enhancement of current drivability is not due to the reduction of junction resistance. This implies that the junction profile is almost the same during SiN deposition. Fig. 3-9 shows the dependence of junction leakage current on different thickness of SiN layer. The leakage current increases with the increase of thickness of SiN layer. The stress elevation could generate more leakage path in the junction area. However, it is not serious and results in little difference with the increase of SiN thickness. Fig. 3-10 ~ Fig. 3-12 illustrate the charge pumping measurement to define the quality of oxide / Si interface after the strain is introduced to channel region. The dependence of charge pumping current on different thickness of SiN layer is shown in Fig. 3-10 and Fig. 3-11. The charge pumping current decreases as the thickness of SiN layer is increased. This result implies that the

decrease of charge pumping current is the cause of the observed reduction of threshold voltage. Fig.3-12 shows the dependence of interface state density on different thickness of SiN layer. It shows that the interface state density decreases as the SiN thickness is increased. This means that the strain elevation in the channel region is prone to improve the quality of oxide / Si interface even though still inferior quality than conventional devices. Fig. 3-13 and 3-14 illustrate the effects of device reliability with different thickness of SiN layer. The dependence of channel hot carrier effect on different SiN thickness is shown in Fig. 3-13 and Fig. 14 (Stress Condition: 3.75V, for 10000sec). The deviation of threshold voltage in conventional device is the largest among these samples (Fig. 13). This might be a different mechanism in change of oxide quality in local strained channel devices. However, the degradation of transconductance is become more significant by increasing the thickness of SiN layer (Fig. 3-14). It might be decreased the fixed oxide charge but increased the electron traps near the oxide / Si interface. Therefore, the improvement of oxide / Si interface quality is an important issue while we attempt to enhance carrier mobility by introducing strain in the channel region on device fabrication.



SiN-capping layer / Gate structure	SiN-200	SiN-500	SiN-1000	SiN-2800
Poly-2000	△	△	△	△
***a*-Si-200+Poly-1800**		△		
***a*-Si-500+Poly-1500**	△	△	△	△
***a*-Si-700+Poly-1300**		△		

Table. I Gate structures and SiN conditions for local strained channel devices.

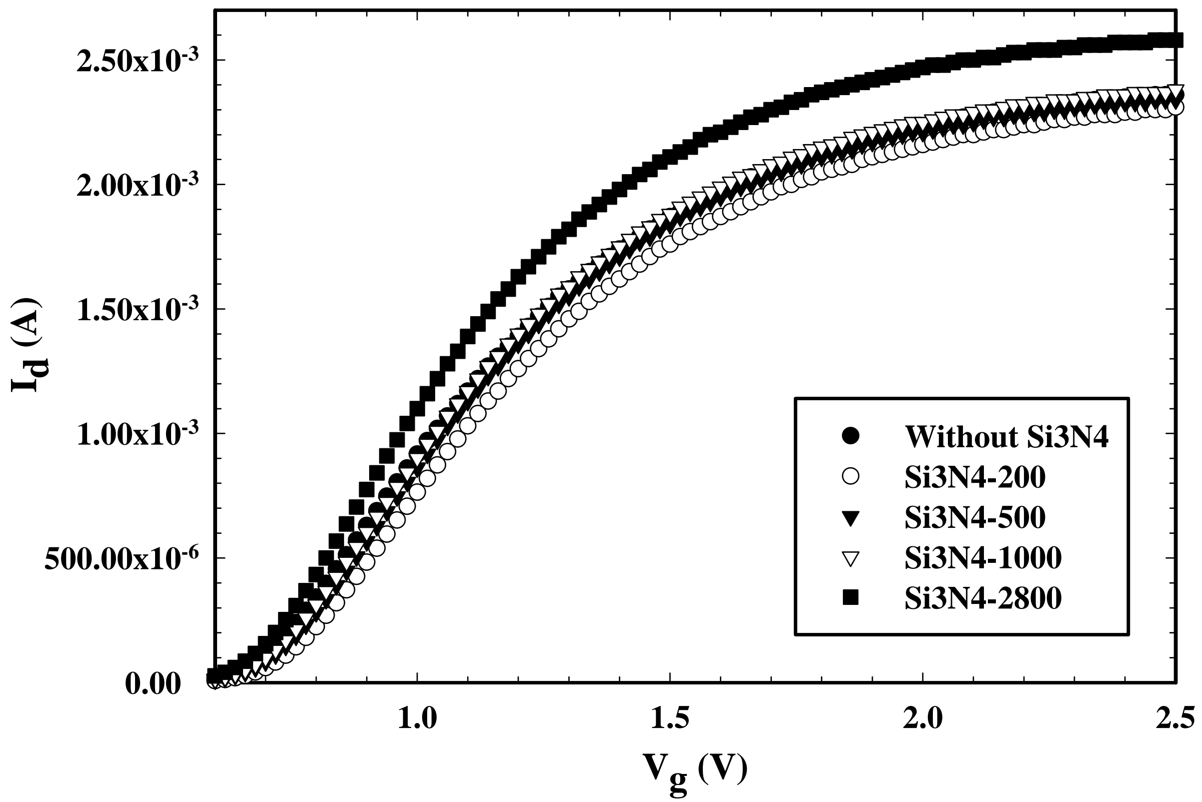


Fig. 3-1 I_d-V_g characteristics for different thickness of SiN-capping layer.

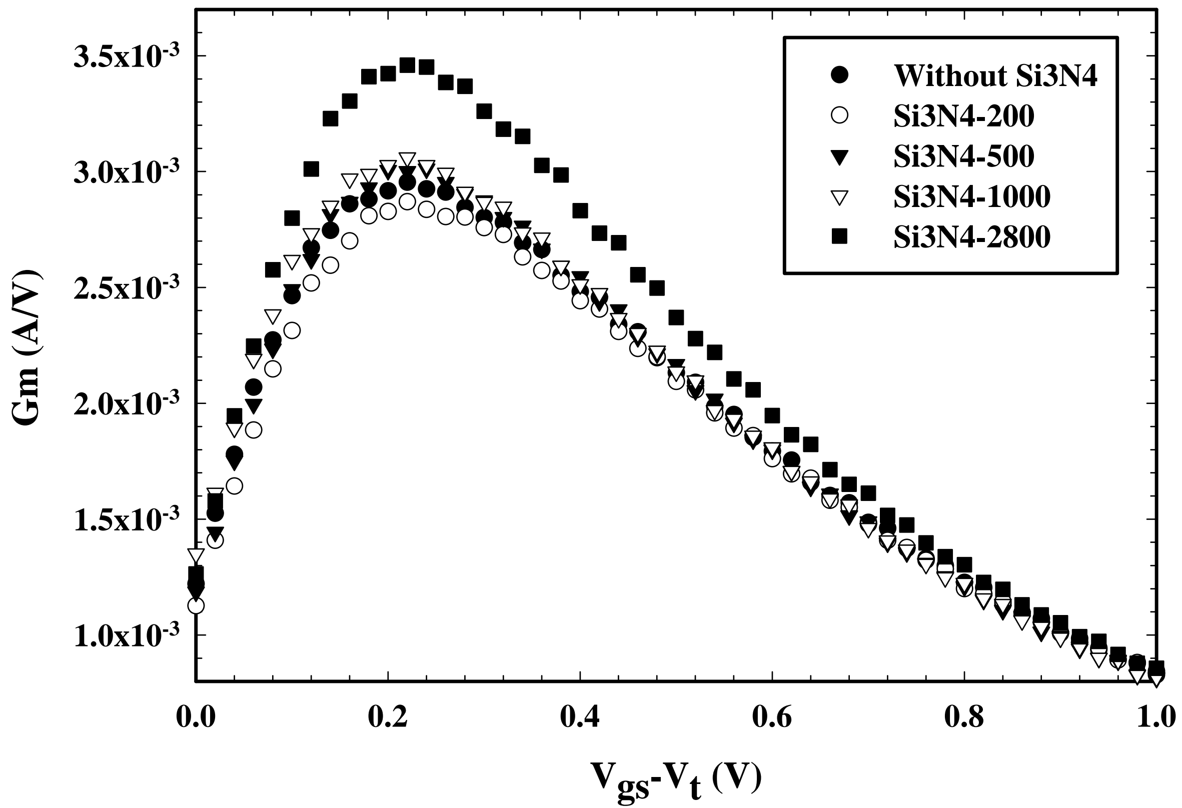


Fig. 3-2 Transconductance for different thickness of SiN-capping layer.

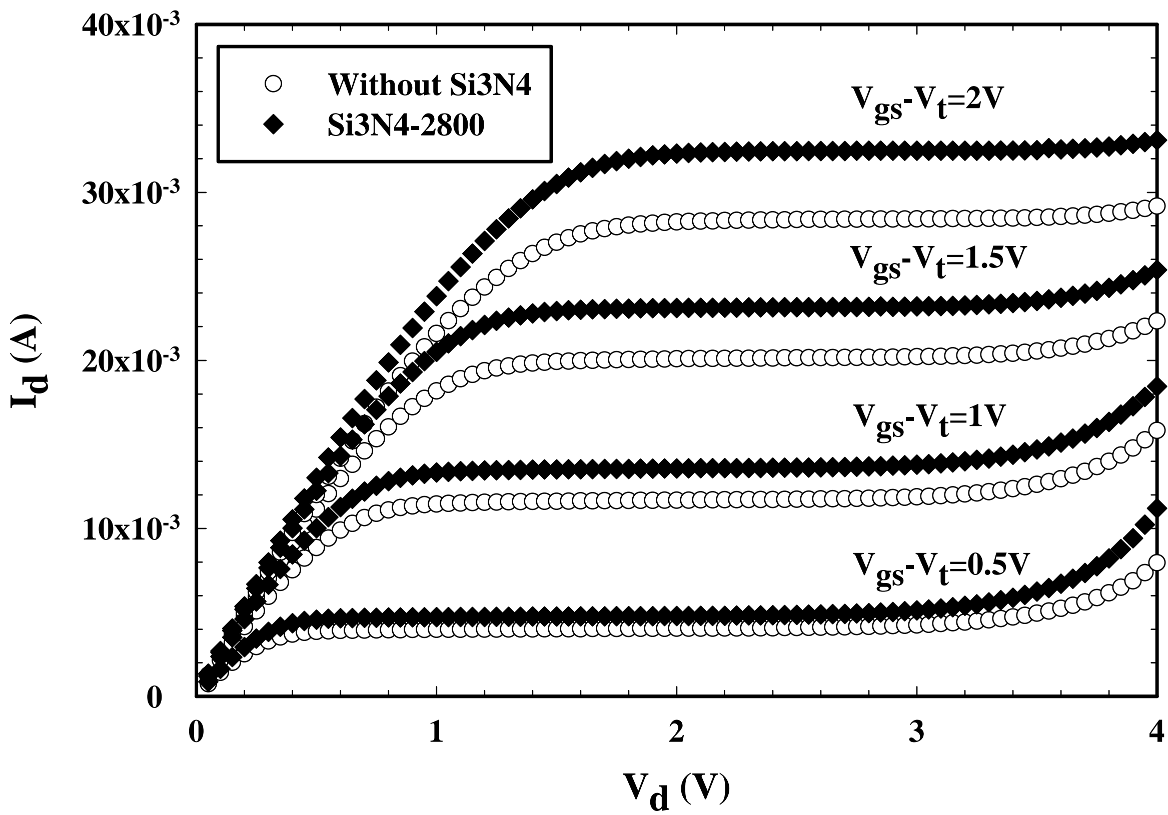


Fig. 3-3 Output characteristics for different thickness of SiN-capping layer.

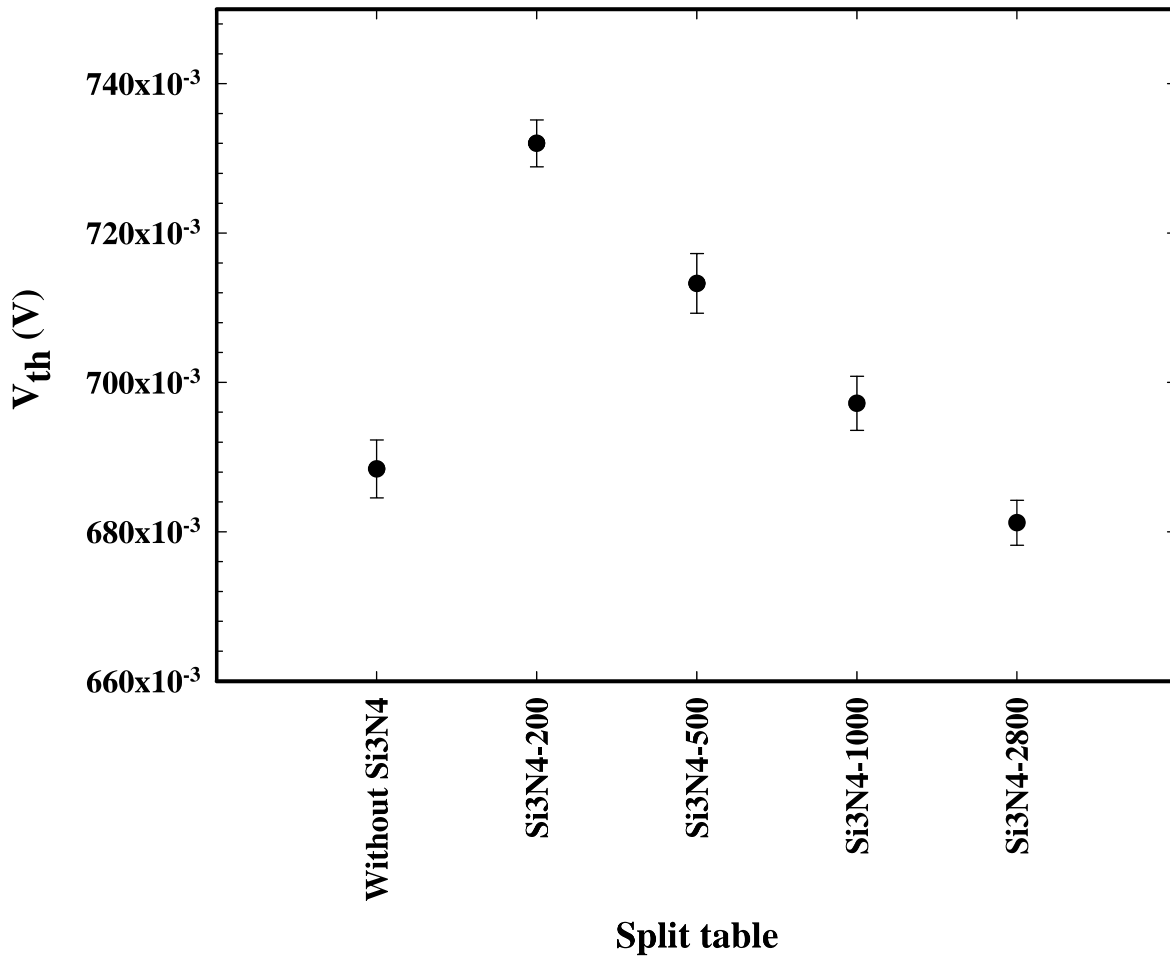


Fig. 3-4 Threshold voltage for different thickness of SiN-capping layer.

Poly-2000+Si3N4 split - C-V

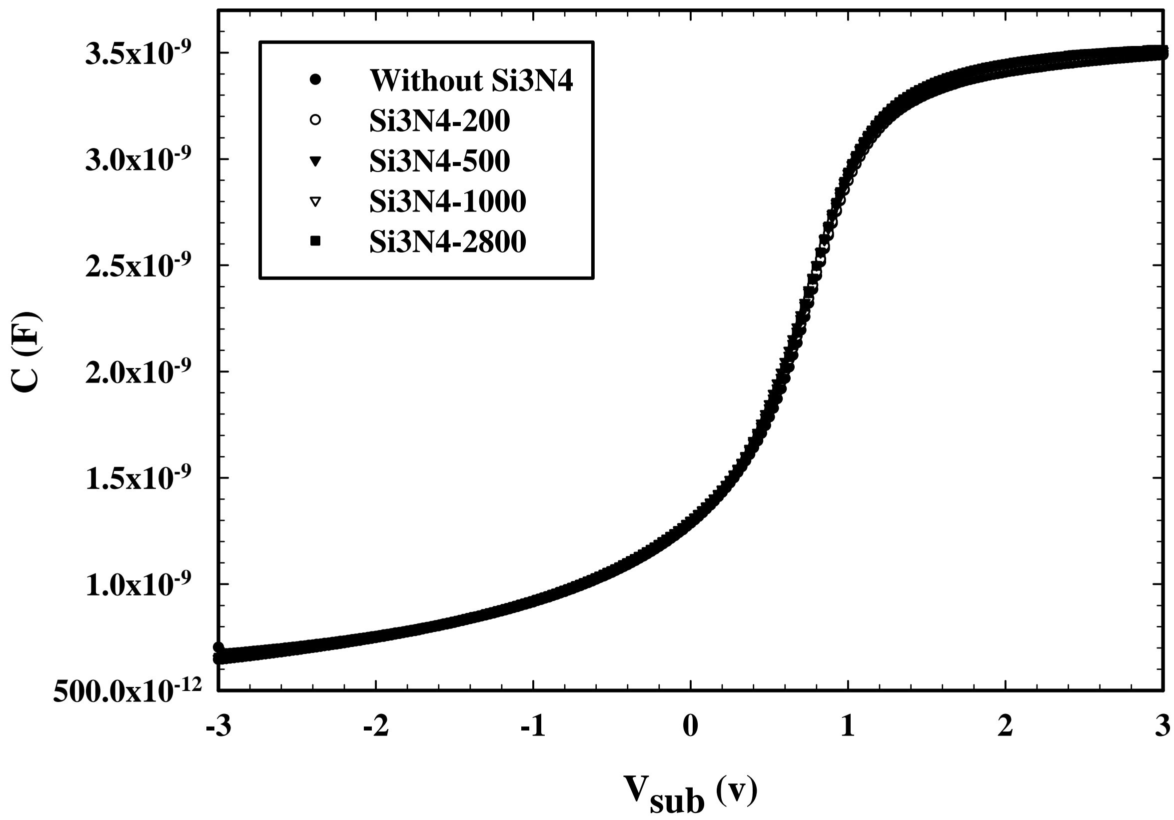


Fig. 3-5 Measured C-V profile for different thickness of SiN layer in 10 μm channel length devices.

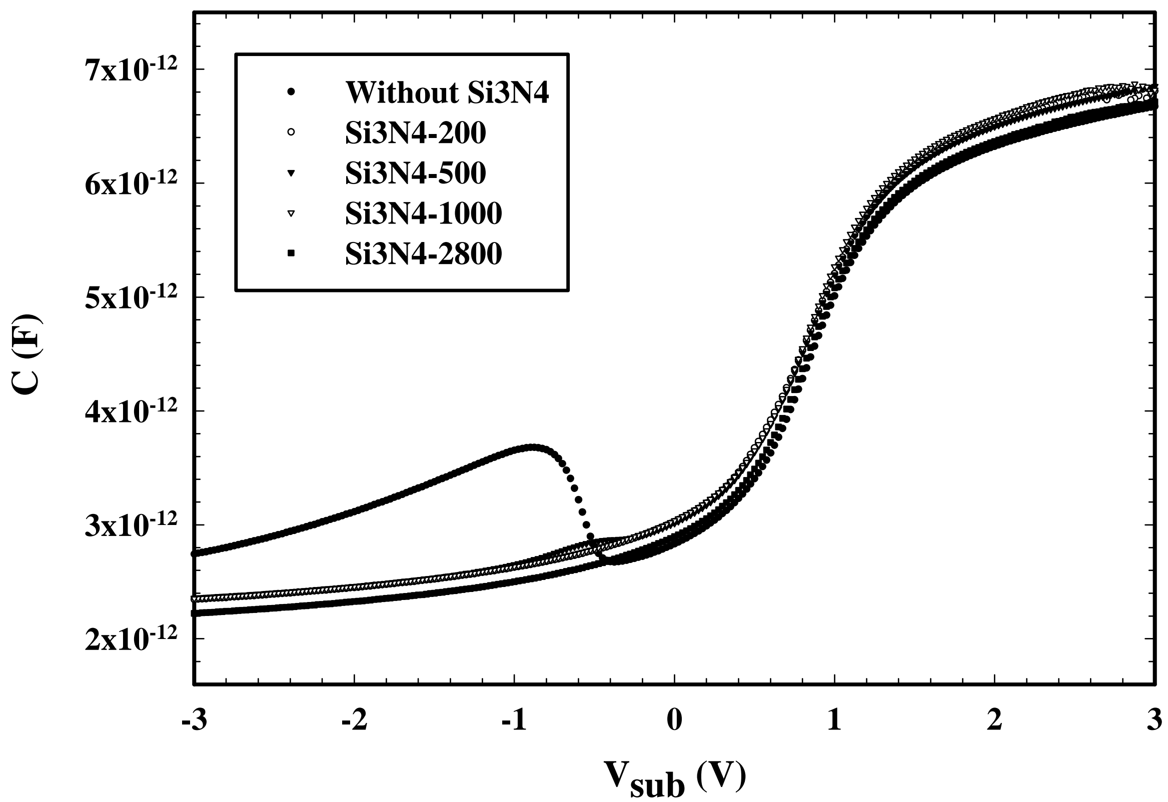


Fig. 3-6 Measured C-V profile for different thickness of SiN layer in 5 μm channel length devices.

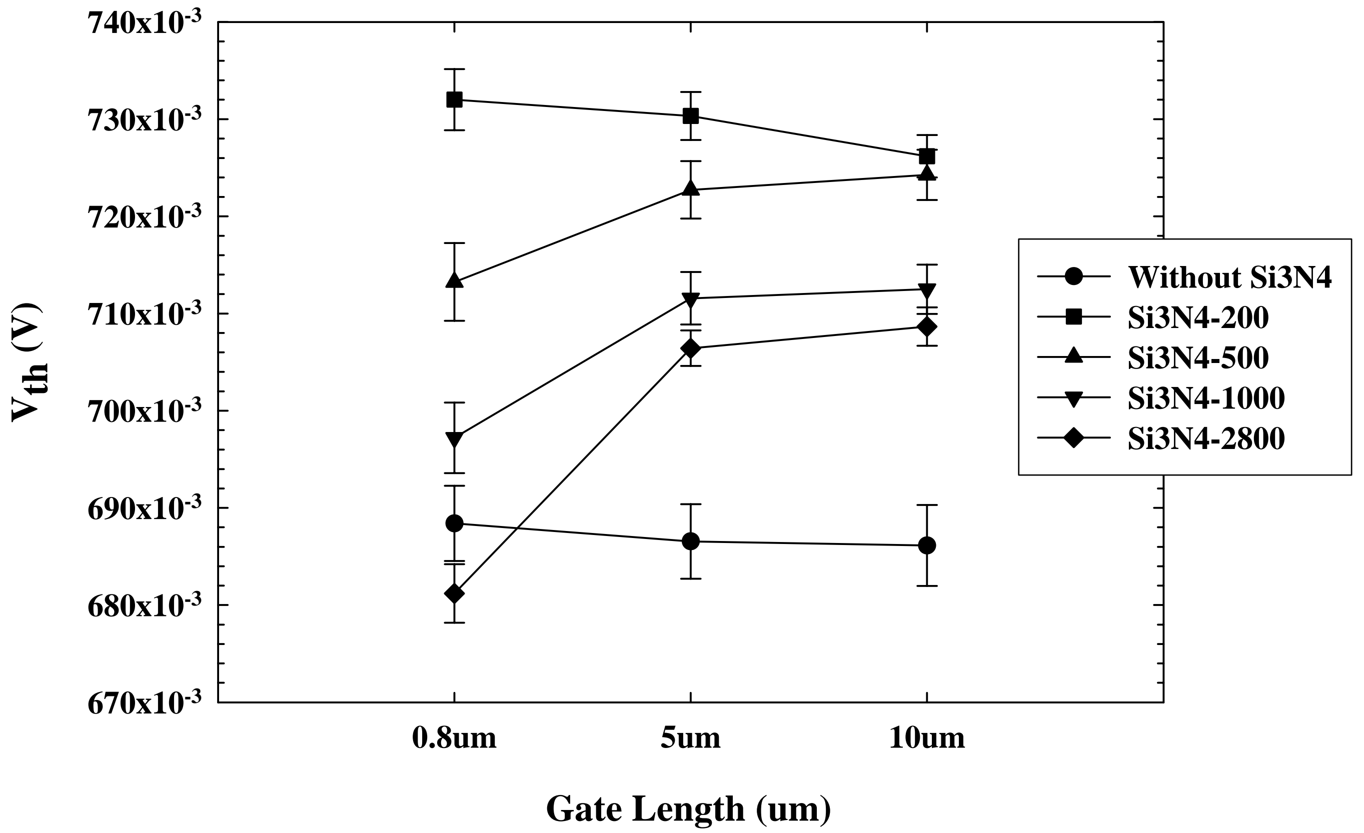


Fig. 3-7 V_{th} roll-off characteristics for different thickness of SiN layer.

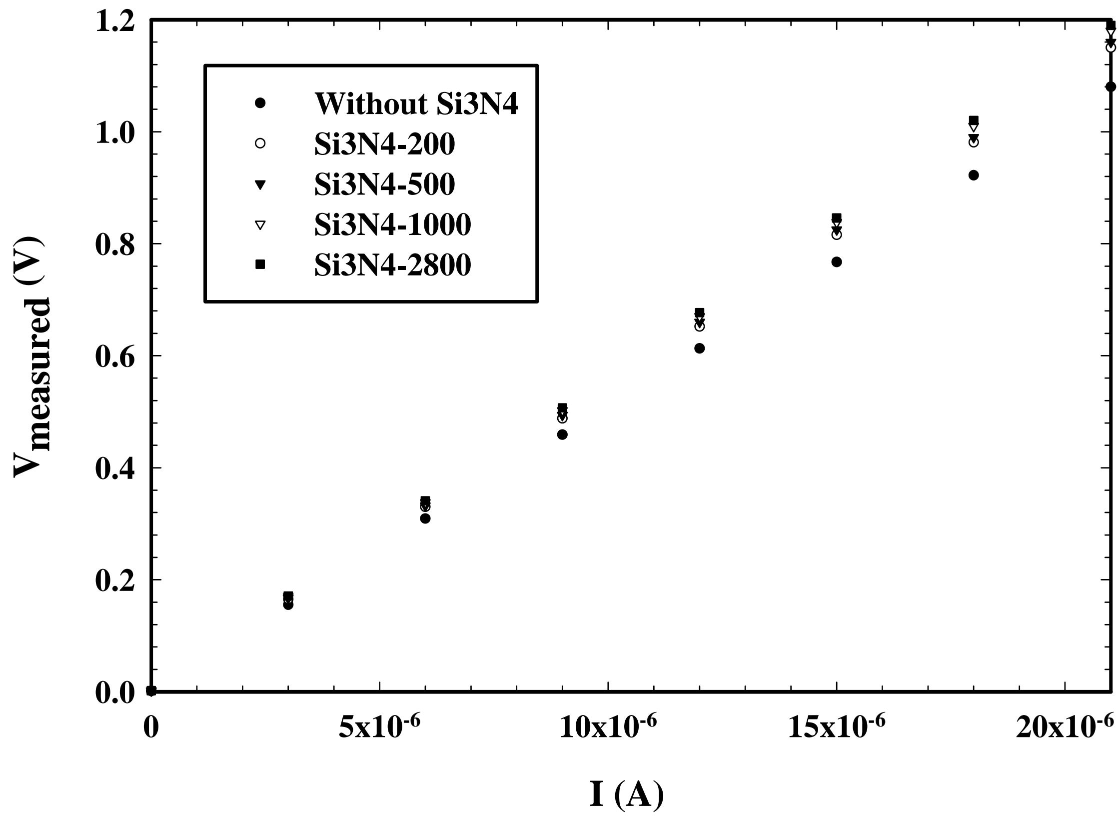


Fig. 3-8 Junction resistance for different thickness of SiN-capping layer.

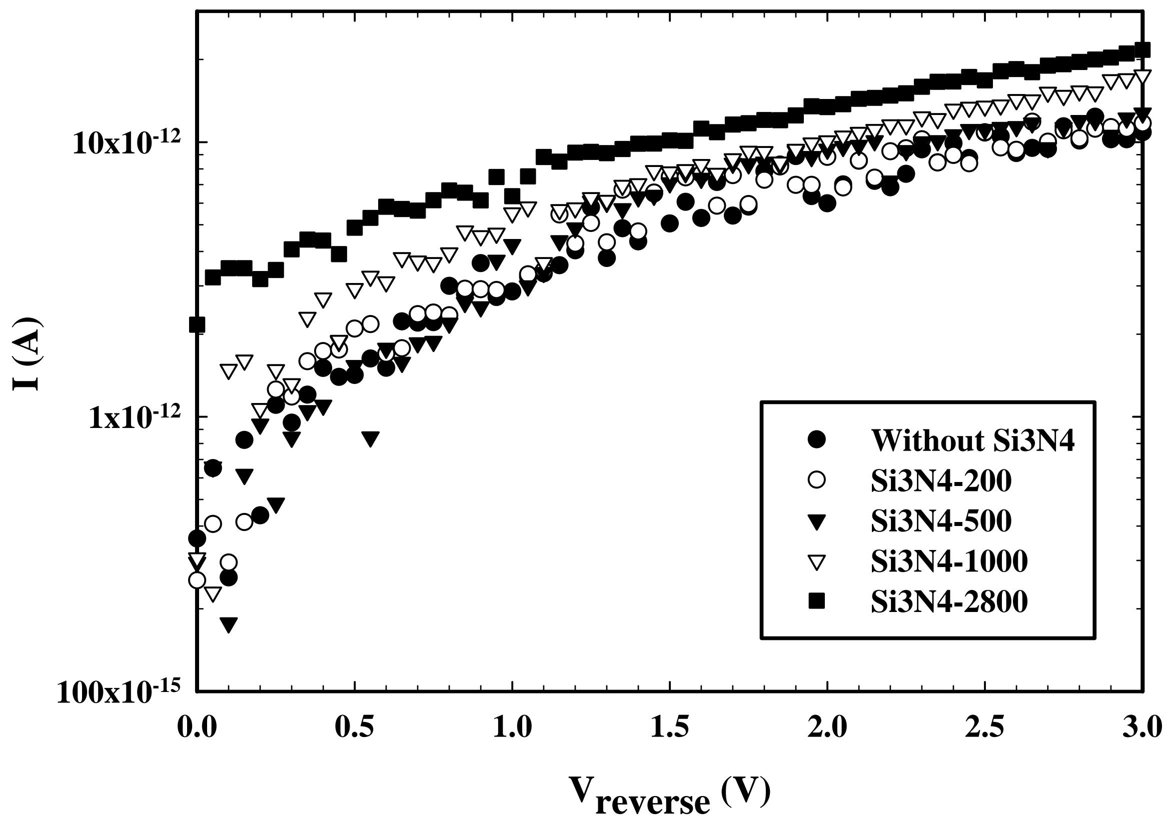


Fig. 3-9 Junction leakage current for different thickness of SiN capping layer.

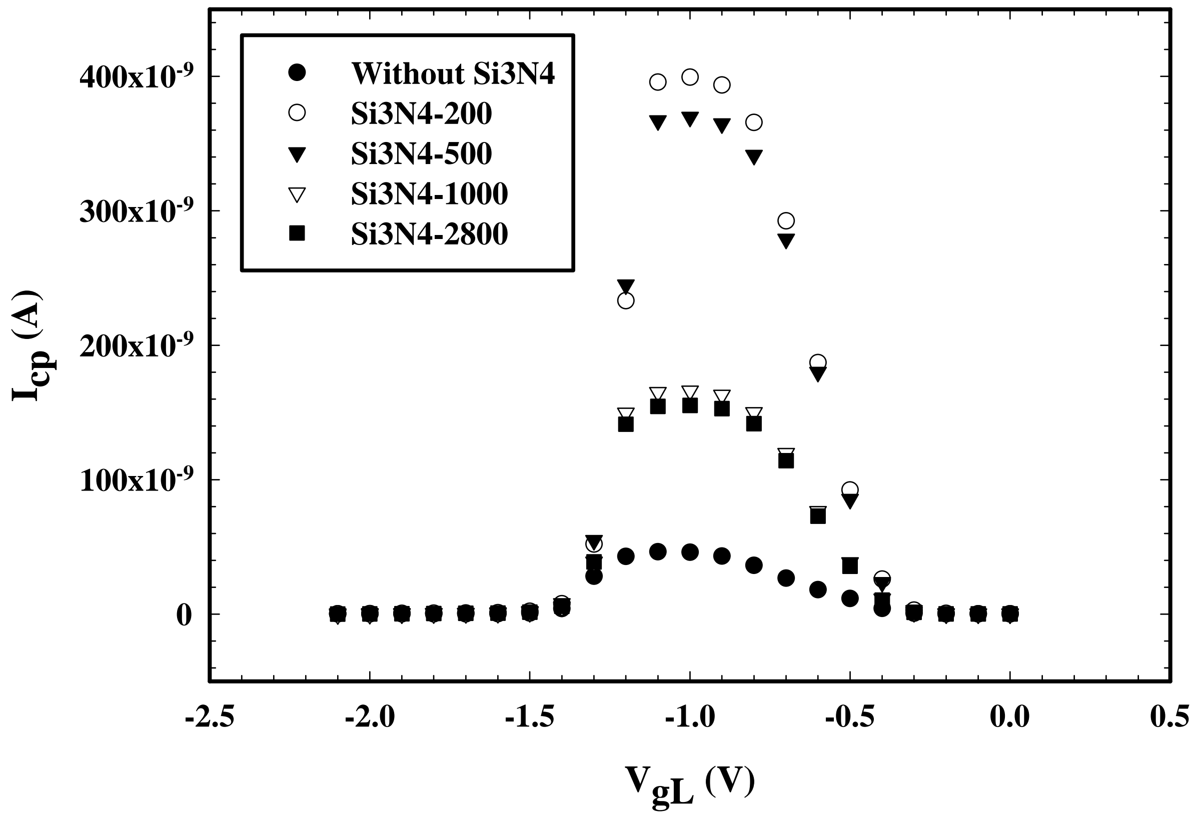


Fig. 3-10 Charge pumping current for different thickness of SiN layer (2MHZ).

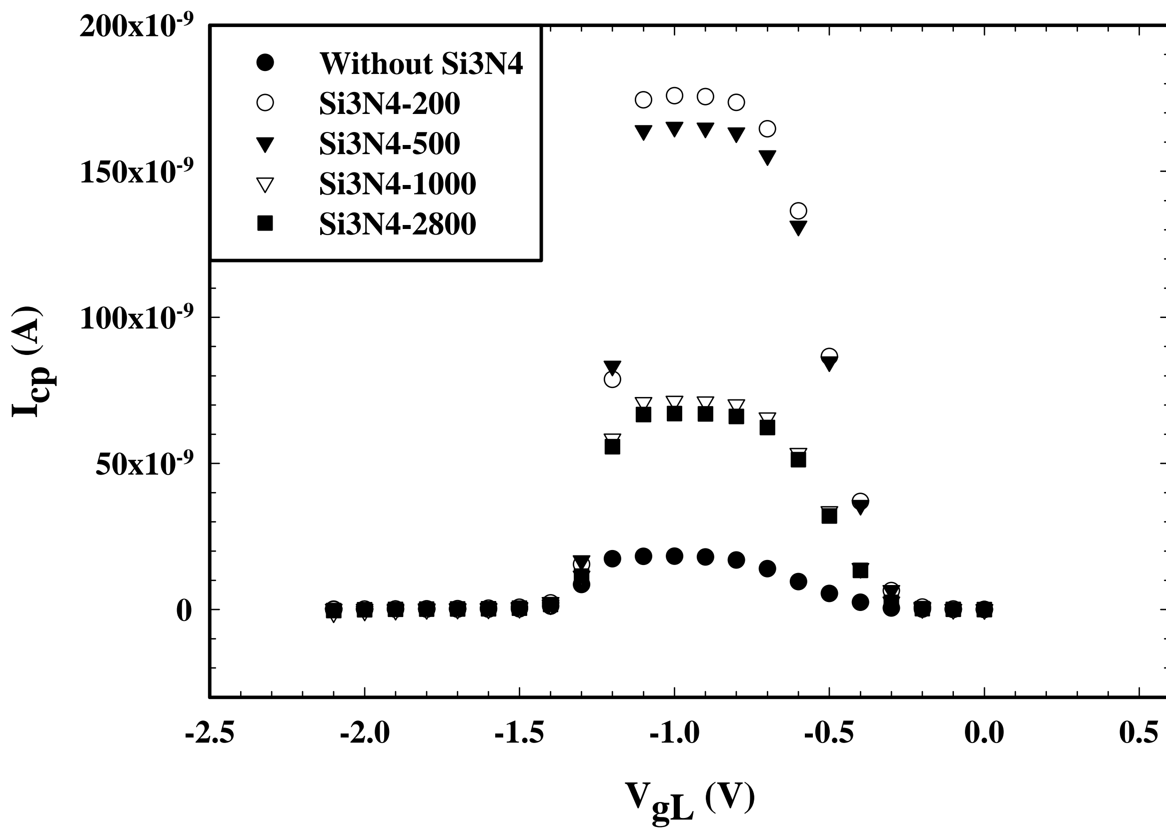


Fig. 3-11 Charge pumping current for different thickness of SiN layer (1MHZ).

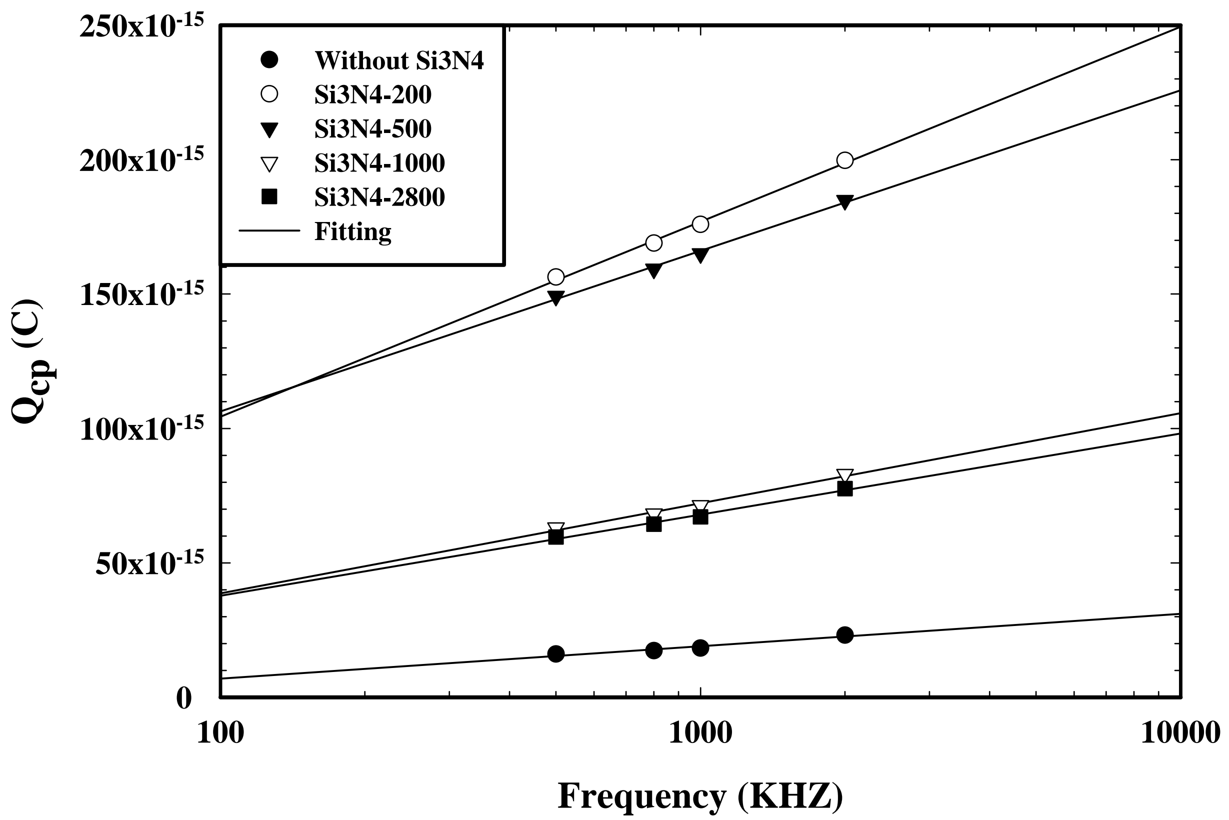


Fig. 3-12 Interface state density for different thickness of SiN-capping layer.

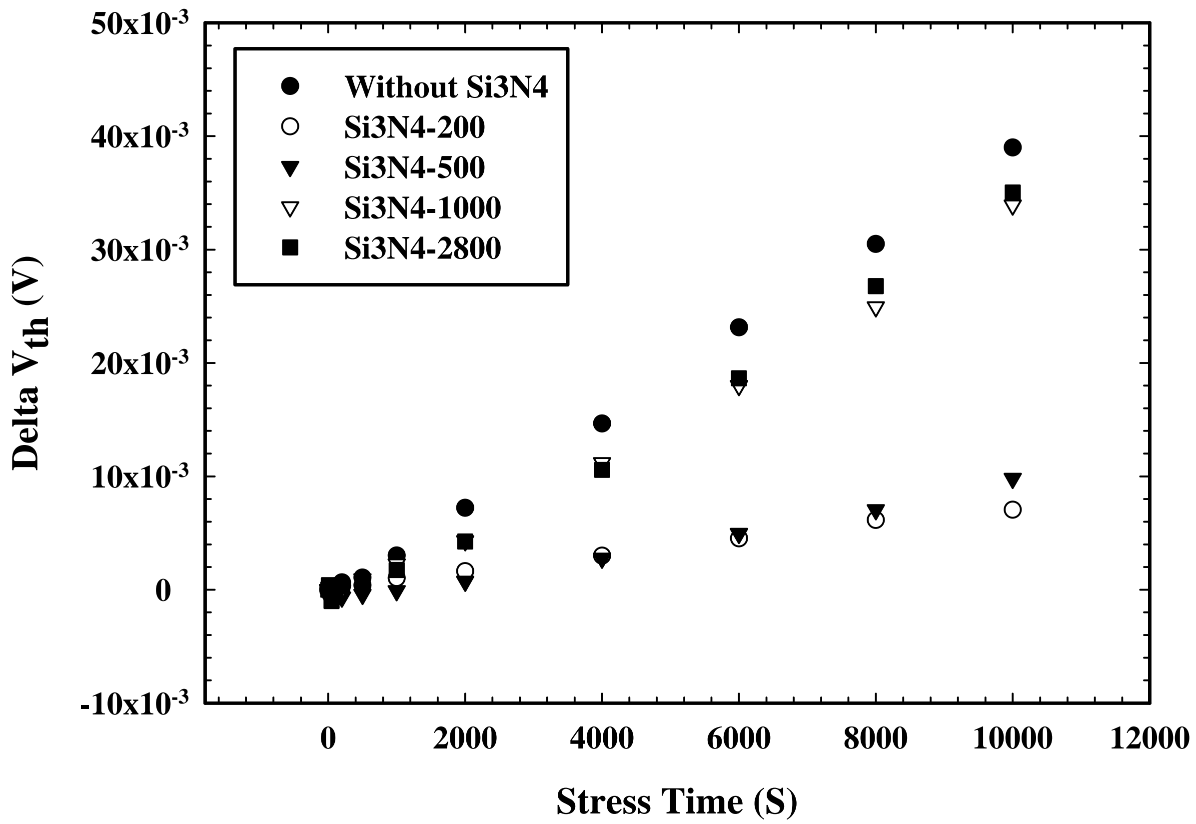


Fig. 3-13 Channel hot carrier characteristics for different SiN thickness.

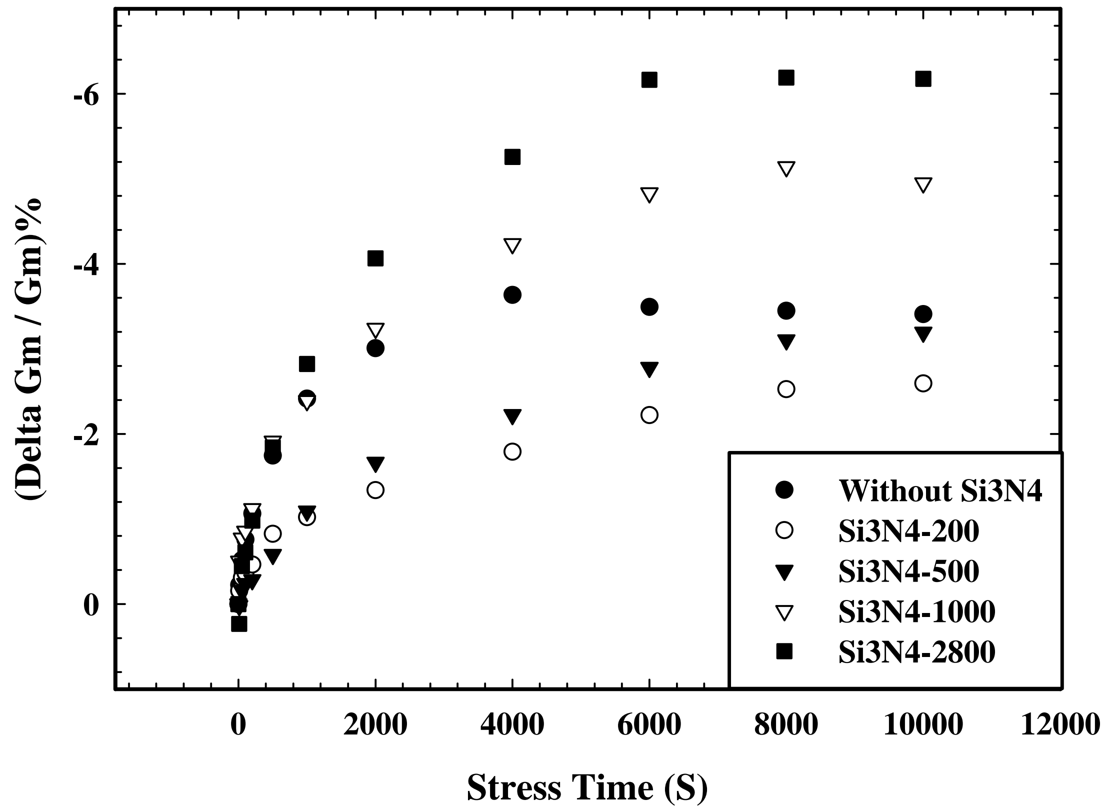
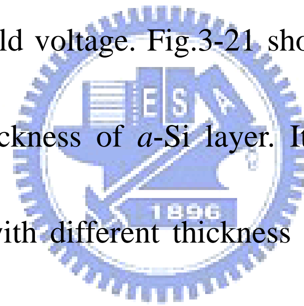


Fig. 3-14 Channel hot carrier characteristics for different SiN thickness.

3-2 Stack of *a*-Si and poly-Si gate with fixed thickness of SiN-capping layer

In this section, we would introduce the strain effect of the stack of *a*-Si and poly-Si gate structure. For comparison, all of the samples are capped a 500Å SiN layer. The dependence of I_d-V_g characteristics on different thickness of *a*-Si layer is shown in Fig. 3-15. The improvement of current drivability is in proportion to the thickness of *a*-Si layer. Fig. 3-16 shows the transconductance increases with the increase of thickness of *a*-Si layer. This result implies that the strain dependence of mobility enhancement by stack of *a*-Si gate structure is similar to the result of SiN-capping layer. The mechanism of the stress elevation could be as follows; before the dopant activation process, the n^+-poly gate is in amorphous phase due to the stack of *a*-Si and high dose implantation of arsenic. The re-crystallization of amorphous region during rapid thermal annealing leads to n^+-poly gate expansion and residual compressive stress. Therefore, the compressive stress in the n^+-poly gate provides high tensile strain to the channel region. The dependence of output characteristics on different thickness of *a*-Si layer is shown in Fig.3-17. The drain current of nMOSFETs with 700Å *a*-Si layer shows 19% increased compare to that of the poly-Si stack with 200Å *a*-Si layer. Fig. 3-18 shows the dependence of threshold voltage on different thickness of *a*-Si layer. The threshold voltage is proportional to the thickness of *a*-Si layer. This result is in the opposite direction to the result of SiN-capping layer. It is very

interesting since the improvement of current drivability increases as the thickness of *a*-Si layer is increased. This means that the strain effect causes the improvement of current drivability is larger than the effect of increases the threshold voltage. Fig. 3-19 ~ Fig. 3-21 illustrate the charge pumping measurement to define the quality of oxide / Si interface after the strain is introduced to channel region. The dependence of charge pumping current on different thickness of *a*-Si layer is shown in Fig. 3-19 and Fig. 3-20. The charge pumping current increases as the thickness of *a*-Si layer is increased. This result implies that the increase of charge pumping current is the cause of the observed elevation of threshold voltage. Fig.3-21 shows the dependence of interface state density on different thickness of *a*-Si layer. It shows that the interface state density is almost the same with different thickness of *a*-Si layer. It means that the stack of *a*-Si gate structure would not degrade the quality of oxide / Si interface. Fig. 3-22 shows the dependence of junction leakage current on different thickness of *a*-Si layer. No significant difference was found when we increase of thickness of *a*-Si layer. The dependence of channel hot carrier effect on different thickness of *a*-Si layer is shown in Fig. 3-23 and Fig. 3-24 (Stress Condition: 3.75V, for 10000sec). It is similar to the result of SiN-capping layer. The deviation of threshold voltage and the degradation of transconductance are getting serious as the increase of thickness of *a*-Si layer. What will be happened while we use SiN-capping layer and stack gate



poly-Si on device fabrication at the same time? We found that the strain dependence of mobility enhancement will become significant by using both SiN-capping layer and stack of *a*-Si gate structures. The detail results will be demonstrated in the next section.

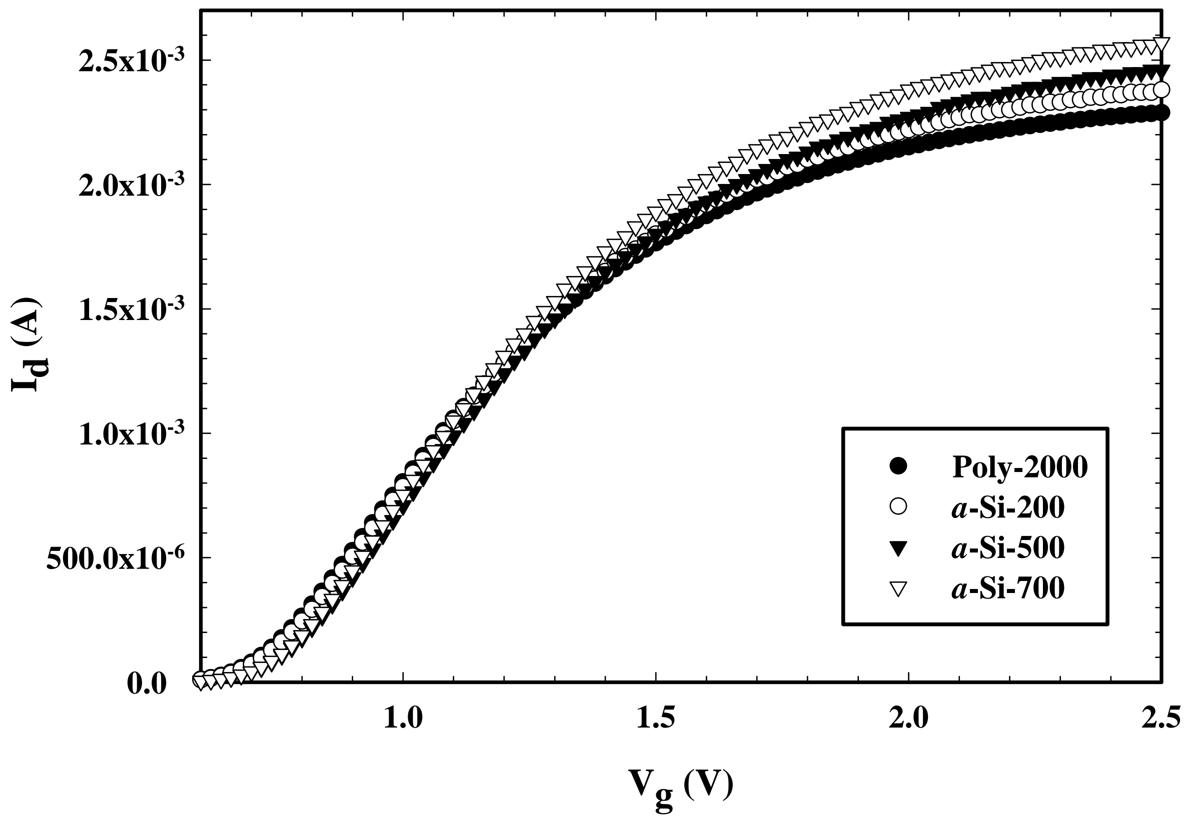


Fig. 3-15 I_d-V_g characteristics for different thickness of *a*-Si layer.

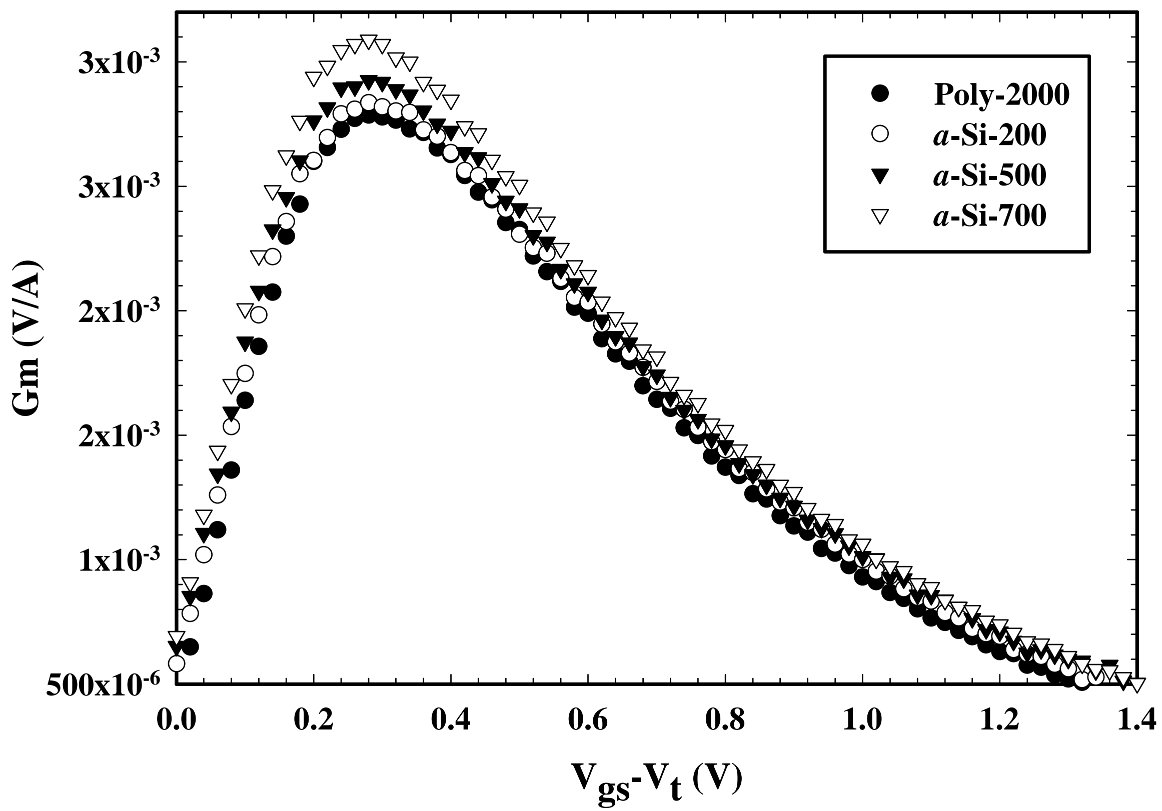


Fig. 3-16 Transconductance for different thickness of *a*-Si layer.

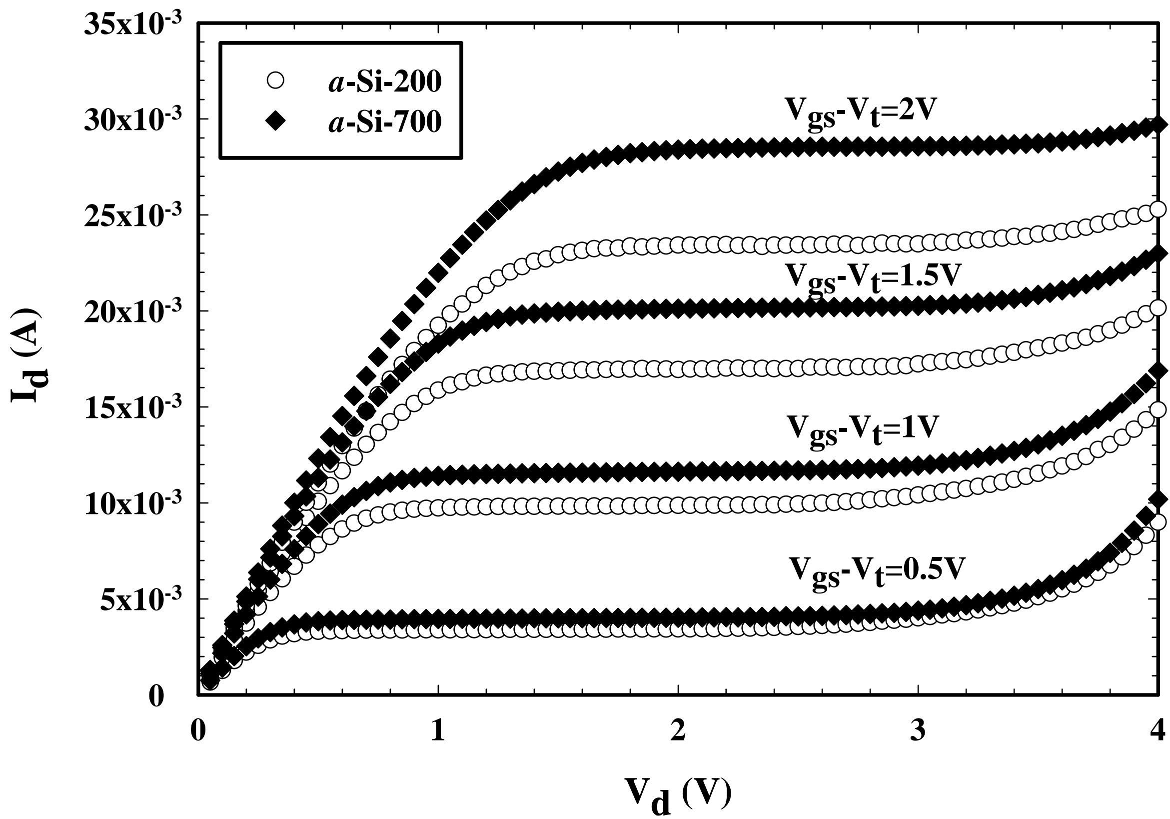


Fig. 3-17 I_d-V_d characteristics for different thickness of *a*-Si layer.

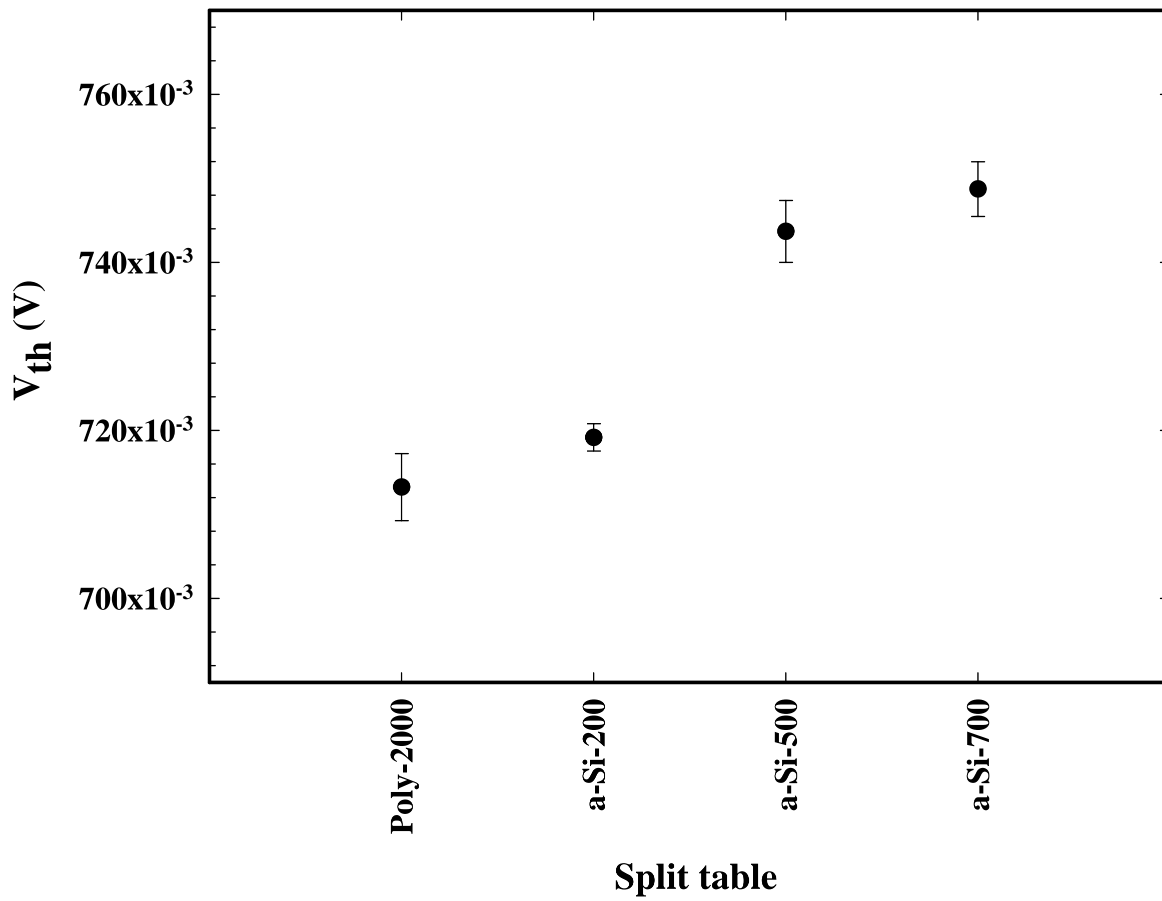


Fig. 3-18 Threshold voltage for different thickness of *a*-Si layer.

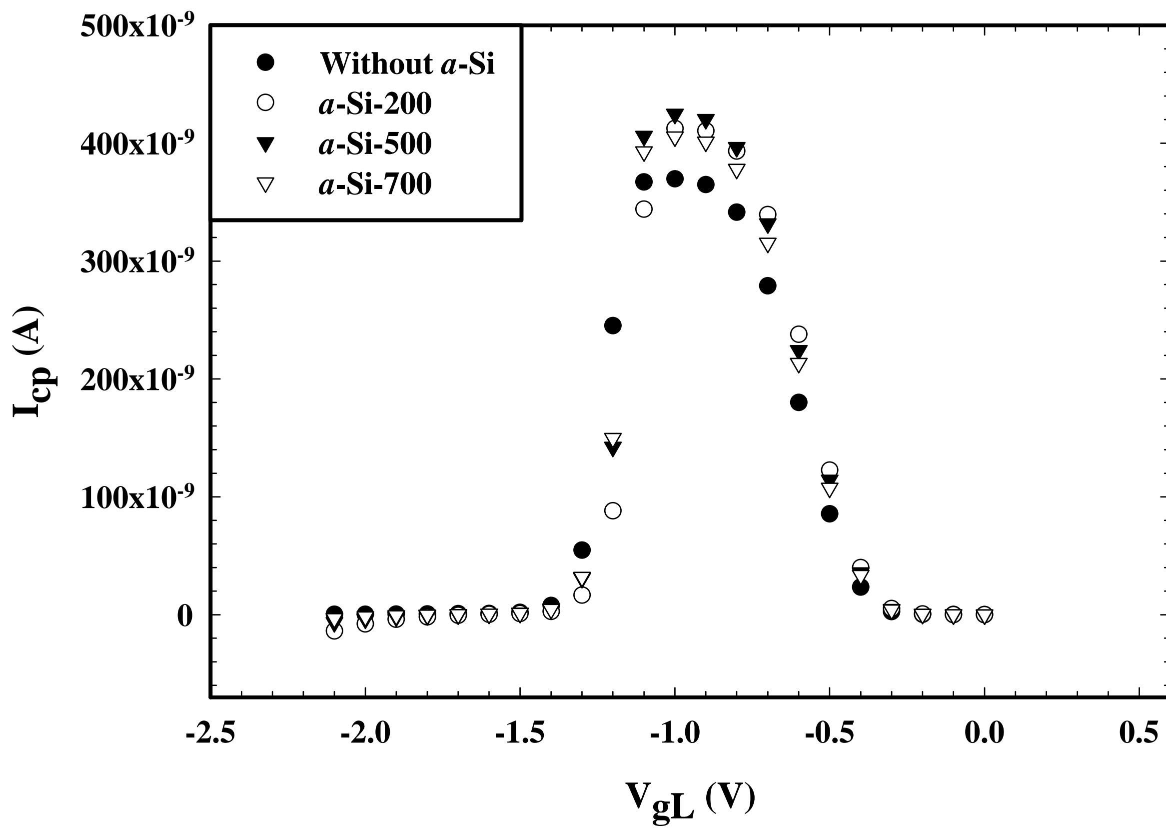


Fig. 3-19 Charge pumping current for different thickness of *a*-Si layer (2MHZ).

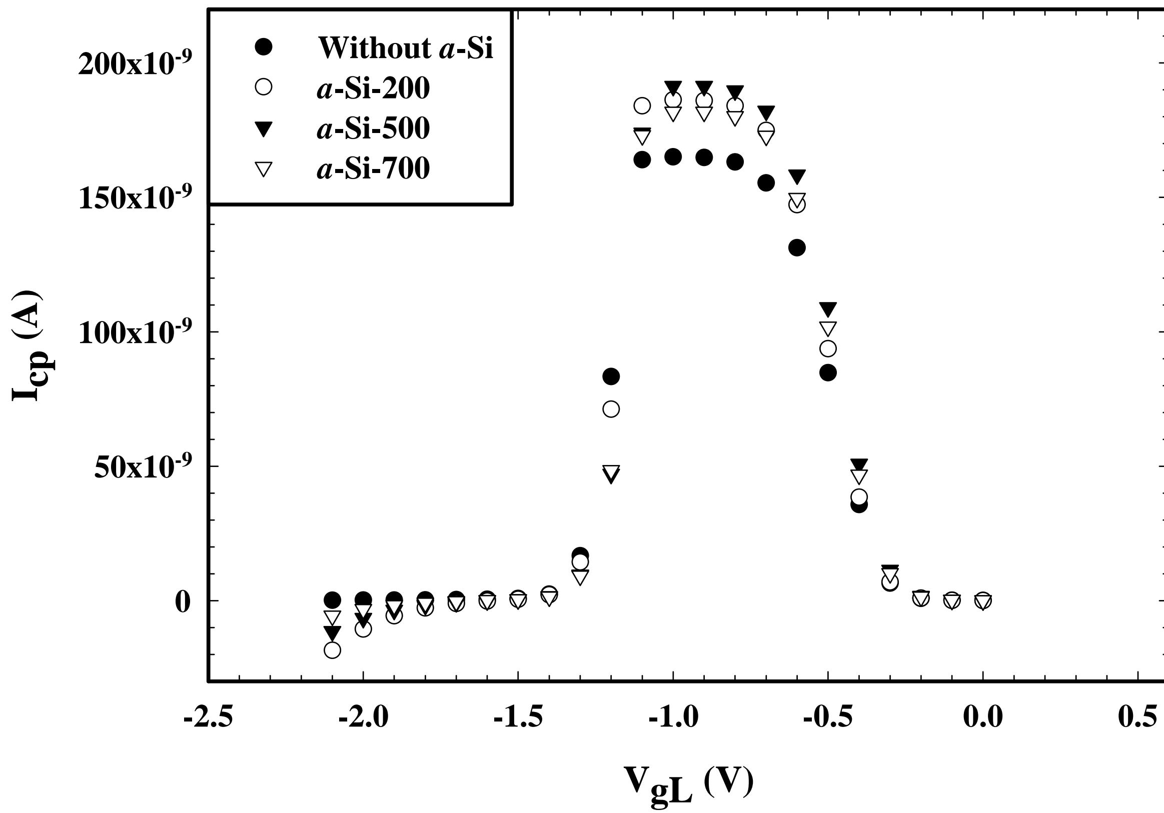


Fig. 3-20 Charge pumping current for different thickness of *a*-Si layer (1MHZ).

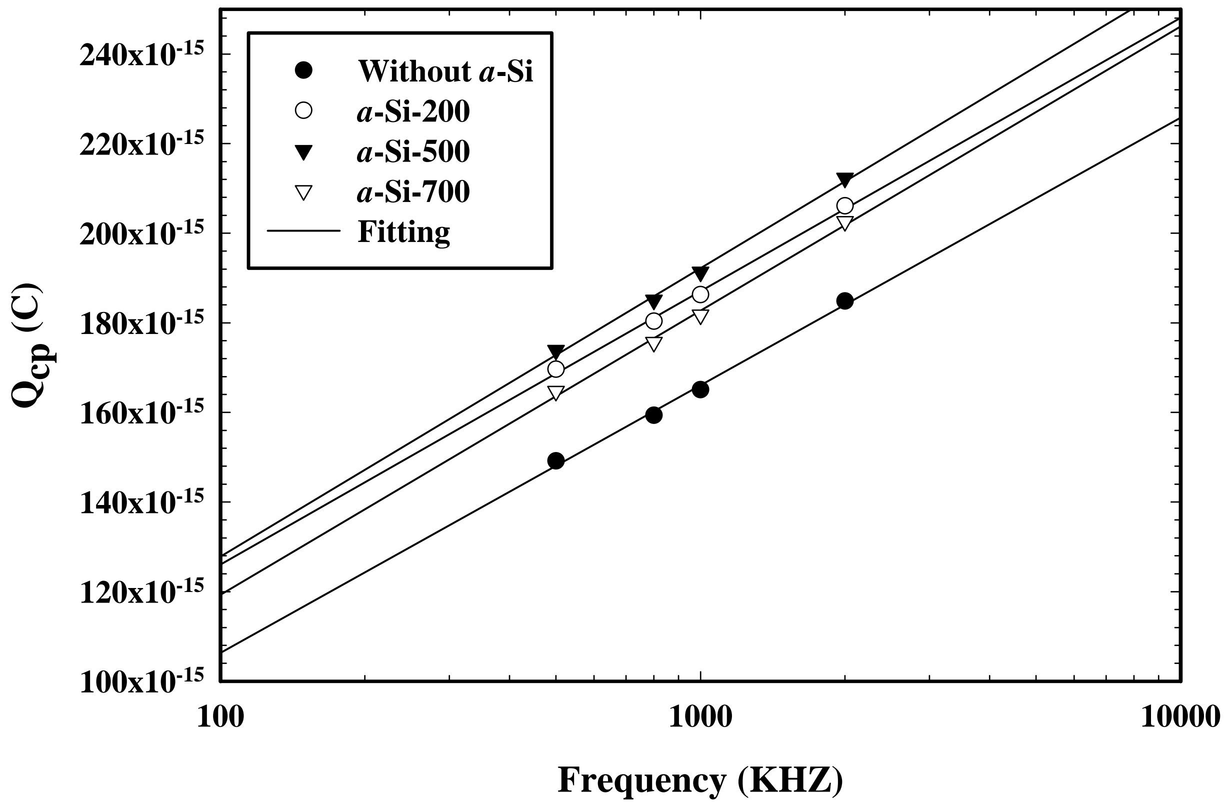


Fig. 3-21 Interface state density for different thickness of *a*-Si layer.

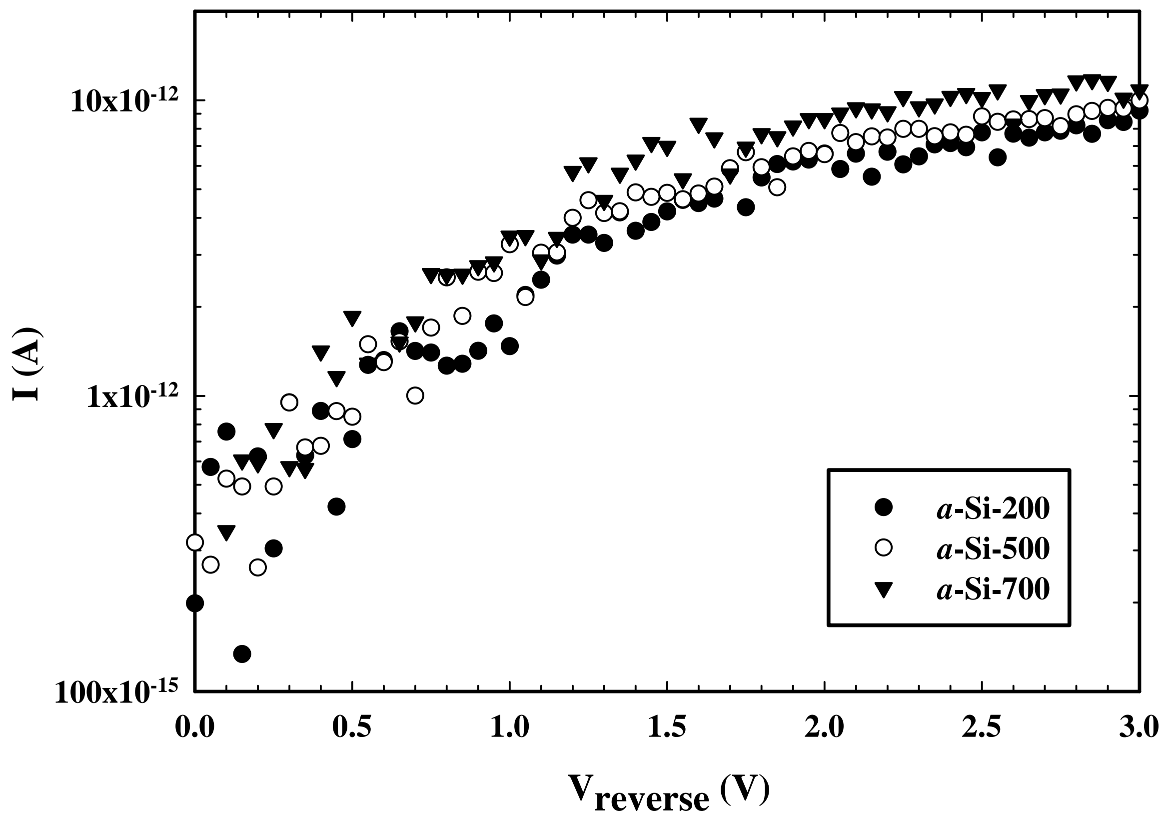


Fig. 3-22 Junction leakage current for different thickness of *a*-Si layer.

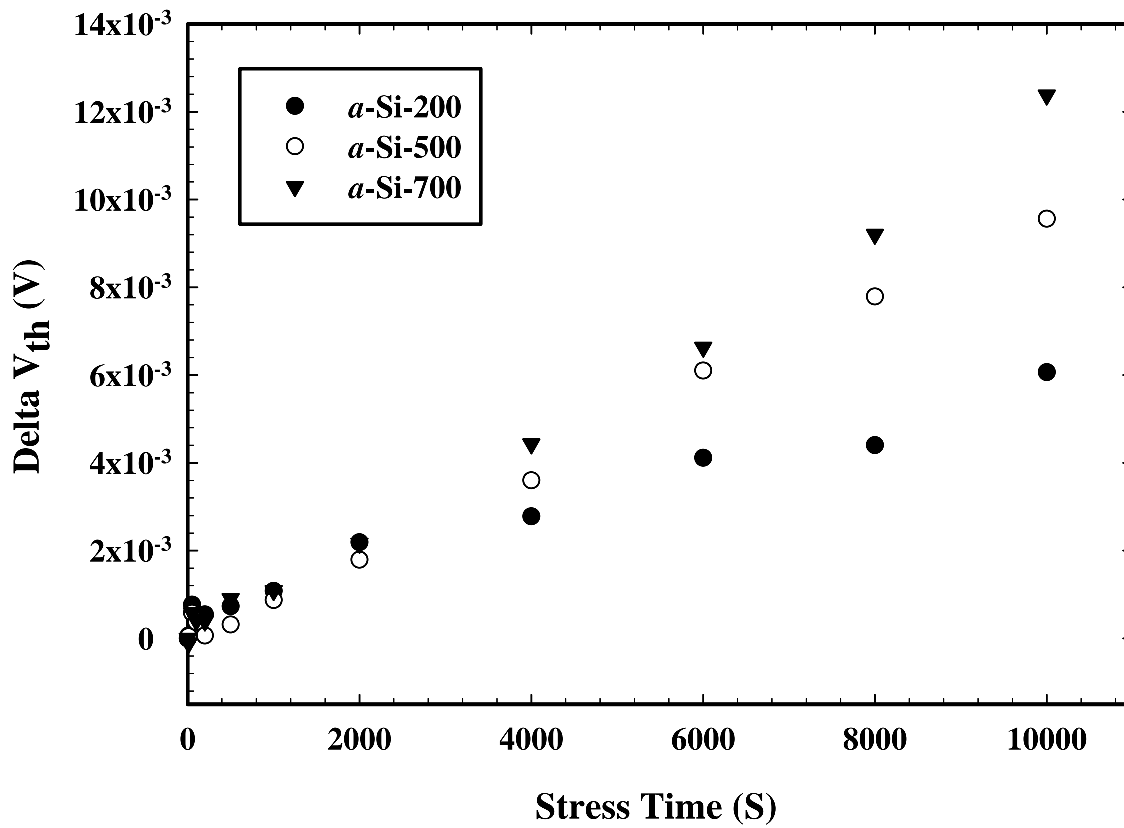


Fig. 3-23 Channel hot carrier characteristics for different thickness of *a*-Si layer.

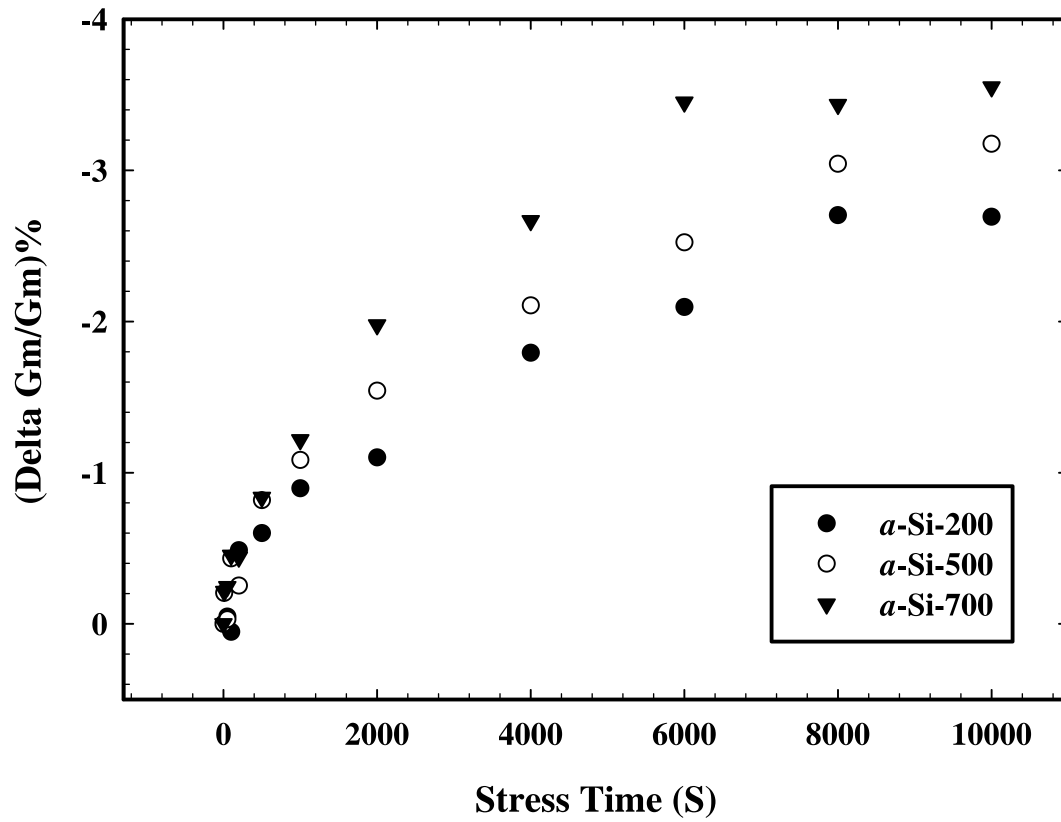
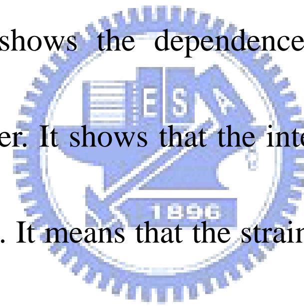


Fig. 3-24 Channel hot carrier characteristics for different thickness of *a*-Si layer.

3-3 Stack of 500Å *a*-Si gate structure with different thickness of SiN layer

Now, we would describe the strain effect by using both SiN-capping layer and stack of *a*-Si gate structures. All of the samples are been with stack of 500Å *a*-Si layer in this stage. The dependence of I_d-V_g characteristics on different thickness of SiN layer is shown in Fig. 3-25. The drain current increases with the increase of thickness of SiN layer. The pronounced improvement of transconductance on different thickness of SiN layer is shown in Fig. 3-26. We found that the strain dependence of mobility enhancement will become significant by using both SiN-capping layer and stack of *a*-Si gate structures. Fig. 3-27 shows the dependence of output characteristics on different thickness of SiN layer. The improvement of current drivability by using both SiN-capping layer and stack of *a*-Si gate structure is more conspicuous. We believe that the tensile strain in the channel region by using both SiN-capping layer and stack gate poly-Si is larger than only use either of them. The mechanism of the stress elevation could be as follows: before the dopant activation process, the n^+-poly gate is in amorphous phase due to the stack of *a*-Si and high dose implantation of arsenic. The re-crystallization of amorphous region during rapid thermal annealing leads to n^+-poly gate expansion and residual compressive stress. Furthermore, thermal CVD SiN-capping layer with highly tensile stress enhances compressive strain in the n^+-poly gate. Therefore, the highly compressive stress in the n^+-poly gate provides

highly tensile strain to the channel region. The threshold voltage decreases as the thickness of SiN layer is increased (Fig. 3-28). It is similar to the result of only capped SiN layer in section 3-1. Fig. 3-29 ~ Fig. 3-31 illustrate the charge pumping measurement to define the quality of oxide / Si interface after the strain is introduced to channel region. The dependence of charge pumping current on different thickness of SiN layer is shown in Fig. 3-29 and Fig. 3-30. The charge pumping current decreases with the increase of thickness of SiN layer. This result implies that the decrease of charge pumping current is the cause of the observed reduction of threshold voltage. Fig.3-31 shows the dependence of interface state density on different thickness of SiN layer. It shows that the interface state density decreases as the SiN thickness is increased. It means that the strain elevation in the channel region is prone to improve the quality of oxide / Si interface even though still inferior quality than conventional devices. The dependence of junction leakage current on different thickness of SiN layer is shown in Fig. 3-32. The leakage current increases with the increase of stress in the junction area. However, it is not serious and results in little difference with the increase of SiN thickness. The dependence of channel hot carrier effect on different thickness of SiN layer is shown in Fig. 3-33 and Fig. 34 (Stress Condition: 3.75V, for 10000sec). The deviation of threshold voltage and the degradation of transconductance are getting serious as the increase of SiN thickness.



Therefore, the improvement of oxide / Si interface quality is an important issue while we use either SiN-capping layer or stack of *a*-Si gate structures to enhance carrier mobility on device fabrication. How to improve the device reliability while we introduce strain to the channel region is what we suppose to do in the future.

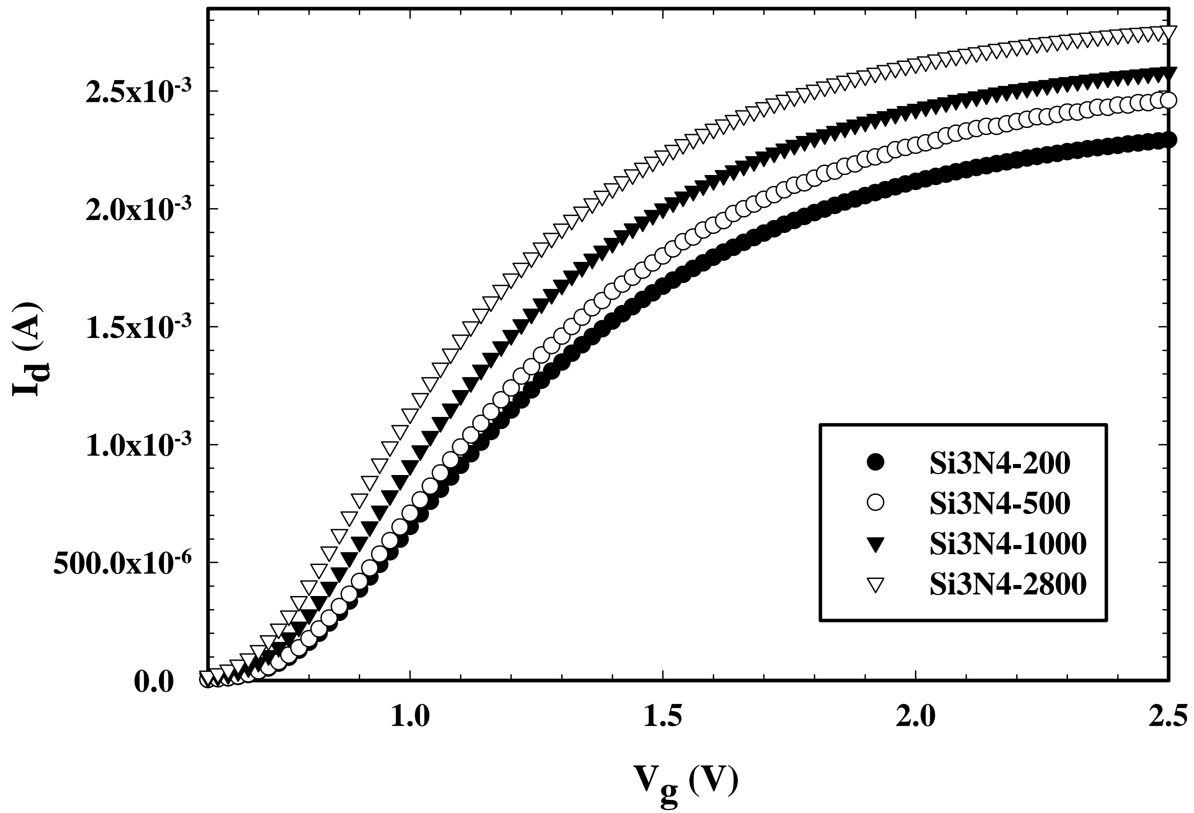


Fig. 3-25 I_d-V_g characteristics for different thickness of SiN capping layer.

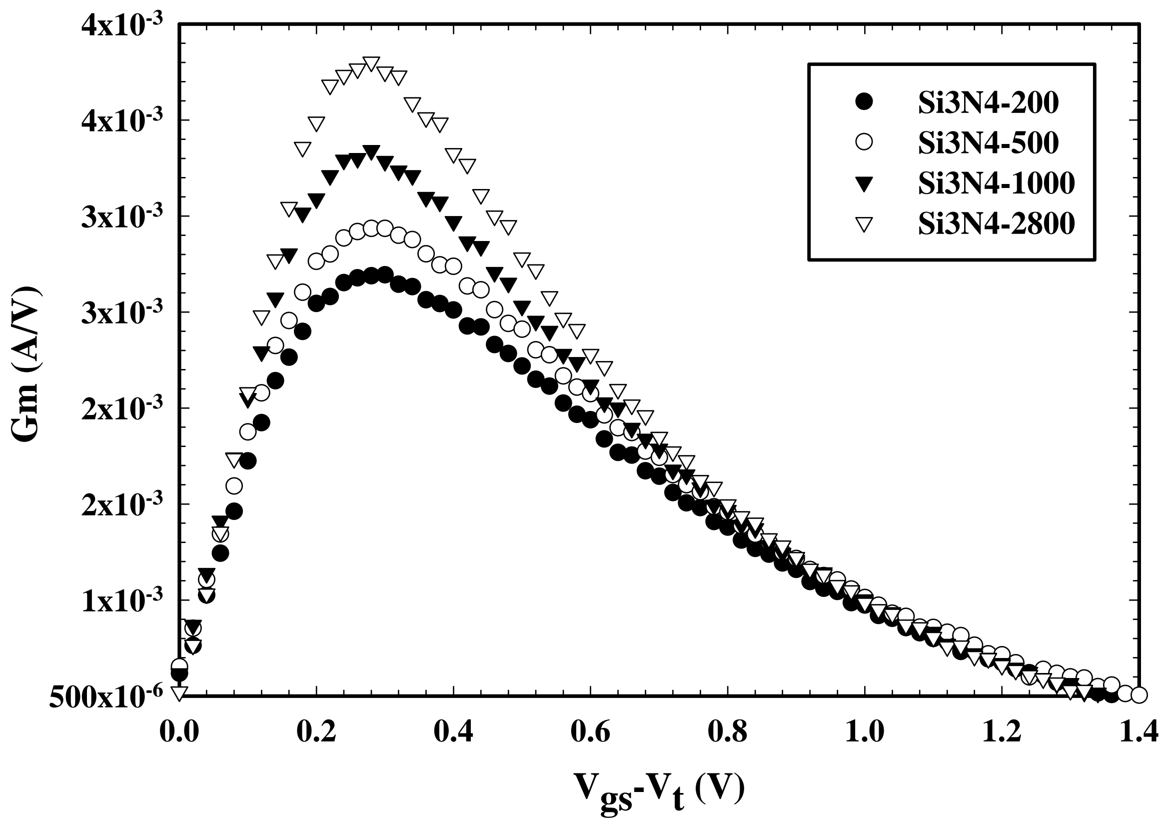


Fig. 3-26 Transconductance for different thickness of SiN capping layer.

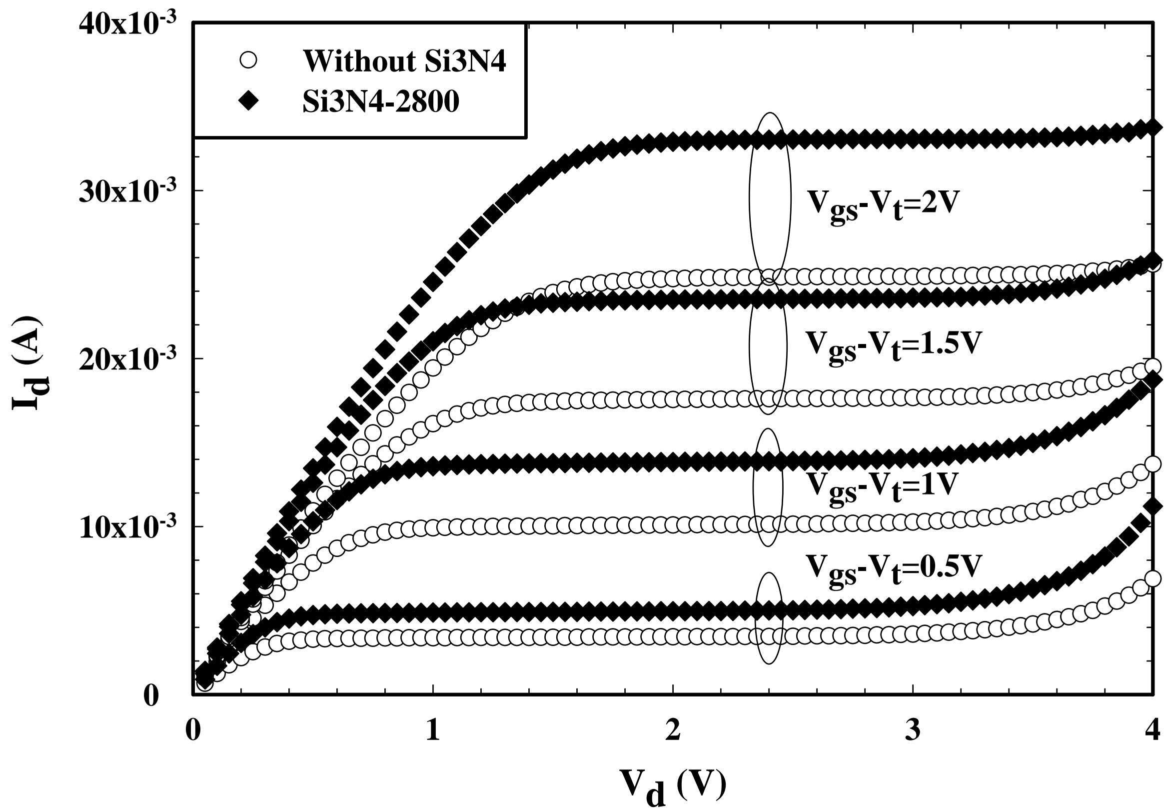


Fig. 3-27 Output characteristics for different thickness of SiN capping layer.

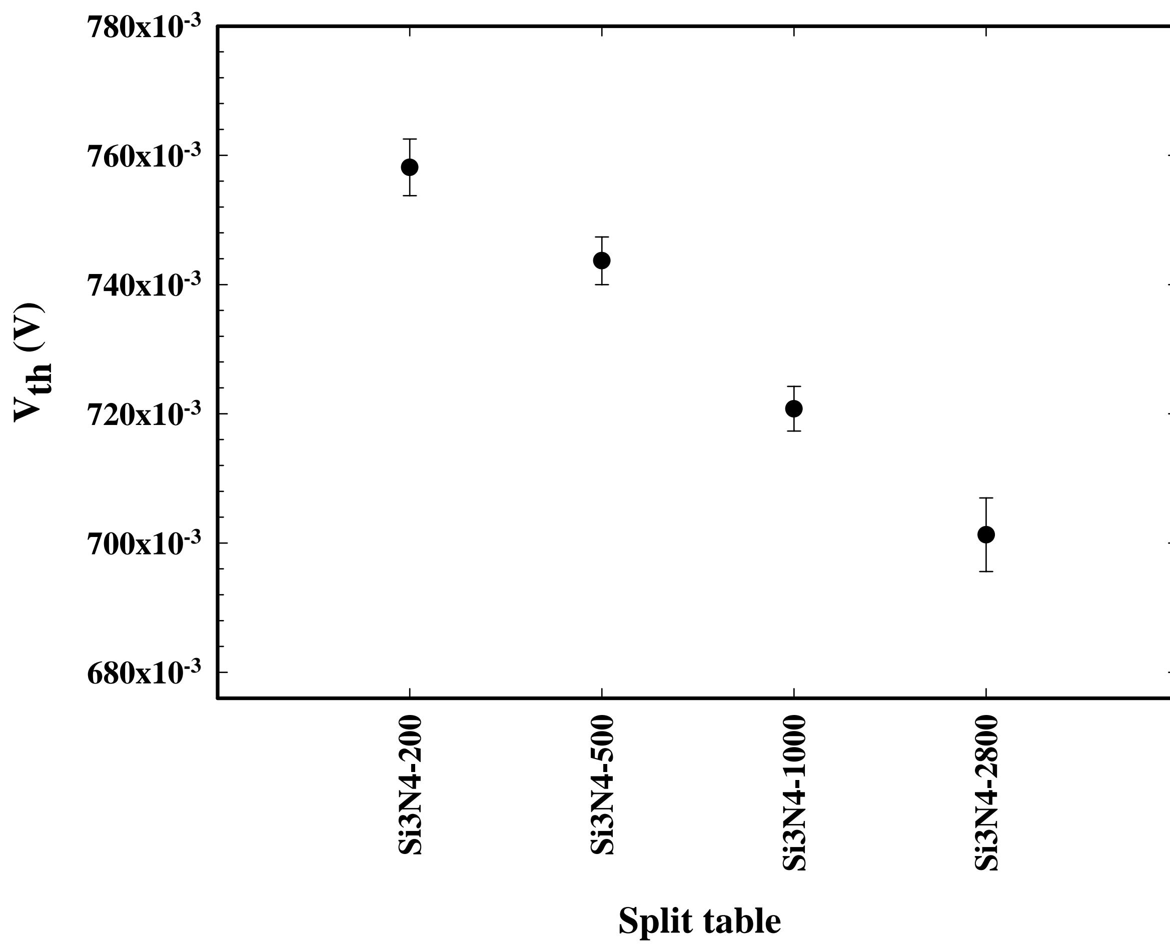


Fig. 3-28 Threshold voltage for different thickness of SiN capping layer.

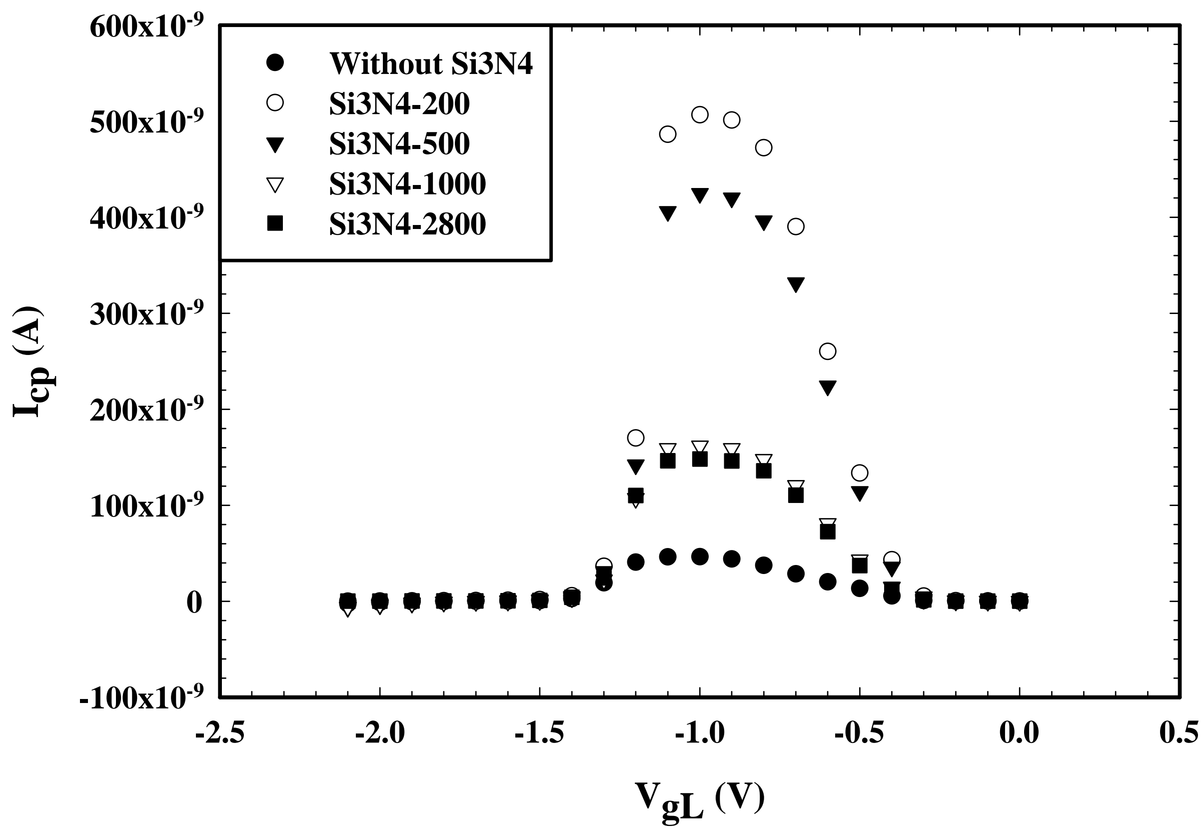


Fig. 3-29 Charge pumping current for different thickness of SiN layer (2MHZ).

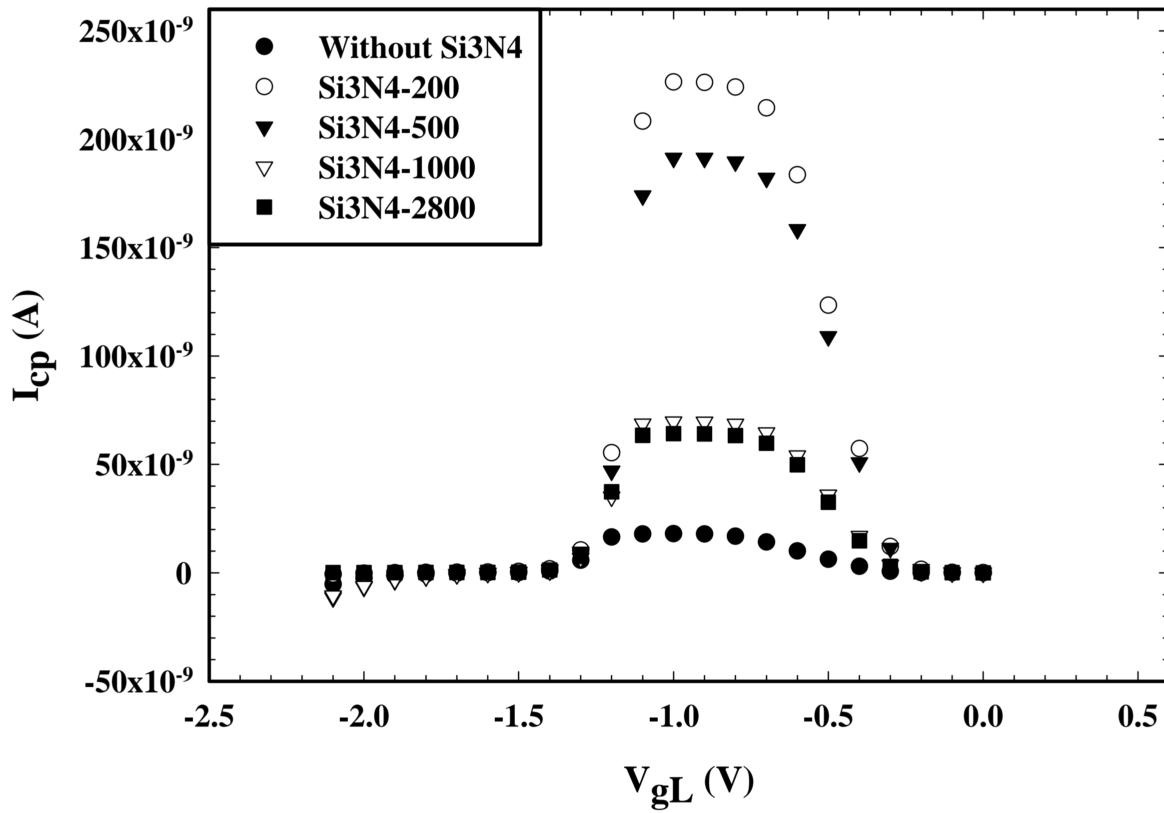


Fig. 3-30 Charge pumping current for different thickness of SiN layer (1MHZ).

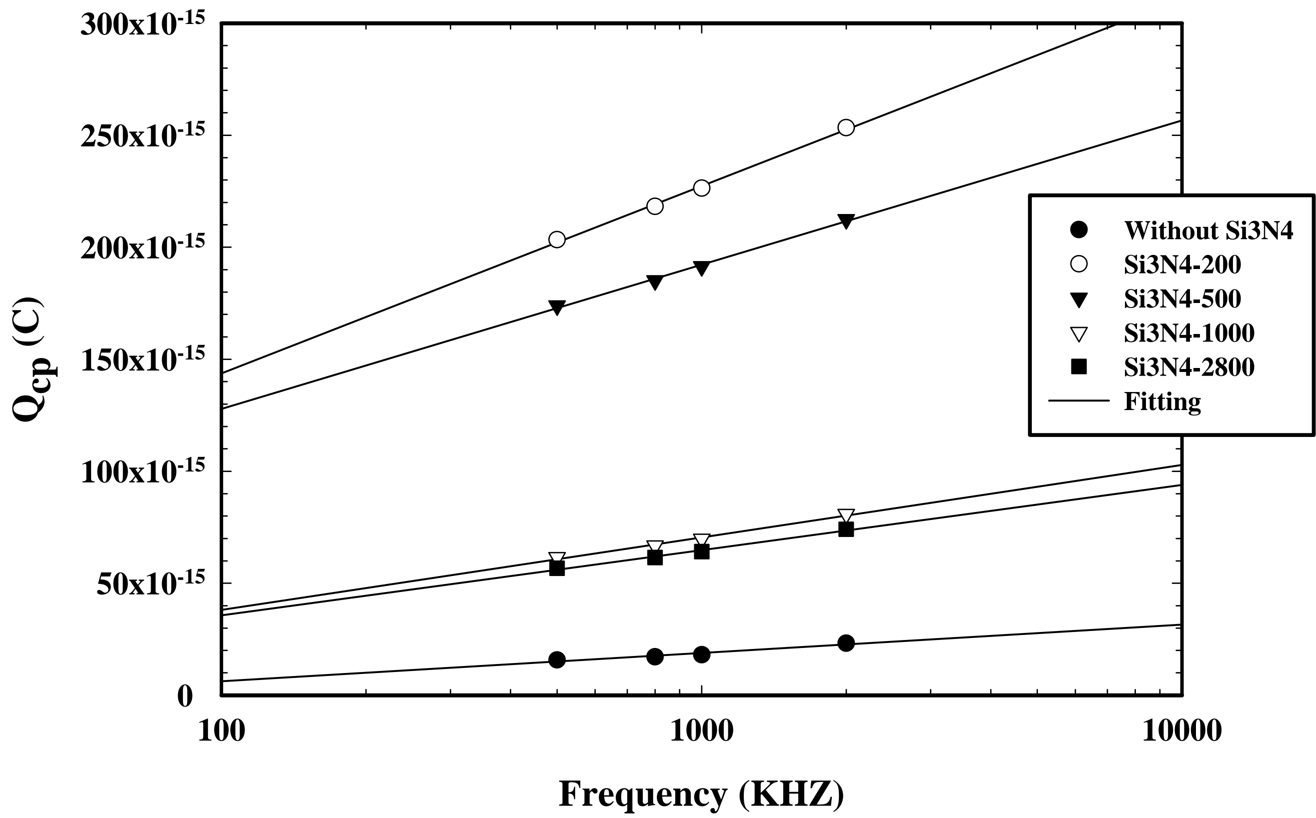


Fig. 3-31 Interface state density for different thickness of SiN capping layer.

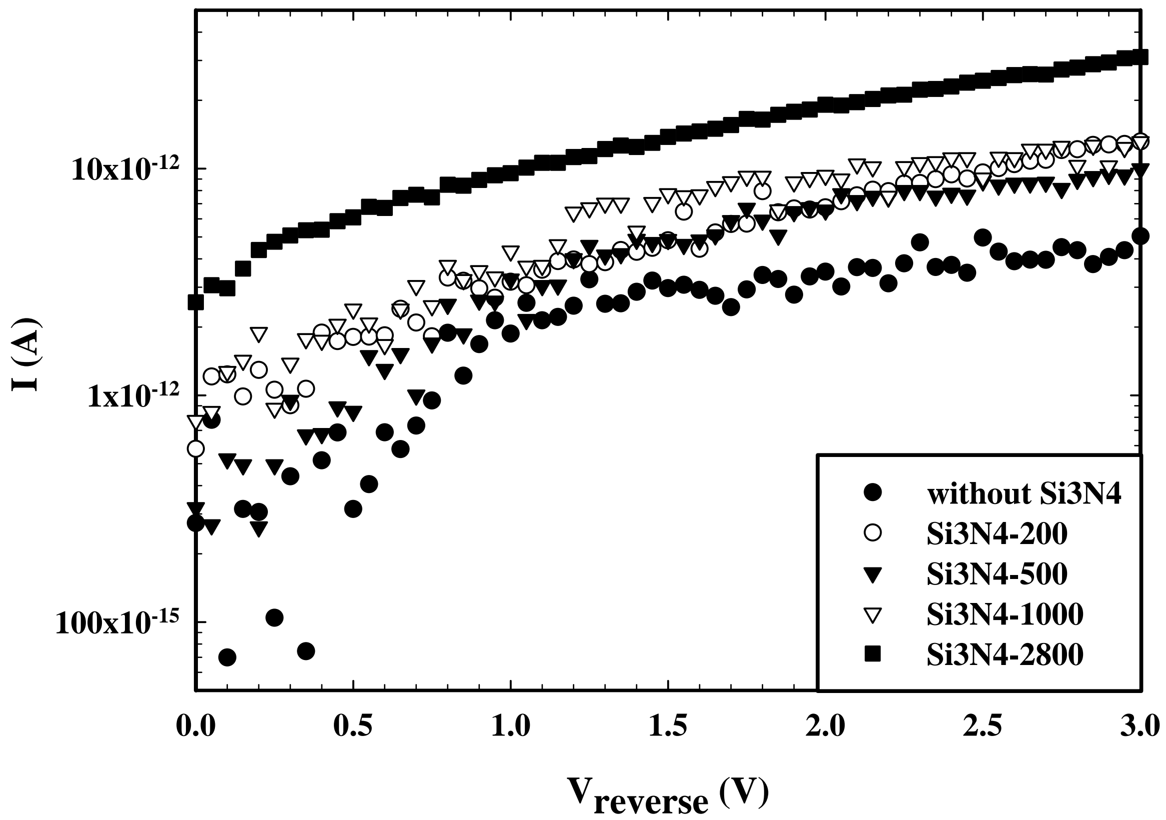


Fig. 3-32 Junction leakage current for different thickness of SiN capping layer.

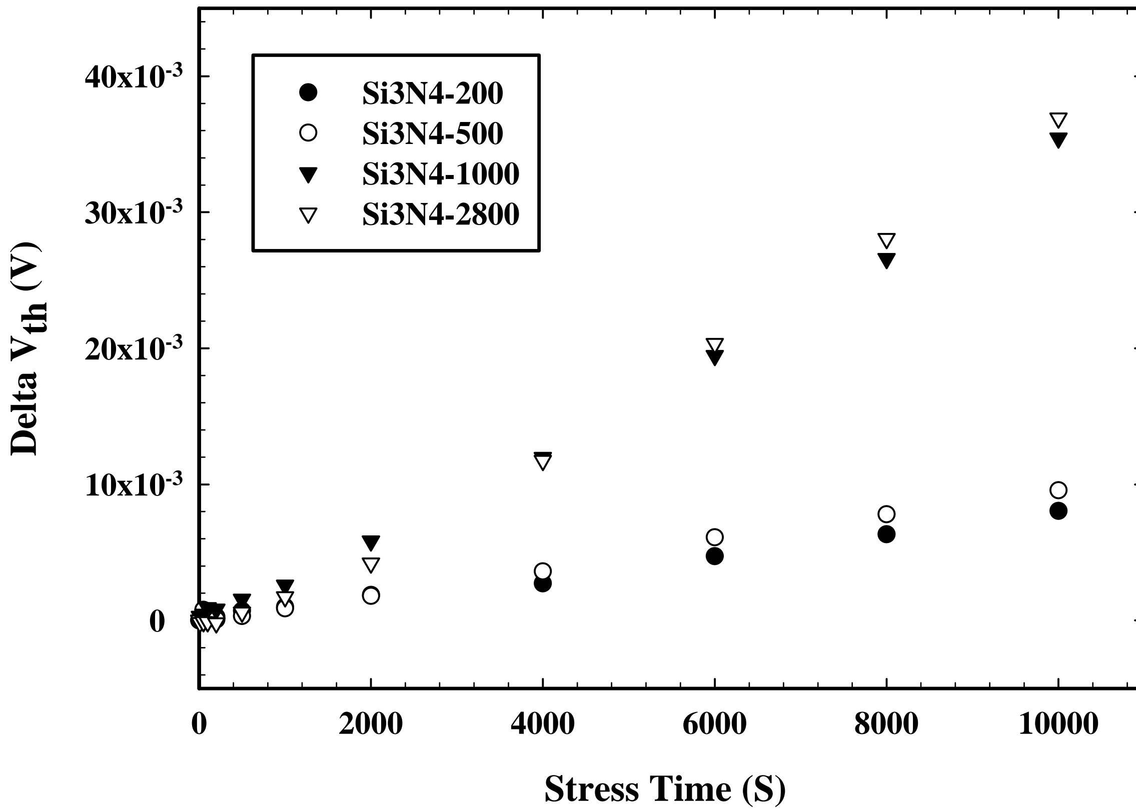


Fig. 3-33 Channel hot carrier characteristics for different SiN thickness.

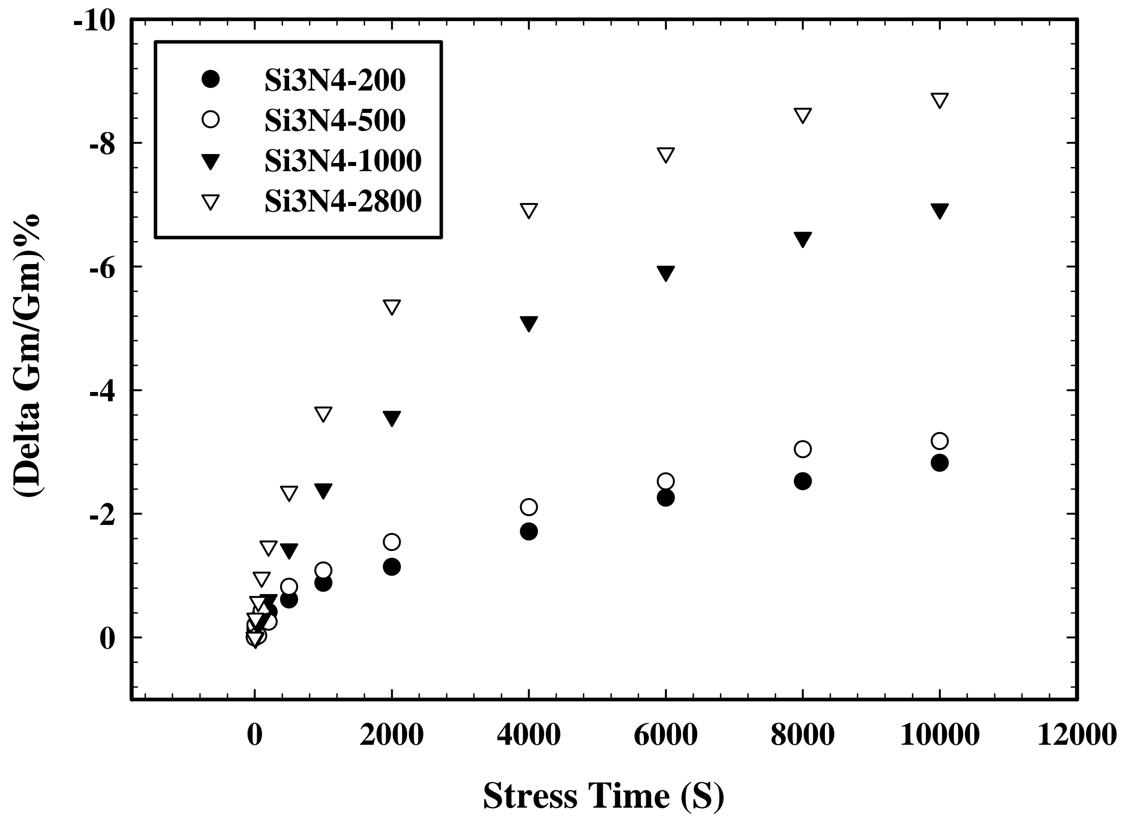
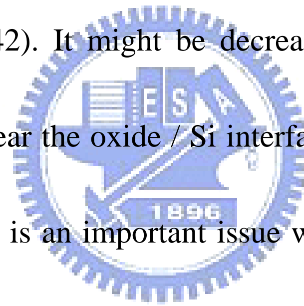


Fig. 3-34 Channel hot carrier characteristics for different SiN thickness.

3-4 Comparison of mobility enhancement in different strained structures

Finally, we would describe the comparison of local strained channel technique by using SiN-capping layer or stack of *a*-Si gate structures compared to that of the conventional devices. The dependence of I_d-V_g characteristics on different strained structures is shown in Fig. 3-35. It shows that the improvement of current drivability by using 2800Å SiN-capping layer is larger than the conventional device. Based on previous result, we have found that the stack of *a*-Si gate structures can increase the strain in the channel region. Therefore, the pronounced enhancement of current drivability can be realized by using both SiN layer and stack of *a*-Si gate structures. The increase of transconductance by using both SiN layer and stack gate poly-Si is the largest among these three samples (Fig. 3-36). We believe that the strain dependence of mobility enhancement will become significant by using both SiN-capping layer and stack of *a*-Si gate structures. Fig. 3-37 shows the dependence of output characteristics on different strained structures. The improvement of drain current becomes conspicuously by using both SiN layer and stack of *a*-Si gate structures. Fig. 3-38 ~ Fig. 3-40 illustrate the charge pumping measurement to define the quality of oxide / Si interface after the strain is introduced to channel region. The dependence of charge pumping current on different strained structures is shown in Fig. 3-38 and Fig. 3-39. The charge pumping current increases as the thickness of SiN layer or stack of *a*-Si

layer is increased. Fig.3-40 shows the dependence of interface state density on different strained structures. It shows that the interface state density increases as the increase of strain in the channel region. The dependence of channel hot carrier effect on different strained structures is shown in Fig. 3-41 and Fig. 42 (Stress Condition: 3.75V, for 10000sec). The deviation of threshold voltage in conventional device is the largest among these samples (Fig. 41). This might be a different mechanism in change of oxide quality in local strained channel devices. However, the degradation of transconductance is become more significant in either SiN capping layer or stack of *a*-Si gate structures (Fig. 3-42). It might be decreased the fixed oxide charge but increased the electron traps near the oxide / Si interface. Therefore, the improvement of oxide / Si interface quality is an important issue while we use either SiN-capping layer or stack gate poly-Si to enhance carrier mobility in local strained channel devices.



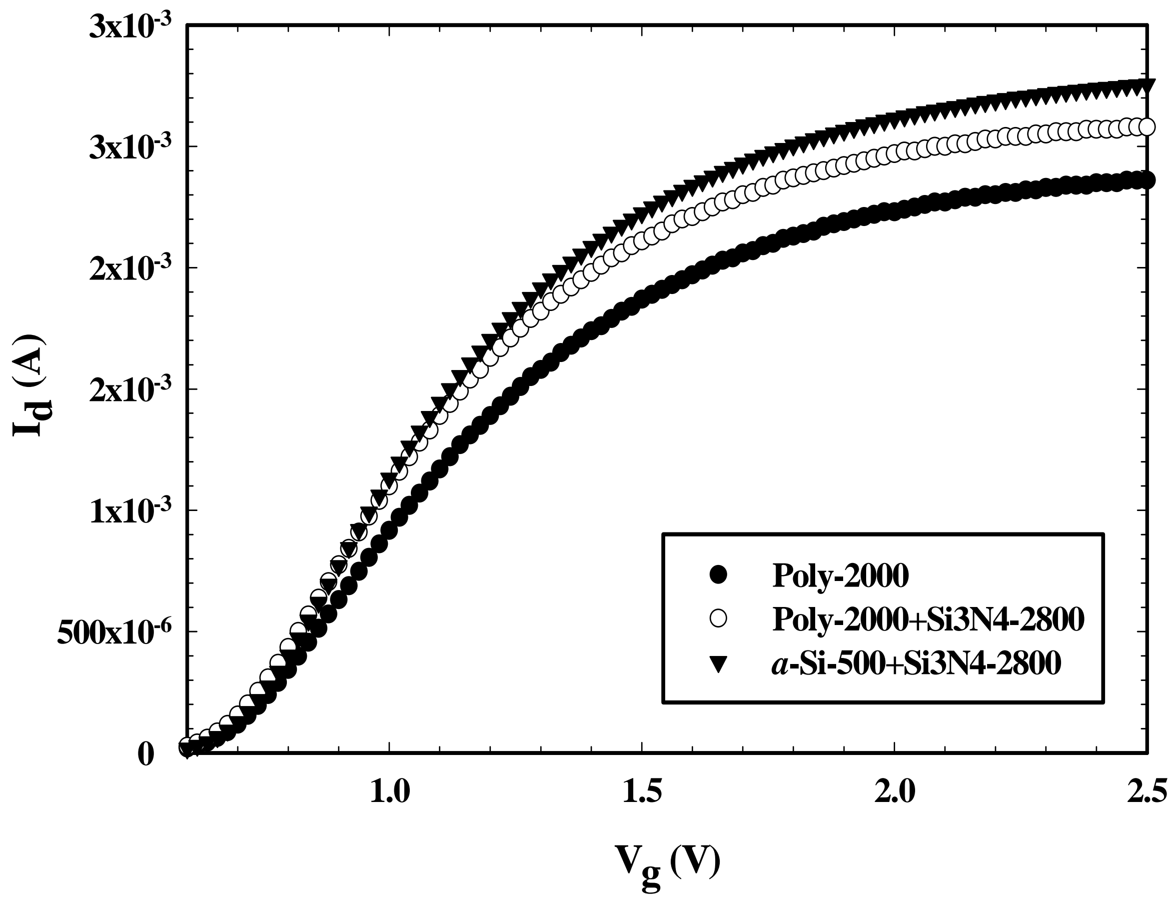


Fig. 3-35 I_d-V_g characteristics for different strained structures.

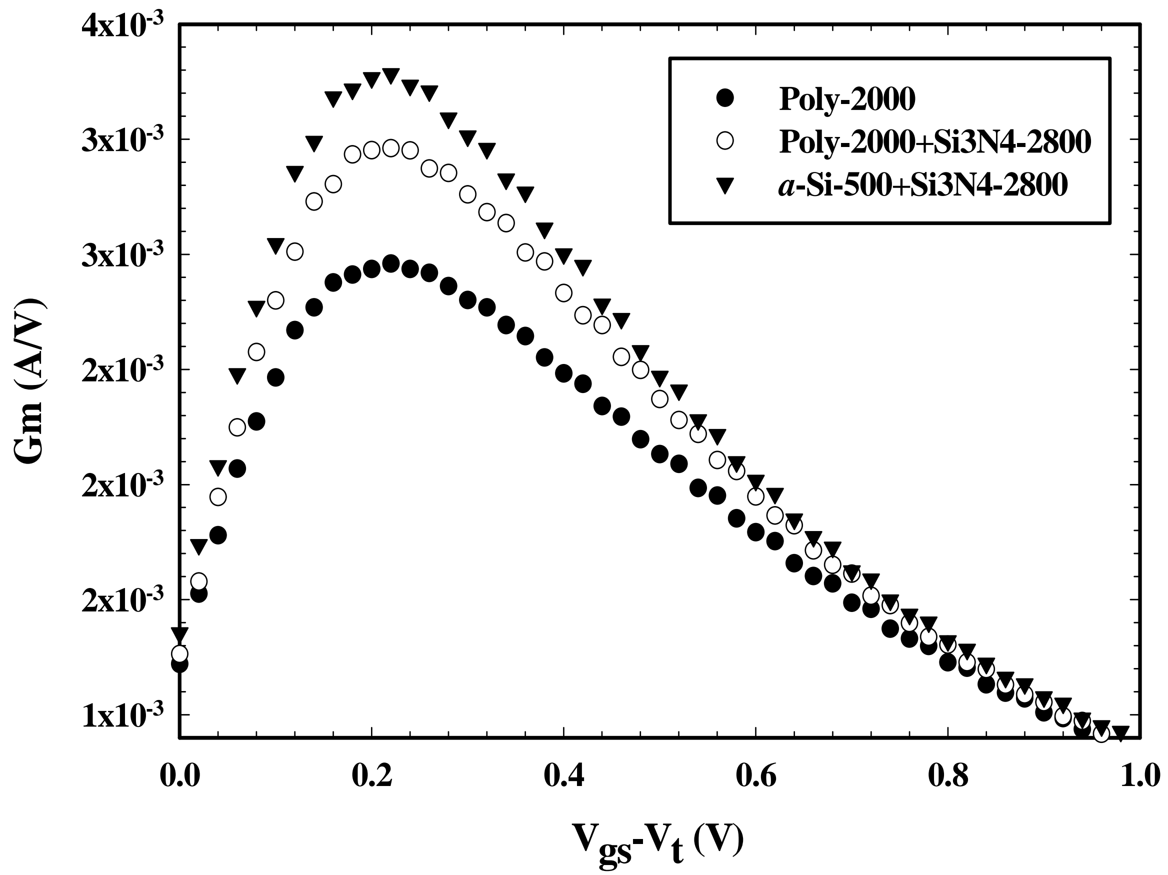


Fig. 3-36 Transconductance for different strained structures.

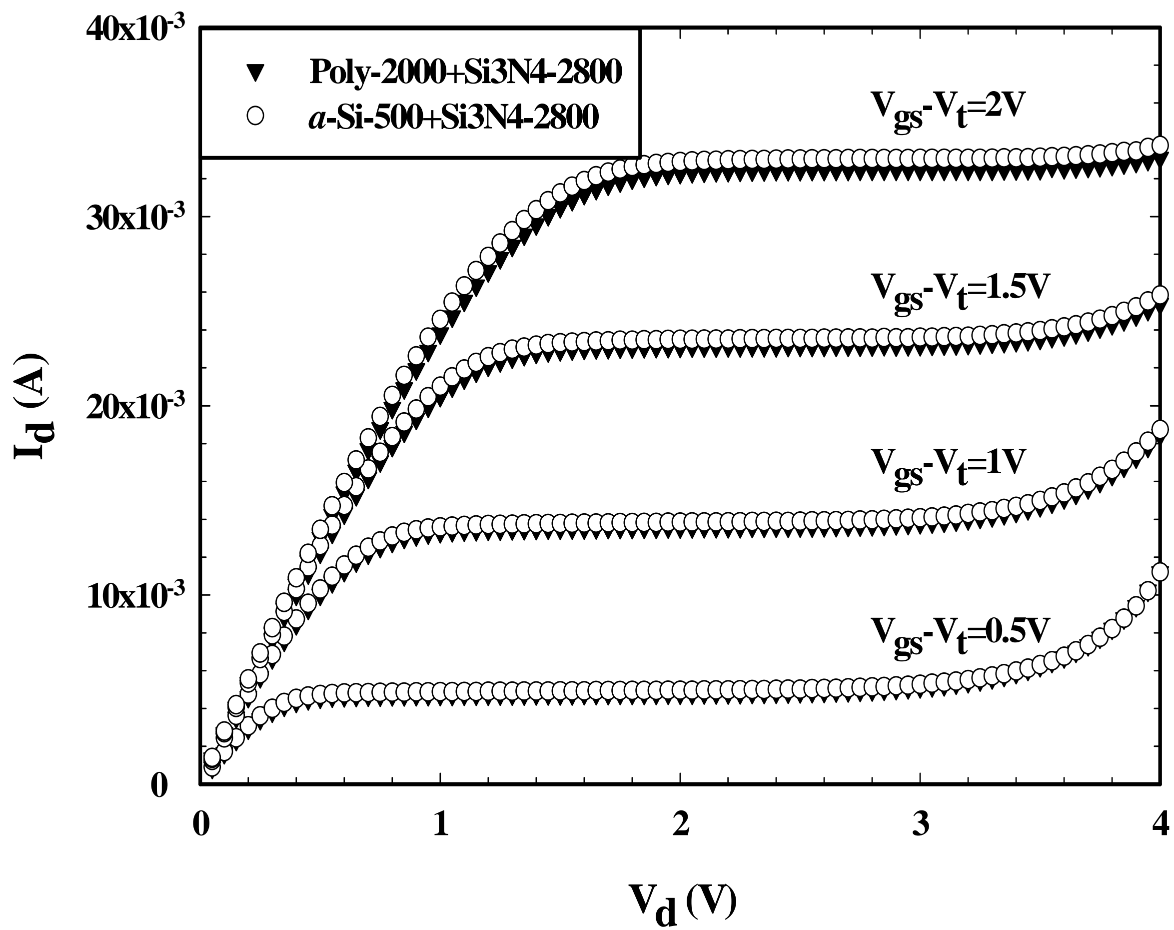


Fig. 3-37 Output characteristics for different strained structures.

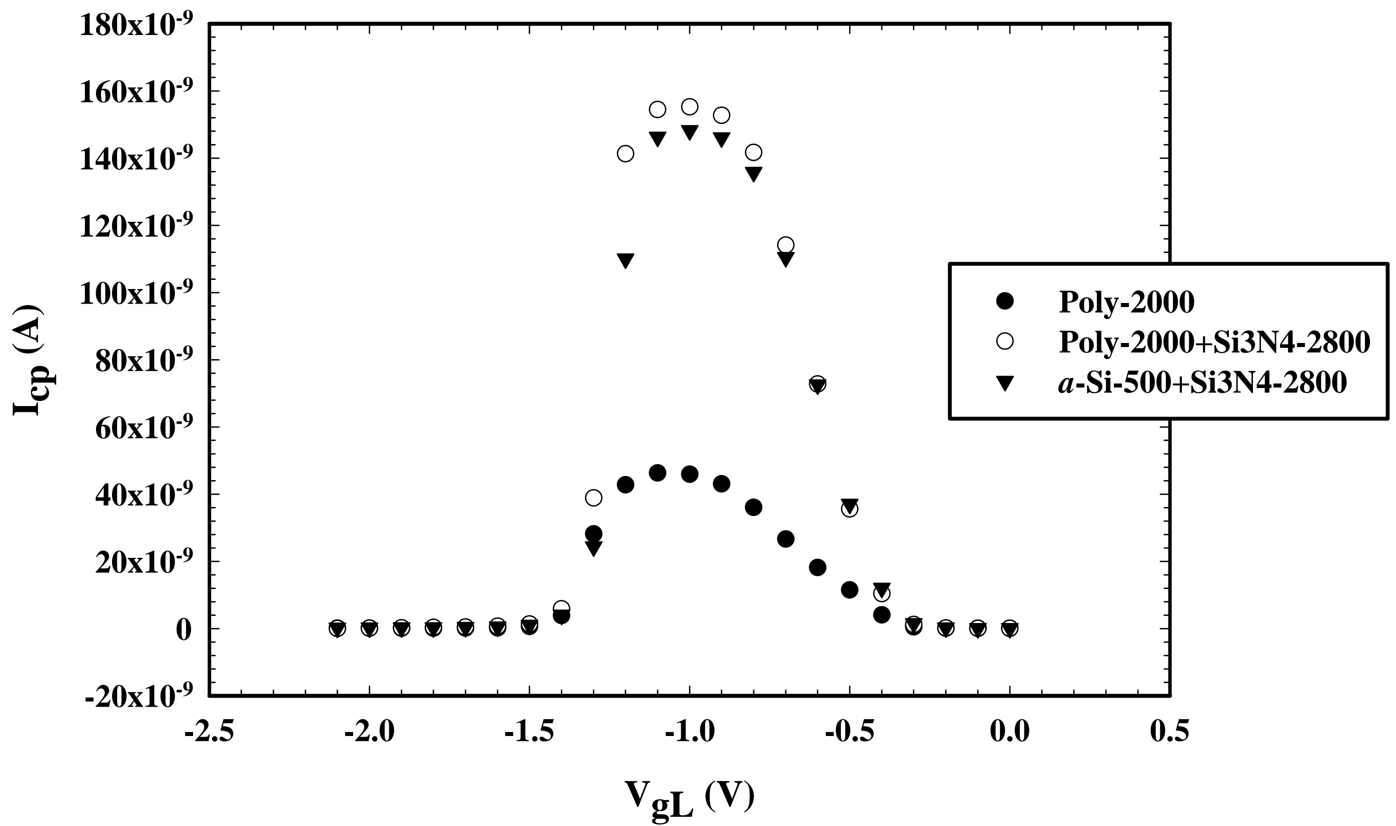


Fig. 3-38 Charge pumping current for different strained structures (2MHZ).

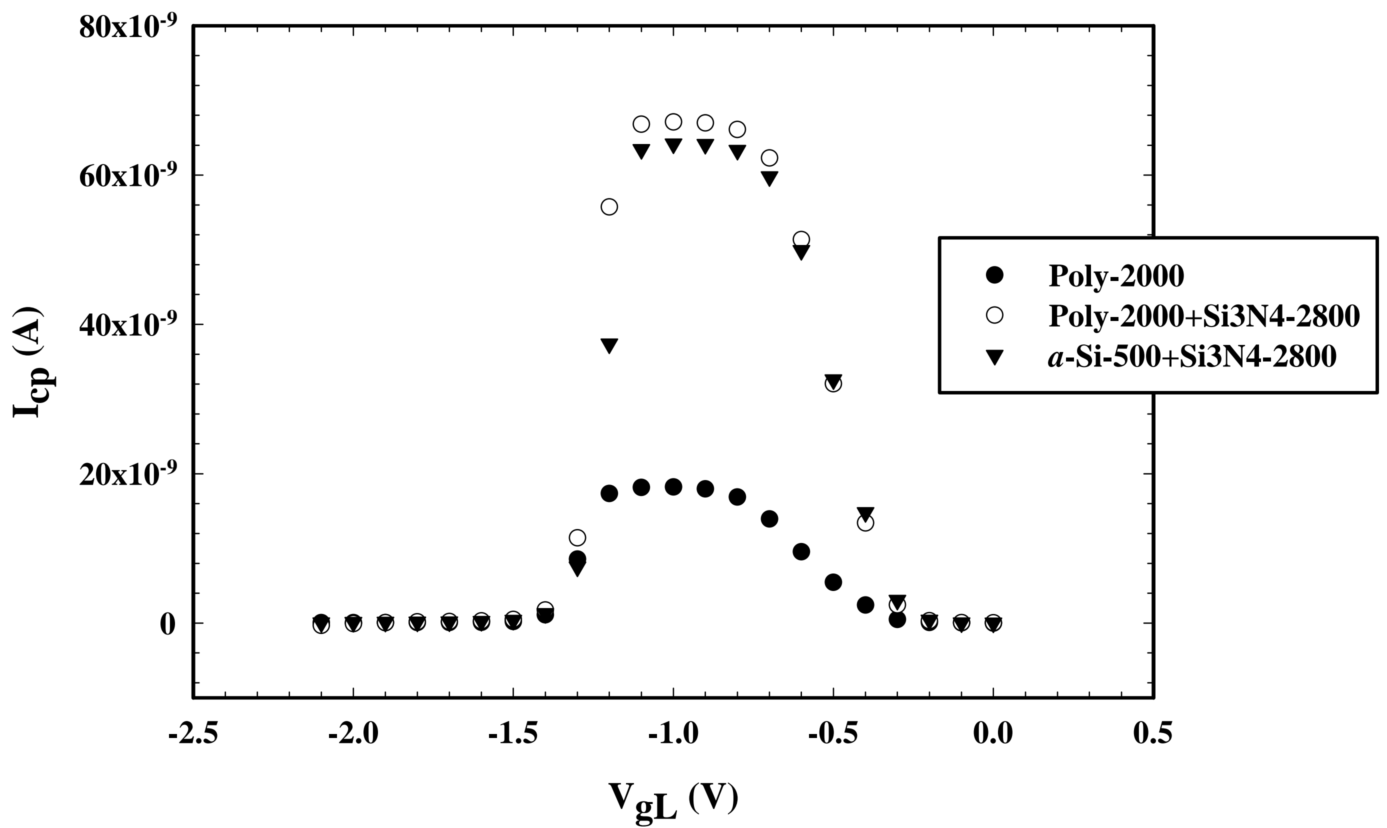


Fig. 3-39 Charge pumping current for different strained structures (1MHZ).

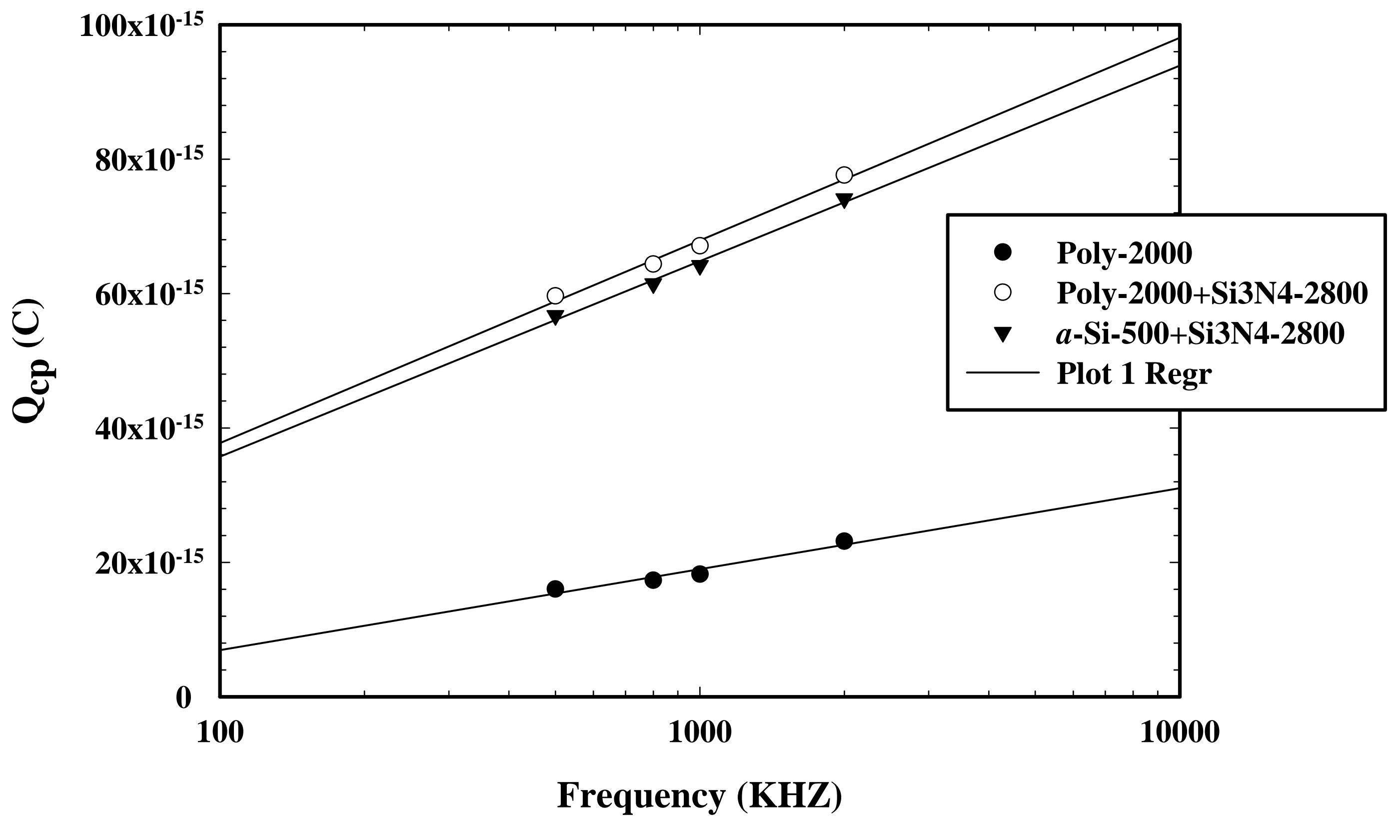


Fig. 3-40 Interface state density for different strained structures.

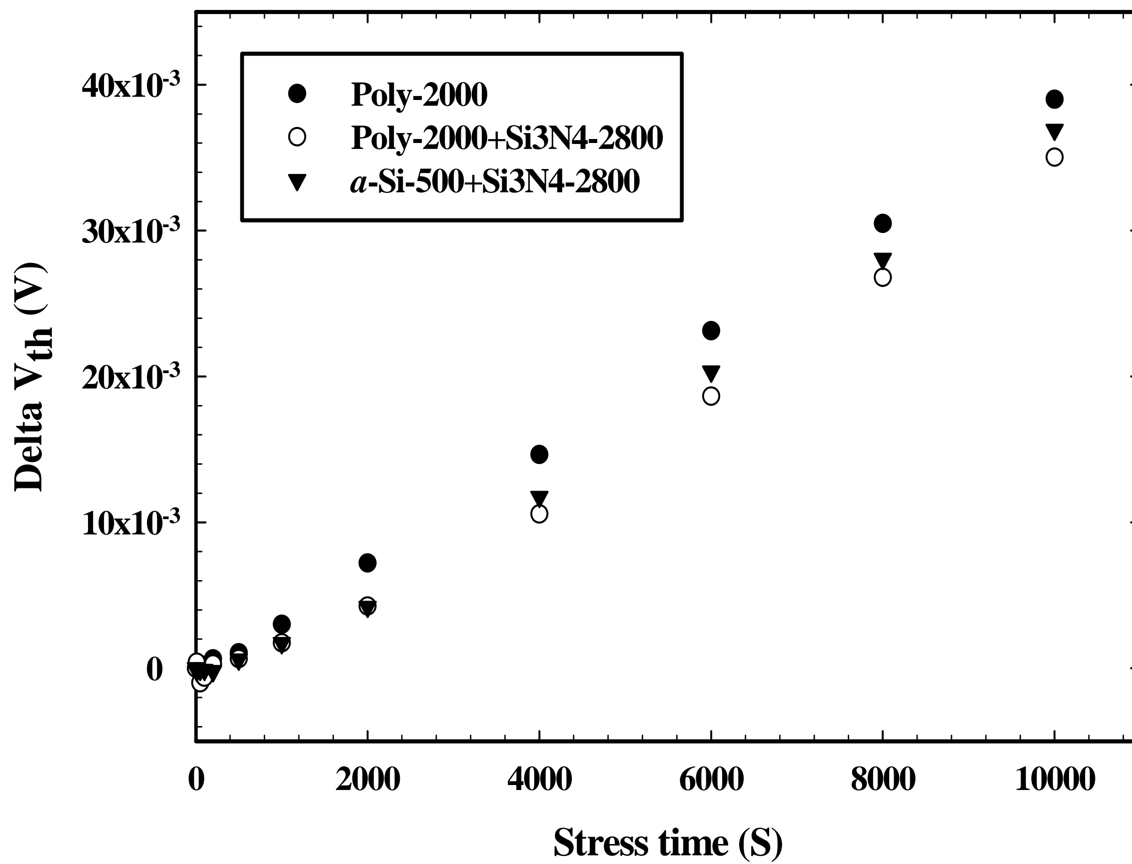


Fig. 3-41 Channel hot carrier characteristics for different strained structures.

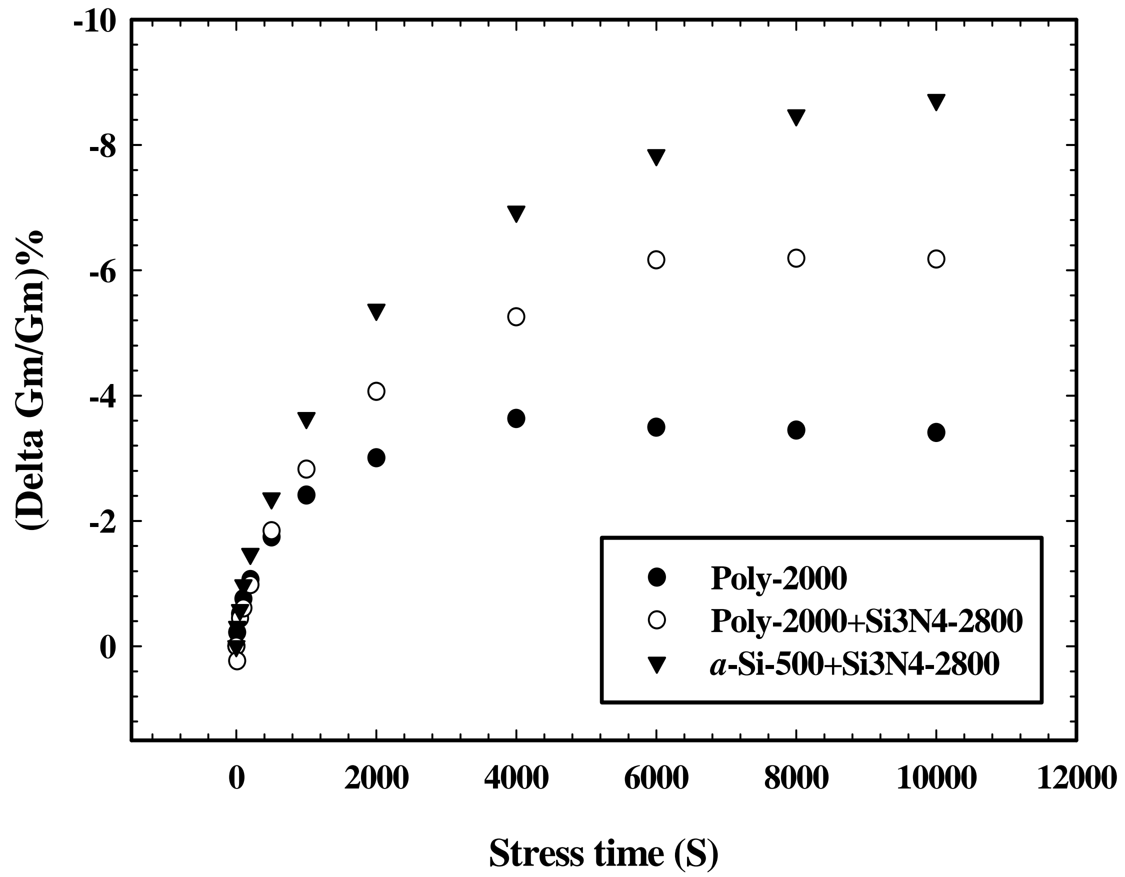
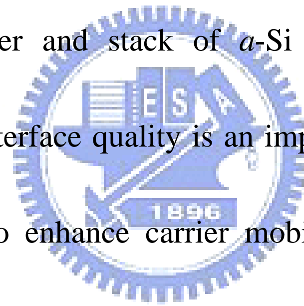


Fig. 3-42 Channel hot carrier characteristics for different strained structures.

Chapter 4

Summary and Conclusion

In summary, we proposed a local strained channel technique that using deposition of SiN layer and stack of *a*-Si gate structures. The drain current is improved 17% compared to that of the conventional devices. The current drivability can be enhanced by controlling the thickness of stack-gate poly-Si and SiN-capping layer. We believe that the performance changes are caused by changes of the electron mobility. We found that the strain dependence of mobility enhancement will become significant by using both SiN-capping layer and stack of *a*-Si gate structures. However, the improvement of oxide / Si interface quality is an important issue while we use local strained channel technique to enhance carrier mobility on device fabrication. We believe that the mobility enhancement by controlling the stress in the channel region will be crucial to future CMOS technology.



Reference

[1] J. Welser, J.L. Hoyt, and J.F. Gibons, "NMOS and PMOS Transistors Fabricated in Strained Silicon/Relaxed Silicon-Germanium Structures," in *IEDM Tech. Dig*., 1992, pp. 1000-1002.

[2] J. Welser, J.L. Hoyt, and J.F. Gibons, "Evidence of Real-Space Hot-Electron Transfer in High Mobility, Strained-Si Multilayer MOSFETs," in *IEDM Tech. Dig*., 1993, pp. 545-548.

[3] J. Welser, J.L. Hoyt, S.Takagi, and J.F. Gibons, "Strain Dependence of the Performance Enhancement in Strained-Si *n*-MOSFETs," in *IEDM Tech. Dig*., 1994, pp. 373-376.

[4] K. Rim, J. Welser, J.L. Hoyt, and J.F. Gibons, "Enhanced Hole Mobilities in Surface-channel Strained-Si *p*-MOSFETs," in *IEDM Tech. Dig*., 1995, pp. 517-520.

[5] Deepak K. Nayak, K. Goto, A.Yutani, J. Murota, and Yasuhiro Shiraki, "High-Mobility Strained-Si PMOSFETs," *IEEE Trans. Electron Devices*, Vol. 43, pp. 1709-1716, Oct. 1996.

[6] Tomohisa Mizuno, Naoharu Sugiyama, Atsushi Kurobe, and Shin-ichi Takagi, "Advanced SOI p-MOSFETs with Strained-Si Channel on SiGe-on-Insulator Substrate Fabricated by SIMOX Technology," *IEEE Trans. Electron Devices*, Vol.

48, pp. 1612-1618, Aug. 2001.

[7] K. Rim, K. Chan, L. Shi, D. Boyd, J. Ott, N. Klymko, F. Cardone, L. Tai, S. Koester, M. Cobb, D. Canaperi, B. To, E. Duch, I. Babich, R. Carruthers, P. Saunders, G. Walker, Y. Zhang, M. Steen, and M. IEong, “Fabrication and Mobility Characteristics of Ultra-thin Strained Si Directly on Insulator (SSDOI) MOSFETs,” in *IEDM Tech. Dig*., 2003, pp. 627-630.

[8] Shinya Ito, Hiroaki Namba, Kensuke Yamaguchi, Tsuyoshi Hirata, Koichi Ando Shin Koyama, Shunichiro Kuroki, Nobuyuki Ikezawa, Takehiro Saitoh, and Tadahiko Horiuchi, “Mechanical Stress Effect of Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design,” in *IEDM Tech. Dig*., 2000, pp. 247-250.

[9] F. Ootsuka, S. Wakahara, K. Ichinose, A. Honzawa, S. Wada, H. Sato, T. Ando, H. Ohta, K. Watanabe, and T. Onai, “A Highly Dense, High-Performance 130nm node CMOS Technology for Large Scale System-on-a-chip Applications,” in *IEDM Tech. Dig*., 2000, pp. 575-578.

[10] A. Shimizu, K. Hachimine, N. Ohki, H. Ohta, M. Koguchi, Y. Nonaka, H. Sato, and F. Ootsuka, “Local Mechanical-Stress Control (LMC) : A New Technique for CMOS-Performance Enhancement,” in *IEDM Tech. Dig*., 2001, pp. 433-436.

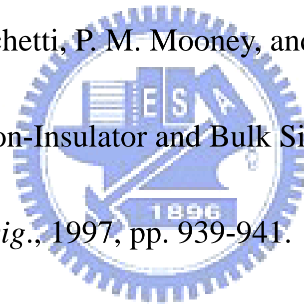
[11] H. S. Momose, T. Morimoto, K. Yamabe, and H. Iwai, “Relationship between

Mobility and Residual-Mechanical-Stress as Measured by Raman Spectroscopy for Nitride-Oxide-Gate MOSFETs," in *IEDM Tech. Dig*., 1990, pp. 65-68.

[12] K. Ota, K. Sugihara, H. Sayama, T. Uchida, H. Oda, T. Eimori, H. Morimoto, and Y. Inoue, "Novel Locally Strained Channel Technique for High Performance 55nm CMOS," in *IEDM Tech. Dig*., 2002, pp. 358-361.

[13] Kuei-Shu Chang-Liao, Ling-Chih Chen, "Silicon dioxide/silicon interfacial strain analyzed by infared spectroscopy," *Surface and Coating Technology*, pp.379-382, 1997.

[14] Sandip Tiwari, M. V. Fischetti, P. M. Mooney, and J. J. Welser, "Hole Mobility Improvement in Silicon-on-Insulator and Bulk Silicon Transistors Using Local Strain," in *IEDM Tech. Dig*., 1997, pp. 939-941.



[15] A. Steegen, A. Lauwers, M. de Potter, G. Badenes, R. Rooyackers, and K. Maex, "Silicide and Shallow Trench Isolation line width dependent stress induced junction leakage," in *VLSI Tech*. Dig., 2000, pp. 180-181.

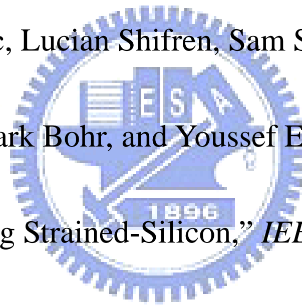
[16] B. Anantharam, R. D. Chang, S. K. Oswal, C. Y. Tu, and S. K. Banerjee, "A Novel Sidewall Strained-Si Channel nMOSFET," in *IEDM Tech. Dig*., 1999, pp. 727-730.

[17] Yoshinao Harada, Koji Eriguchi, Masaaki Niwa, Takanobu Watanabe, and Iwao Ohdomari, "Impact of Structural Strained Layer near SiO2/Si Interface on

Activation Energy of Time-Dependent Dielectric Breakdown," *Jpn. J. Appl. Phys*. Vol. 39, pp. 4687-4691, July. 2000.

[18] J. R. Shih, J. J. Wang, Ken Wu, Peng Yeng and J. T. Yue, "The Study of Compressive and Tensile stress on MOSFET' I-V, C-V Characteristics and It's Impacts on Hot Carrier Injevtion and Negative Bias Temperature Instabillity," in *IRPS*, 2003, pp. 612-613, 2003.

[19] Scott E. Thompson, Mark Armstrong, Chis Auth, Steve Cea, Robert Chau, Glenn Glass, Thomas Hoffman, Jason Klaus, Zhiyong Ma, Brian Mcintyre, Anand Murthy, Borna Obradovic, Lucian Shifren, Sam SiVakumar, Sunit Tyagi, Tahir Ghani, Kaizad Mistry, Mark Bohr, and Youssef EI-Mansy, "A Logic Nanotechnology Featuring Strained-Silicon," *IEEE Trans. Electron Devices Lett*, Vol. 25, pp. 191-193, Apr. 2004.



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Strain Dependence of Mobility Enhancement in

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