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An automatic parameter extraction technique for advanced CMOS device modeling using genetic algorithm

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Abstract

We in this paper present an computational intelligence technique to extract semiconductor device model parameters. This solution methodology is based on a genetic algorithm (GA) with an exponential type weight function, renew operator, and adaptive sampling scheme. The proposed approach automatically extracts a set of complete parameters with respect to a specified compact model, such as a BSIM model for deep-submicron and nanoscale complementary metal-oxide-semiconductor (CMOS) devices. Compared with conventional artificial step-by-step fitting approaches, the proposed extraction methodology automatically tracks the shape variation of current–voltage (I–V) curves and examines the first derivative of I–V curves; therefore, highly accurate results can be obtained directly. Applying the renew operator will keep the evolutionary trend improving by removing the individuals without mainly features. The sampling strategy will speed up the evolution process and still maintain the extraction accuracy in a reasonable range. A developed prototype is successfully applied to extract model parameter of N- and P-metal-oxide-semiconductor field effect transistors (MOSFETs). This optimization method shows good physical accuracy and computational performance, and provides an alternative for optimal device modeling and circuit design in nanodevice era. Genetic algorithm based automatic model parameter extraction bridges the communities between circuit design and chip fabrication; in particular, it will significantly benefits design of system-on-a-chip.

Keywords: Computational intelligence; Genetic algorithm; Extraction methodology; Computer-aided design; Compact model; Parameter quality; CMOS devices

1. Introduction

Using technology computer aided design (TCAD) and electronic CAD (ECAD) tools to investigate VLSI device's characteristics currently plays a central role in academic research and industry applications [1–16]. Genetic algorithm is a self-adaptive optimization strategy that mimics a living system [17]. This global optimal strategy has been of great interest for a wide range of applications [18–27]. In particular, in microelectronics it has been applied for various VLSI physical designs, such as cell placement, channel routing, test pattern generation, and design for test.

For nanoscale CMOS devices and VLSI circuit design, a designer defines a target set of I–V curves on a designed device firstly, and finds out the corresponding parameters manually. This procedure is time-consuming and low performance task in modern microelectronic industry. Combined with the Newton-liked techniques some optimization approaches, such as the direct and numerical methods have been proposed in solving such problems. However, these local methods often require accurate initial guesses to start the iteration and apparently encountered seriously convergent problem in practical CAD implementation. In semiconductor industry, a foundry will produce different size of devices at one time and it is necessary to find a set of parameters to represent the electrical characteristics for all devices. For example, there are 4 families of I–V curves to be optimized for a given MOSFET, each I–V family contains 5 I–V curves, and each I–V curve has

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more than 80 I–V points. To extract parameters from various devices with different geometries is even more difficult and time-consuming task. Therefore, any improved evolution strategies for intelligent optimization will significantly reduce the dependency of computing resource.

In this work combining with an optimization technique we applied the GA in optimal I–V curves characterization, optimization, and parameter extraction for deep-submicron and nanoscale MOSFETs. Our GA methodology is based on a floating-point operator and a renew operator. The floating-point operator is suitable for solving this numerical optimization problem, and the renew operator reveals good evolving behaviors to skip over local optimal conditions. In addition, an exponential type weight function is applied to mimic many sets of I–V curves precisely. For a specified stopping criterion, this unified intelligent computing technique can automatically extract parameter from a single as well as multiple VLSI devices. Application of our optimization technique to extract parameter of N- and P-MOSFETs with different channel length and width is successfully obtained in terms of model accuracy and computational efficiency. This paper is organized as follows. Taking a BSIM model as an example, Section 2 states the role of compact models for VLSI devices. Section 3 discusses the proposed extraction and optimization technique. Section 4 shows our results for deep-submicron and nanoscale MOSFETs. Section 5 draws conclusions and suggests future works.

2. Equivalent circuit model for VLSI devices

In semiconductor fabrication and microelectronics industry, various compact models, such as BSIM, EKV, MOS models for VLSI devices have been widely applied to device characterization and optimization, circuit design and simulation, and system verification [18,19]. These models for solving physical phenomena of devices are through applying multiple physical-based approximations. A set of well-defined parameters plays a significant role to the simulated results. Finding out a set of optimal parameters for a specific device characterization is a very tedious and complicated task. This process, known as parameter extraction, is not only laborious but also requires extensive expertise to achieve the meaningful parameter. Among well-known compact models, Berkeley short-channel IGFET model (BSIM) is one of physics-based deep-submicron MOSFET models for digital and analog circuit designs [18,19]. Nowadays, it is widely used by many research organizations, semiconductor fabrication, and integrated circuit design companies.

For advanced CMOS devices and VLSI circuit simulation, without loss of generality, we focus here on the BSIM3v3 model parameter extraction with the developed GA-based CAD prototype. We note that our solution methodology can be applied to different compact models, such as BSIM4, MOS, SP, EKV, HiSIM, and diverse macro models. Completely equations of the BSIM3 model are more than 50 nonlinear algebraic equations. As shown in Fig. 1 MOSFET typically has four control sources: V_D, V_G, V_S, and V_B. Fig. 1 shows a typical DC base band equivalent circuit of the BSIM3v3 model for a corresponding MOSFET. In the BSIM3v3 model, there are several hundreds of parameter for a complete DC/AC simulation and characterization. For DC simulation, there are about 80 parameters have to be extracted, and these parameters can be grouped into five categories which include general parameters, threshold voltage parameters, mobility parameters, sub-threshold current parameters, and rout parameters. Table 1 partially shows the model parameters and possible numerical range to be extracted [19]. Grouping the parameters into various sets gives us suggestions in designing encoding methodology and choosing proper cross over behavior in this work.

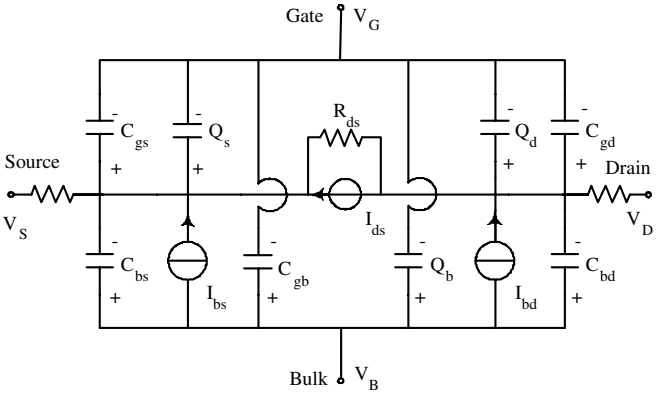

Fig. 1. A schematic diagram of the BSIM3v3 equivalent circuit for advanced MOSFETs.

Table 1
A partial list of BSIM3v3 model parameters

Name	Range	Res.	Unit	Name	Range	Res.	Unit
V_{th0}	−1.0 to 1.5	$1e^{-3}$	V	k_1	0.0 to 1.5	$1e^{-3}$	$V^{1/2}$
k_2	−0.1 to 0.1	$1e^{-4}$	–	k_3	−5.0 to 0.0	$1e^{-3}$	–
D_{vt0}	0.0 to 2.0	$1e^{-3}$	–	D_{vt1}	0.0 to 1.5	$1e^{-3}$	–
D_{vt2}	−0.15 to 0.0	$1e^{-4}$	1/V	D_{vt0w}	−0.03 to 0.0	$1e^{-5}$	1/m
D_{vt1w}	−0.2 to 0.2	$1e^{-3}$	1/m	D_{vt2w}	−0.2 to 0.4	$1e^{-3}$	1/V
N_{lx}	−0.2 to 0.2	$1e^{-3}$	m	K_{3b}	0.0 to 0.4	$1e^{-4}$	1/V
V_{sat}	0.0 to $2e^5$	$1e^3$	m/s	U_a	$-3e^{-9}$ to $3e^{-9}$	$1e^{-11}$	$(m/V)^2$
U_b	0.0 to $8e^{-18}$	$1e^{-20}$	$(m/V)^2$	U_c	0.0 to $8e^{-10}$	$1e^{-13}$	m/V^2

Due to the inconsistently manufacturing techniques, devices may have different electrical behaviors even though they are produced with the same process. However, the foundry still tries to find a set of featured parameters which can fit all device's behaviors. For examples, Figs. 2 and 3 demonstrate our examination for the continuity property of the BSIM3v3 model with respect to different device channel length and device width. We note that channel length and device width are the most important parameters in the BSIM3v3 compact model. With this continuity property, we can apply the adaptive sampling to accelerate the parameter extraction procedure.

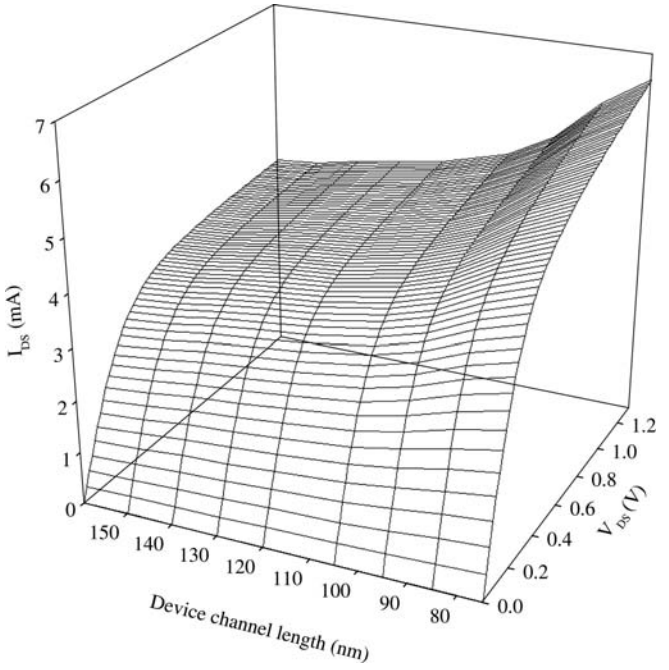

Fig. 2. A continuity analysis of the BSIM3v3 model with respect to device channel length, where device width is fixed at 10 μm.

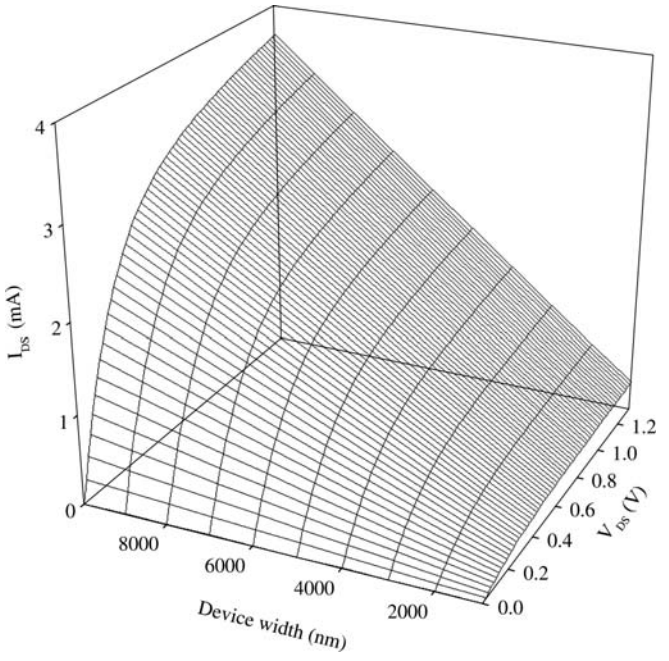

Fig. 3. A continuity analysis of the BSIM3v3 model with respect to device width, where device channel length is fixed at 0.18 μm.

3. Intelligent computing technique

Genetic algorithm is developed to solve the multiobjective optimization task above. We apply the engineering- and physical-based GA procedures with two special operators, floating-point operator and renew operator, to perform the model parameter extraction [23]. Implementation of the proposed GA is described as follows.

```
The GA-based parameter extraction procedure
Begin
  Problem definition
  For i = 1 To number of parameters
    GeneEncode(Parameter[i])
  End For
  Sampling()
  While ErrorNorm > Stop Criteria
    Fitness()
    Reproduction()
    If the diversity of the population decreasing
      Renew()
    End If
    CalculateErrorNorm()
  End While
End The GA-based parameter extraction procedure
```

3.1. Problem definition

To perform the parameter extraction systematically, we first write the function in terms of the input variables. The relationship between model input parameters (V_D, V_S, V_B, V_G), and simulated output result, for example I_D can be expressed mathematically as follows:

$$f(V_D, V_S, V_B, V_G, \vec{p}) = I_D, \tag{1}$$

where the function f can be regarded as the BSIM3's I_D–V_D current equation, and the vector $\vec{P}$ contains all parameters to be extracted. All I_D–V_D and I_D–V_G points form a family set of I–V curves. The goal of evolution is to minimize the difference between a set of measured targets and simulated I–V curves, and then eventually find out their corresponding model parameter for all dimension of devices.

3.2. Encoding method

The design of gene encoding strategy strongly depends on the property of the problem. For a DC MOSFET circuit, there are typically about 100 parameters. All unknowns to be extracted are floating-point numbers. We

transform these continuous floating-point numbers into discrete steps (P_{steps}) through step function as shown in Eq. (2) instead of real numbers, and we encode the discrete steps as genes on chromosomes. The discrete steps show the strongly combinatorial properties, and we have found this representation not only has better results in crossover and mutation but also is suitable for the MOSFET parameter extraction,

$$P_{value} = P_{min} + P_{steps}\frac{P_{max} - P_{min}}{R_{esolution}} \quad (2)$$

3.3. Sampling strategy

As shown in Fig. 4 the typical I–V curves can be separated in two parts: the linear region and the saturation region at least. The linear region is rather sensitive, while the saturation region appears more flat. We use exponential type weight function to put significantly emphasize on the linear region. Moreover, reducing the problem's complexity is rather important in this investigation. After analyzing the properties of the BSIM3v3 model in the Section 2, the correct continuous quality suggests us to fit some candidate devices and I–V points. First, we choose some characteristic devices to fit, and for each selected device, we put densely sampling points on the linear region, and less sampling points on the saturation region. The sampling step determines total points to be fitted in the linear and saturation regions, and the determination function is given by

$$\text{Sampling Point} = \text{Total Point}/\text{Sampling Step} \quad (3)$$

3.4. Fitness function

We consider the fitness function F as follows:

$$F = W * \sqrt{(I_{Dr} - I_{DS})^2}, \quad (4)$$

where W is the weight function, shown in Fig. 4. I_{Dr} and I_{Ds} are the sets of target and simulated I–V points, respectively. The linear region of the I–V curves is rather sensitive, so we define a physical-based weight function to emphasize correlation relationship for all I–V points. It decreases as the applied voltage increases. This exponential-liked weight function plays an important role in tracking device's I–V curves. We evaluate the discrepancy for the two I–V sets with the proposed weight function.

3.5. Reproduction

We adopt the tournament selection with floating-point operator as our selection strategy. This hybrid strategy not only selects better chromosomes but also keeps weak ones for few generations to achieve higher population diversity. For the crossover scheme, in the BSIM3v3 compact model, all parameters to be optimized can be classified into five categories which represent different numerical constraints. We take a uniform crossover scheme [8]; and based on our simulation experience, it is more effective than single and two-point cuts crossover schemes. Intuitionally, it is meaningless to crossover the genes of different categories of a chromosome into the offspring. Therefore, we choose uniform crossover corresponding to the five categories. Finally, the mutation strategy changes the mutation rate dynamically to keep the population diversity. When the evolutionary trend appears to be saturated, we increase the mutation rate to achieve larger population diversity for breaching current bottleneck.

3.6. Renew operator

Even though GA shows interesting performance for various problems, it is easily trapped into local optimal in such multiobjective problems. We introduce a renew operator which ensures the evolvement of GA escaping from local optimal results. After certain generations, the population is filled with old individuals. These individuals have similar

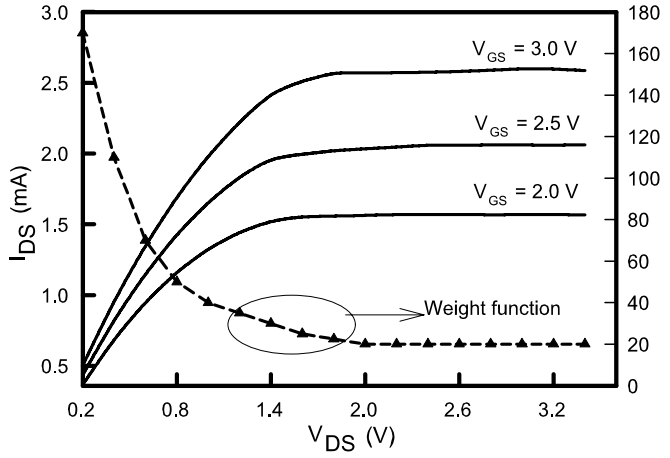

Fig. 4. An illustration of the relationship between the I–V curves and the proposed weight function.

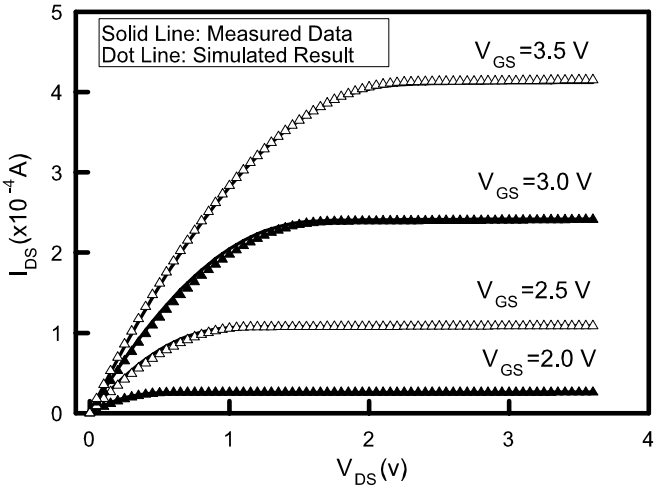

Fig. 5. Plot of I_{DS}–V_{DS} curves, where the maximum error < 2%).

features in their genes hence decrease the diversity of the population. The renew operator will save some featured chromosomes which include better, and/or worse chromosomes to keep the mainly features of the evolutionary trend, and flush the population pool, then restart the evolution process.

4. Results and discussion

In this section, we first demonstrate the accuracy of simulated results compared with measured data from a realis-

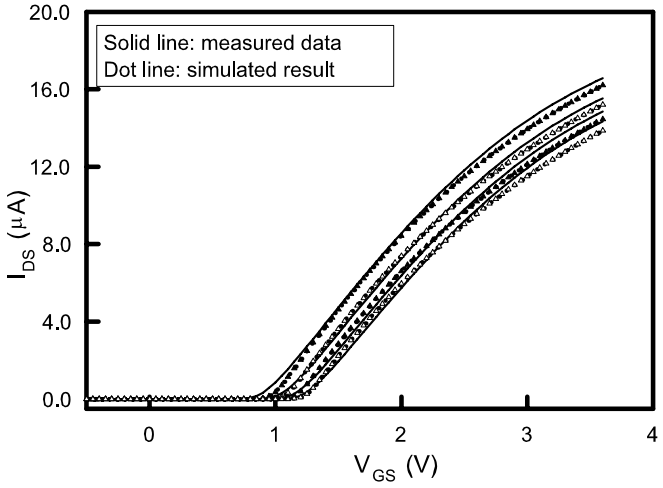

Fig. 6. Plot of I_{DS}–V_{GS} curves, where the maximum error < 2%.

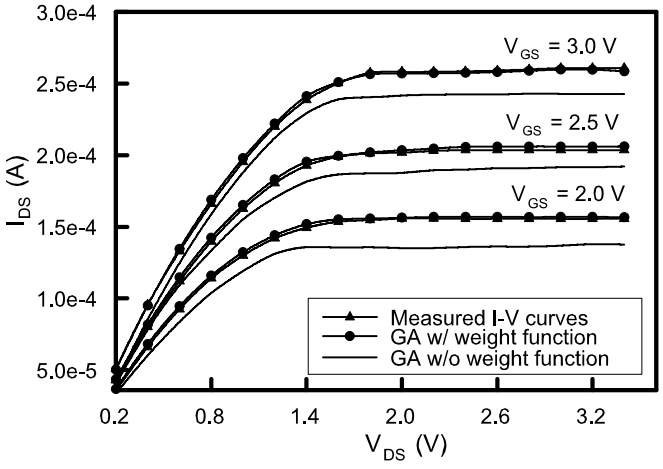

Fig. 7. An investigation of efficiency of the weight function.

Table 2
A comparison of score and time cost vs different population sizes

Population size	Elapsed time-1	Score-1	Elapsed time-2	Score-2
25	201	0.254634	401	0.254581
50	407	0.215359	806	0.207444
75	663	0.185788	1291	0.182184
100	949	0.179823	1748	0.156866

Time-1 and score-1 are for 1000 generations, and time-2 and score-2 are for 2000 generations.

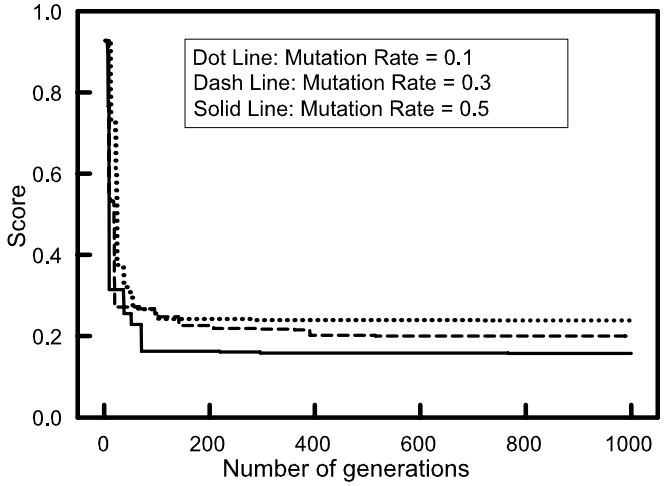

Fig. 8. A plot of score convergence vs the number of generations with respect to different mutation rates.

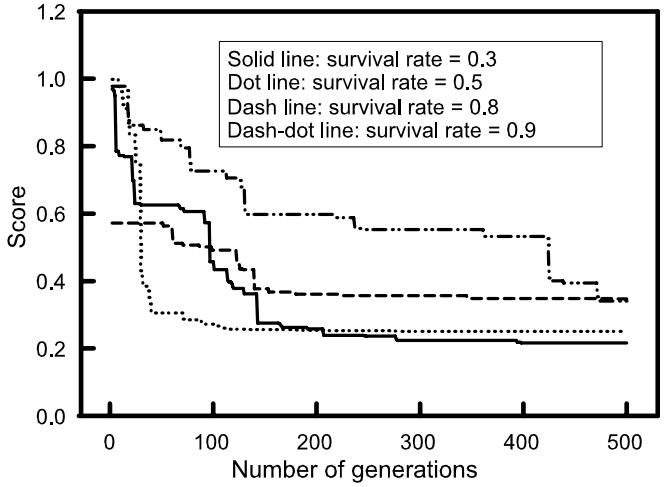

Fig. 9. A plot of score convergence vs the number of generations with respect to different survival rates.

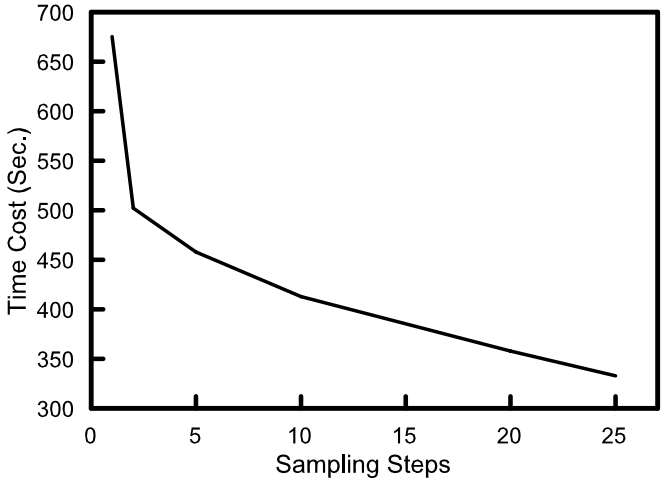

Fig. 10. A plot of time cost vs different sampling steps.

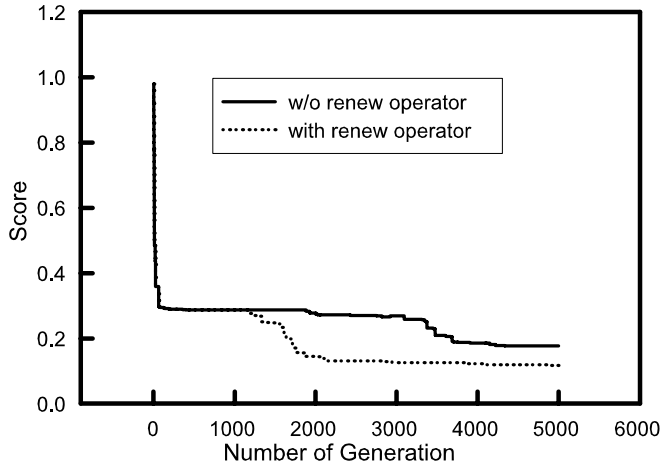

Fig. 11. A plot of score convergence vs the number of generations with and without renew operator.

Fig. 12. A logo of the developed extraction prototype.

tic fabricated N-MOSFET. Secondly, a series of examinations will be given to show the achieved effect upon the evolutionary trend with varying different genetic factors, and the influence of each factor will be discussed later. All demonstrated results are with average results of 10 experiments.

Figs. 5 and 6 show the evolutionary accuracy. We perform a parameter extraction for 10 different dimensions of devices, and these two figures are the results of one device (the device length and width are 0.25 and 10 μm) among the ten. The solid lines are measured data and the dot lines are the simulated results which are simulated with the BSIM3v3 model together with our extracted parameters. It is obvious that simulated results match the measured data approximately. Both two figures show the accuracy of the developed extraction prototype for deep-submicron MOSFETs.

As shown in the Fig. 7, it shows a comparison between multiple I–V curves evolution with and without applying weight function after 300 generations. The evolutionary

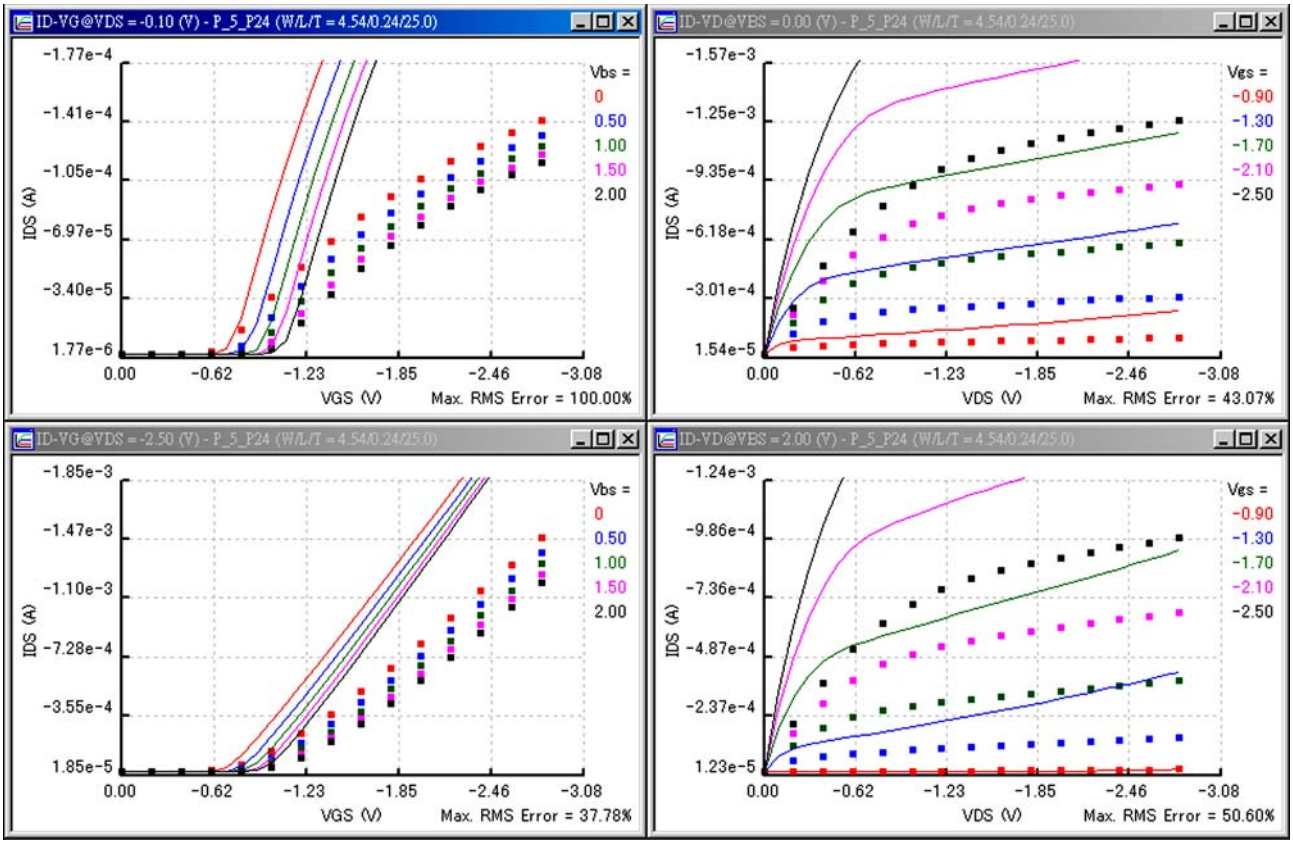

Fig. 13. The first generation of extraction process.

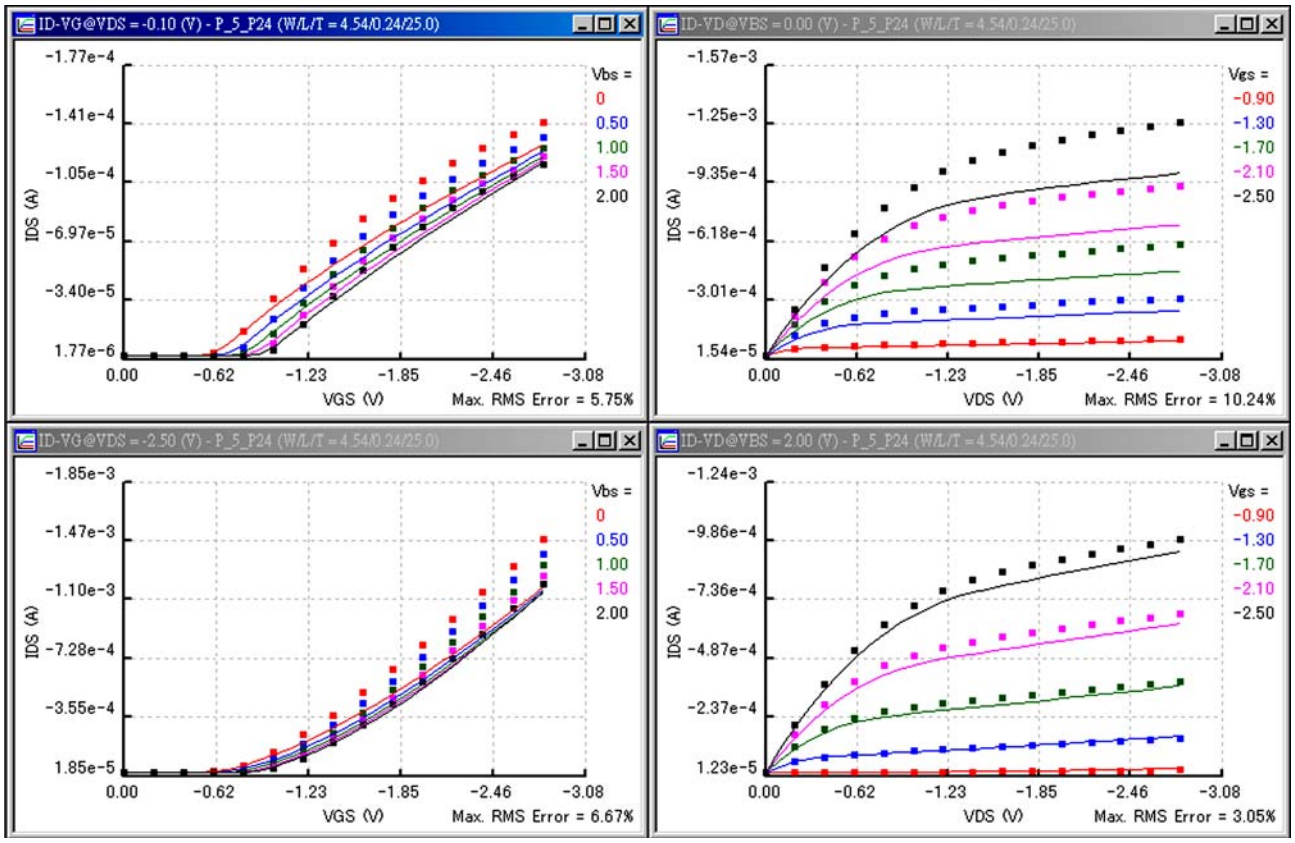

Fig. 14. The 100th generation of extraction process.

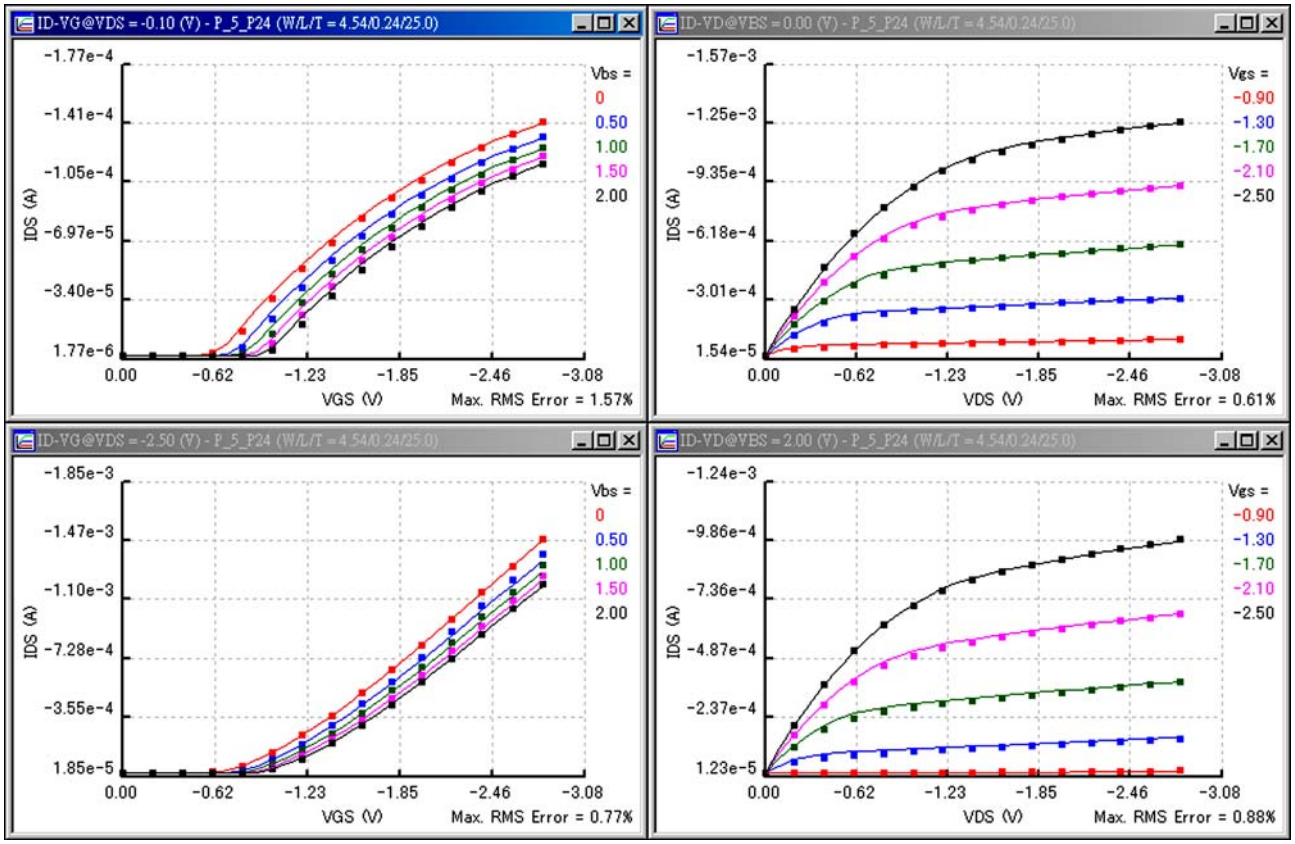

Fig. 15. The final evolution to reach the global result.

I–V curves with applying weight function achieve the target I–V curves rapidly, and it has a good evolution behavior. The importance of weight function introduced here not only redirects the evolution trend to better direction but also reduces the searching space in this multiobjective evolution problem, where the efficiency can be obtained.

Table 2 lists a comparison of score and time cost with respect to the different population sizes. In the comparison, the other parameters are fixed and the number of generations is equal to 1000 and 2000. We find out that the score convergence behavior cannot be improved anymore if the population size is too small. On the other hand, the result shows that the huge population size does not significantly affect the score even the extra time elapsed. In our simulation, a population size equals to 75 is suggested for the model parameter extraction of advanced CMOS devices. Because it maintains better evolutionary tendency and does not increase the time cost significantly.

Table 3
A list of the extracted BSIM3v3 parameters for the P-MOSFET with $L/W = 0.24/4.54$ [μm/μm]

Name	Value	Name	Value
V_{th0}	−0.54966545	k_1	0.622128342
k_2	−0.0649642599	k_3	0
D_{vt0}	0	D_{vt1}	0
D_{vt2}	−0.032	D_{vt0w}	0
D_{vt1w}	0	D_{vt2w}	−0.032
N_{lx}	0	K_{3b}	0
V_{sat}	94,750.9048	U_a	−2.8465687e-010
U_b	2.63994867e-018	U_c	4.01068575e-011

In addition, Fig. 8 shows the fitness score convergence behavior for multiple I–V curves evolution with different mutation rates, where the survival rate used in this testing is equal to 0.5. We note that generations increase, the results suggest that the high mutation rate which equals to 0.5 keeps the population diversity and finally has better evolutionary results. Fig. 9 is the fitness score convergence behavior vs the number of generations with respect to different survival rates for each chromosome, where the mutation rate is equal to 0.5. The survival rate indicates how many chromosomes should be preserved to next generation. Our results suggest that less survival rate has better convergence behavior. According to our experience, most chromosomes that have good fitness score are generated from mutation. For a deep-submicron N-MOSFET, there are more than 4 different sets of families of I–V curves should be characterized, we further develop an adaptive sampling scheme to accelerate the simulation process and extracted procedure.

Fig. 10 demonstrates our examination for the effect of applying sampling strategy. We compare the time that the average error reached 5% for different sampling steps. The sampling steps equal to 1 means no sampling strategy is applied. This figure shows that the sampling strategy pro-

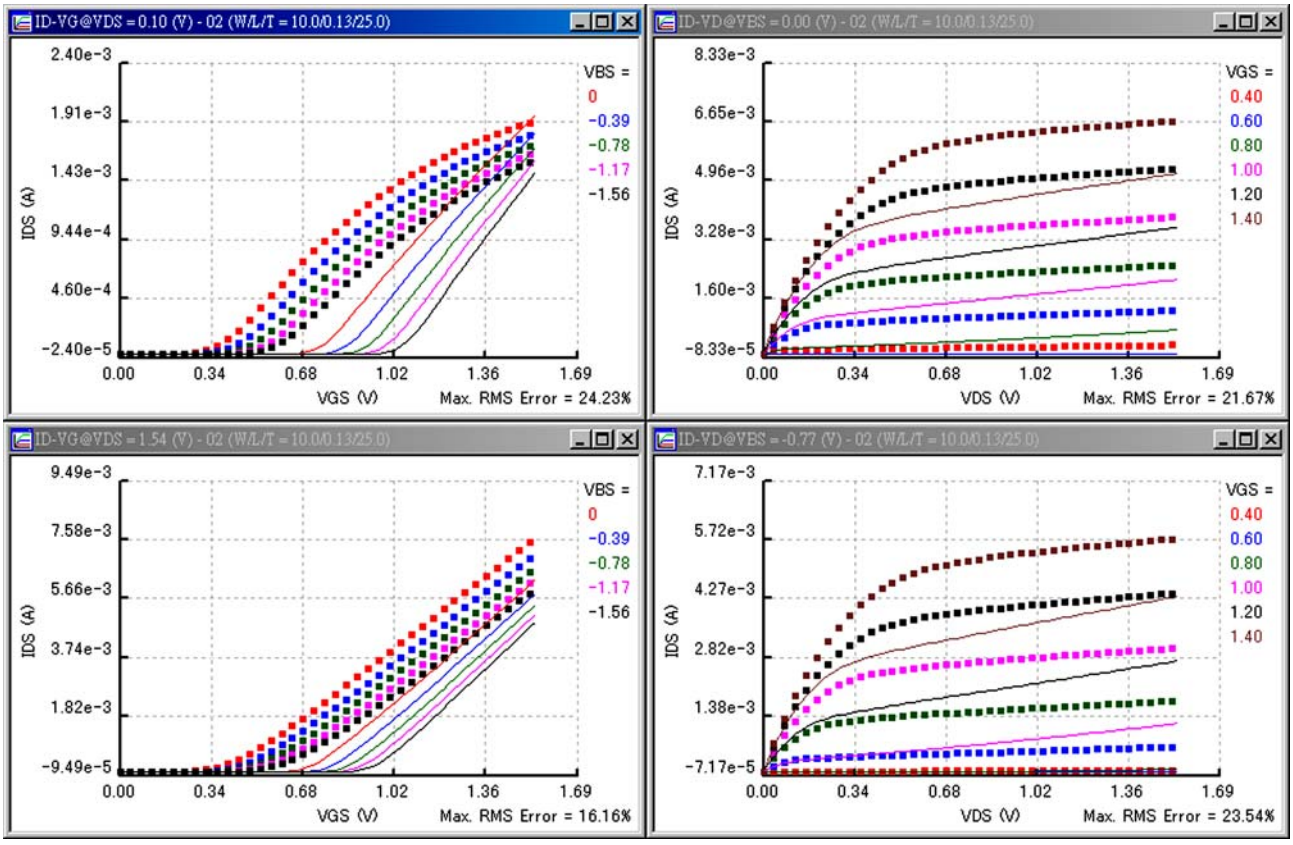

Fig. 16. The first generation of extraction process.

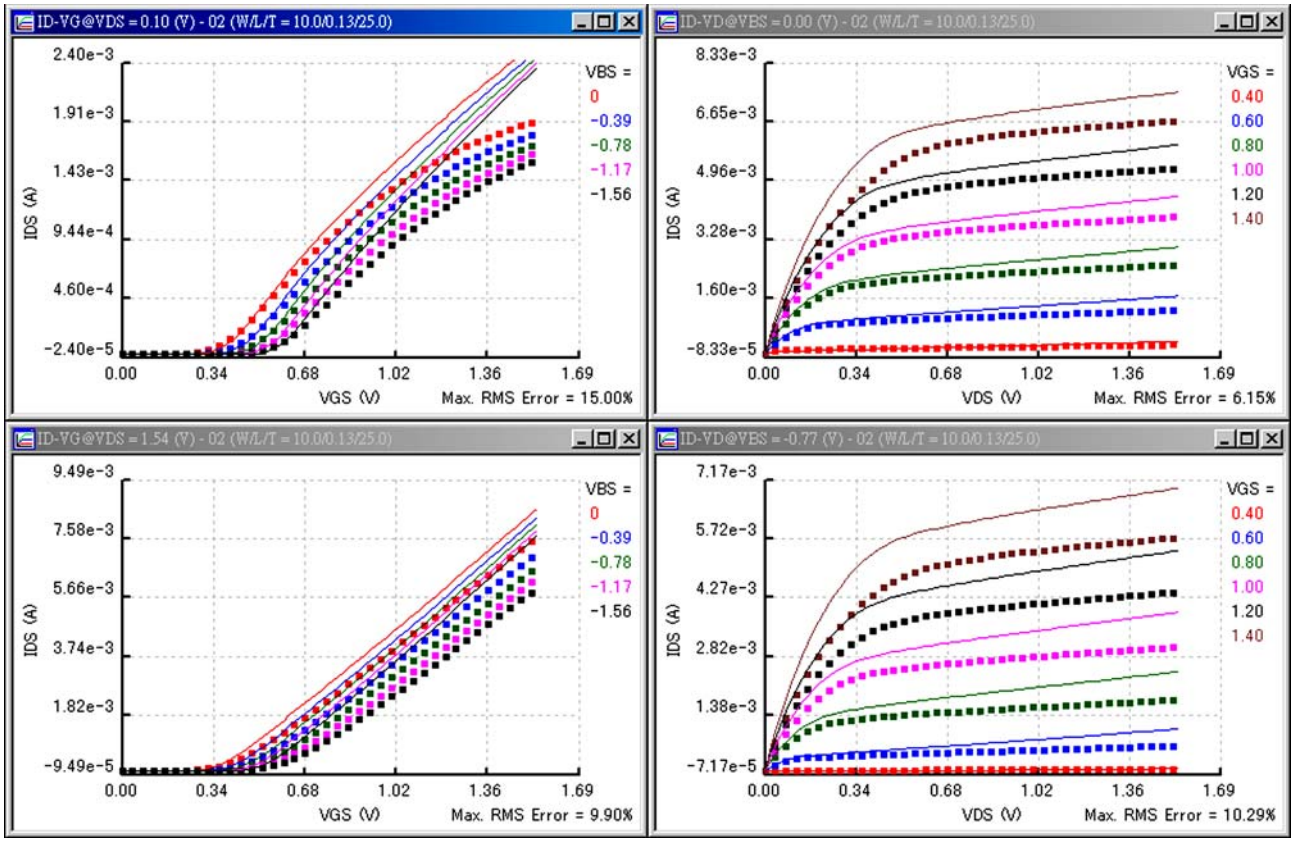

Fig. 17. The 100th generation of extraction process.

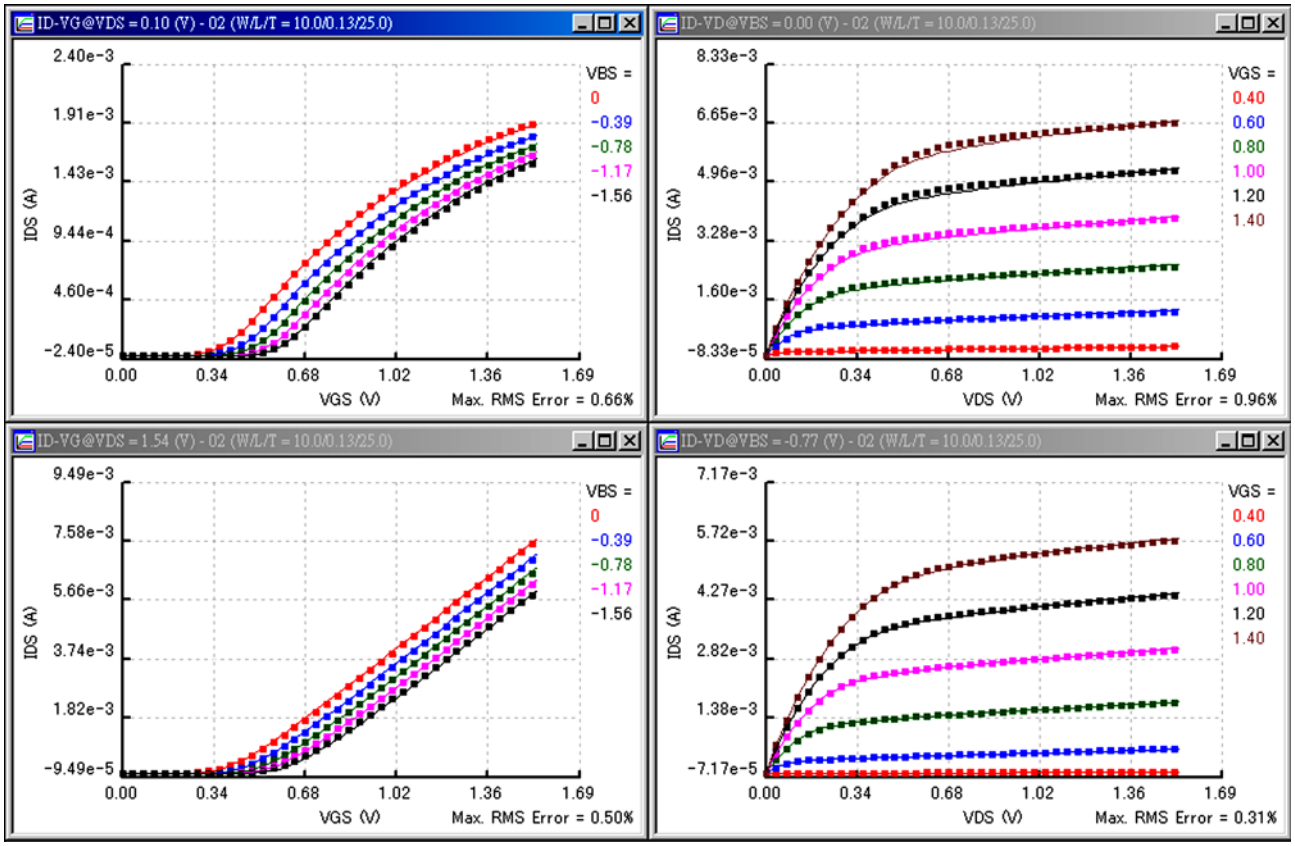

Fig. 18. The final evolution to reach the global result.

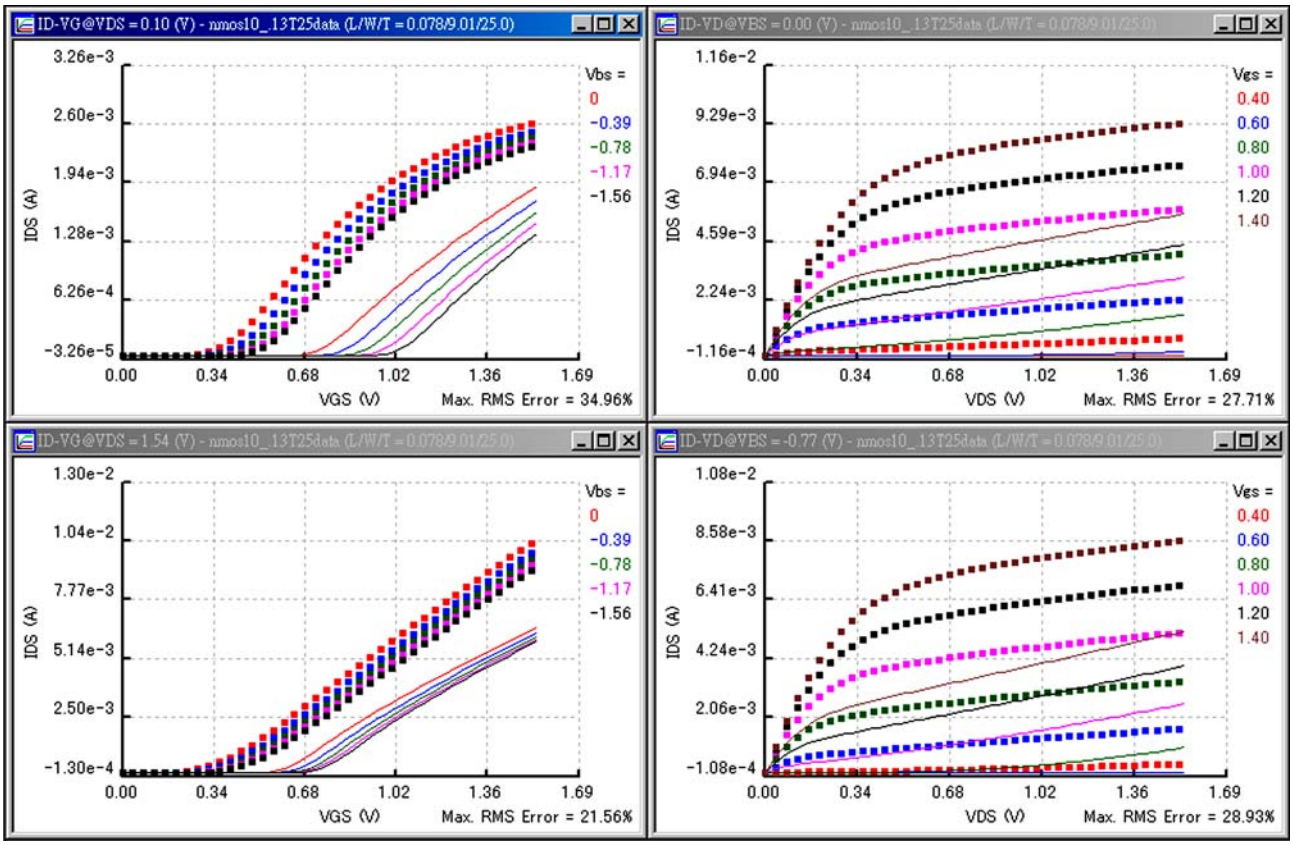

Fig. 19. The first generation of extraction process.

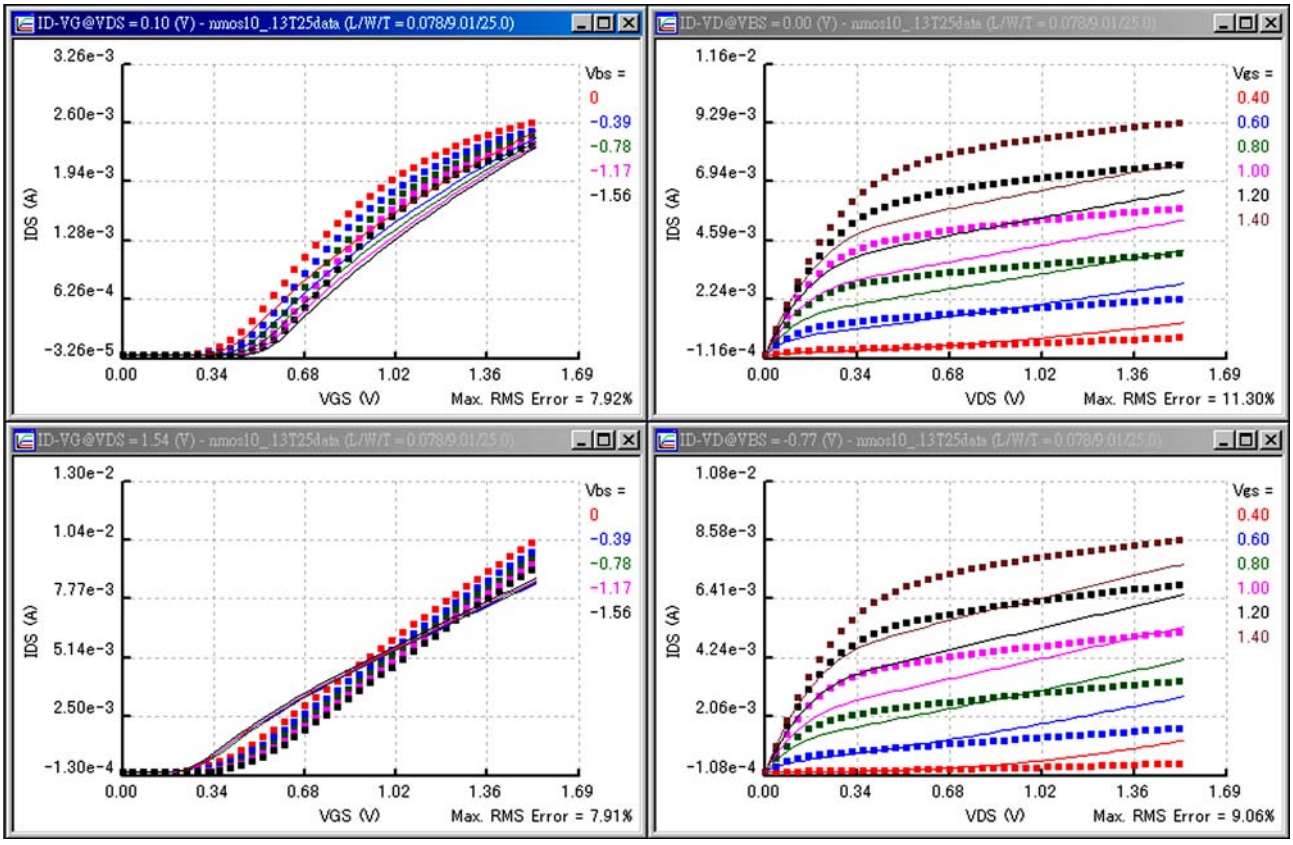

Fig. 20. The 100th generation of extraction process.

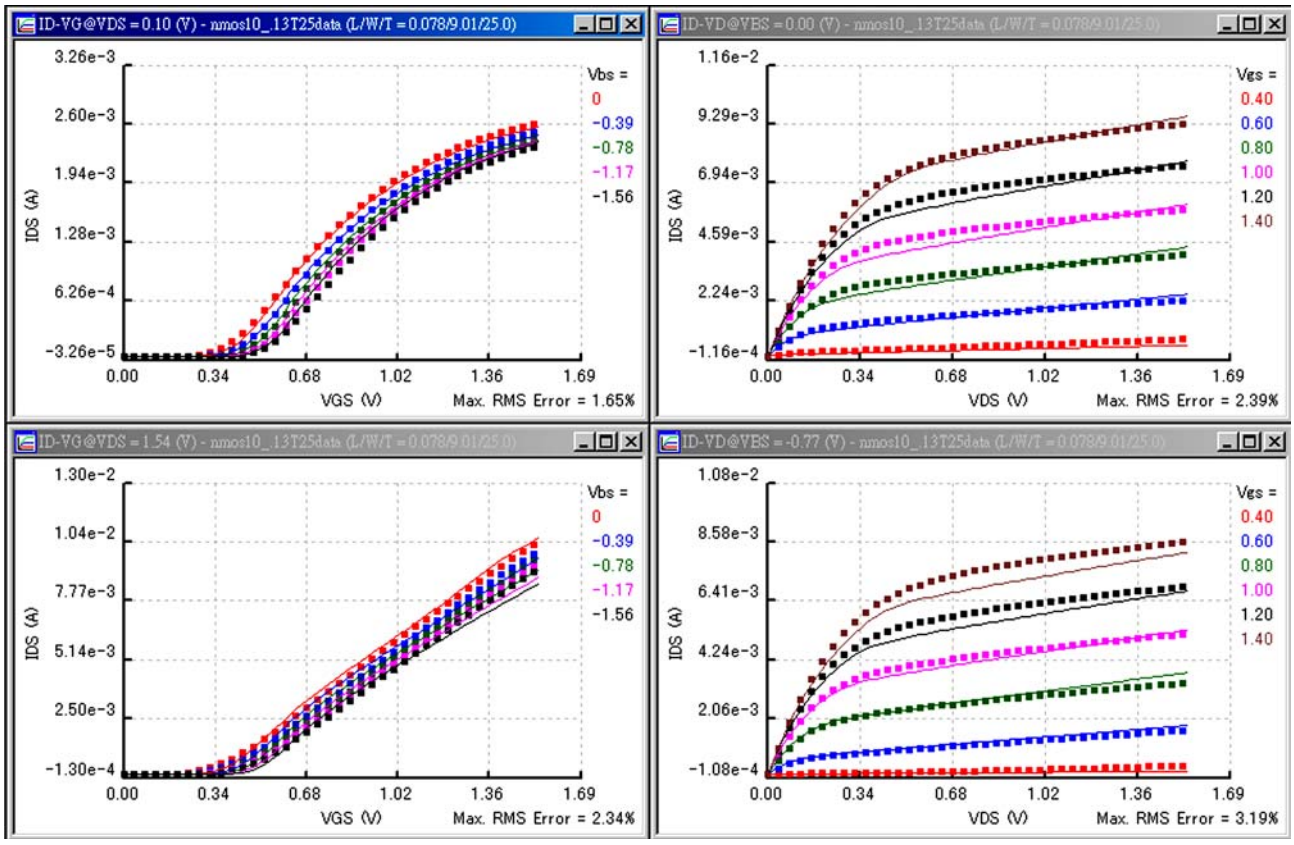

Fig. 21. The final evolution to reach the global result.

vides a way to reduce the evolution time. Fig. 11 shows a comparison of evolutionary behaviors with and without applying renew operator. Mathematically, parameter extraction of the BSIM3v3 model is a multi-dimensional optimization problem. Existence and uniqueness of solution is still an open problem. It is difficult to find the global solution using GA without applying special genetic operators. As shown in Fig. 11, the renew operator will be triggered while evolutionary trend was trapped into local optimal, and better evolutionary results can be obtained eventually. All settings are with the best conditions when we perform the tests as shown in Figs. 10 and 11, respectively.

As shown in the following figures, we apply our developed extraction prototype, shown in Fig. 12), to extract the parameter for the fabricated P-MOSFET with $L/W = 0.24/4.54$ [μm/μm] and N-MOSFET with $L/W = 0.13/10$ and 0.078/9.01 [μm/μm], respectively. The extraction is tested on a personal computer (Pentium IV 2.5 G CPU with 512 MB RAM) running with the Linux operation system. Fig. 13 shows the first generation of the extraction in the P-MOSFET. Figs. 14 and 15 are the generations of the 100 and the final evolution process. Table 3 partially lists extracted BSIM3v3 parameters for a global model of the 0.24 μm P-MOSFET, where the notation is the same with the BSIM3v3 [19]. Similarly, the Figs. 16–21 show the extraction process of the 0.24, 0.13, and 0.078 μm N-MOSFETs, respectively. Tables 4 and 5 partially list extracted BSIM3v3 parameters. The CPU time taking on these extractions is less than 300 second. We note that this computational technique has been tested success-

Table 4
A list of the extracted BSIM3v3 parameters for the N-MOSFET with $L/W = 0.13/10$ [μm/μm]

Name	Value	Name	Value
V_{th0}	0.342369724	k_1	0.334546475
k_2	0.000124829272	k_3	0
D_{vt0}	0	D_{vt1}	0
D_{vt2}	−0.032	D_{vt0w}	0
D_{vt1w}	0	D_{vt2w}	−0.032
N_{lx}	0	K_{3b}	0
V_{sat}	98,840.4986	U_a	1.23289835e-009
U_b	1.66640106e-018	U_c	2.29199308e-010

Table 5
A list of the extracted BSIM3v3 parameters for the N-MOSFET with $L/W = 0.078/9.01$ [μm/μm]

Name	Value	Name	Value
V_{th0}	0.357405144	k_1	0.436230858
k_2	−0.0743034512	k_3	0
D_{vt0}	0	D_{vt1}	0
D_{vt2}	−0.032	D_{vt0w}	0
D_{vt1w}	0	D_{vt2w}	−0.032
N_{lx}	0	K_{3b}	0
V_{sat}	95,364.9514	U_a	−7.91330757e-010
U_b	7.042222e-018	U_c	5.15594885e-010

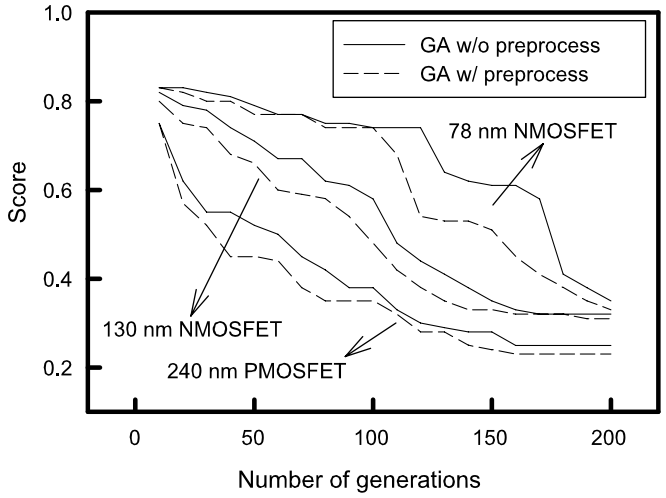

Fig. 22. A comparison of score convergence with and without preprocess for different VLSI devices.

fully with more than 20 nanoscale MOSFETs to perform a complete global parameter extraction. To explore the global parameter of nanoscale MOSFETs, the simulation model has also been extended to include more advanced the BSIM4 model. The extraction capability has been verified with the 90 and 65 nm MOSFETs. Fig. 22 shows the fitness score convergence behavior for multiple I–V curves evolution with or without preprocess and all settings are with the best conditions in this test. From engineering point of view, preprocess finds out some physical quantities that can be derived from measured data such as V_{th}, g_m, etc. GA can take these quantities into consideration when examining the physical meanings of the extracted parameter. As shown in Fig. 22, GA with preprocess has better convergence behavior. However, the difference becomes small when evolution increases.

5. Conclusions

In this paper, we have proposed an intelligent parameter extraction technique for advanced VLSI device modeling. Based on the exponential type weight function, the renew operator, and the adaptive sampling strategy, this automatic optimization approach for deep-submicron and nanoscale MOSFET devices have successfully been developed and implemented. The integrated parameter extraction prototype is mainly relied on the intelligence of floating points based GA method. Numerical results, fitness score, and convergent behavior for different deep-submicron and nanoscale CMOS devices have comprehensively been presented to show the accuracy and efficiency of the method. This GA-based computational method for advanced VLSI device characterization can be generalized to perform, such as thin-film transistor parameter extraction, and optimization of analog and high frequency circuits [22]. By a concept of model re-use, our approach benefits optimal design of system-on-a-chip. Parallel computation on a PC-based Linux cluster is under implemented for an acceleration of the evolution. Integration of this pure GA approach with other optimization methods, such as numerical optimization technique and neural network algorithm becomes more challenge task. Such hybrid methodology may provide more flexible approach to advanced CMOS model parameter extraction.

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