Sub-1 V Input Single-Inductor Dual-Output (SIDO) DC–DC Converter With Adaptive Load-Tracking Control (ALTC) for Single-Cell-Powered Systems

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***Abstract*—In this paper, a sub-1 V input single-inductor dual-output (SIDO) dc–dc converter with an adaptive load-tracking control (ALTC) technology is proposed for single-cell-powered portable devices. Having a minimal number of switches and an optimum current sequence, the proposed ALTC technique adaptively and accurately adjusts storage energy in the form of inductor current according to the actual load condition, without wasting surplus charge and without increasing cross regulation. Moreover, a current-mode ring oscillator with a self-bias current source circuit, in place of the conventional start-up ring oscillator, is proposed to produce a nearly constant system clock for the requirement of sub-1 V start-up procedure. Because the proposed current-mode ring oscillator operates between the start-up process and steady state of the SIDO dc–dc converter, its simplified design efficiently addresses the high switching frequency losses at sub-1 V start-up procedure, reducing chip area and power consumption. The proposed sub-1 V input SIDO dc–dc converter was fabricated via Taiwan Semiconductor Manufacturing Company 0.25 μm 2.5 V/5 V Bipolar-CMOS-DMOS process, and the experimental results show high efficiency of 92% with a good cross regulation smaller than 10 mV.**

***Index Terms*—Adaptive load-tracking control (ALTC) technique, dc–dc converter, single-inductor dual-output (SIDO) self-bias current source (SBCS) circuit, single-cell-powered systems, sub-1 V input.**

I. Introduction

MINIATURIZATION and low-power consumption are essential features of portable devices; these devices are expected to have small volume and long battery life [1]. To achieve these advantages, single-cell-powered systems that scale down the supply voltage is one effective solution. In particular, the AA- and AAA-size nickel-based rechargeable batteries, having high capacities and 1.2-V terminal potentials, are widely and conveniently applied for use in portable devices. However, the terminal potential decreases below 1 V when the battery delivers its stored energy to a portable device. Small-input battery voltage swings cause analog circuitries to become more sensitive to noise, signal perturbation, and ground bounce [2], [3]. For example, all load conditions detected from multiple output terminals can determine the exact inductor current level. The accuracy deteriorates, thus the output-regulation further worsens. Furthermore, the headroom voltage of the control circuit is limited by the battery and becomes a critical design issue in the single-cell-powered system. As illustrated in Fig. 1, a portable device commonly composed of a variety of submodules can provide several functions, such as LED backlight, liquid crystal display (LCD) monitor, and several signal-processing utilities. For basic power management, the distributive voltage and current-control methodology are needed to increase power efficiency in order to extend the battery life. As a result, the design of power management IC needs to contain several switching converters with different conversion ratios and some low-dropout (LDO) regulators to provide multiple output voltages to address the requirements of portable devices. Unfortunately, several external inductors and capacitors are needed and occupy a large area on the printed circuit board (PCB). These are not consistent with the features of miniaturization and low-power consumption of portable devices [4].

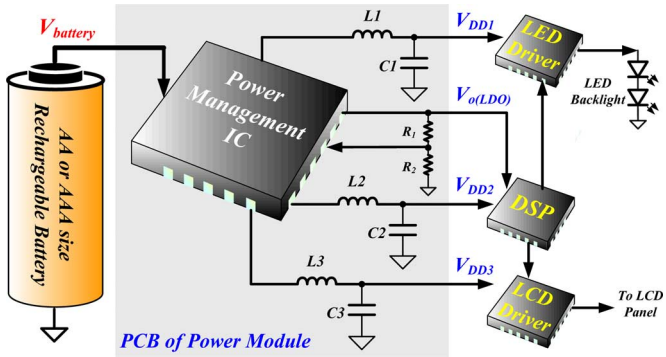

Fig. 1. Applications of a low-voltage input power converter.

In order to effectively reduce the number of external inductors, the design of a single-inductor multiple-output (SIMO) dc–dc converter was presented for application to portable devices [4]–[6]. The design challenges of the SIMO converter include the reduction of the number of power switches, conduction loss, switching loss, and cross regulation. A lesser number

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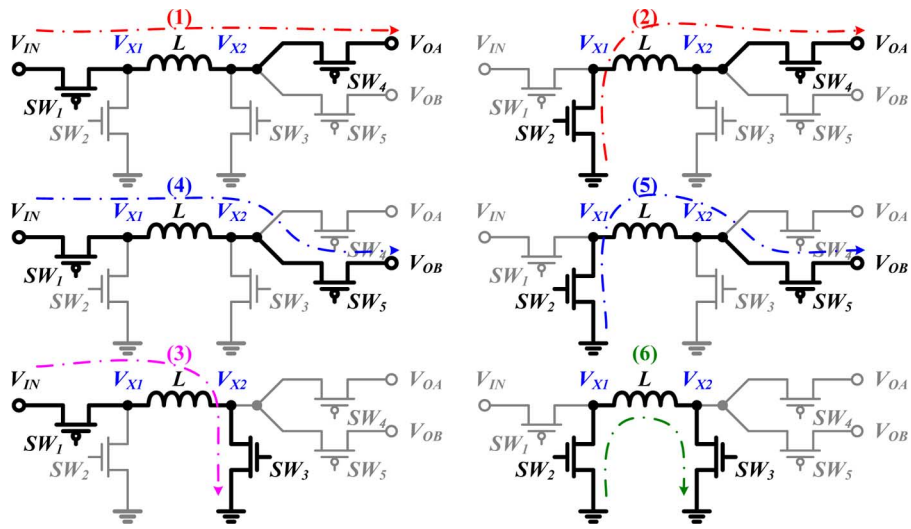


Fig. 2. Operating current paths of SIDO dc–dc converter.

of power switches can reduce the silicon area and switching loss. Less conduction and switching losses can improve the power-conversion efficiency. Having reduced cross regulation ensures a minimized crosstalk effect between these output terminals through the use of a single inductor. There are many design methodologies proposed to achieve some of these requirements; however, it is difficult to address all the requirements at the same time. Particularly, the design needs to involve the sub-1 V characteristic in the single-cell-powered system.

Woo *et al.* [5] proposed a freewheeling current feedback as a current-control method to regulate multiple boost output voltages without any buck output voltages. The freewheeling current level is dynamically adjusted cycle by cycle according to the load condition. Since the freewheeling current is monitored and compared to a reference in order to increase or decrease energy in the inductor, the main control loop of converter can indirectly detect an instantaneous load condition of each output without sensing each output load condition. As a result, the inductor current can be kept at a level adequate enough to react to any transient load response. Furthermore, the PI compensation only needs to be applied on the current loop of the freewheeling adjustment, thereby reducing the external compensation components. Unfortunately, the transient response is slowed down due to the slow adjustment of the freewheeling current, and thus, the cross regulation becomes worse due to low system bandwidth.

In order to provide different output types simultaneously, the conventional single-inductor dual-output (SIDO) dc–dc converter, which is shown in Fig. 2, uses five switches and one external inductor to provide one buck output and one boost output. Therefore, the power management IC of portable devices can simultaneously provide power sources higher or lower than the battery voltage with a small PCB area [6]. Furthermore, the SIDO dc–dc converter, proposed in [6], reorganizes the possible inductor current paths in conventional SIDO converter design to constitute an adaptive current-control sequence, and simultaneously provides buck and boost output voltages with the minimum number of power switches. Since the adaptive current-control sequence, proposed in [4], reorganizes the inductor current sharp and does not affect the regulation of each output, the number of power switches can be reduced to about three, as compared to five in the conventional design. Here, the small freewheeling power switch is not counted. Having a reduced number of power switches decreases the conduction and switching losses, thus increasing the power-conversion efficiency to about 90%. Although this design increases power efficiency, it also induces other problems. The serious cross regulation that occurs in the delivery power of buck output is larger than that of boost output and the complex control circuit becomes the major issue. In this respect, the design challenge of the SIDO converter becomes more difficult, aiming to ensure minimized cross regulation and provide multiple buck and boost output voltages with small output ripples in the single-cell-powered system.

This paper presents a sub-1 V SIDO dc–dc converter with the proposed adaptive load-tracking control (ALTC) technique to provide one buck and one boost output voltages, which operates with AA- and AAA-size rechargeable batteries. Minimized cross regulation can be ensured without being affected by small input voltage headroom. The conduction and switching losses, large start-up current, and disordered power-on sequence can be further reduced due to the low-voltage operation. As a result, the proposed SIDO converter can still operate under sub-1 V input battery voltage; therefore, miniaturization and low-power consumption can be achieved in a single-cell-battery-powered system. The organization of this paper is as follows. Section II describes the structure and the controlling sequence necessary to achieve high efficiency and guarantee system stability. Section III describes the proposed ALTC technique for minimum cross regulation. Section IV describes the implementation of the proposed SIDO circuit. Section V shows experimental results, and finally, conclusions are made in Section VI.

TABLE I
SPECIFICS OF OPERATION CURRENT PATHS

Path	1		2	3	4		5	6
Output	V_{OA}		V_{OA}	$V_{OA,B}$	V_{OB}		V_{OB}	-
Action	Deliver		Transfer	Store	Deliver		Transfer	Freewheel
Function	buck	boost	buck	boost	buck	boost	Buck	Reserve
Sign	+	-	-	+	+	-	-	-
Slope, m_i	$\frac{V_{IN}-V_{OA}}{L}$		$\frac{V_{OA}}{L}$	$\frac{V_{IN}}{L}$	$\frac{V_{IN}-V_{OB}}{L}$		$\frac{V_{OB}}{L}$	
HS- MOS	SW_1, SW_4		SW_4	SW_1	SW_1, SW_5		SW_5	-
LS- MOS	-		SW_2	SW_3	-		SW_2	SW_2, SW_3
P_D	$2P_{HS}+2P_C$		$P_{HS}+2P_C$	$P_{HS}+2P_C$	$2P_{HS}+2P_C$		$P_{HS}+2P_C$	$2P_C$

HS-MOS: high-side MOSFET and LS-MOS: lo-side MOSFET.
P_D: power dissipation, $P_{\rm HS}$: high-side switching losses, and P_C: conduction losses.

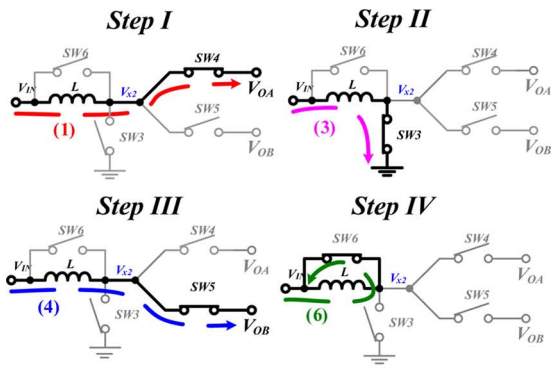
II. CURRENT-CONTROLLING SEQUENCE WITH MINIMIZED SWITCHES FOR HIGH POWER EFFICIENCY AND SYSTEM STABILITY

Only one cell serves as the energy supply source in single-cell-powered portable devices. In order to propose an energy delivery topology that can produce one buck and one boost output voltages with minimum power loss, the structure of the conventional SIDO dc–dc converter, as depicted in Fig. 2, is usually used to analyze the inductor current paths, segment current slope, and fundamental control methodology [6]. Because the inductor current I_L of the SIDO converter indicates the energy delivery and transfer status, six current delivery paths listed in Fig. 2 and Table I can be used to constitute the desired inductor current waveform during one switching cycle. As shown in Fig. 2, when the high-side (HS) MOSs SW_1 and SW_4 turn ON, current Path 1 is created and the output terminal V_{OA} is connected to supply the voltage. In the meantime, energy is delivered to the output terminal V_{OA} and the current slope can be calculated by the equation $(V_{\rm IN}-V_{OA})/L$. If output V_{OA} is lower than supply voltage $V_{\rm IN}$, then the converter is a buck converter, and the current slope is positive. On the contrary, if output V_{OA} is higher than supply voltage $V_{\rm IN}$, then the converter is a boost converter, and the current slope is negative. Moreover, the power dissipation P_D can be determined by the combination of two HS-switching loss $P_{\rm HS}$ and two conduction losses P_C. In comparison with the behavior of current Path 1, current Path 4, which delivers energy to output terminal V_{OB}, exhibits the same characteristics. Once the output terminals get enough energy from a supply source, current Path 1 expires. Then, as shown in Fig. 2, the HS-MOS SW_4 and the low-side (LS) MOS SW_2 turn ON. Path 2 is created to transfer storage energy to output terminal V_{OA}. Since the current paths connect the output terminals to ground, it has a negative current slope, as determined by the equation $(V_{OA})/L$. The LS-switching loss can be ignored because the crossover voltage of LS-MOS is zero during the switching transient. Therefore, the power dissipation of Path 2 is counted as one HS-switching loss and two conduction losses. Similarly, Path 4 exhibits the same performance for output terminal V_{OB}. As illustrated in Fig. 2, there are two special current paths Path 3 and Path 6, which are used to rapidly store and hold energy. When the output terminals of the SIDO converter require more energy from the supply source to boost output voltage level, the HS-MOS SW_1 and LS-MOS SW_3 are turned on to connect the inductor with supply source and ground. It generates a positive current slope $V_{\rm IN}/L$ and rapidly stores energy in the form of inductor current. If the output terminals have a reduction in demanded energy, current Path 6 keeps the storage energy of the inductor in. The LS-MOSs SW_2 and SW_3 are turned on to form an inner current loop in the SIDO converter without delivering energy to output terminals. Therefore, the power dissipation is only in the two conduction losses of LS-MOSs.

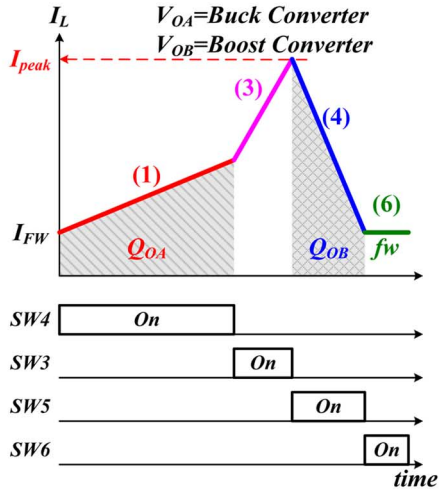
Six current delivery paths can be simply classified into two categories. Current delivery paths that can increase the inductor current level belong to the first category. Current delivery paths that can decrease the inductor current level belong to the second category. This classification is shown by the symbols "+" and "−" in Table I. Depending on the increase or decrease of the inductor current level, the system stability can be guaranteed if the inductor current level can be kept constantly below the desired current peak current level $I_{\rm peak}$. As a result, the combination of the six current delivery paths can determine the current-controlling sequence. Furthermore, in order to react to fast load-transient response, the energy in the inductor will not be decreased to zero through the freewheeling path. With the existence of the freewheeling stage, which is composed by Path 6, the system order is reduced to one and the compensation can be simplified to PI compensation. Therefore, the system bandwidth can be extended without being limited, unlike in previous literature [7], [8].

According to the demand of one buck and one boost output voltages in the SIDO converter, it follows that Paths 1, 3, and 4 must be kept in the structure [4]. Therefore, the transistors SW_3, SW_4, and SW_5 are necessary. The transistors SW_1 and SW_2 can be removed to reduce the number of the power switches. The freewheeling path disappears with the removal of transistor SW_2. Therefore, a small transistor SW_6 is added to connect the two terminals of the inductor to form a freewheeling path. According to the reorganized structure, the function of current paths needs to be clearly defined. Paths 1 and 4 can respectively deliver energy from supply source to output terminals V_{OA} and V_{OB}. Path 1 increases the inductor current level, but Path 4 decreases the inductor current level, as we let V_{OA} be the buck terminal and V_{OB} be the boost terminal. The difference between Paths 1 and 3 is the increasing rate of the inductor current level. Path 3 works better than Path 1 if the inductor needs to rapidly increase without affecting output terminals. As a result, the current-controlling sequence becomes Path 1, Path 3, Path 4, and Path 6, as shown in Fig. 3(a).

The adaptive controlling sequence of the previous work [4], as shown in Fig. 3(b), is used to properly regulate two output voltages. At the beginning of the switching period, Path 1 turns ON and delivers energy to buck output V_{OA}. The inductor current simultaneously increases according to the listed current slope of Table I. Once the V_{OA} gets enough energy Q_{OA} from the supply source, the controller ends Path 1 and turns ON Path 3. This is to increase inductor current to the load-dependent peak-current control (LDPCC) level $I_{\rm peak}$, which is proportional to the load condition of two output terminals and is determined by the LDPCC circuit in [4]. For the demand of boost output,



(a)



(b)

Fig. 3. (a) LDPCC controlling sequence in [4] and (b) the inductor current waveform of LDPCC controlling sequence.

Path 3 expires when inductor current is higher than the LDPCC level $I_{\rm peak}$, and Path 4 turns ON to deliver the required energy Q_{OB} to boost output. As the boost output acquires enough energy, Path 4 expires and the extra inductor current is reserved by Path 6. Overall, the current sequence properly delivers the required energy to each output terminal and effectively controls the inductor current without unexpected value [9] to regulate output terminals. Therefore, the cross-regulation issues can be minimized. Besides, if the current-decreasing capability due to Path 4 is smaller than the current-increasing capability due to Path 1, the inductor current will continuously increase, thus causing the SIDO converter to become unstable. In order to minimize this risk, the output loading of the boost terminal must be kept higher than that of the buck terminal. The supply voltage of the controller is thus connected to the boost terminal to increase its output loading. As a result, the risk of being unstable, which has been analyzed in [4], is reduced. However, the situation of unbalanced loading certainly exists in various load application, and the risk of instability cannot be avoided if we only depend on the energy demand of the controller. The hysteresis mode, which has been proposed, simultaneously turns ON the transistors SW_1 and SW_6 to avoid increasing the inductor

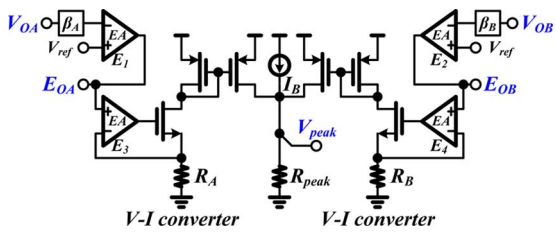


Fig. 4. Proposed LPDCC circuit in [4].

current with unbalanced loading. Furthermore, the buck terminal is regulated by a hysteresis voltage window at the cost of a large voltage ripple. The proposed method in this study, which increases the loading of boost terminal, alleviates the design constraint of the previous design [4], thus, further reducing the output ripple.

III. Proposed ALTC Technique for Reduced Cross Regulation and Power Consumption

As discussed earlier, the surplus energy stored in the inductor affects the performance of cross regulation and power consumption. The LDPCC circuit, which was proposed in [4], can dynamically adjust peak current level $I_{\rm peak}$ to determine the surplus energy in the inductor. However, the inductor current level is not well defined due to the function of summation in the design of the LDPCC circuit. In this respect, an ALTC technology is proposed to accurately predict the peak current level and minimize cross regulation and power consumption. The detailed analyses of LDPCC and ALTC technology are described in the following sections.

A. LDPCC Circuit

In accordance with the proposal of previous work [4], the LDPCC level $I_{\rm peak}$ needs to follow the load variation and then achieve high power efficiency. At light loads, a value of bias current I_B ensures the small freewheeling current level, in order not to waste energy. The LDPCC circuit, as depicted in Fig. 4, uses two error amplifiers E_1 and E_2 to monitor two output load conditions. As a result, the error amplifiers' output signals E_{OA} and E_{OB} are converted to two current signals by the voltage-to-current (V–I) converters. The summation current, which is composed by the two current signals and one bias current I_B, is converted by resistor $R_{\rm peak}$ to a converted-signal $V_{\rm peak}$. And then, the converted-signal $V_{\rm peak}$ determines the LDPCC level $I_{\rm peak}$ and varies with load conditions. A minimum LDPCC level can be set by I_B to avoid zero-inductor current. For instance, a dip in one of the output terminals due to an increase in load current will increase the duty ratio and indirectly cause an increasing LDPCC level. As we know, once the disappearance of the freewheeling stage happens when a sudden load current rises from light to heavy and the load current exceeds the maximum power limitation, the stability and output regulation will be deteriorated, since the system order becomes two. The system stability cannot be guaranteed through the use of the PI compensation. Fortunately, the LDPCC technique can adaptively store suitable energy in the inductor to prevent the output from having a too

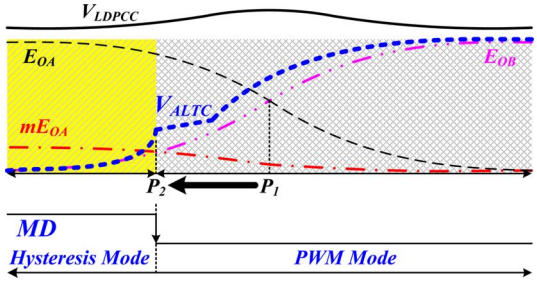


Fig. 5. Behavior of the proposed ALTC technique.

large transient dip voltage and ensure high power-conversion efficiency at light loads. Besides, the freewheeling period can be maintained in case of load variation after the adoption of the LDPCC technique. However, the LDPCC level is obviously not well defined due to the different weight of output voltage levels. As illustrated in Fig. 4, the LDPCC level $V_{\rm peak}$ directly converts from the output signals E_{OA} and E_{OB} of error amplifiers. In order to compare with the same reference voltage $V_{\rm ref}$, there have been different weight of the feedback ratios β_A and β_B in the SIDO converter. As discussed earlier, the directly converted information will induce an exceeding current level to control the storage energy. It contradicts the purpose, which achieves high power efficiency, of SIDO converter. In this respect, the ALTC technique has been proposed to solve this problem in the following section.

B. ALTC Technique for Solving the Exceeding Current Problem

In a nutshell, the SIDO converter uses two different ratios of feedback-divided resistors to regulate the two streams of output as one buck and one boost output voltages. The values of error amplifiers' output E_{OA} and E_{OB} indicate the load conditions of two output terminals and directly convert them to LDPCC level. Therefore, the problem of having an exceeding current occurs in the previous design. This easily causes higher freewheeling current, thus contradicting the requirement for power-conversion efficiency. Moreover, once the loading of buck output becomes higher than that of boost output, the increasing current level of Path 1 becomes higher than the decreasing current level of Path 4. The increasing inductor current causes serious cross regulation at the output terminals. A power detector circuit and delta-voltage generator in [4] has been proposed to address the current crowding issue and to switch on the hysteresis mode. At the hysteresis mode, Path 6 is used instead of Path 1 to regulate the buck output and output terminal V_{OA} regulated by a hysteresis voltage window. Therefore, the increasing current can be addressed. Although the current crowding issue is addressed, the complex design of the power detector and delta-voltage generator has a large chip area and high-power consumption. In this study, we take on the challenge of simultaneously addressing both the issues of exceeding current and current crowding, providing a simple and adaptive solution.

Fig. 5 illustrates how the load condition at the buck output changes from heavy to light, while the load condition at the boost output changes from light to heavy. The output signals E_{OA} and E_{OB} of error amplifiers reacts to the original load condition without correction. The summation of signal $V_{\rm LDPCC}$ always keeps at the same level and even increases slightly to a higher level. Obviously, the LDPCC level is over defined to control peak current level. In order to solve the problem of exceeding current, the ALTC technique is proposed to automatically determine the inductor current level through the weight of error amplifiers' output E_{OA} and E_{OB}. Therefore, a weighted value mE_{OA} is proposed to redefine the inductor current level, since the output voltages V_{OA} and V_{OB} have different values. The proportional ratio m is defined as the ratio of V_{OA}/V_{OB}. The weighted value mE_{OA} shifts the original crossover point P_1 to a new crossover point P_2 and indicates an accurate and suitable transition point of operation mode. Moreover, if the hysteresis mode is turned on, the buck output is regulated by a hysteresis window, thus not increasing the inductor current. The ALTC level thus needs to follow the demand of the boost output when operating in the hysteresis mode. Since the stored energy needs to be delivered to the boost output V_{OB}, the ALTC current adjusts according to the weight of error amplifiers' output E_{OB}. Once the required energy of the boost output is higher than that of the buck output, the operation mode of the SIDO converter switches to the pulsewidth modulation (PWM) mode. As a result, the ALTC current follows the two weights of error amplifiers' output mE_{OA} and E_{OB}, since the energy stored in the inductor needs to be delivered to the two output terminals V_{OA} and V_{OB}. Furthermore, the storage current of buck output V_{OA} can be delivered to the boost output V_{OB}. The summation current level between output signals mE_{OA} and E_{OB} is switched to indicate the ALTC level. Therefore, the real load condition can be indicated by the signal $V_{\rm ALTC}$, which will not result in an exceeding inductor current. Above all, the corrected weight of error amplifiers' output mE_{OA} and E_{OB} reflects the actual load condition. The crossover point P_2 can be used to define the boundary of hysteresis and PWM mode. This is easily implemented by a simple comparator circuit.

IV. Implementation of Proposed Sub-1 V SIDO Converter

The block diagram of the proposed sub-1 V SIDO dc–dc converter with the ALTC technique is illustrated in Fig. 6. Transistors M_N, M_F, M_A, and M_B constitute the minimum-switch structure in order to reduce the power loss and chip area. Output voltages are directly monitored by the ALTC controller and convert the load condition to the proposed ALTC level. The output signals of the ALTC controller connect to a charge reservation circuit, which was proposed in [4], to generate the duty cycle of each output terminal and detect the inductor current level. The charge reservation circuit synchronously records the delivered energy on the inner capacitors and uses this to compare with output signals of error amplifier and current sensor. The digitized control signal, which is converted by charge reservation circuit, is connected to a sequence controller. The output of the sequence controller is then converted by a fixed dead time driver to eliminate shoot-through current in case of switching issues and drives the power MOSFETs. During dead time

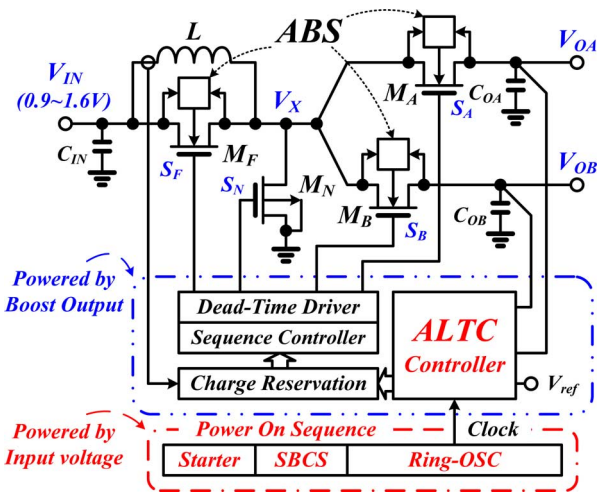


Fig. 6. Proposed structure of sub-1 V input SIDO dc–dc converter with ALTC technique.

operation, the voltage level of node V_X will be higher than the input voltage $V_{\rm IN}$ and the two output voltages V_{OA} and V_{OB}. It will result to a potential latch-up issue if the bulk voltage of p-type power MOSFETs does not connect to the highest voltage of its drain or source voltage. Hence, an adaptive body switch (ABS) circuit is proposed to decrease the possibility of leakage current and the potential latch-up problem of p-type power MOSFETs [6]. Once the input voltage $V_{\rm IN}$ is lower than 1 V at the start up of the SIDO converter, a reliable, stable, and low-quiescent current power-on sequence is required to judge the start-up performance. In this respect, a self-bias current source (SBCS) circuit is proposed to bias a current-mode ring oscillator in order to generate a nearly constant clock with the characteristic of high power supply rejection ratio (PSRR). The start-up procedure and design consideration of each block in the sub-1 V SIDO dc/dc converter are described in the following section.

A. Start-up Procedure for the Sub-1 V Operation

In order to achieve the sub-1 V operation, a low-voltage power-on procedure has been proposed, as shown in Fig. 7. The power-on procedure is divided into four stages: Stage 0 to Stage 3. In Stage 0, the converter is disabled, unless the supply voltage $V_{\rm IN}$ has been charged to the minimum operating voltage of SBCS circuit. When the condition of Stage 0 is satisfied, the power-on sequence then turns ON the power MOSFETs M_F and M_B to deliver energy to output terminal V_{OB}. The voltage of output terminal V_{OB} is ramped up to 90% of the supply voltage $V_{\rm IN}$ during Stage 1. Then, power-on procedure enters Stage 2, which turns ON the starter, the SBCS circuit, and the ring oscillator, according to priority. The generated clock signal *Clock* is used in boost terminal V_{OB} until the regulated voltage level reaches the 90% of the predefined voltage. At Stage 2, only the ring oscillator and driver are enabled; the open-loop control is used to regulate output voltage. In order not to exhibit an over-shot voltage during start-up transition, the clock has a duty cycle of 50%, with a limitation of twice the necessary supply voltage. When the voltage level of terminal V_{OB} is higher than

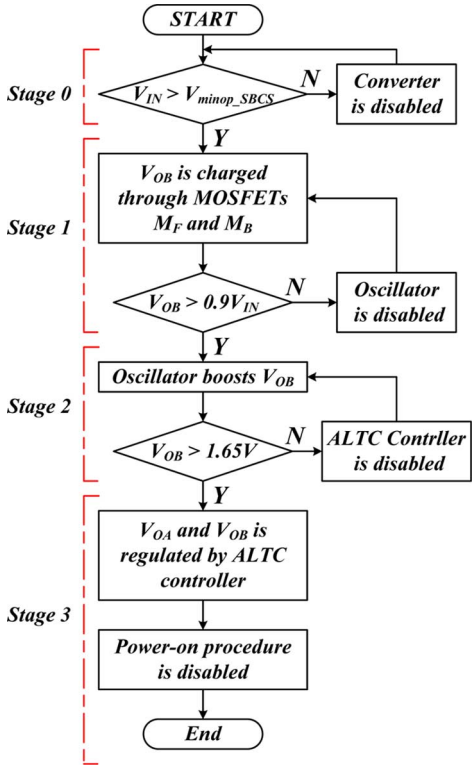


Fig. 7. Power-on procedure of sub-1 V input SIDO dc–dc converter with ALTC technique.

1.65 V, which is the 90% voltage level of the predefined voltage, the ALTC controller is enabled and added into the control loop to form a closed-loop control. At this time, the ring oscillator behaves as a system clock generator. The output terminals V_{OA} and V_{OB} are finally regulated by the ALTC controller to the defined voltage level. Therefore, the power-on sequence properly controls the converter to be modulated by the power-on procedure circuit and the ALTC controller until two output voltages successfully ramp up to the regulated levels. The power-on sequence is therefore an important part of sub-1 V operation.

B. Start-up Circuit and the Ring Oscillator With a SBCS

During the start-up period, an auxiliary ring oscillator necessary to generate a clock signal can initiate the operation, since the ramp-up input voltage is not high enough to ensure the correct closed-loop operation. In a conventional sub-1 V converter, the oscillating frequency of the auxiliary ring oscillator depends highly on the supply voltage deviation and operates at several megahertz, sometimes even at tens of thousands megahertz. Such a high switching frequency increases the possibility of latch-up and induces too much switching loss and may cause the start-up procedure to fail. Besides, the closed-loop normally operates when the main ring oscillator takes over the character of the auxiliary ring oscillator after the start-up procedure is finished. This shows that two oscillators are needed, and thus, the cost and the silicon area are increased. As depicted in Fig. 8, the proposed start-up circuit can solve certain design problems and guarantees the success of start-up procedure. In order to address

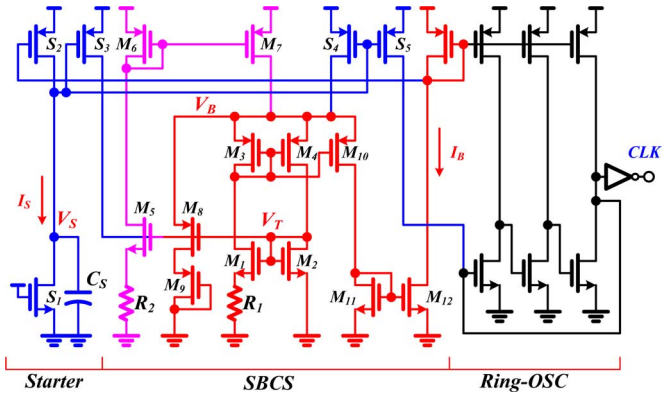


Fig. 8. Proposed SBCS circuit and ring oscillator.

latch-up and switching loss issues, as well as to simplify the design of oscillator, an SBCS circuit drives a current-mode ring oscillator to generate a nearly constant clock *CLK*. Transistors S_1–S_5 and capacitor C_S constitute a starter. At the beginning of Stage 2 of the power-on sequence, the voltage V_S is too low to turn ON the transistors S_3–S_5, the SBCS circuit starts when the supply voltage is higher than the threshold voltage of p-type MOSFET. A simple current mirror that is composed of transistors M_1–M_4 and a resistor R_1 is used to define the biasing current I_B. Transistors M_5–M_7 and the resistor R_2 constitute a self-bias loop to provide a preregulated voltage to supply the simple current mirror. Since the preregulated voltage V_B is clamped to a value of $V_T + V_{\rm GSP}$ and the threshold voltage V_T is independent of the supply voltage, a nearly constant bias current I_B is therefore generated to bias the current-mode ring oscillator without being affected by the supply voltage deviation. Furthermore, the oscillation frequency of current-mode ring oscillator depends on the bias current I_B and the threshold voltage V_T of the n-channel MOSFET (NMOS). Therefore, the SBCS circuit and the ring oscillator can attain high PSRR. The oscillation frequency will not increase to a higher value and switching loss can be reduced. The start-up procedure can also be guaranteed without being affected by the high-switching loss. Once bias current I_B is generated, a mirrored current I_S flows through the transistor S_2, pulls the value of V_S to a high level, and the start-up procedure ends. Here, the problems associated with a ring oscillator operated at high frequency and an extra regular oscillator are addressed and serious problems that were never pointed out in conventional designs can be solved [1]–[3]. The sub-1 V SIDO converter can be started and operated with low-power consumption.

C. ABS Circuit

A voltage spike still appears at node V_X in Fig. 6 even if a well-defined dead time is inserted during the switching transition. As a result, the voltage level at node V_X may be higher than the input voltage $V_{\rm IN}$ and the two output voltages V_{OA} and V_{OB}. Unfortunately, this will induce a potential latch-up issue because the bulk voltage of the p-type power MOSFETs is not connected to the highest voltage. The latch-up phenomena may damage the chip and cause function failure. Thus, an ABS

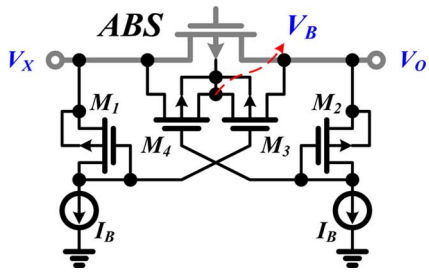


Fig. 9. Proposed ABS circuit in [10].

circuit is needed to connect the bulk terminal to the highest voltage. In previous ABS circuits [10], the complex circuit is used to distinguish which terminals have the highest voltage. This has the disadvantage of lowering the converter's performance and immunity to the latch-up phenomena, while at the same time inducing higher power consumption. In this paper, the ABS circuit depicted in Fig. 9 is proposed to address the possibility of current leakage and the potential latch-up problem of p-type power MOSFETs [6]. The ABS circuit with the simplest structure provides low-power consumption, high decision speed, and high accuracy of voltage comparison even if the source and drain voltages are nearly equivalent. In Fig. 9, transistors M_1 and M_2 are used to bias transistors M_3 and M_4 at the boundary of cutoff and inversion regions to improve the capability in order to determine which terminals has the highest performance. The transistors M_3 and M_4 work as two common-gate amplifiers. Once node V_X is higher than output terminal V_O, the transistor M_4 enters the inversion region and fully turns ON. The transistor M_3 enters the cutoff region and turns OFF entirely. The n-well voltage V_B of the p-type power MOSFET connects to node V_X. Contrarily, when output terminal V_O is higher than node V_X, the transistor M_3 fully turns ON and the transistor M_4 enters the cut-off region. The bulk node V_B is connected to output terminal V_O. Therefore, the ABS circuit can automatically select the highest voltage level between the drain and source terminals of a p-type power MOSFET. The potential of latch-up occurrence can be completely eliminated. Interestingly, the power consumption merely involves two biasing currents. The advantage of low-power consumption is achieved as compared to previous ABS circuits [10], [11].

D. ALTC Controller

According to the functionality of ALTC technique as shown in Fig. 5, the implementation of the ALTC circuit is illustrated in Fig. 10. The operational transconductance amplifier (OTA) g_{mA} converts the difference between the output voltage V_{OA} and the reference voltage $V_{\rm ref}$ to a current signal I_A. The weighted factors β_A and β_B come from the feedback-divided resistors. Similarly, current signal I_B is converted from the difference between the output voltage V_{OB} and reference voltage $V_{\rm ref}$ through the OTA g_{mB}. Current signals I_A and I_B can therefore be expressed as follows:

$$I_A = (\beta_A V_{OA} - V_{\rm ref}) g_{mA} \tag{1}$$

$$I_B = (\beta_B V_{OB} - V_{\rm ref}) g_{mB}. \tag{2}$$

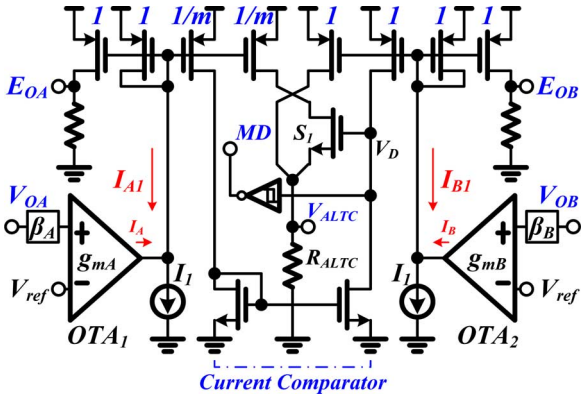


Fig. 10. Proposed ALTC Circuit.

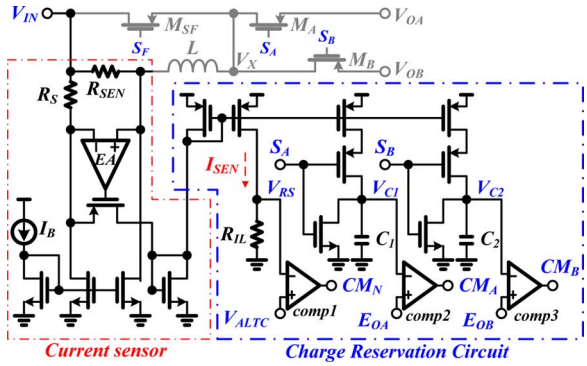


Fig. 11. Current sensor and the charge reservation circuits in [4] for controlling duty cycle of each output terminal.

Equations (1) and (2) indicate the load conditions of two output terminals V_{OA} and V_{OB}, respectively. Assume that the gm_A is equal to gm_B because of good layout matching considerations. The corrected ratio m defined as (3) can then be used to represent the relationship between the output voltages V_{OA} and V_{OB}. The bias current I_1 is used to define the minimum inductor current level and to avoid the negative current. Therefore, the converting currents I_{A1} and I_{B1} can be expressed as (4) and (5), respectively. The inductor current level $V_{\rm ALTC}$ is defined by (6), which is converted by the current mirrors and the resistor $R_{\rm ALTC}$

$$\beta_A V_{OA} = \beta_B V_{OB} \Rightarrow \frac{\beta_B}{\beta_A} = \frac{V_{OA}}{V_{OB}} = m \tag{3}$$

$$I_{A1} = I_1 - I_A = I_1 - (\beta_A V_{OA} - V_{\rm ref})\, g_{mA} \tag{4}$$

$$I_{B1} = I_1 - I_B = I_1 - (\beta_B V_{OB} - V_{\rm ref})\, g_{mB} \tag{5}$$

$$V_{\rm ALTC} = R_{\rm ALTC}\left(\frac{1}{m} I_{A1} + I_{B1}\right) \text{ when boost energy} > \text{buck energy}$$

$$V_{\rm ALTC} = R_{\rm ALTC} I_{B1} \text{ when boost energy} < \text{buck energy}. \tag{6}$$

The weighted current I_{A1}/m is used to adjust the energy of the buck output and relate to that of the boost output. At PWM operation, the energy of the boost output is larger than that of the buck output. The ALTC circuit selects the summation value as the storage energy in the inductor, which is shown in (6). As a result, the value of $V_{\rm ALTC}$ has a step wherein the SIDO converter enters PWM operation to ensure sufficient stored energy in the inductor. On the other hand, the hysteresis operation addresses the current crowding issue in the inductor. Thus, the buck output acquires energy through the turning-ON transistors M_F and M_A shown in Fig. 6, and will therefore not increase inductor current. The ALTC level is therefore necessary to determine the energy demanded of boost output; the value of $V_{\rm ALTC}$ is merely calculated by the product of I_{B1} and $R_{\rm ALTC}$. In Fig. 10, the current comparator is used to decide the operation mode, instead of the power comparator and delta-voltage generator in [4]. If I_{A1}/m is larger than I_{B1}, MD is set to high state and $V_{\rm ALTC}$ is decided only by I_{B1}. Contrarily, if I_{A1}/m is smaller than I_{B1}, MD is equal to low state, then $V_{\rm ALTC}$ is decided by the summation of I_{A1}/m and I_{B1}. Therefore, the crossover point P_2, as shown in Fig. 5, can indicate an accurate load condition. The boundary condition of the hysteresis mode is easily defined by the proposed ALTC technique without using numerous analog circuits. The exceeding current problem can also be improved.

E. Charge Reservation Circuit and the Current Sensor

As shown in Fig. 6, the charge reservation circuit receives the output signals of the ALTC circuit and current sensor. It then digitizes the received signal to the sequence controller to generate related inductor current. The current sensor is depicted in Fig. 11, and the sensing resistor $R_{\rm SEN}$ is set to 0.5 Ω to reduce power consumption. A large resistor R_S, which is N times the sensing resistor $R_{\rm SEN}$, is used to reduce the power consumption of current sensor [4]–[6]. In the ALTC technique, since the current sensor cannot be turned off during the whole switching period, the freewheeling switch M_F is connected between the input power source and the node V_X. This ensures that the operation of the current sensor can be maintained during entire switching period. However, the consequence of this is that the small sensing resistor $R_{\rm SEN}$ slightly decreases power efficiency during the switching period. Moreover, the ALTC technique can dynamically adjust the peak inductor level, and thus, improve power efficiency. According to the sensing resistor ratio, the sensing current $I_{\rm SEN}$ has $1/N$ times of the inductor current I_L. It is mirrored to charge the inner capacitors C_1 and C_2 of the charge reservation circuit, which is shown in Fig. 11. The voltage V_{RS} converts from sensing current $I_{\rm SEN}$ and the resistor R_{IL} is compared with the ALTC level $V_{\rm ALTC}$ to determine the operation period of Path 3. As a result, the energy stored in the inductor will be increased to the peak value defined by the ALTC technique. Moreover, the sensing current $I_{\rm SEN}$ is also used to determine the individual operation periods of the buck and boost output terminals. The inner capacitors C_1 and C_2 are used to monitor the buck and boost output voltages, respectively. The sensing current $I_{\rm SEN}$ flows into capacitor C_1 or C_2, to indicate the energy delivery condition of the buck or boost output voltage when the voltage level of S_A or S_B is changed from high to low. The voltages V_{C1} and V_{C2} on capacitors C_1 and C_2 are compared with the output signals E_{OA} and E_{OB} of the ALTC circuit, deciding the operation

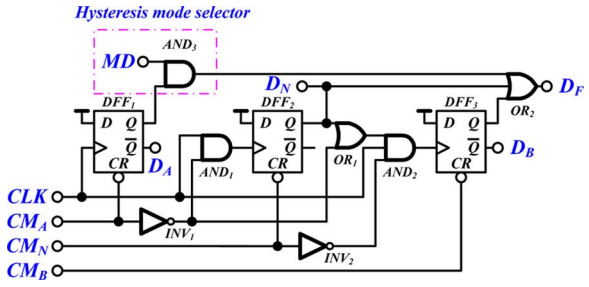


Fig. 12. PWM control logic generator and the mode switch controller.

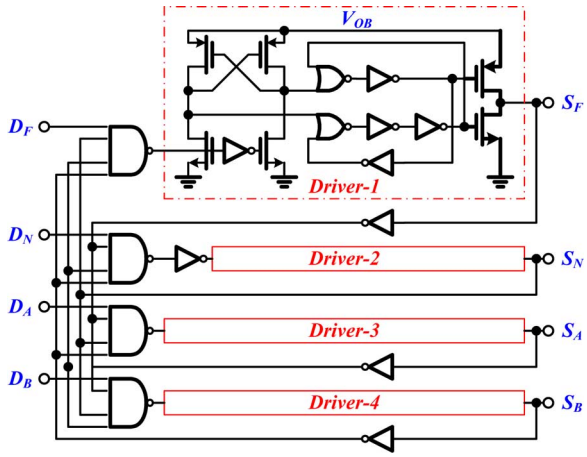


Fig. 13. Dead time driver.

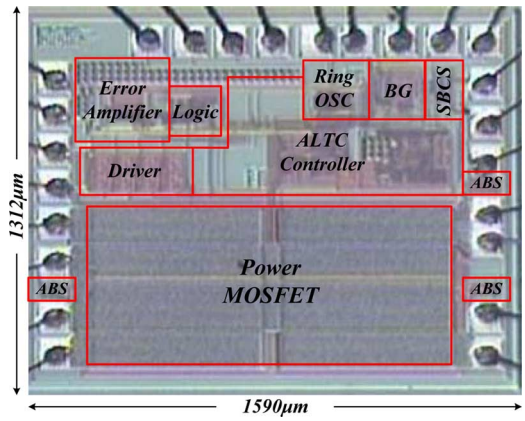


Fig. 14. Micrograph of proposed sub-1 V SIDO dc–dc converter with ALTC technique.

period for related current path. Once the voltages V_{C1} and V_{C2} are respectively larger than output signals E_{OA} and E_{OB}, the driving signals S_A and S_B, change from low to high and the inner capacitor is fully discharged. Thus, the charging time of inner capacitors C_1 and C_2 indicates the operation period of the related current path. As a result, the duty cycle of each output terminal can be determined by the voltages V_{C1} and V_{C2} on the inner capacitors C_1 and C_2, and the output signals E_{OA} and E_{OB}. The digitized-values CM_N, CM_A, and CM_B are used to decide the operation period of each energy delivery path through the use of the sequence controller and the dead time driver.

F. Sequence Controller and the Dead Time Driver

The sequence controller depicted in Fig. 12 is used to generate the current-controlling sequence for energy delivery to each output terminal. The operation of the sequence controller can determine four durations, which are Paths 1, 3, 4, and 6, corresponding to the four energy delivery paths in Fig. 3. At the beginning of Path 1, the sequence controller is triggered by a positive edge of clock signal *CLK* that has duty cycle of 90%. The energy can be delivered to the buck output through Path 1. Once CM_A, which is determined by charge reservation circuit, is set from high to low, the energy delivery Path 1 is ended and Path 3 is triggered to store enough energy to the inductor. During the interval of Path 3, the inductor current rapidly increases to the ALTC level. When the current-sensing signal V_{RS} is higher than the ALTC level V_{ALTC}, the signal CM_N, is set from high to low by the charge reservation circuit, and the energy delivery path changes to Path 4. According to the duty cycle of Path, 4 which is determined by the charge reservation circuit, Path 4 properly delivers energy to the boost output terminal V_{OB}. Once the voltage V_{C2} is higher than error the signal E_{OB}, CM_B is set from high to low and the energy delivery of Path 4 ends. Consequently, the controlling sequence enters Path 6, which is the freewheeling stage. In other words, the surplus energy is reserved in the form of inductor current. All the output signals D_A, D_N, D_B, and D_F of the sequence controller are converted by the dead time driver, as shown in Fig. 13, to the gate driving signals S_A, S_N, S_B, and S_F, respectively. The dead time driver contains a level shifter, which raises the boost output voltage for fully turning OFF the power MOSFETs. The driver is composed of a nonoverlapping circuit, which helps to avoid the shoot-through issue during the switching transition of different current paths. These gate-driving signals are used to switch the power MOSFETs M_A, M_N, M_B, and M_F. The hysteresis mode addresses the current crowding issue by having a structure with the least switches and is triggered by the hysteresis mode selector. The signal MD generated by the ALTC circuit in Fig. 10, and an AND gate AND_3 shown in Fig. 12, constitute the hysteresis mode selector. When the load condition of buck output V_{OA} is larger than that of boost output V_{OB}, the output signal MD is set to a high state for entering the hysteresis mode. Inversely, if the signal MD is in the low state, the PWM mode is selected. At hysteresis mode, the switches M_F and M_A directly connects the power supply to V_{OA}, with a slightly increased output ripple to ensure system stability. However, the important issue is that the power source of the controller comes from the boost output, i.e., the possibility of the buck energy being larger than the boost energy is reduced. The converter seldom enters the hysteresis mode after the deliberated power consideration.

V. Experimental Results

The chip micrograph of the proposed sub-1 V SIDO dc–dc converter with the ALTC technique, as shown in Fig. 14, was fabricated via 0.25 μm 2.5 V/5 V process. The threshold voltages of NMOS and PMOS are 0.48 and -0.6 V, respectively. The

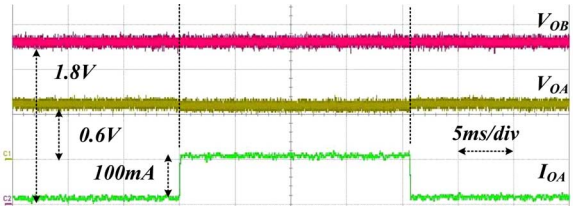


Fig. 15. Step load condition at buck output V_{OA}.

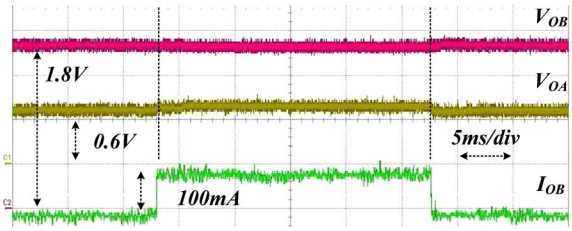


Fig. 16. Step load condition at boost output V_{OB}.

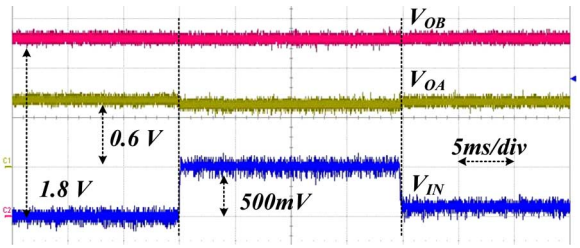


Fig. 17. Line-transient response at $I_{OA} = I_{OB} = 10$ mA.

chip area is $1312 \times 1590\ \mu\text{m}^2$. The input supply voltage is 1 V and the two output voltages are set to 0.6 V as buck output and 1.8 V as boost output.

In Fig. 15, a load current step of 100 mA is applied to the buck output V_{OA} to measure the load-transient performance and cross regulation of the two output terminals. The value of V_{OB} is merely affected by the load change at the output V_{OA}, since the ALTC technique can dynamically adjust the inductor current level. According to the hysteresis mode operation, the current crowding issue is addressed when the buck energy is larger than the boost energy. On the other hand, Fig. 16 shows a 100-mA step load condition at the boost output V_{OB}. The cross regulation at the output V_{OA} is worse than the result shown in Fig. 15, since the power of the controller comes from the boost output. As a result, the cross regulation becomes worse in cases of load variation. Fig. 17 shows the measurement results of the line-transient response. A stepping voltage, which changes from 1 to 1.5 V, is applied to the sub-1 V SIDO converter and *vice versa*. As illustrated in Fig. 17, the output terminal V_{OB} shows a good performance during line transient. However, the output terminal V_{OA} has a slight drop in voltage level. The voltage drop is caused by the resolution of the charge reservation circuit, since the different supply voltage level causes the different conversion ratio. Therefore, there is a tradeoff with voltage headroom, output ripple, and cross regulation.

Fig. 18 shows the stable inductor current waveform of the ALTC technique in steady state. Obviously, the controlling sequence is consistent with the desired inductor waveform to reduce output ripple, cross regulation, and power loss. The measured load regulations of the output terminals V_{OA} and V_{OB} are 0.24 and 0.39 mV/mA, respectively. The voltage at the node V_X has a large voltage swing in the design of sub-1 V SIDO converter. The proposed ABS circuit can ensure that the bulk of the p-MOSFET always can be tied to the highest voltage. Thus, the leakage due to the parasitic diode can be avoided and the efficiency can be improved.

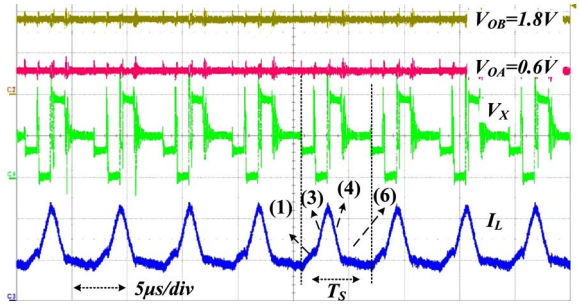


Fig. 18. Inductor current-control sequence in steady state.

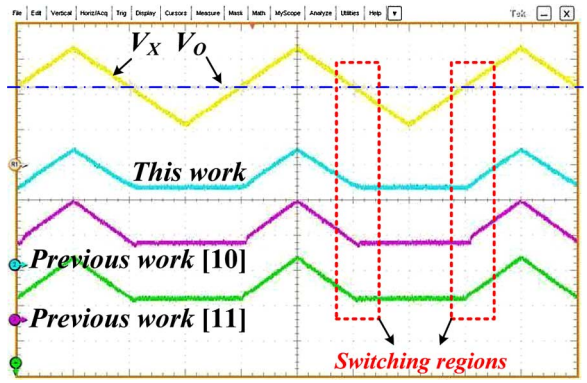


Fig. 19. Measurement results of the proposed ABS circuit in steady state.

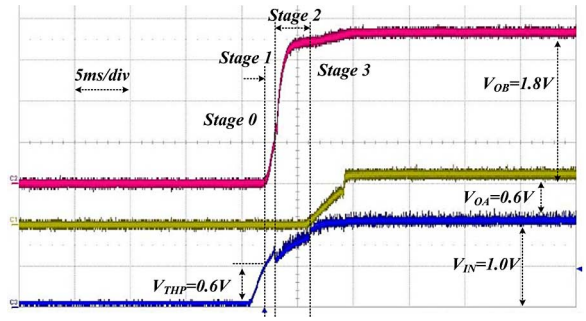


Fig. 20. Proposed power-on sequence.

Fig. 19 shows the measurement result of ABS circuit. In comparison with the performance of the ABS circuit with the previous works [10], [11], we used a triangular waveform as an input to compare with a constant reference voltage of 2 V. We found that the output waveforms contain undershoots/overshoots in voltage during the switching regions due to the slow response of the previous designs. The crossover point of test waveforms of the proposed ABS circuit exhibited smooth transition to the

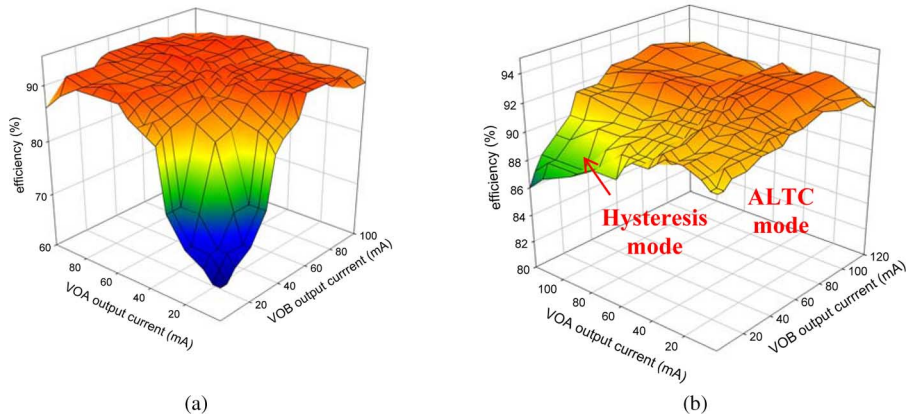


Fig. 21. Power efficiencies of (a) the conventional SIDO converter and (b) the proposed SIDO converter with the ALTC technique.

TABLE II
PERFORMANCE OF PROPOSED SIDO DC–DC CONVERTER

Supply Voltage	0.9~1.6V @ Room Temperature 25°C	
Inductor L	22 µH	
Oscillator frequency	450 KHz	
Process	TSMC 2.5V/5V 1P5M BCD	
Die Area	1312*1590 µm^2	
Quiescent Current	2 mA	
Output Voltage	V_{OA}=0.6V	V_{OB}=1.8V
Output Capcitor C	10µF w/i Low ESR	
Output Ripple @ 100mA	0.61mV	0.754mV
Load Regulation	0.24V/A	0.39V/A
Line Regulation	0.155mV/V	1.42mV/V
Cross-Regulation	Step Load (10→100mA)	6mV/5mV
	10mV/8mV	Step Load (10→100mA)

maximum voltage between the input terminals. Furthermore, the measured quiescent current of 6 μA is proposed in an ABS circuit, while the previous designs in [10] and [11] needed 56 and 15 μA, respectively. Furthermore, the circuit complexity in [11] occupies a large silicon area. Therefore, the proposed ABS circuit alleviates potential leakage and latch-up, which occurs at the bias of the N-well that needs to connect to the highest supply voltage, in order to design on-chip power switches. Certainly, fast response and low-power consumption are achieved in this design.

Fig. 20 shows the power-on procedure when the proposed start-up mechanism is adopted. The power-on procedure is divided into four stages. At Stage 0, the supply voltage ramps up to the p-MOSFET threshold voltage $V_{\rm THP}$. The sub-1 V SIDO dc–dc converter is disabled since the supply voltage is not high enough. When the supply voltage is larger than $V_{\rm THP}$, the power-on procedure starts to directly deliver energy to the boost output V_{OB} through the power MOSFETs M_F and M_B at Stage 1. At Stage 2, the ring oscillator is enabled to generate the switching clock *CLK* with a 50% duty cycle. The fixed clock boosts the output terminal V_{OB} to about 1.65 V, which is 90% of the regulated output voltage. Then, the closed loop takes over the rest of the task of boost regulation at Stage 3. Simultaneously, the power-on procedure also starts to regulate the buck output voltage V_{OA}.

Fig. 21(a) represents the measurement result of the conventional SIDO converter illustrated in Fig. 2. It shows poor power efficiency at light load condition. Since the conventional structure has two power MOSFETs in the energy delivery path, the measurement result only presents with a 90% maximum efficiency. Fig. 21(b) shows the measurement results of the proposed sub-1 V SIDO dc/dc converter with ALTC technique. A comparison of the power efficiency between the conventional and the proposed SIDO converters shows a power efficiency improvement from 65% to 85% at light load condition. Moreover, the proposed sub-1 V SIDO dc–dc converter shows more than 90% efficiency in all load conditions except in the hysteresis mode. As the energy delivery path does not flow through the inductor in hysteresis mode, the conversion efficiency drops to 85%. The performance of the proposed sub-1 V SIDO dc–dc converter with the ALTC technique is summarized in Table II.

VI. CONCLUSION

In this paper, an effective ALTC technique is proposed. In the proposed ALTC technique, the ALTC current level $V_{\rm ALTC}$ properly stores enough energy in the inductor current. Hence, the sub-1 V SIDO dc–dc converter achieves high conversion efficiency without over storage of energy. Moreover, the ALTC technique also minimizes cross regulation during the load transitions of two output terminals. A current-mode ring oscillator with the proposed SBCS circuit simplifies the design of power-on sequence. It generates a nearly constant clock to simplify the design of the internal oscillator. The test chip was fabricated via Taiwan Semiconductor Manufacturing Company 0.25 μm 2.5V/5V Bipolar-CMOS-DMOS process, and experimental results showed efficiencies of 85% and 92% at light and heavy loads, respectively, with a cross regulation smaller than 10 mV.

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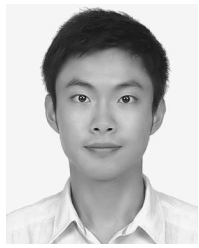

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