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Influence of the device geometry on the Schottky gate characteristics of AlGaN/GaN HEMTs

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Abstract
In this work, we investigate the relevance of device geometry to the Schottky gate characteristics of AlGaN/GaN high electron mobility transistors. Changes of three-terminal gate turn-on voltage and gate leakage current on the gate—drain spacing, source—gate spacing and recess depth have been observed. Further examinations comparing device simulations and measurements suggest that gate turn-on voltage is influenced by the distribution of electric potential under the gate region which is related to the geometry. By proper design of the device, high gate turn-on voltage can be obtained for both depletion-mode and recessed enhancement-mode devices.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

AlGaN/GaN heterostructures are material systems with unique properties such as a high concentration of the two-dimensional electron gas (2DEG), a high carrier saturation velocity and a large band gap. AlGaN/GaN high electron mobility transistors (HEMTs) with these basic or modified structures have shown excellent performance for radio-frequency high-power applications [1–5]. For these devices, the current in the channel is typically modulated by a metal—semiconductor Schottky gate. However, Schottky contacts may be compromised by high gate leakage current in the reverse-biased region and gate conduction in the forward-biased region. For the AlGaN/GaN HEMTs, lowering of the reverse leakage current can be achieved with the use of metals with a higher work function such as Pt, Ir, Cu and Re [6–9]. But the forward turn-on voltage of the Schottky gate $V_{GS\,on}$ (the gate voltage, V_{GS}, when I_{GS} reaches +1 mA mm^{-1}) could not be effectively postponed because the work function difference of the metal only shifts it by several tenths of a volt. This forward conduction limits the safe operation region and additionally has been shown to degrade the gate contact and devices through the presence of high current and temperature [10]. To increase the available voltage swing and improve the reliability, metal—insulator—semiconductor (MIS) structures with SiO_2, Al_2O_3 or SiN_x [11–14] have been demonstrated and they can effectively reduce the leakage current and postpone the $V_{GS\,on}$ of the gate contact.

In this paper, we approach this issue from another perspective and focus on the influence of lateral and vertical positions of the gate on $V_{GS\,on}$ during a three-terminal operation. This is of particular interest for devices using a recessed gate to yield normally-off operation [15] or to suppress high-voltage drain leakage currents [16]. Furthermore, this will provide further understanding of the device in operation and can be adopted to improve the device performance.

2. Experiments

The epitaxial structure was grown by MOCVD on a *c*-plane sapphire. The layers consisted of a 1.5 μm thick unintentionally doped (UID) GaN buffer layer, followed by

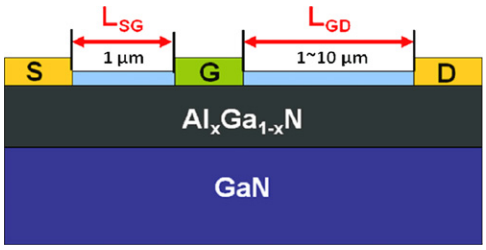

Figure 1. Schematic of the dimension variation of the device.

25 nm $Al_{0.25}Ga_{0.75}N$ and finished with a 5 nm GaN n-doped cap layer (Si doped to 7×10^{18} cm^{-3}). Sheet resistivity is 320 Ω/□. The ohmic contacts were formed by deposition of Ti/Al/Mo/Au using an e-beam evaporator, followed by rapid thermal annealing in N_2 atmosphere at 830 °C for 30 s. Reactive ion etching (RIE) with $Cl_2/BCl_3/Ar$ plasma was used to isolate the device. Device passivation was done with PECVD SiN_x and the gate foot was defined by using electron beam lithography followed by dry etching for realizing an opening through SiN_x. The dimension of the gate foot is 0.5 μm. For selected wafers, recessing was done using SF_6 plasma with different etch times to obtain shallow-recessed, 10 nm (depletion-mode), or deep-recessed, 22 nm (enhancement-mode), AlGaN/GaN HEMTs. The second electron beam lithography was then carried out to define the gate head. Pt/Ti/Au metal stacks were evaporated as the gate metal. Other dimensions for the device are as follows: the source—gate spacing, L_{SG}, is fixed to 1 μm and the gate—drain spacing, L_{GD}, is varied from 1 μm to 10 μm; the schematic is shown in figure 1. The total gate width was 250 μm (2×125 μm). Pad connections of these devices were done by electrochemically plated 6 μm thick gold.

The dc characteristics of these devices were measured. A transconductance curve was extracted with the drain voltage V_{DS} fixed to 15 V, while the gate voltage V_{GS} swept from −5 V to +8 V with the gate current being monitored at the same time. The compliance limit of the gate current was 5 mA mm^{-1} to avoid destruction of the device, and the measurement was stopped when the limit was reached. After the measurement, the source and drain connections were interchanged and characterized again as devices with the fixed gate—drain spacing, L_{GD}, of 1 μm and variations of the source—gate spacing, L_{SG}, from 1 μm to 10 μm. Additional measurements with the drain voltages of $V_{DS} = 10$ V and 5 V were also done to evaluate the effect of the drain bias on the device characteristics.

The device simulation was carried out on a two-dimensional physical-based device simulator (Silvaco—'Atlas' [17]) to give an insight into the electric potential distribution of the device with a variation of the geometry.

3. Results and discussion

The characteristics of AlGaN/GaN HEMTs with different gate—drain and source—gate spacing when the drain contact is biased at $V_{DS} = 15$ V are shown in figure 2. As can be seen in figure 2(*a*), with the reduction of L_{GD}, an increase in the maximum channel current was observed. Moreover, $V_{GS\,on}$ was shifted to a higher value and accompanied with the increase of the negative gate leakage current. Figure 2(*b*) shows the results for the L_{SG} variation. In this figure, the larger channel resistance with an increment of the distance is consistent with [18]. As for the gate characteristics, a different trend was observed. The increase rather than the decrease of the distance leads to a more pronounced positive shift of $V_{GS\,on}$, and the negative gate leakage current decreases at the same time. The change in the gate negative current cannot be correlated to the source–gate or gate–drain distance. Furthermore, since the Schottky gate contact is still in the reverse-biased region, this leakage current could not be due to fluctuation of the potential but could possibly be caused by changes in the channel temperature due to the self heating of the device; this is evident in figure 2 as the same drain current density yields a similar level of negative gate leakage current.

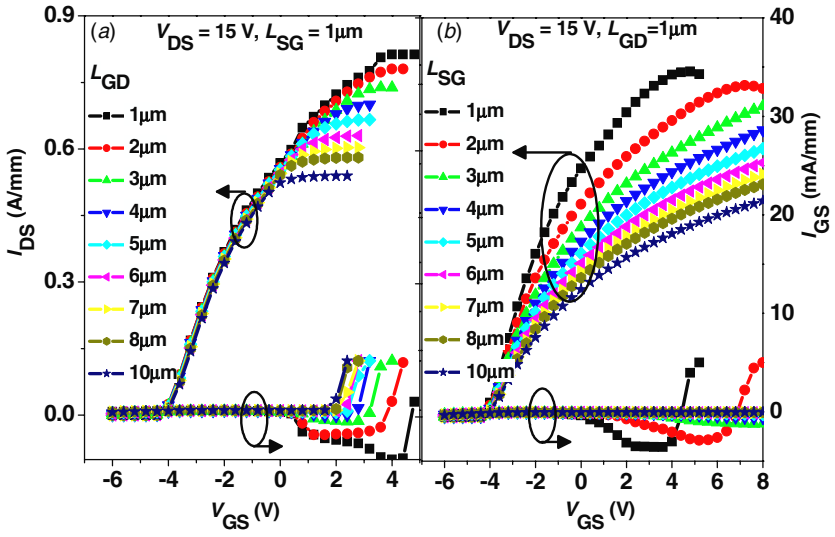

Figure 2. Influence of the (*a*) gate–drain spacing and (*b*) source–gate spacing on the channel current and gate leakage current.

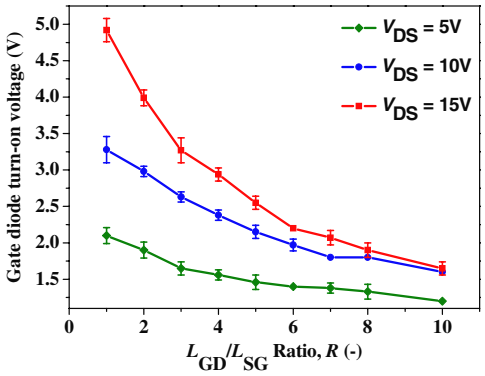

Figure 3. Dependence of the gate diode turn-on voltage on the drain bias and geometry ratio.

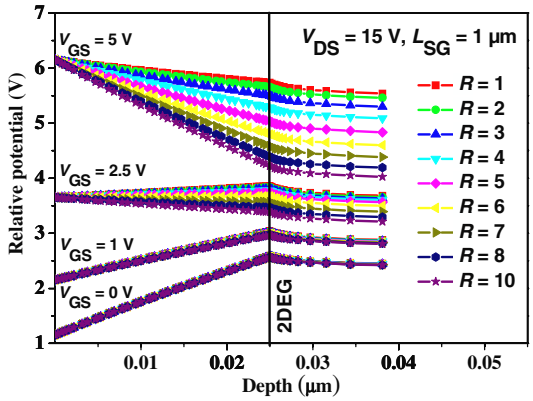

Figure 4. Simulated electric potential distribution below the source-side gate edge for devices with different geometry ratio R at $V_{GS} = 0$ V, 1 V, 2.5 V and 5 V. Drain bias is fixed to 15 V.

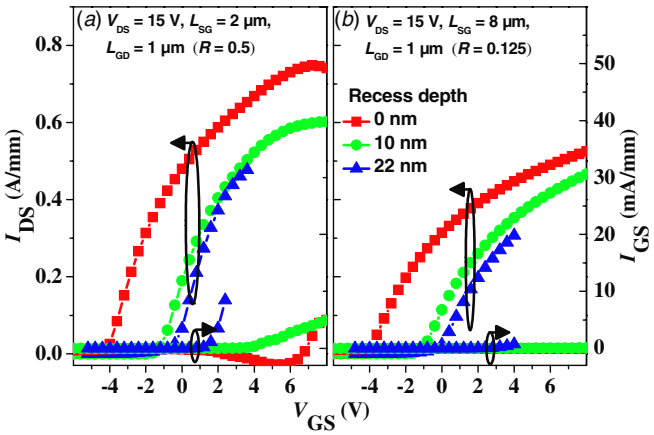

Figure 5. Comparison of the characteristics between devices with different recess depths. The geometry ratios, R, are (*a*) 0.5 and (*b*) 0.125.

Nevertheless, the magnitude of the leakage current is still low compared to the drain current.

To probe into the origin of shift of $V_{GS\,on}$, more measurements were performed with drain voltage set to lower values of 5 V and 10 V and a normalized distance $R = L_{GD}/L_{SG}$ was used to simplify the geometry factor. The results are plotted in figure 3. As can be seen in this figure, $V_{GS\,on}$ is strongly dependent on both relative gate position and the value of the drain voltage. Combination of the above observations suggests that the phenomenon is driven by the potential distribution inside the device. However, since the electric potential and electric field distribution are nonlinear and sometimes abrupt in the device, as reported in [18], a physical device simulation study is needed as was performed for devices with dimensions given in figure 2(*a*) at a fixed drain voltage V_{DS} of 15 V, and the electric potential profiles below the source side of the gate are plotted in figure 4. This location is of particular interest because the start of the forward conduction of the Schottky diode should occur here rather than near the drain side of the gate, where it is still effectively reverse biased by the drain voltage. In this figure, the distribution of the potential under the gate contact becomes dependent on R with the increment of V_{GS}. In the device with smaller R, the potential of the channel can still remain reverse biased with respect to the Schottky contacts due to the penetration of the drain potential into the region under the gate, while for the larger R, the gate contact starts to open. However, it has to be noted that if a smaller R is achieved through the decrease in L_{GD}, the device will have a lower breakdown voltage, since the breakdown is related to the gate–drain spacing [19]. On the other hand, a decrease in R by means of a larger L_{SG} will lead to an increase in the channel resistance, as shown in figure 2.

Devices with vertical position variation of the gate contact (recessed gate) device were also investigated. The results measured at $V_{DS} = 15$ V are shown in figure 5. The magnitude of the negative gate leakage current is low in the recessed device. This supports the hypothesis that the origin of this current is related to the level of drain current, which is generally lower in the recessed device. Furthermore, a comparison between figures 5(*a*) and (*b*) again suggests that a smaller R can effectively increase $V_{GS\,on}$. However, it also reveals that $V_{GS\,on}$ is generally lower when the gate is placed closer to the channel. This has to be considered when using gate recessing for obtaining normally-off devices with threshold voltages $V_{th} > 0$ V. The gate swing is then severely limited to both sides, to the negative side by V_{th} and to the positive side by the reduced $V_{GS\,on}$. The phenomenon is demonstrated by comparing the deeply-recessed 22 nm normally-off device in both figures; $V_{GS\,on}$ of only 2.5 V is observed for the device with $L_{GD} = 1\ \mu$m and $L_{SG} = 2\ \mu$m ($R = 0.5$) while the use of $L_{GD} = 8\ \mu$m and $L_{SG} = 1\ \mu$m ($R = 0.125$) results in $V_{GS\,on}$ of more than 4 V. Thus by shifting the gate position toward the drain side, the gate swing can again get extended toward larger $V_{GS\,on}$, but channel resistance or breakdown voltage will have to be scarified as with the case of the non-recessed device.

4. Conclusion

The turn—on characteristics of the Schottky gate of the AlGaN/GaN HEMTs with respect to device geometry and applied bias were investigated. With device simulation, this behavior is found to be related to the electric potential distribution in the AlGaN/GaN heterostructures. Proper

design of the geometries can be done to extend the possible gate swing toward positive gate bias with trade-off between breakdown voltage or channel resistance. This is another option for gate-recessed AlGaN/GaN HEMTs.

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References

[1] Wu Y F, Saxler A, Moore M, Smith R P, Sheppard S, Chavarkar M, Wisleder T, Mishra U K and Parikh P 2004 *IEEE Electron Device Lett.* **25** 117–9
[2] Chini A, Buttari D, Coffie R, Heikman S, Keller S and Mishra U K 2004 *Electron. Lett.* **40** 73–4
[3] Okamoto Y *et al* 2001 *IEEE Trans. Electron Devices* **51** 2217–22
[4] Wu Y F, Moore M, Saxler A, Wisleder T and Parikh P 2006 *Proc. Device Res. Conf.* pp 151–2
[5] Palacios T, Chakraborty A, Rajan S, Poblenz C, Keller S, DenBaars S P, Speck J S and Mishra U K 2005 *IEEE Electron Device Lett.* **26** 781–3
[6] Guo J D, Feng M S, Guo R J, Pan F M and Chang C Y 1995 *Appl. Phys. Lett.* **67** 2657–9
[7] Venugopalan H S and Mohney S E 1998 *Appl. Phys. Lett.* **73** 1242–4
[8] Ao J P, Kikuta D, Kubota N, Naoi Y and Ohno Y 2003 *IEEE Electron Device Lett.* **24** 500–2
[9] Jeon M, Jang H W and Lee J L 2003 *Appl. Phys. Lett.* **82** 391–3
[10] Joh J, Xia L and del Alamo J A 2007 *IEEE IEDM Technical Digest* pp 385–8
[11] Khan M A, Hu X, Simin G, Yang J, Gaska R and Shur M S 2000 *Appl. Phys. Lett.* **77** 1339–41
[12] Hashizume T, Ootomo S, Inagaki T and Hasegawa H 2003 *J. Vac. Sci. Technol.* B **21** 1828–38
[13] Hu X, Koudymov A, Simin G, Yang J, Khan M A, Tarakji A, Shur M S and Gaska R 2001 *Appl. Phys. Lett.* **79** 2832–4
[14] Chang Y C, Chang W H, Chiu H C, Tung L T, Lee C H, Shiu K H, Hong M, Kwo J, Hong J M and Tsai C C 2008 *Appl. Phys. Lett.* **93** 053504
[15] Uren M J, Nash K J, Balmer R S, Martin Morvan T E, Caillas N, Delage S L, Ducatteau D, Grimbert B and De Jaeger J C 2006 *IEEE Trans. Electron Devices* **53** 395–8
[16] Saito W, Takada Y, Kuraguchi M, Tsuda K and Omura I 2006 *IEEE Trans. Electron Devices* **53** 356–62
[17] SILVACO International 2009 *ATLAS User's Manual, Device Simulation Software* (Santa Clara, CA: SILVACO International)
[18] Russo S and Carlo A D 2007 *IEEE Trans. Electron Devices* **54** 1071–5
[19] Vescan A, Dietrich R, Wieszt A, Tobler H, Leier H, Van Hove J M, Chow P P and Wowchak A M 2000 *J. Cryst. Growth* **201** 327–31