Chapter 1 Introduction

1.1 Introduction

Wireless communication has developed dramatically in recent years and plays an important role in scientific and technical evolutions. Wireless communication is extensively applied in many fields, such as telegram, phone and radio. However, numerous physical characteristics are complicated so that hard to be overcome in the early days. Furthermore, high cost also restricts the cordless systems coming to popularization. Recently, integrated-circuit technology on fabrication brings new processes and improved properties gradually. Moreover, higher density of integrated transistors is available so that previous bulky devices are probably manufactured on a smaller chip. Personal communication, local area network (LAN) or some interactive services with wireless technique are realistic nowadays since device technologies that are capable to produce high volumes at extremely low cost. A potentially easier and faster System on Chip (SoC) integration is also important, further these requirements are best met by Complementary Metal Oxide Semiconductor (CMOS) technology.

A Wireless communication system consists of high frequency block and low frequency block. The high-frequency block locates at the front-end of overall system and operates at a relatively higher frequency range about few giga-hertz to mega-hertz. Receiver (Rx), Transmitter (Tx) and Frequency Synthesizer are the three main portions of front-end circuits [1-3]. The main functions of a receiver are to receive, amplify, filter and downconvert the desired RF signal to lower frequencies namely IF signal. The functions of frequency synthesizer are generating local oscillator (LO)

signals and feeding to receiver and transmitter for channel or band selection. Transmitter upconverts and radiates signals with proper power level. These three portions are roughly classified RF components. The function block diagram of receiver and transmitter is shown in Fig. 1-1. The low-frequency part which is classified Baseband includes most components of overall system and operates at lower frequencies, hence signal is processed, modulated or demodulated in this part.

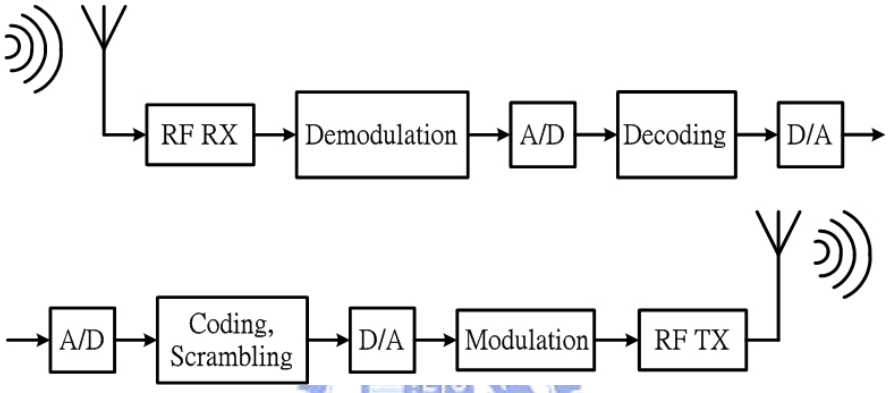

Fig. 1-1 Receiver and transmitter function block diagram.

Many kinds of specifications are made depending on various applications, such as GSM and GPRS for mobile communication or Bluetooth and IEEE 802.11 family for short-range wireless local area network (WLAN). RF front-end circuits dissipate most power in full transceiver, although they only occupy a small portion. Owing to the complexity on the analog and high-frequency characteristics, it is difficult to design wireless equipments with high performance. Especially in early days, the RF circuits are designed and fabricated with GaAs or Bipolar technology since they have better properties than CMOS technology. But CMOS technologies are dominant in the digital circuits, while in the analog RF regime, the performance of CMOS circuits is not superior and considered slow and noisy. By above, more than two chips plus peripheral passive components will be used in overall transceiver system, raise the

cost and device size. To reduce the total cost of a transceiver system, the standard CMOS technology is the best choice since it is inexpensive and high integration ability. Fortunately, as the benefit of the technology scaling down, it is desirable to design RF circuits with low cost, high integration level, improved noise performance and many other requirements.

Owing to front-end circuits are power-hungry blocks and portable communication devices are usually with limited battery energy, hence, the demand for low-power wireless transceivers in portable application has led to extensive research on RF architecture and circuit design. A number of low-power transceivers have been reported [4-9], but it is desirable to achieve even lower power levels.

1.2 Thesis organization

Chapter 1 takes an overview on some popular receiver architecture. Receiver architecture selection is an important design issue since high integration and achieve SoC are preferred. Chapter 2 and 3 illustrate fundamentals, design considerations and design steps of LNA and mixer, respectively. Since LNA and mixer are two power-hungry blocks in portable receiver front-end circuits, designing low power consumption circuits with proper performance is our main purpose. Chapter 4 provides a proposed LNA/mixer combination circuit named “Stacked LNA-Mixer” in this thesis. We illustrate the design considerations, design steps and provide simulation results using “Advanced Design System” CAD tool (ADS) here. This stacked LNA-mixer is designed to operate at 2.42GHz ISM band with proper performance and low-power dissipation properties. The layout of stacked LNA-Mixer is presented in Chapter 5. Finally, conclusions and future works are described in Chapter 6.

1.3 Overview of recent popular receiver architectures

In this section, we briefly review some of recent popular receiver architectures [1-3]. Heterodyne (superheterodyne), direct conversion, low-IF and image reject receivers are four main topologies shown as Fig. 1-2. We discuss the benefits and drawbacks of them in the following pages, respectively.

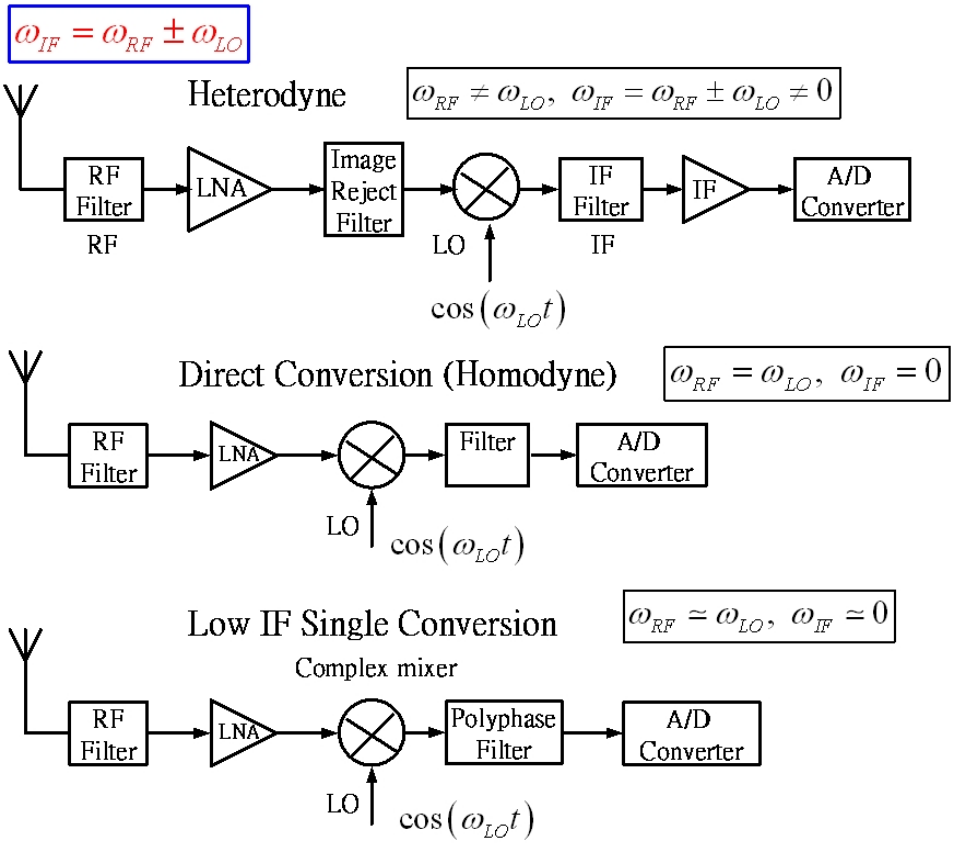

Fig. 1-2 Three topologies of receiver architecture (a) heterodyne (b) direct conversion (c) low-IF receiver architecture.

1.3.1 Heterodyne (super-heterodyne) architecture

The first kind of receiver architecture is the heterodyne receiver shown in Fig. 1-3. In this topology, the RF input signal is first amplified, and then converted to a lower intermediate frequency (IF) by an offset-frequency generated by a local

oscillator (LO) signal. The frequency translation is performed by means of a downconversion mixer, which is viewed as a simple analog multiplier, will be illustrated in Chapter 3. The IF signal is substantially amplified by IF stage containing highly selective passive band-pass filters. The IF filter suppresses out-of-channel interferes, performs channel selection, are named channel select filter. A low noise amplifier in front of the downconversion mixer used to reduce the noise figure of the following stage is needed since the mixer usually generates high noise.

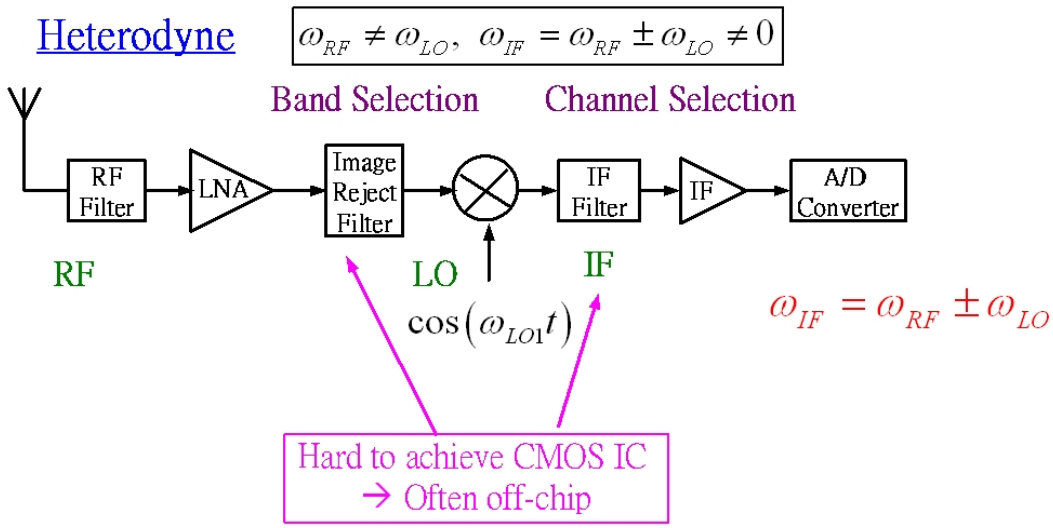

Fig. 1-3 Heterodyne receiver.

The receiver architecture of Fig. 1-3 suffers from a number of drawbacks. The problem of image is serious in heterodyne receiver, then we need to add image reject filter. But the image-reject filter and IF filters are bulky, expensive, low-impedance devices that raise the device size, cost and the power dissipation in the LNA and the first mixer, respectively. Hence, it is hard to achieve system-on-chip since these components are usually off-chip. Moreover, the choice of IF is another problem trade-off among the amount of image noise, the spacing between the desired band and image, and the loss of the image-reject filter. If the IF is high, the image can be

suppressed but complete channel select is difficult, and vice versa. On the other hand, we must to trade-off between selectivity and sensitivity.

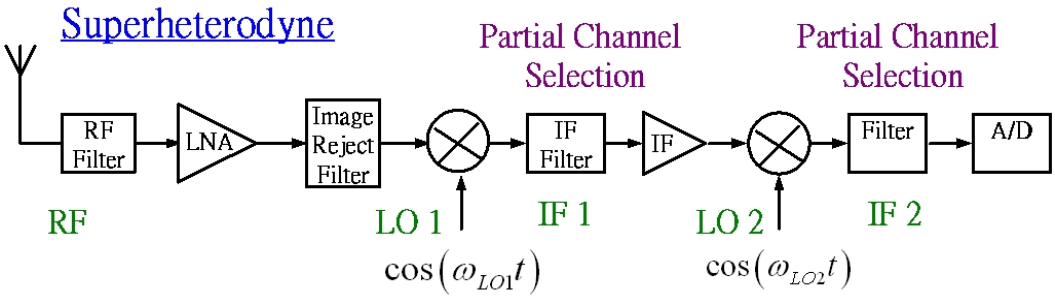

Fig. 1-4 Superheterodyne receiver.

To resolve the problem between selectivity and sensitivity, a modified receiver architecture called superheterodyne is presented. Most RF communication receivers manufactured today adopt the conventional superheterodyne architecture. The superheterodyne receiver diagram is shown in Fig. 1-4, it consist of more than two downconversion stages, each followed by filtering and amplification.

As mentioned before, the passive components such as spiral inductors and capacitors with high-Q values are not available in standard CMOS technology, it is difficult and somewhat impractical to realize as an on-chip solution.

1.3.2 Direct conversion (homodyne) architecture

The direct conversion architecture also called “homodyne” or “zero-IF” architecture is shown in Fig. 1-5. It is widely applied in paging receiver in recent years, which use a very simple FSK modulation technique. The main characteristic of homodyne receiver is the wanted RF signal directly downconvert to the baseband. In other words, the LO frequency is equal to the input carrier frequency. The simplicity

of the homodyne receiver has many benefits. First, it is more easily to be implemented in integration circuit than heterodyne receivers. Second, the problem of image is circumvented because $\omega_{IF} = 0$. Hence, no image filter is required, and the LNA need not to drive a 50 Ω load.

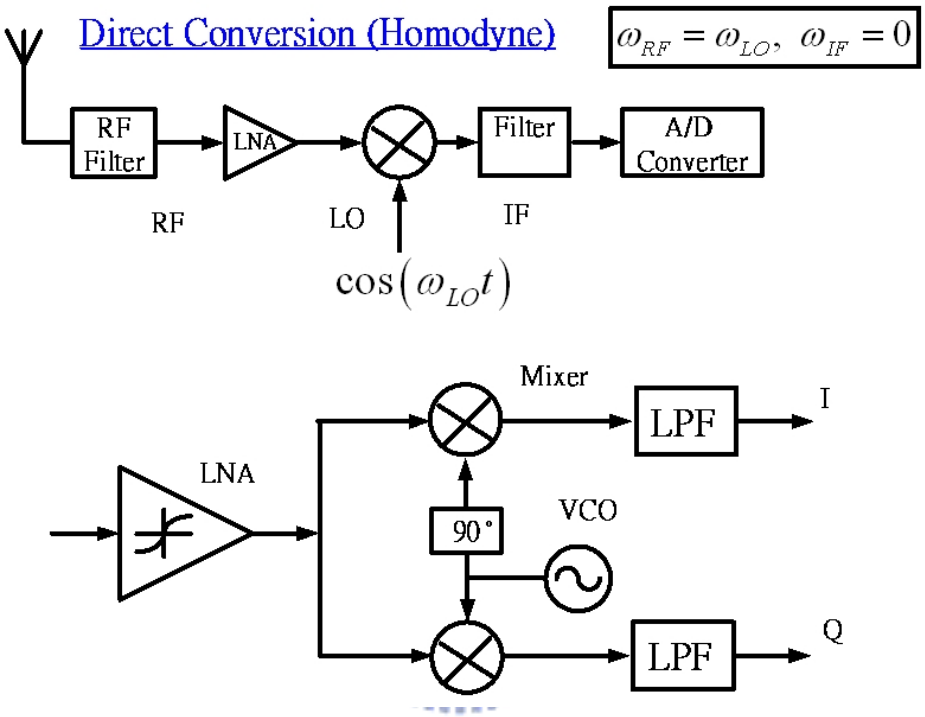

Fig. 1-5 Homodyne (direct-conversion) receiver

The homodyne receiver architecture is best suitable for simple FSK receivers. However, in applications requiring greater sensitivity and selectivity such as GFSK modulation, the homodyne architecture has some disadvantages and limitations due to its sensitivity to dc offset and flicker (1/f) noise. Because the local oscillator is tuned to the RF frequency, it can radiate back out the antenna and interfere with other receivers or reflect and be re-received and downconverted into a substantial stages, cause dc offset. Moreover, the flicker noise limits the overall noise figure of the receiver.

The circuit of Fig. 1-5 (a) can not operates properly for frequency-modulated and phase-modulated signals since it overlaps positive and negative parts of the input spectrum. To overcome this problem, a modified homodyne receiver with quadrature VCO as shown in Fig. 1-5 (b) is adopted. It can avoid the loss of information. In this case, the errors in the nominally 90° phase shift, and mismatches between the amplitudes of the I and Q signals corrupt the downconverted signal, thereby raising the bit error rate. We must avoid above error as possible as we can.

1.3.3 Low-IF single conversion architecture

The homodyne (zero-IF) receiver has been introduced in many applications in recent years, but its performance cannot be compared to that of the heterodyne (superheterodyne) receiver. This lower performance is closely related to its baseband operation, resulting in filter saturation and distortion, both caused by dc offsets and self mixing at the inputs of the mixers. On the other hand, the heterodyne receiver maintains the signal at a higher IF, typically 50 to 200 MHz, and therefore, it does not compete with flicker noise or dc offset. However, heterodyne receivers require off-chip filters for channel selection and image rejection. This opposes the trend of single-chip integration, and disqualifies this architecture. In addition, driving off-chip low-impedance filters increase the overall receiver current consumption.

A modified receiver architecture, low-IF receiver, combines the advantages and avoids the drawbacks of both heterodyne and homodyne receiver is presented as shown in Fig. 1-6 (a), It has a topology which is closely related to zero-IF receiver, but it does not operate in the baseband, only near the baseband. The consequences are that, as for the zero-IF receiver, the implementation of a low-IF receiver can be done with a high degree of integration, however, its performance can be better. For

frequency-modulated and phase-modulated signals, a modified topology with quadrature VCO and polyphase filter would be adopted as shown in Fig. 1-6 (b).

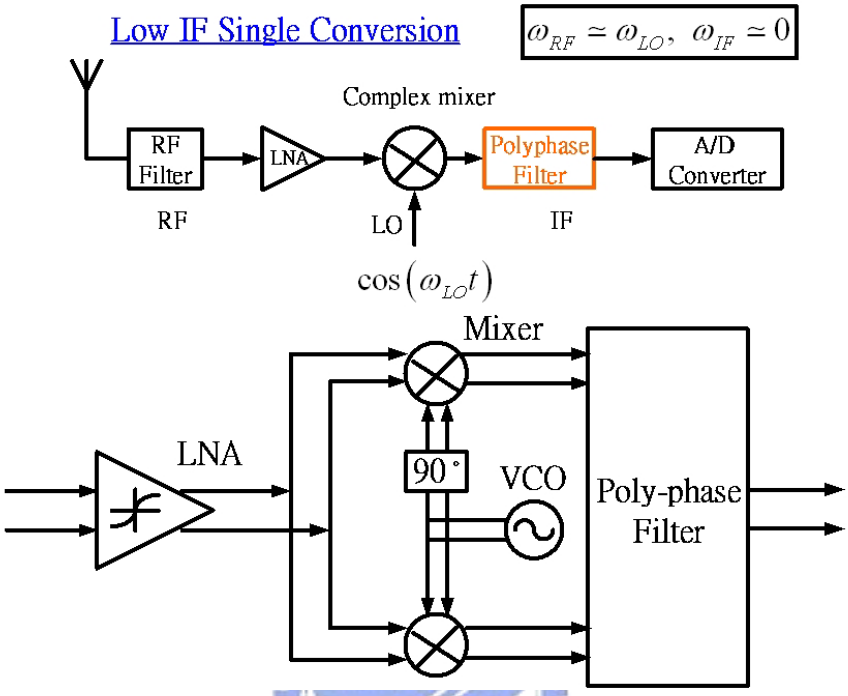

Fig. 1-6 (a) Low-IF receiver architecture.

(b) Low-IF receiver with quadrature VCO and polyphase filter.

1.3.4 Image reject architecture

Another alternative architecture well suited for system-on-chip is the image-reject receiver. Image reject receivers seek to eliminate multiple stages of frequency translation and high-Q off-chip image-reject filter in favor of image cancellation by utilizing mathematical operation and a single stage of on-chip filter. The idea in image reject receiver architecture is to process the desired signal and the image differently, allow image cancellation by its negated replica. A pair of mixer with quadrature VCO shown in Fig. 1-7 can process the desired signal and image with different phase change.

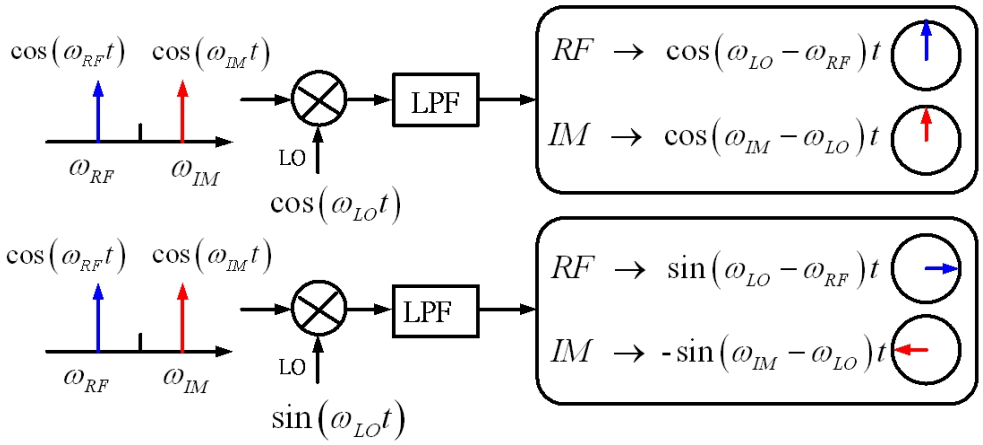

Fig. 1-7 The desired signal and image with different phase change.

■ Hartley architecture

The one of commonly used image-reject receiver architecture is the Hartley architecture introduced by Hartley in 1918, is illustrated in Fig. 1-8. In this circuit , it mixes the RF input with the quadrature VCO, then shift the results by 90° phase shift and add them together to perform the image cancellation function. See Fig. 1-8, we can clearly understand the procedures of image cancellation.

Sensitivity to mismatches is the principal drawback of Hartley architecture. Due to phase and gain imbalance, the image is only partially cancelled. Image rejection ratio (IRR) is a parameter to indicate the performance of image rejection. We should note that in practice the 90° phase shift is replaced with a +45° shift in one path and -45° shift in the other path as shown in Fig. 1-9. To implement the phase shift stage of Fig. 1-9, we can add a RC-CR sub-circuit as shown in Fig. 1-10. The circuit of Fig. 1-10 suffers from gain error since the absolute value of R and C varies with process and temperature especially in IC implementation, hence limits the image-rejection-ratio (IRR). Other drawbacks of the Hartley receiver topology include the loss and noise of the shift-by-90° stage and the linearity and noise of the adder.

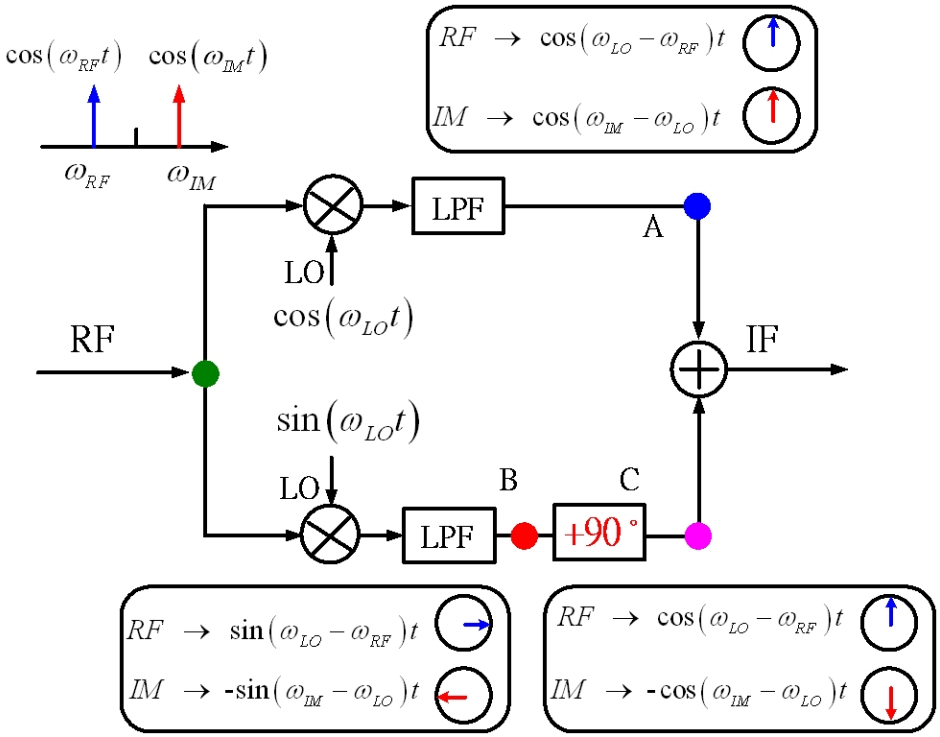

Fig. 1-8 Hartley image-reject receiver architecture.

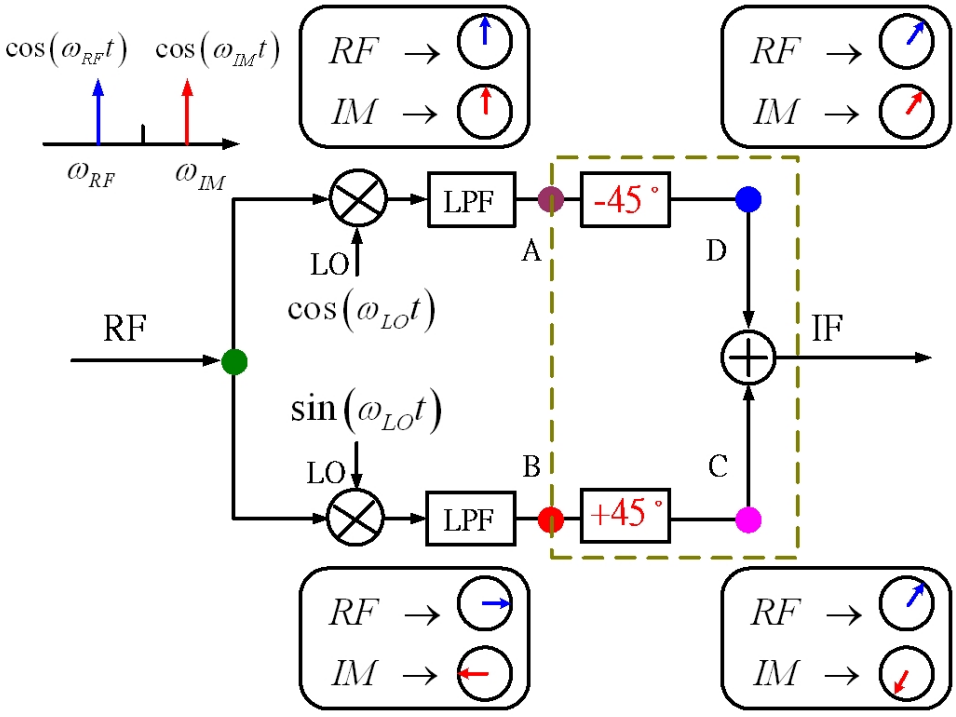

Fig. 1-9 Modified Hartley image-reject receiver architecture.

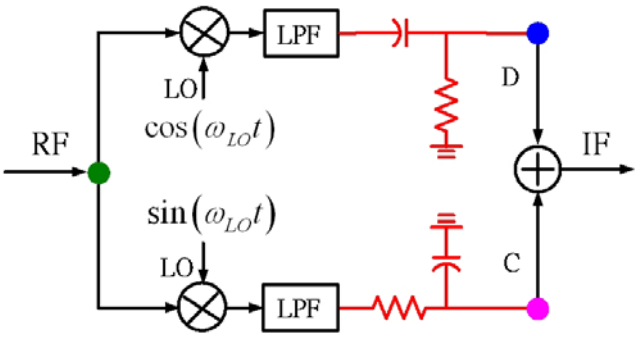

Fig. 1-10 Implement the phase shift stage of Fig. 1-9

■ Weaver architecture

The Weaver architecture, originally invented as an alternative to Hartley's single-sideband modulator, can also serve as an image-reject receiver, illustrated in Fig. 1-11. The circuit replace the 90˚stage by a second quadrature mixing stage to perform the same image-reject function as Hartley architecture. The Weaver approach is also sensitive to mismatches, but it avoids the use of an RC-CR network, thereby achieves greater IRR despite process and temperature variations.

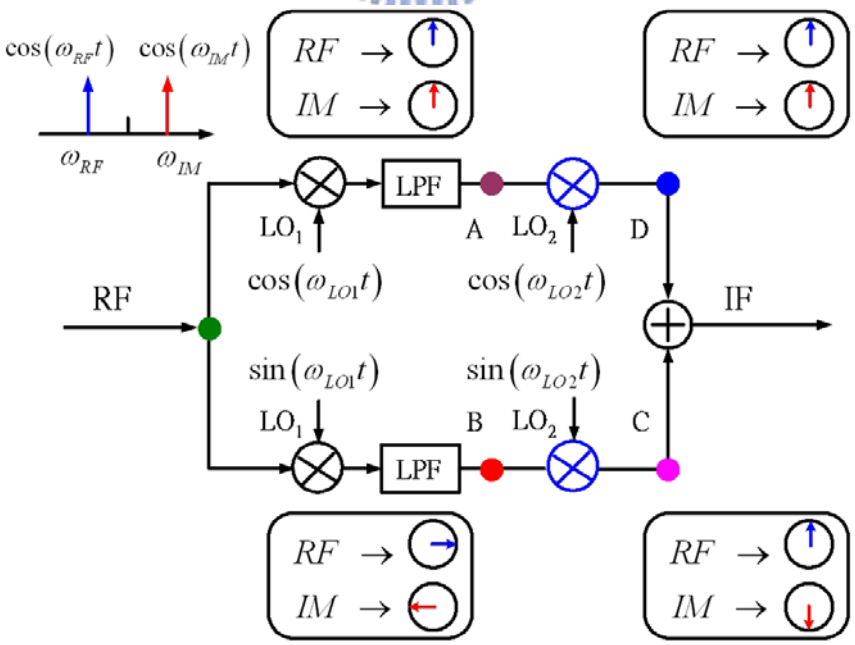

Fig. 1-11 Weaver image-reject receiver architecture.

An important issue in Weaver architecture is the "secondary image". To understand this issue, suppose the input spectrum contains an interferer at $2\omega_{LO2} - \omega_{RF} + 2\omega_{LO1}$, it will be downconverted to the IF frequency the same as the signal downconverted which is Illustrated in Fig. 1-12. This effect constrains the choice of the second LO frequency.

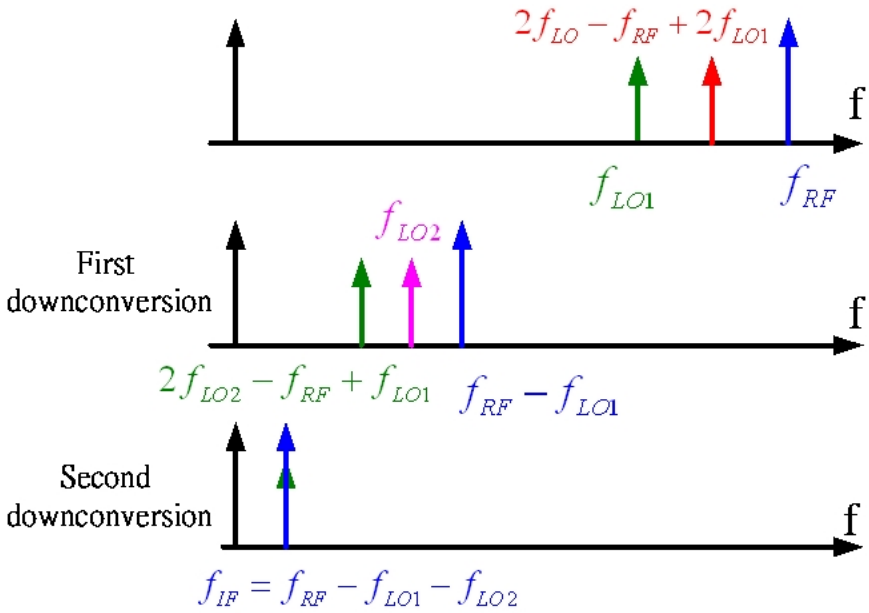

Fig. 1-12 Problem of secondary image in Weaver architecture.

The Hartley and Weaver architectures share one problem: incomplete image rejection due to gain and phase mismatch. But these effects can be properly eliminated by careful layout. Low-IF image reject receiver is a popular architecture in RFIC applications since it has the potential of achieving single-chip.

■ Comparisons of different receiver architectures

The choice of receiver architecture is strongly dependent on the desired circuit complexity, cost, ability of single-chip integration, power dissipation, sensitivity,

selectivity… etc. Comparison between the different architecture performances of the heterodyne receiver, direct-conversion receiver, image-reject receiver, and low-IF receiver are summarized in Table 1-1.

	IF frequency	Image-reject device	Need gain	DC-offset problem	SoC
Heterodyne (Superheterodyne)	High	Off-chip	Medium	No	Low
Direct-Conversion	Zero	No need	High	High	High
Low-IF	Low	On-chip	Medium	No	High
Image-rejection	Medium or Low	On-chip	Medium	No	High

Table 1-1 Comparisons of different receiver architectures.

1.4 Bluetooth RF requirements

Bluetooth is a short-range wireless communication standard [10] that spans telecommunications, personal computing, networking, industrial, automotive and consumer electronic device, allowing voice and data connections up to 10 meters. It defines connections between mobile phones, mobile PCs and other portable devices. Bluetooth use the unlicensed 2.4GHz industrial medicine (ISM) band (2.402 ~ 2.480GHz), with 79 channels of 1MHz bandwidth per channel, and supports a moderate date rate of 1 Mb/s. The modulation scheme is Gaussian binary FSK (GFSK), with frequency deviations of ±160-kHz around the carrier. The input power level range is -70 ~ -20 dBm. A summary of the most important specification items of the Bluetooth standard is shown in Table 1-2.

Carrier frequency	2.402 to 2.480 GHz
Channel numbers	79
Modulation	GFSK with Index 0.32
Input power range	-70 ~ -20 dBm
Hopping	1600 hps, T=23h 18min
Hop sequence length	2^{24} bit, $\Delta f = 78$ MHz
Transmit power	0 to +20 dBm
Distance	0.1 to 10 m
Max. Data rate	721/57.6 or 442.6 kb/s

Table 1-2 Summaries of Bluetooth standard.