Chapter 4 Simulation Results of a 1.8 V 2.42 GHz Stacked LNA-Mixer

4.1 Motivation

As mentioned before, owing to receiver front-end circuits are power-hungry blocks and portable communication devices are usually battery-limited. Hence, low-power wireless transceivers in portable applications are required and have led to extensive researches on transceiver architectures and circuit designs. Up to now, a number of low-power wireless receivers have been reported [4-9], but it is still desirable to make devices consuming power as lower as possible.

4.2 The Stacked LNA-Mixer circuit block

The front-end low noise amplifier and mixer are two power-hungry devices in overall transceiver system. Two means can be used to save power, lower down the supply voltage or integrate more than two stages into a single stage. As we adopt the front mean to lower down the supply voltage, the following stages such as the baseband section and PLL block are also limited by this lower supply voltage. Hence, the performances of them may suffer from serious problems. For example, low supply voltage will decrease the tuning range of a VCO. For this reason, we must research other means to relax these issues, for instance, achieve a single device with multi-functions. LNA/mixer combination circuit is a best example in receiver part, this idea has been presented in [4] by Alireza Zolfaghari and Behzad Razavi. It

integrates the low noise amplifier and mixer function into a single stage by stacking the mixer on the top of a low noise amplifier. In other words, it uses a low noise amplifier to replace the current source stage of a Gilbert cell mixer which is shown in Fig. 4-1. Based on current-reuse idea, the low noise amplifier and mixer are biased by the same dc current simultaneously. It consists of two blocks, the bottom is a low noise amplifier and the top is a mixer, the bias current flows through the bias current path, the RF signal pass through signal path, can be illustrated by Fig 4-2. Here, the inductors as the load can be used since the IF frequency in the transceiver architecture shown in Fig. 4-3 is high enough, $Z_L = j\omega L = j\bullet(2\pi)\bullet(800\times10^6)\bullet(15nH) \approx j75(\Omega)$, the impedance is large enough to provide high conversion gain. Moreover, the inductive load is better than resistive load since it won't consume dc power and no dc voltage-drop problem. The coupling capacitor C_C is used to couple RF signal from LNA output into mixer input, the bypass capacitor C_{b1} is used as the ac ground for RF signal avoiding RF current feedthrough.

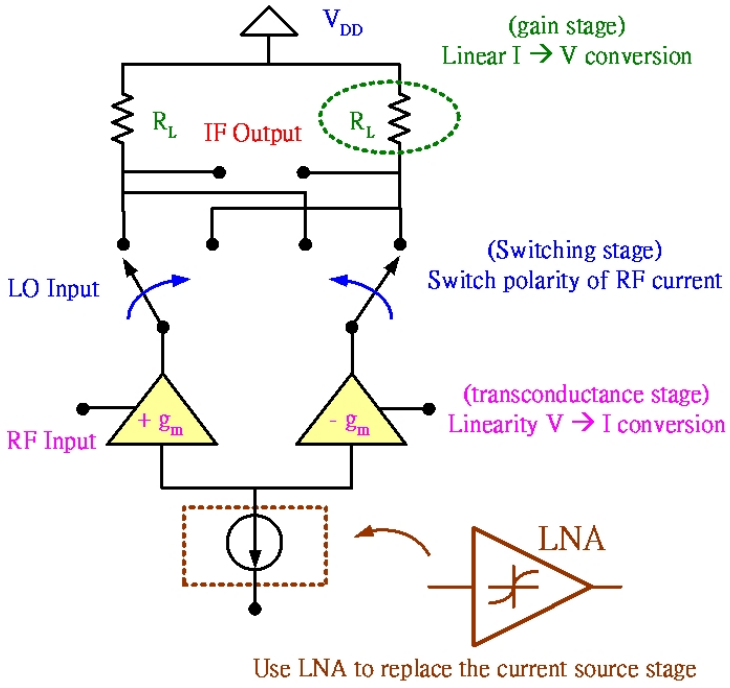


Fig. 4-1 Using a low noise amplifier to replace the current source stage.

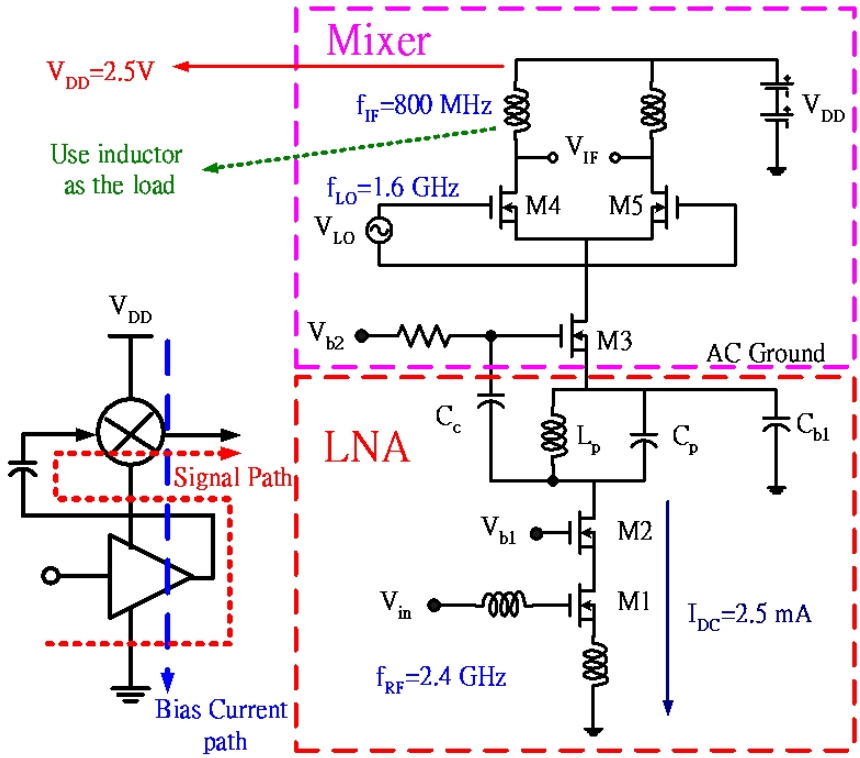


Fig. 4-2 Stacking the LNA on top of the mixer. [4]

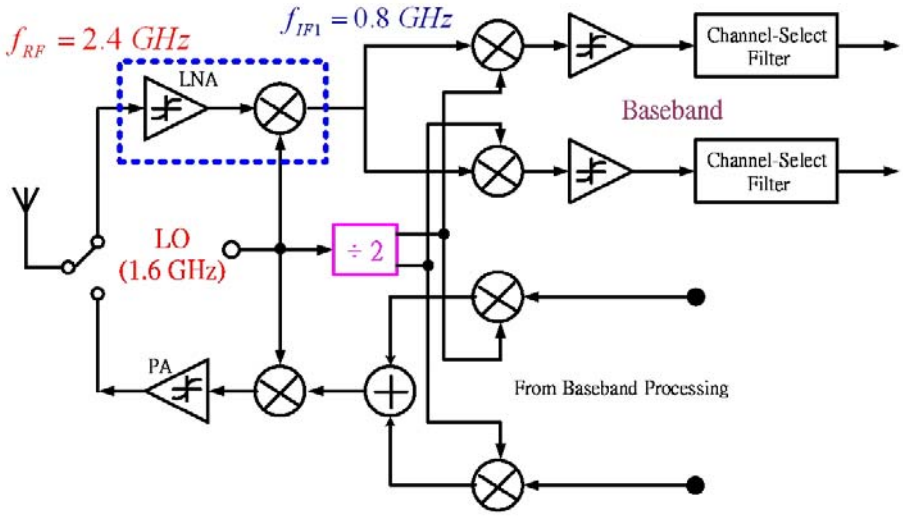


Fig. 4-3 Transceiver architecture in [4]

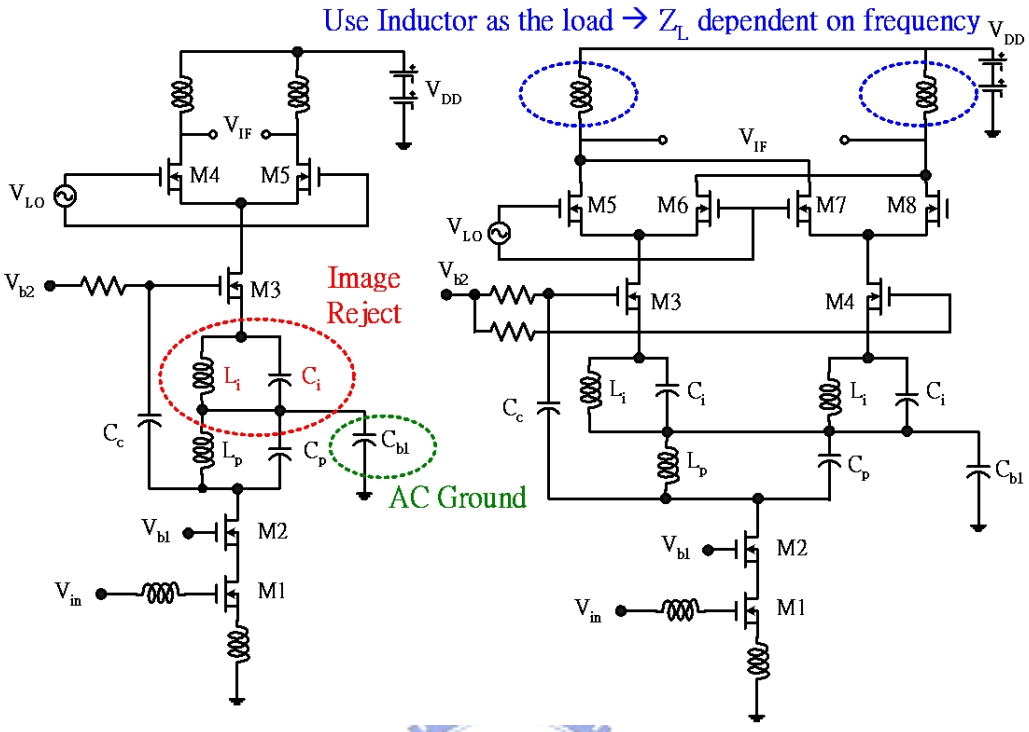


Fig. 4-4 Modified LNA/mixer combination circuits in [4]

Two modified LNA/Mixer combination circuits are presented in Fig. 4-4, they improve the port-to-port isolation and image-rejection problems. Here, the LC tank consists of L_i and C_i is designed to reject the image signal at 800 MHz. However, in order to reject the image signal, by assuming C_i equal to 1pF and referring to Eq. (4-1), large inductance is needed, but it will occupy large die area and exhibit low-Q property in CMOS technology.

$$f_{IM} = 800(MHz) = \frac{1}{2\pi\sqrt{L_i C_i}} \Rightarrow L_i = \left(\frac{1}{800\times10^6\times2\pi}\right)^2 \times \frac{1}{C_i} = 39(nH) \qquad (4\text{-}1)$$

To implement large inductance values while occupying minimal chip area, two stacked multi-layer spiral inductors shown in Fig. 4-5 are employed in [4]. These two inductors with 7 nH and 50 nH are presented by stacking two-layer and four-layer

spiral-type planar metal, respectively. The inductors exhibit a Q of approximately 3 at the frequency of interest. Another, the coupling and bypass capacitors are two passive components used in the LNA/Mixer combination circuit, are Limited by the digital CMOS process, the former (C_C) is made of a three-layer metal sandwich to reduce area. The bypass capacitor C_{b1} must be large enough to avoid current coupling to the source of the mixer input device. To implement large capacitance values with a reasonable chip area, MOS transistors with the source and drain connected to ground are used.

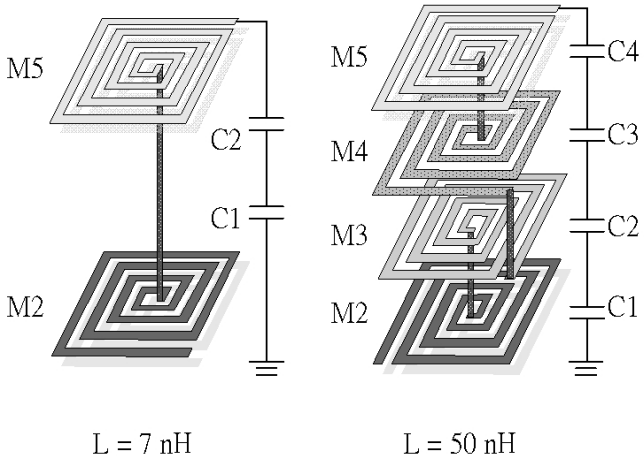


Fig. 4-5 Multi-layer inductors used in [4]

Above transceiver has been simulated, implemented and measured, the measurement results are summarized in Table 4-1. The simulation results of LNA/mixer combination circuit are also shown in Table 4-2. (using 0.25 μm CMOS technology, supply voltage is equal to 2.5 V). In this simulation, the thermal noise of transistors is lumped into the channel noise with a γ of 2.5. $\left(\overline{I_n^2} = 4kT\gamma g_m\right)$

Receiver		Transmitter	
Noise Figure	6 dB	Output Power	0 dBm
Voltage Gain	50 dB	Sidebands	-30 dBc
Image Rejection Ratio	41 dB	Power Dissipation	12 mW
Input Return Loss	12 dB	Technology	0.25- μ m CMOS
Signal/Intermodulation Ratio	26 dB	Supply Voltage	2.5 V
Power Dissipation		Area	1.83 mm × 2 mm
LNA and Mixers	6.25 mW		
Divider	3.75 mW		
Baseband Amplifiers	3.5 mW		
Baseband Filters	4 mW		
Total	17.5 mW		

Table 4-1 Measured performance of Rx/Tx in [5]

NF	3 dB
IIP3	-16dBm
I (supply current)	2.5 mA
Power consumption	6.25 mW
Total Gain	29 dB

Table 4-2 Simulation results of LNA/mixer combination circuit in [5]

In Taiwan, a research group also presents a similar LNA/mixer combination circuit for low-IF transceiver architecture [17], under the same current-reuse concept. The transceiver architecture they adopted is shown in Fig. 4-6. Also, the transistor implementation of this LNA/mixer combination circuit is shown in Fig. 4-7. Amazing, this LNA/mixer combination circuit integrates two mixers and one LNA into a single stage. The simulation results of above circuit [17], using TSCM 0.25μm 1P5M CMOS technology, will be presented in Table 4-9, comparing with [4] and this thesis.

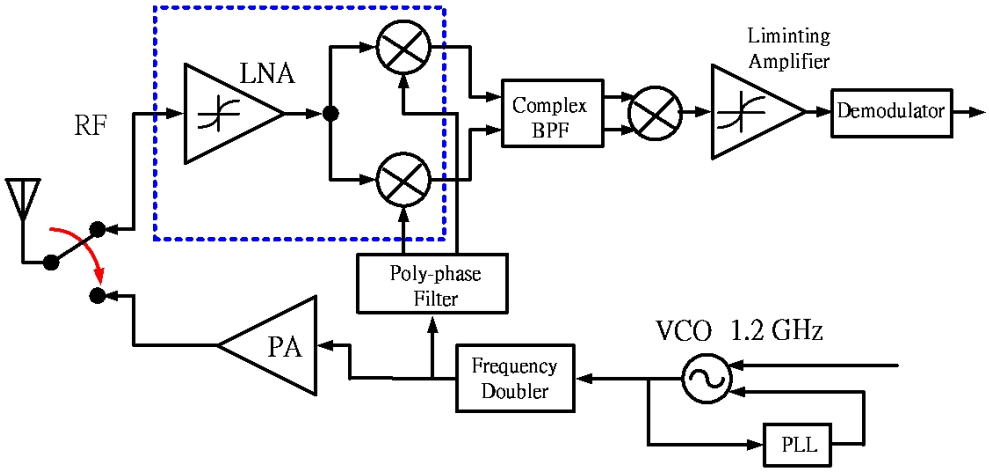


Fig. 4-6 Transceiver architecture in [17]

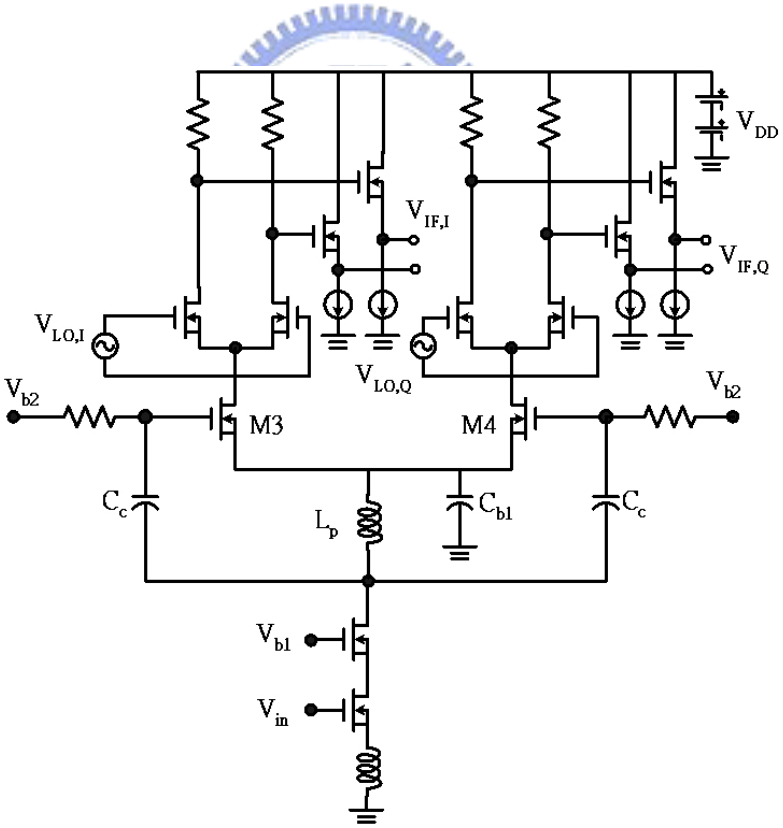


Fig. 4-7 Transistor implementation of LNA/mixer combination circuit in [17].

4.3 Proposed stacked LNA-Mixer circuit diagram

Based on above discussions about LNA/Mixer combination circuit, we also present a stacked LNA-Mixer circuit to achieve low power purpose, under the same current-reuse idea. Here, all circuits are designed, simulated and implemented by TSMC 0.18μm 1P6M CMOS technology.

■ Receiver architecture

Numbers of low-power RF receivers/transmitters have been reported [3] [4] [5] [6] [7] [8] [18]. Here, we propose a transceiver architecture for Bluetooth application as shown in Fig. 4-8. The receiver part of Fig. 4-8 is more clearly shown in Fig. 4-9. It consists of two downconversion stages and an image-reject stage, in the first downconversion stage, we propose a stacked LNA-Mixer to realize this circuit, in the second downconversion stage, the second downconversion mixer and RC-CR network realize an image-reject function illustrated in chapter 1.3.4 Hartley architecture. In this thesis, we focus on the first downconversion stage and give the simulation results and circuit layout of the highlight block named stacked LNA-Mixer.

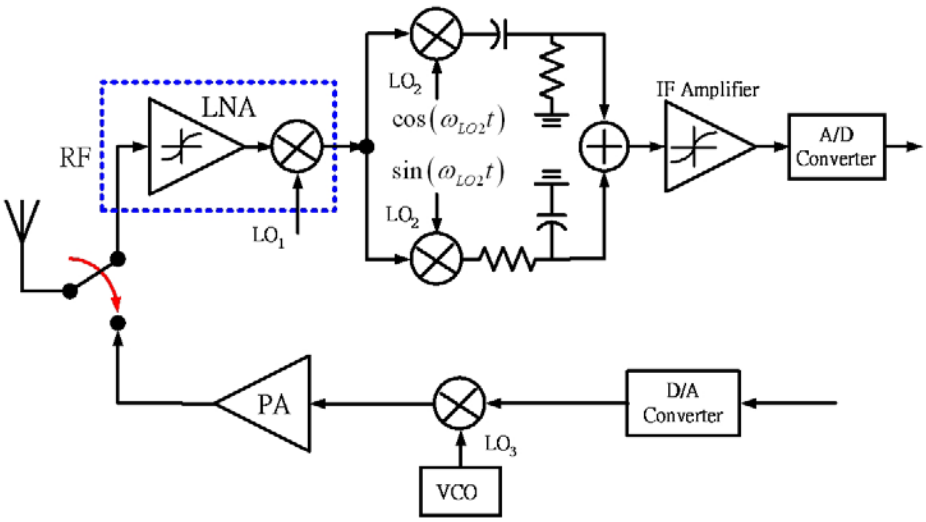


Fig. 4-8 Transceiver architecture for Bluetooth application.

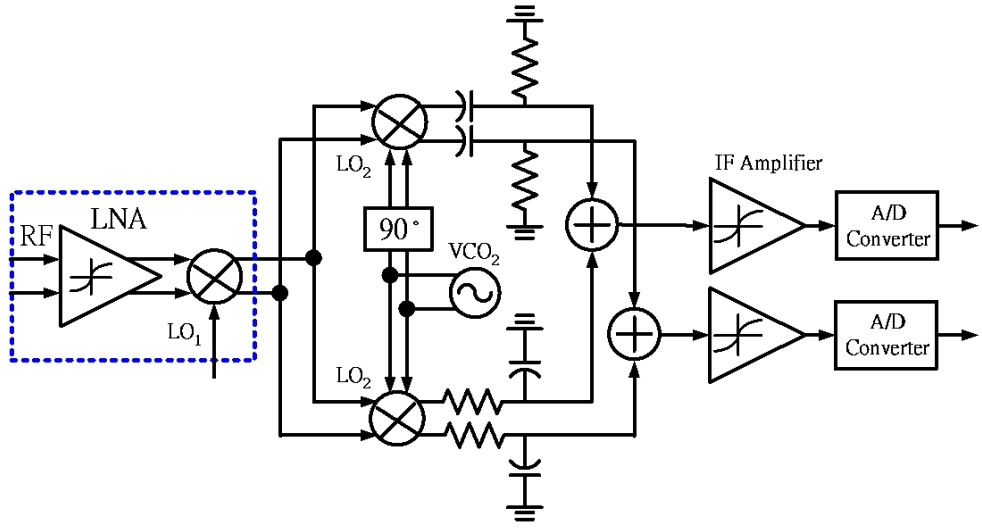


Fig. 4-9 Receiver part of Fig. 4-8.

■ Stacked LNA-Mixer circuit diagram

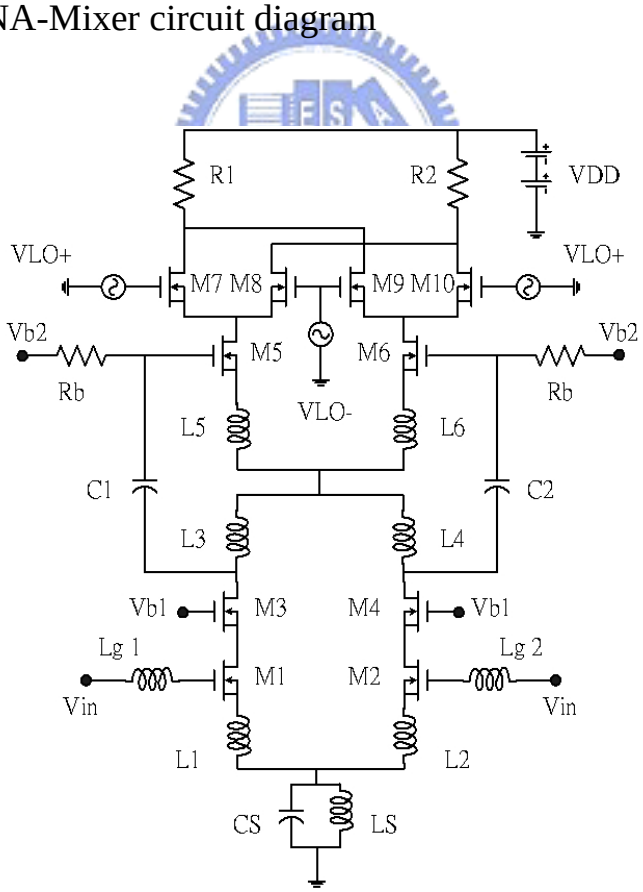


Fig. 4-10 Proposed LNA/mixer combination circuit diagram.

We propose a stacked LNA-Mixer circuit which is shown in Fig. 4-10. It consists of a fully-differential cascode low noise amplifier with inductive source degeneration and a Gilbert double-balanced illustrated in chapter 2 and 3, respectively, is shown in Fig. 4-11. The operations of this circuit can be separated into two parts: dc biasing current path and ac signal transmitted path, are shown in Fig. 4-12 clearly. The frequencies of RF input, local oscillator and intermediate band are 2.42 GHz, 2.38 GHz and 40 MHz, respectively. The capacitors C_1 and C_2 are used to couple the LNA output signals into mixer inputs. Both of them are fully-differential types.

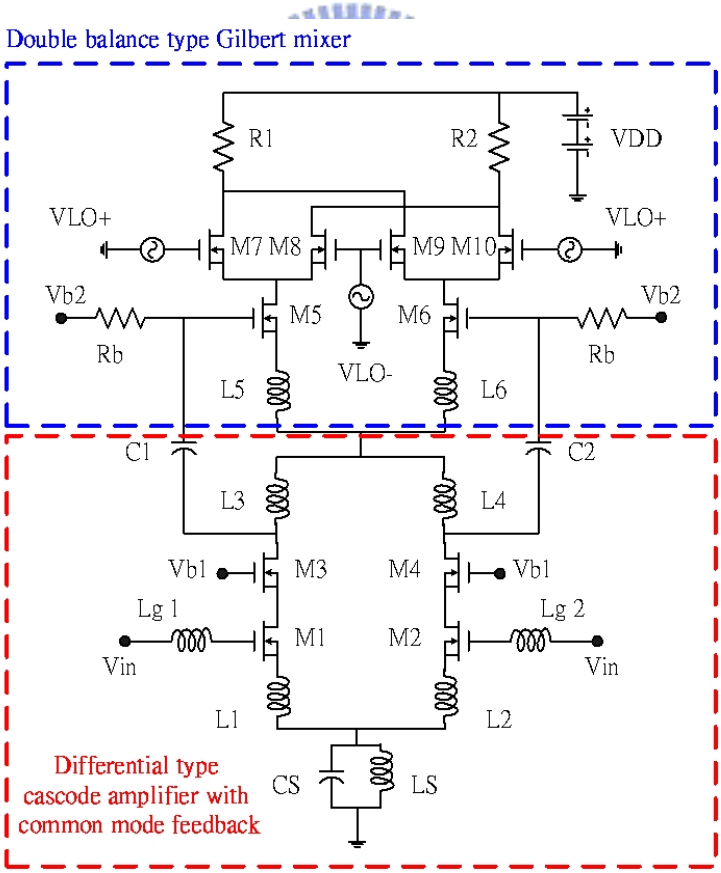


Fig. 4-11 Proposed circuit consists of a fully-differential LNA and Gilbert mixer

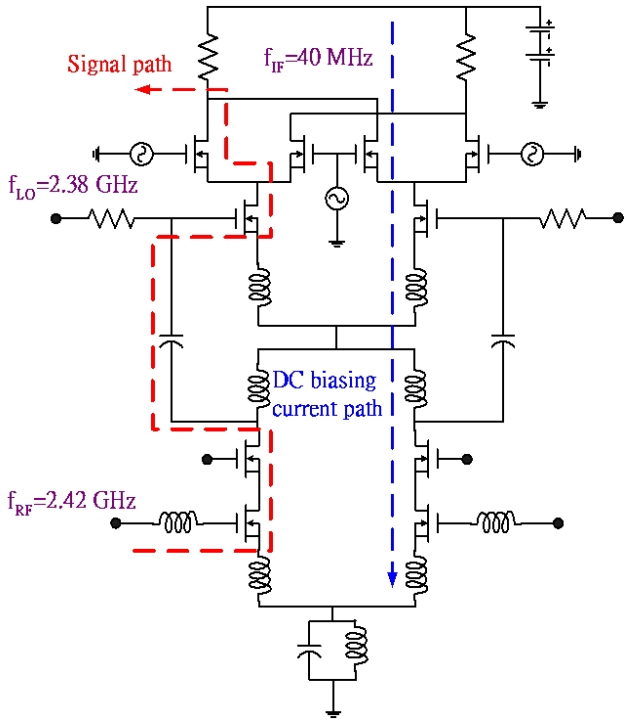


Fig. 4-12 DC biasing path and ac signal transmitted path of stacked LNA-Mixer.

■ Design considerations and steps

Next, we will illustrate the design considerations and provide the design steps while we prepare to implement such a stacked LNA-Mixer circuit. First, see Fig. 4-13, the design considerations and design steps of proposed stacked LNA-Mixer circuit are highlighted in this diagram. Refer to chapter 3, the bottom block of Gilbert mixer is a current source. Here, we use a fully-differential low noise amplifier replace this current source. The capacitor C_S and inductor L_S form a LC tank, works as a common-mode source degeneration, can degrade the common-mode gain and increase the common-mode rejection ratio (CMRR) since LC-tank provides much higher impedance than a MOS device being current source in desired RF range. For instance, the impedance of a LC-tank resonated at 2.42GHz using TSMC 0.18μm 1P6M CMOS technology is shown in Fig. 4-14. It provides very high impedance about 800 Ohm at resonated frequency 2.42 GHz.

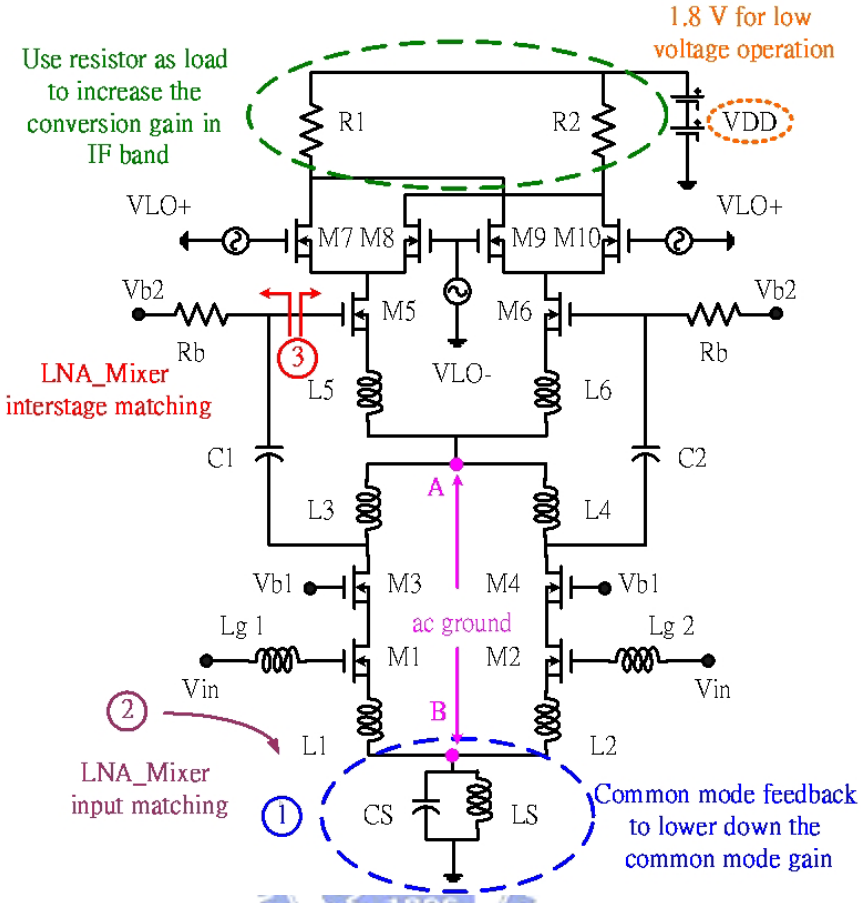


Fig. 4-13 Design considerations of proposed LNA/mixer combination circuit.

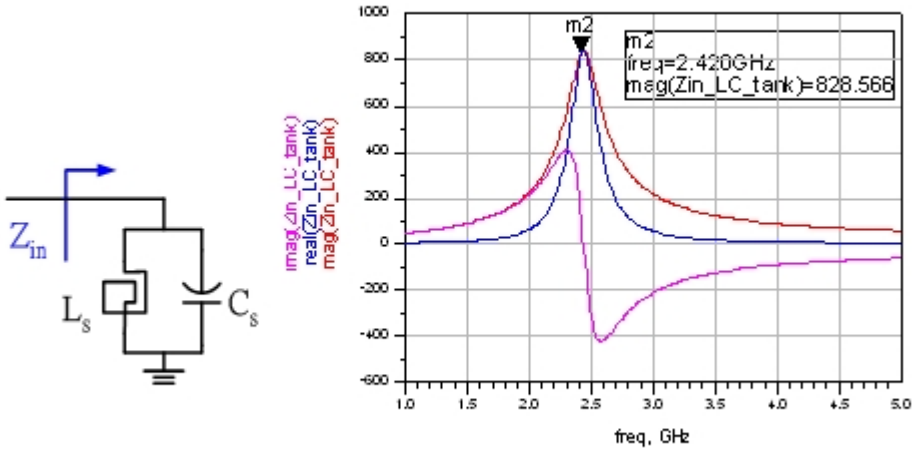


Fig. 4-14 Impedance of a LC-tank.

In order to transfer input impedance to lower level, typically 50Ω, we adopt cascode amplifier with inductive source degeneration as the low noise amplifier, that has been discussed in chapter 2. To link these two blocks, we add capacitors C_1 and C_2 to create a signal path. For maximum power transfer, complex conjugate matching is needed. In conventional design, the output impedance of LNA and input impedance of mixer must be 50Ω. Here, in RFIC design, for high integrated reason, we choose the matching conditions more freely. Since the input impedance of mixer in this circuit is $a - jb \ \ (a, b > 0)$, we must realize a output impedance of the LNA nearly to be $a + jb$. Another, why we choose fully-differential amplifier? The reason is not sensitive to the parasitic ground inductance and resistance, owing to ac ground at these nodes, has been illustrated in chapter 2. The effect that RF current feedthrough to the source of mixer is also reduced. However, an important property that we must keep in mind, the noise figure of differential type amplifier is higher than its single-ended type amplifier while consuming equal power. In other words, the differential amplifier consumes twice power compared to its single-ended amplifier while achieving the same noise figure.

Moreover, while CMOS process technology continues to scaled-down, more and more problems appear. For example, input matching to 50Ω using inductive source degeneration is more and more difficult since higher ω_T in short channel device.

$$Z_{in} = \frac{g_m}{C_{gs}} L_s = \omega_T L_s \tag{4-3}$$

From above equation, a higher ω_T needs a lower inductance value L_s to realize 50Ω input impedance. Take an example, assume $\omega_T = 2\pi f_T = 2\pi \times \left(5 \times 10^9\right)$, then $L_s = \frac{50}{\omega_T} \simeq 1(nH)$ is needed. In standard TSMC 0.18μm 1P6M CMOS technology, the minimal inductance of spiral inductor is about 2.369 (nH). To realize a

smaller inductance value, parallel several spiral inductors can be used, as shown in Fig. 4-15. However, wasting large die area is the primary drawback of this mean since spiral inductors usually occupy larger die area than other components.

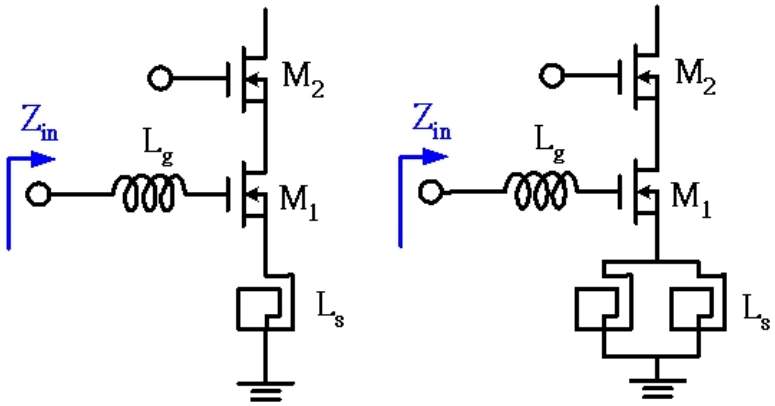


Fig. 4-15 Parallel several spiral inductors to produce lower inductance value.

Recall Eq. (3-15), the conversion (voltage) gain is proportion to R_L. According to proposed receiver architecture, the IF frequency (40MHz) is so low, using inductor as load is not feasible. In other words, large inductance value is needed if using inductors as the load. For instance,

$$Z_L = 50(\Omega) = j\omega L = j2\pi \bullet 40\times 10^6 \bullet L \Rightarrow L = \frac{50}{2\pi \bullet 40\times 10^6} = 198(nH) \qquad (4\text{-}2)$$

To realize such a large inductance value, we may series several spiral inductors, but has the same drawback, large die area and high cost. Instead of above mean, using resistor as the load is another choice, it can save the die area. Resistor is a frequency-independent component. However, using resistor as the load has another disadvantage of consuming dc power and voltage-drop on it. This problem is more serve in our stacked LNA-Mixer circuit since it decreases the dynamic range of this circuit.

Now, start up our simulations about proposed stacked LNA-Mixer. First, since in TSMC 0.18μm 1P6M CMOS technology, the typical supply voltages are 1.8V and 3.3V respectively, we set up the supply voltage of proposed stacked LNA-Mixer to be 1.8V, relax the design restrictions of PLL block and subsequent Baseband section. Separate the stacked LNA-Mixer into LNA section and Gilbert cell mixer section, design and simulate their performances individually. The supply voltages of LNA section and Gilbert cell mixer section are set to be 0.8 V and 1 V respectively, since we limit the supply voltage of stacked LNA-Mixer to be 1.8 V. Finally, we integrate them together and simulate the performances of overall stacked LNA-Mixer circuit.

4.3.1 Simulation results of LNA section

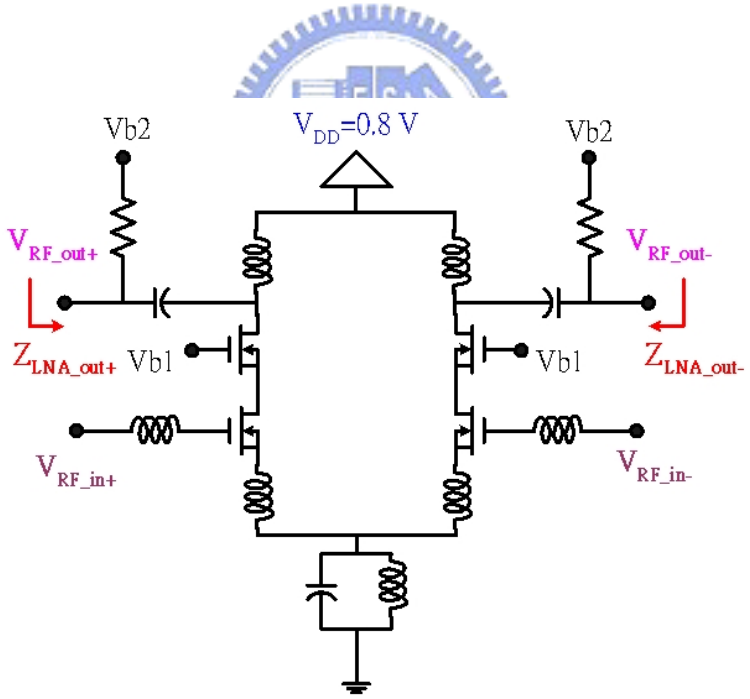


Fig. 4-16 Simulated circuit of LNA section.

The simulated circuit of LNA section is shown in Fig. 4-16. As mentioned before, it is a fully-differential cascode amplifier with inductive source degeneration, a

LC-tank is used to realize common-mode feedback and lower down common-mode gain. Here, the supply voltage is set to be 0.8V, so low that only two MOSFET can be cascode. The bottom inductors are used to match input impedance, the top inductors are used to be gain stage and match output impedance. For low-power purpose, we limit the total bias current not over 5mA, the total power dissipation of LNA section not over 4mW. According the design steps that we have illustrated in chapter 2.6, we can determine the optimum width of MOSFET under the noise figure optimization technique – fixed P_D optimization, presented by Thomas H. Lee and Derek K. Shaeffer [3]. Moreover, modify above results by note in chapter 2 since the transistors are operated in moderate inversion region. Francesco Gatta [13] suggests the optimum gate width decreases by 20~25% comparing with noise figure optimization technique presented by Thomas H. Lee and Derek K. Shaeffer [3]. The numerical calculation results are shown in Fig. 4-17 and Fig. 4-18.

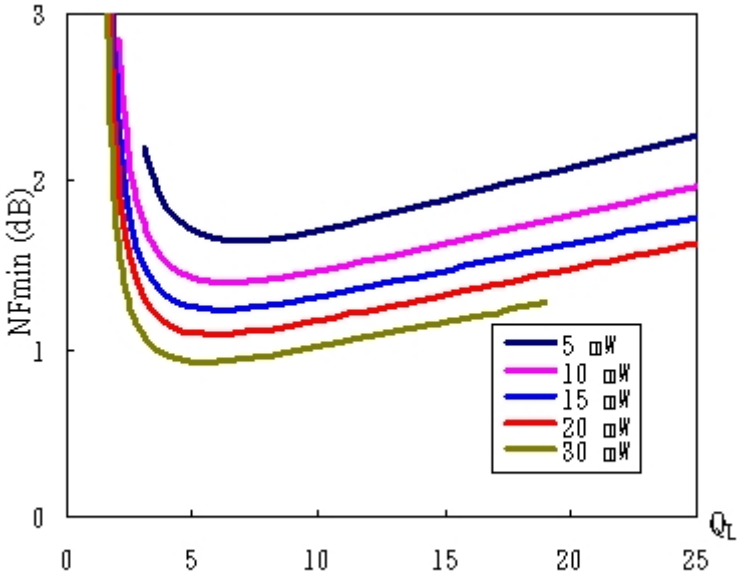


Fig. 4-17 Q value curves to device width and power consumption P_D.

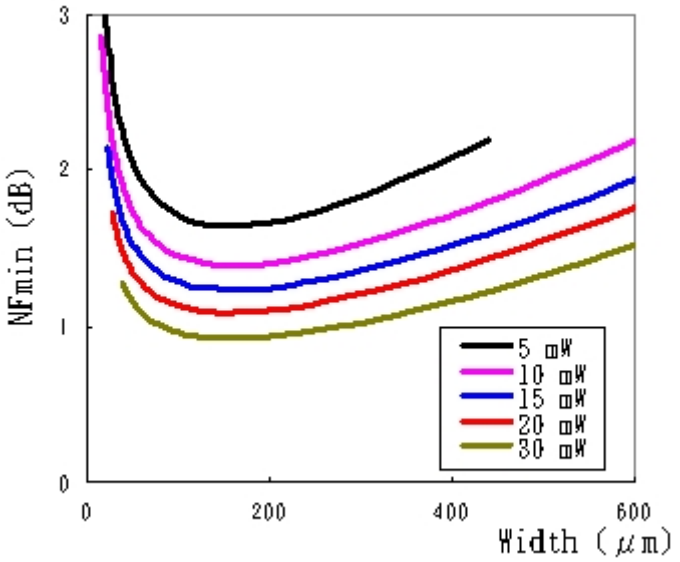


Fig. 4-18 $NF_{\min}$ curves to device width and power consumption P_D.

After that, we can determine the biasing condition and device size. Following, continue to check common-mode gain and do input and output matching. The simulation data are shown below, including S parameters, stability factor and noise figure. We also tabulate all of them in Table 4-3. Here, the IIP3 of this LNA is not simulated since the total IIP3 of a cascade stage is mainly determined by the last stage, assuming each stage has a gain greater than unity [1].

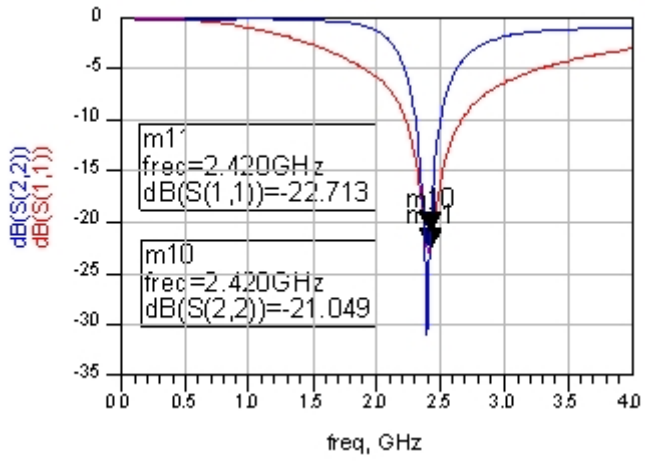


Fig.4-19 S_{11} and S_{22} of the LNA.

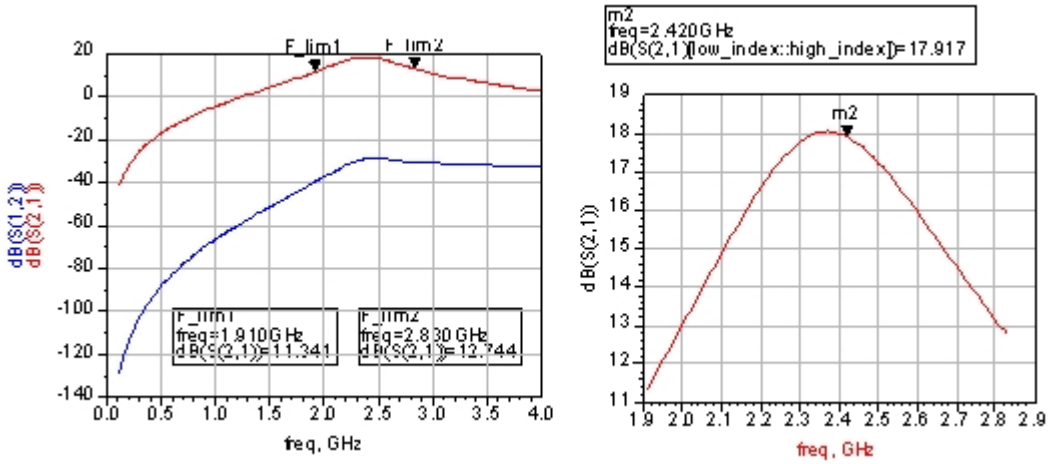


Fig.4-20 S_{21} and S_{12} of the LNA.

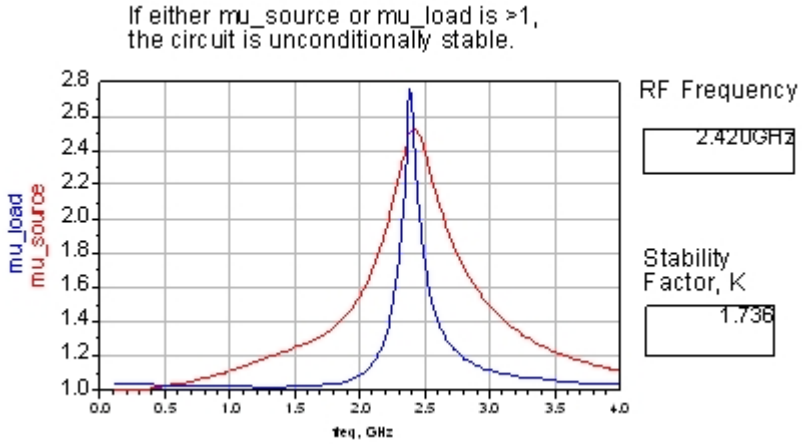


Fig. 4-21 Stability factor of the LNA

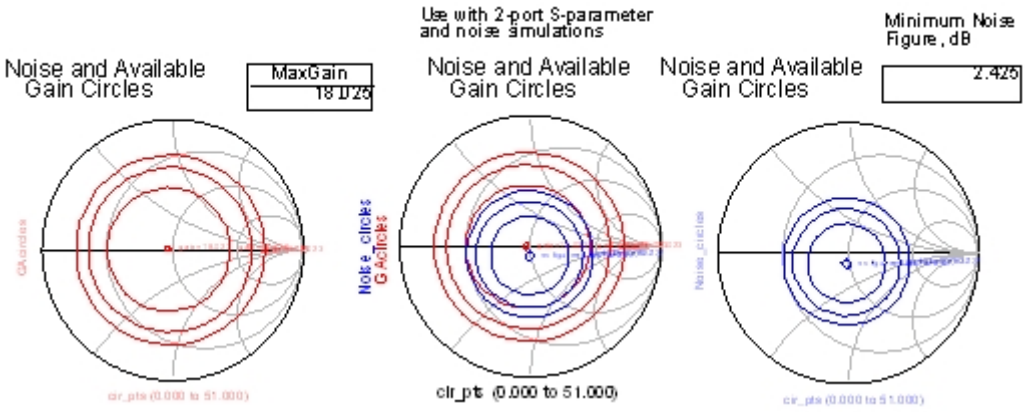


Fig.4-22 Noise circles and available gain circles of proposed LNA.

Technology	TSMC 0.18μm 1P6M
Power supply	0.8 V
Frequency	2.42 GHz
S11	-22.7 dB
S22	-21 dB
Gain	17.9 dB
Common-mode gain	-2 dB
Noise figure	2.5 dB
Power dissipation	2.8 mW

Table 4-3 Simulation summary of the LNA

4.3.2 Simulation results of Gilbert cell mixer section

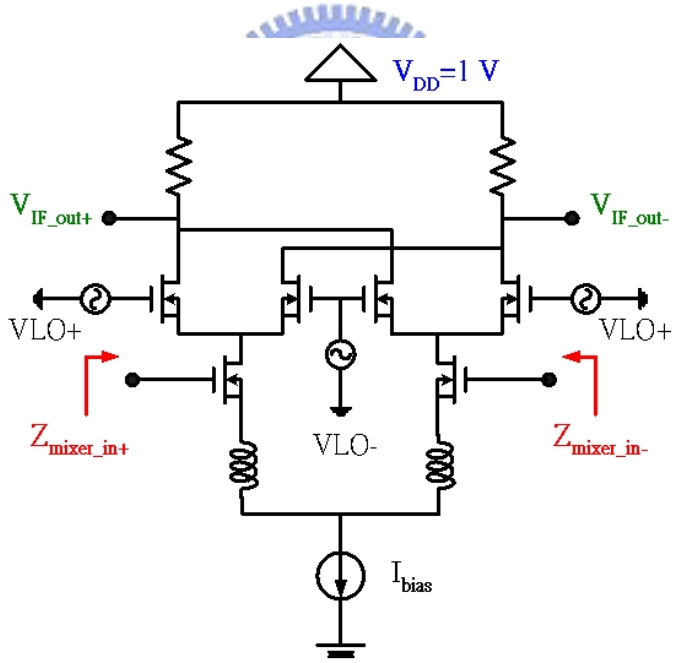


Fig. 4-23 Simulated circuit of Gilbert cell mixer section.

The simulated circuit of mixer section is shown in Fig. 4-23. As mentioned before, it is a Gilbert double-balanced mixer with inductive source degeneration to improve linearity issue, stability and match input impedance, since it provides a

positive real impedance. Here, the supply voltage is set to be 1V. The bottom of the mixer is an ideal current source, the bias current of above LNA is used here. The top resistors, have been discussed yet, are used to be gain stage. Large resistance improve the conversion gain but degrade the dynamic range. Similar to LNA design, we need to determine the devices size of the transconductance stage, provide high g_m, saturation at low V_{DS} (for low power supply operation) and low noise, also power consumption must be concerned. Based on [15], the simulation data are completed and shown below, including conversion gain, 1dB gain compression point, third-order intercept point and port-to-port isolation. The conversion gain and 1dB gain compression point of Gilbert cell mixer, both lower sideband and upper sideband, are simulated with sweeping the RF input power from -50dBm to 0dBm, are shown in Fig. 4-24 and Fig. 4-25. The V_{out} of lower sideband and upper sideband vs. RF input power are shown in Fig. 4-26. The port-to-port isolations between RF port, LO port and IF port are shown in Table 4-4. The IIP3, OIP3 and conversion gain of the Gilbert mixer vs. I_bias are presented in Fig. 4-27. Moreover, Table 4-5 is the simulation summary of this Gilbert mixer section.

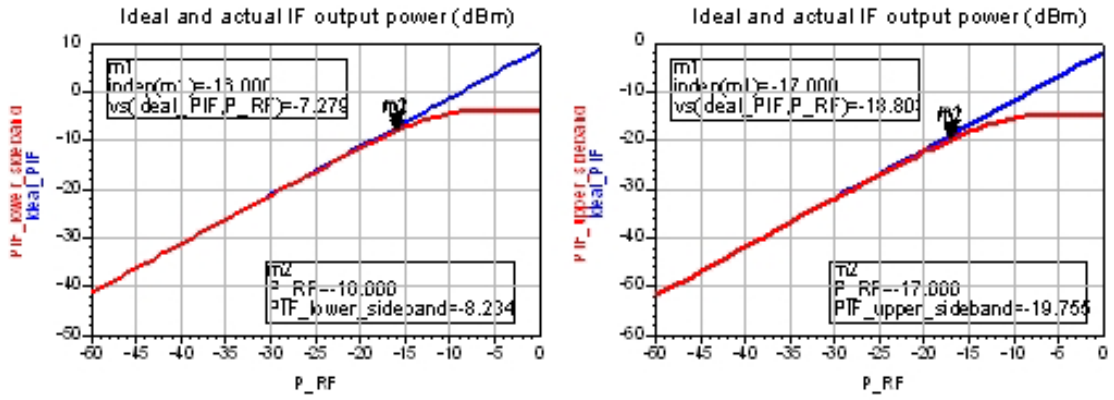


Fig. 4-24 1dB gain compression point of lower sideband and upper sideband.

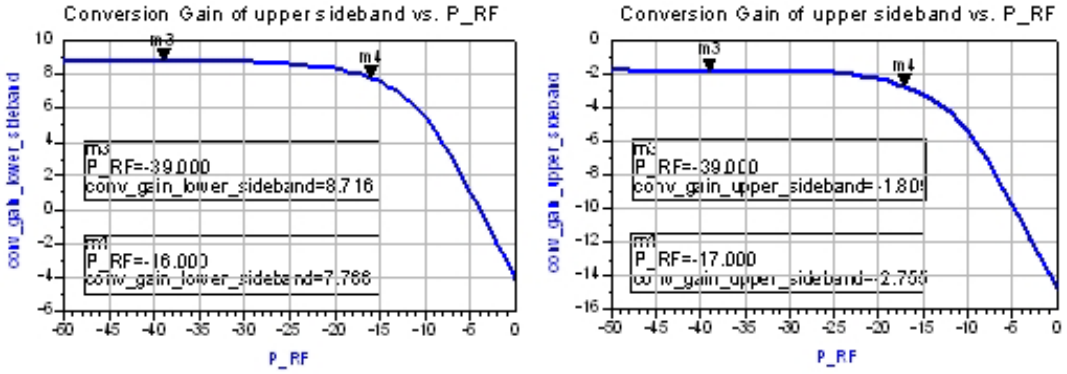


Fig. 4-25 Conversion gain of lower sideband and upper sideband signal.

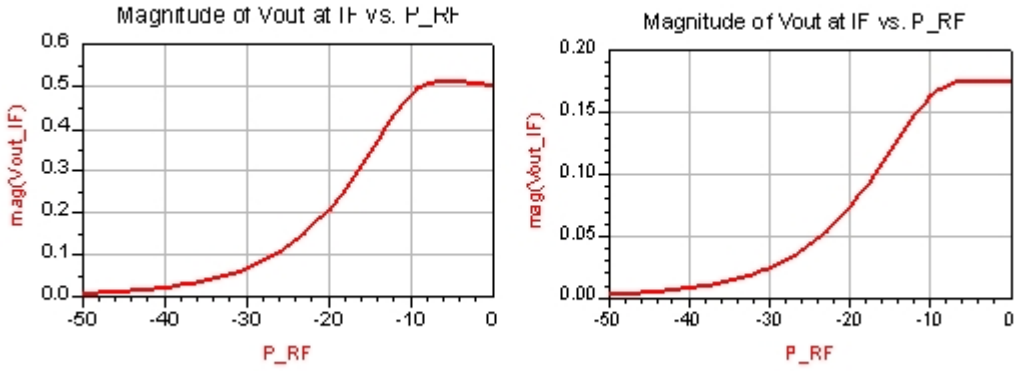


Fig. 4-26 V_{out} of lower sideband and upper sideband vs. RF input power.

freq	LO2IF	LO2RF	freq	RF2IF
2.380GHz	-183.376	-172.391	2.420GHz	-145.668

Table 4-4 Port-to-port isolation of Gilbert cell mixer section.

I_bias	conv_gain	IIP3	OIP3
0.00340	8.94235	-7.18743	1.75492
0.00345	8.94183	-7.35115	1.59068
0.00350	8.93743	-7.34342	1.59401
0.00355	8.92895	-7.13310	1.79585
0.00360	8.91620	-6.90598	2.01022

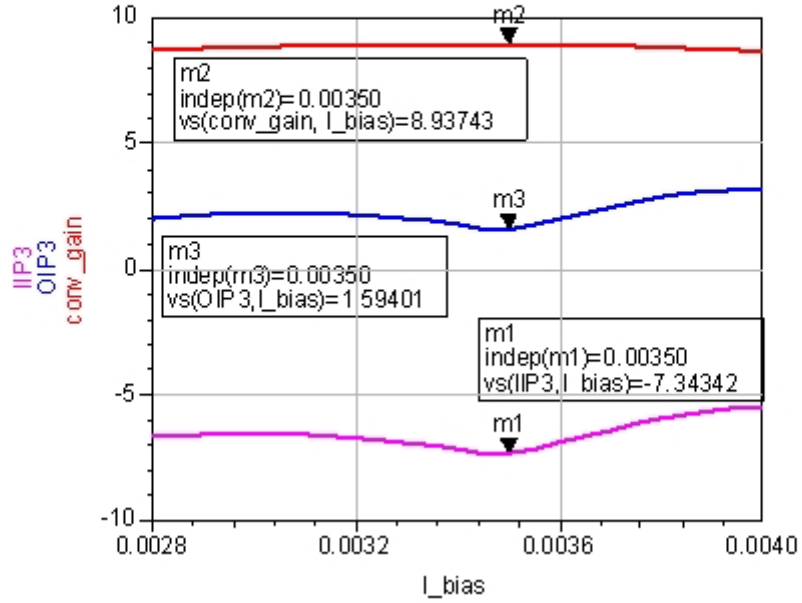


Fig. 4-27 IIP3, OIP3 and conversion gain of mixer section vs. I_bias.

Technology		TSMC 0.18μm 1P6M
Power supply		1 V
RF frequency		2.42 GHz
LO frequency		2.38 GHz
IF frequency		40 MHz
Conversion gain	(upper sideband)	-1.8 dB
	(lower sideband)	8.7 dB
P_{-1dB}	(upper sideband)	-17 dB
	(lower sideband)	-16 dB
IIP3		-7.3 dBm
Power dissipation		3.5 mW

Table 4-5 Simulation summary of the Gilbert mixer.

4.3.3 Simulation results of overall circuit

After completing simulations of above two individual sections, we start to integrate them together and simulate the overall circuit. All simulation data are completed and shown below, including input matching, conversion gain, 1dB gain compression point, third-order intercept point, noise figure and port-to-port isolation. Finally, we take a summary of overall circuit and compare with other similar arts.

- Input matching

To optimize low noise amplifier performance, both noise figure and power transfer, proper input matching is desired, has been illustrated in chapter 2. The input impedance and input return loss S_{11} of stacked LNA-Mixer are 52.2Ω and -33 dB, shown in Fig. 4-28 and Fig. 4-29, respectively. Here, the input matching network, including gate inductor and balun, are implemented by off-chip components.

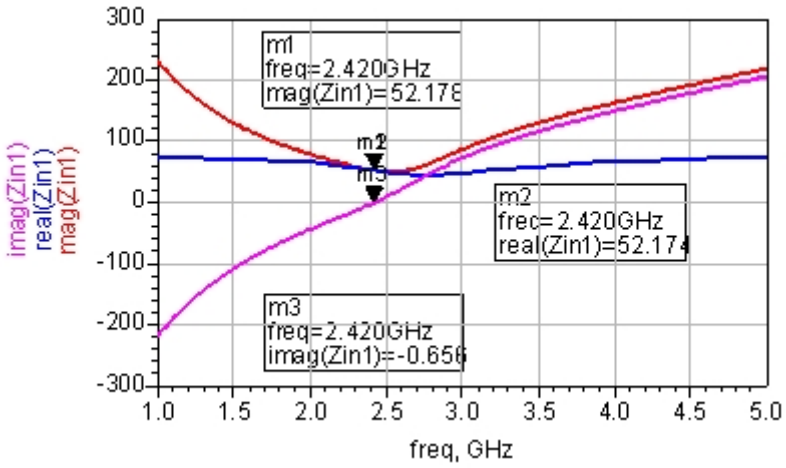


Fig. 4-28 Input impedance of stacked LNA-Mixer circuit.

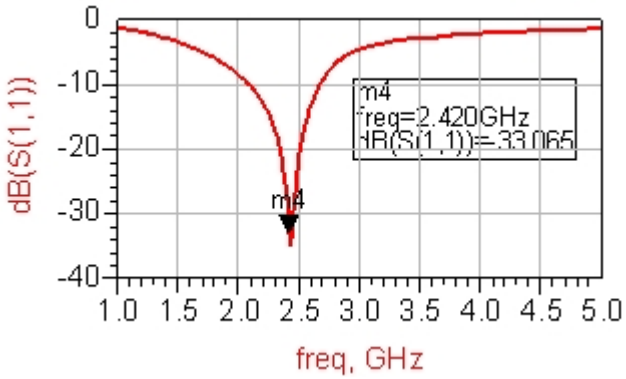


Fig. 4-29 S_{11} of stacked LNA-Mixer.

■ Conversion gain and 1dB gain compression point

Similar to mixer section, the conversion gain and 1dB gain compression point of overall circuit, both lower sideband and upper sideband, are simulated with sweeping the RF input power from -50dBm to -24dBm while LO power fixed to -5dBm, are shown in Fig. 4-30 and Fig. 4-31. The V_{out} of lower sideband and upper sideband vs. RF input power are shown in Fig. 4-32. Keep in mind one thing, the frequencies of RF input, local oscillator and intermediate band are 2.42 GHz, 2.38 GHz and 40 MHz, respectively. Based on simulation data, the conversion gain and P_{-1dB} are 24.2 dB and -28.8 dBm respectively, while the LO power fixed to -5dBm.

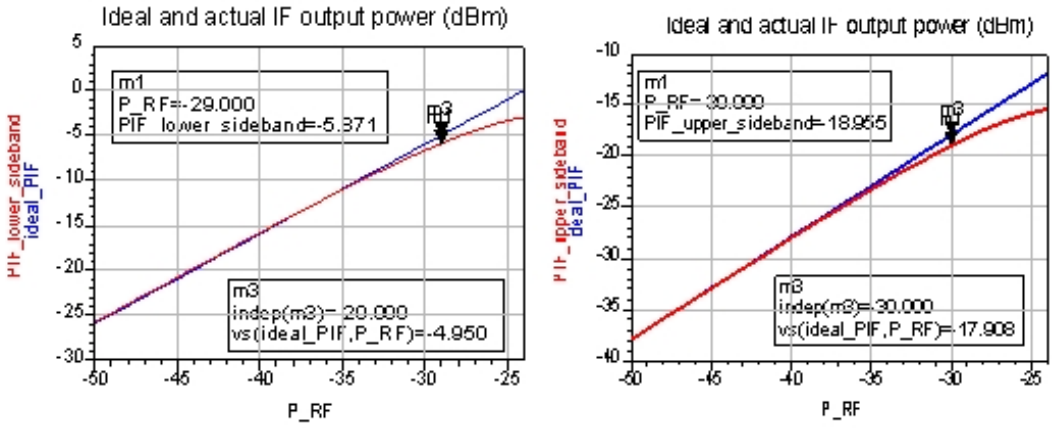


Fig. 4-30 1dB gain compression point of lower sideband and upper sideband.

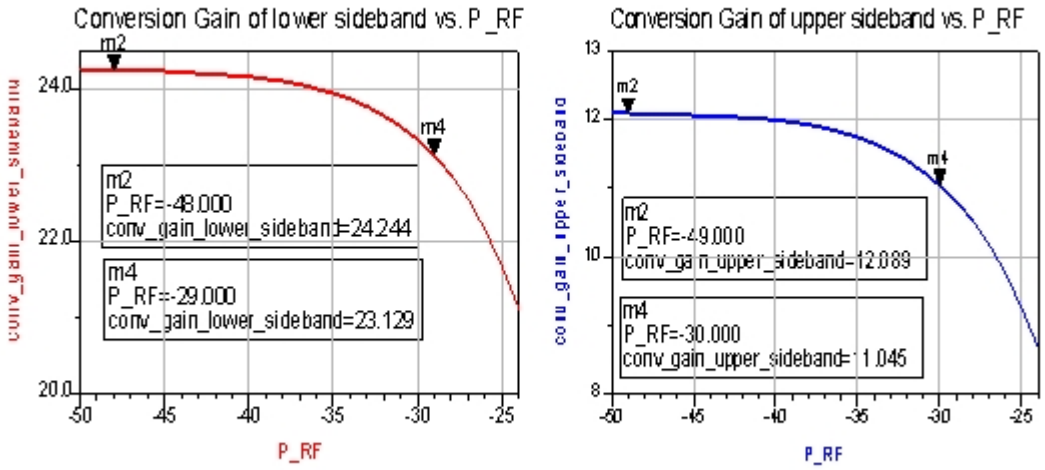


Fig. 4-31 Conversion gain of lower sideband and upper sideband signal.

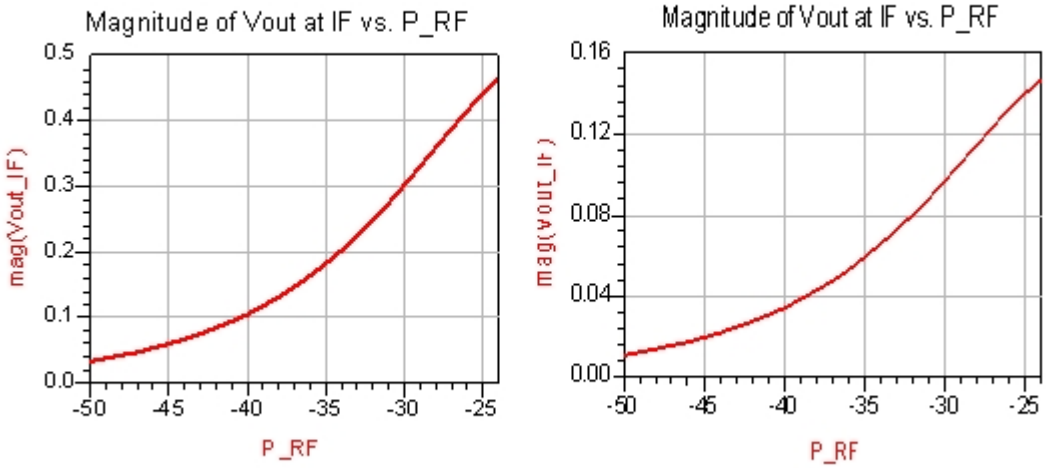


Fig. 4-32 V_{out} of lower sideband and upper sideband vs. RF input power.

■ IIP3

The IIP3, OIP3 and conversion gain of stacked LNA-Mixer are presented in Table 4-6. As mentioned before, the total IIP3 of a cascade stage is mainly determined by the last stage. In this stacked LNA-Mixer, it is mainly determined by Gilbert mixer

section, has been simulated yet. The IIP3 of Gilbert mixer section is about -7.2 dBm. However, the overall IIP3 of stacked LNA-Mixer is about -20.4 dBm, not superior enough and barely confirm to Bluetooth requirement.

freq	conv_gain	freq	IIP3	OIP3
39.99MHz	24.439	<invalid>Hz	-20.425	4.014

Table 4-6 Conversion gain and IIP3 of overall stacked LNA-Mixer.

- Noise figure

The noise figure of stacked LNA-Mixer is presented in Table 4-7. As mentioned before, the total noise figure of a cascade stage is mainly determined by the first stage, usually a low noise amplifier. In the LNA section, we get the noise figure of LNA is about 2.45 dB and a 17.9 dB available power gain, by S parameter simulation with 50 Ω source termination and $a - jb\,\Omega$ load termination. The noise figure of overall circuit is about 3.8 dB.

noisefreq	nf(2)
40.00MHz	3.776

Table 4-7 Noise figure of overall stacked LNA-mixer.

- Port-to-port isolation

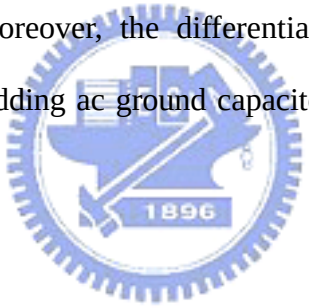
The port-to-port isolations between RF port, LO port and IF port are shown in Table 4-8. However, the isolation of RF-to-IF is not good enough, some feedthrough occurred.

freq	LO2IF	LO2RF	freq	RF2IF
2.380GHz	-112.135	-126.535	2.420GHz	-62.730

Table 4-8 Port-to-port isolation of stacked LNA-Mixer.

- Others

Initially, we assume ac ground at highlighted nodes A and B of fully-differential LNA, shown in Fig. 4-13. Hence, no ac ground device is needed. However, high frequency signal, upper sideband mixing signal at 4.8 GHz, appears at these nodes during transient analysis, especially at node A, degrade the performance of this circuit. To resolve this problem, we add large capacitance at node A to realize ac ground, and resimulate overall circuit. Moreover, the differential mixer input signal must be out-of-phase perfectly, after adding ac ground capacitor, the waveform is better than no ac ground device.



- Comparison with other arts

The overall simulation results of stacked LNA-Mixer are listed in Table 4-9. We also make a comparison with other similar arts, with LNA/mixer combination circuit [4] [17]. Table 4-10 lists the recent receiver performance, fabricated in CMOS technology. We compare with their performance in LNA section and mixer section, respectively. The stacked LNA-Mixer exhibits lower IIP3 and P_{-1dB} since the transistors are operated in edge of saturation region. But, proposed stacked LNA-Mixer consumes very low power, only 6.3 mW, without limiting the supply voltage of other stages, is the most charming excellence.

Process	0.25μm CMOS Technology [4]	TSMC 0.25μm 1P5M CMOS Technology [17]	TSMC 0.18 μm 1P6M Technology [This Thesis]
Receiver Architecture	Superheterodyne	Low-IF	Low-IF image-reject
Frequency Band	f_{RF}=2.4 GHz f_{LO}=1.6 GHz f_{IF}=800 MHz	f_{RF}=2.402 GHz f_{LO}=2.4 GHz f_{IF}=2 MHz	f_{RF}=2.42 GHz f_{LO}=2.38 GHz f_{IF}=40 MHz
Power Supply	2.5 V	2.7 V	1.8 V
I_{total}	2.5 mA	5.3 mA	3.5 mA
Conversion Gain	29 dB	19 dB	24.4 dB
Noise Figure	3 dB	3.8 dB	3.8 dB
IIP3	-16 dBm	-24 dBm	-20.5 dBm
P_{-1dB}	N/A	-34.9 dBm	-29 dBm
Power Consumption	6.25 mW	14.3 mW	6.3 mW

Table 4-9 Stacked LNA-Mixer comparison with other arts

	LNA	Mixer	Total
A 1.8 GHz CMOS low-noise amplifier 2001 [19] (Measured)	Process=0.35 um S21=10.5 dB NF=3.94 dB Power=40 mW Voltage=2.5 V		
A 1-V 2.4-GHz CMOS RF receiver front-end for Bluetooth application 2001 [20] (Simulation)	Process=0.35 um Gain=18 dB NF=5.7 dB Power=8.5 mW Voltage=1 V	Conversion Gain=-2.7 dB NF=22 dB Power=1.5 mW	
A 2 V 2.4 GHz fully integrated CMOS LNA 2001 [21] (Simulation)	Process=0.35 um Gain=19.9 dB NF=2.5 dB Power=14.7 mW Voltage=2 V		
A 6.5-mW receiver front-end for Bluetooth in 0.18-μm CMOS 2002 [6] (Measured)			Process=0.18 um Gain=21.4 dB NF=13.9 dB Power=6.5 mW Voltage=1.8 V
A Low-Power 2.4-GHz Transmitter/Receiver CMOS IC 2002 [4] (Simulation)			Process=0.25 um Gain=29 dB NF=3 dB Power=6.25 mW Voltage=2.5 V (First-Stage)
A 1V, 2.4GHz fully integrated LNA using 0.18μm CMOS technology 2003 [22] (Measured)	Process=0.18 um Gain=23 dB NF=3.8 dB Power=13 mW Voltage=1 V		

Table 4-10 Comparison with other receiver.