Chapter 5 Layout of a 1.8 V 2.42GHz Stacked LNA-Mixer

The stacked LNA-Mixer is designed and implemented in a 0.18μm 1P6M CMOS technology of Taiwan Semiconductor Manufacturing Co. Ltd. (TSMC). TSMC 0.18μm CMOS technology is a single poly, six metal layers process with low-k dielectrics. The main feature of the process is the option of copper interconnects in the top two metal layers. Upper metal layer traces, generally used to interconnect functional blocks, are typically longer and have higher resistance than intra-block traces. Using copper, rather than aluminum, reduces interconnect resistance and makes higher speeds possible. An additional property of the process is the shallow trench isolation (STI). It improves surface planarity, compared to older isolation techniques, making it possible to achieve high-reliability metallization. STI also reduces capacitive coupling between adjacent transistors, increasing circuit density and reducing power consumption.

5.1 Used components in TSMC 0.18 μm 1P6M CMOS technology

In the design of stacked LNA-Mixer, we have used several components: RF-MOS, MIM (Metal-Insulator-Metal) capacitor, spiral inductors and n+ poly resistors within and without silicide. Here, we illustrate some properties about them.

■ RF-MOS model

The models of 1.8 V RF-MOS are valid for 1.8V operation with length ranging from 0.18 ~ 0.5 μm at fixed finger width of 2.5 μm, and the valid finger numbers ranged from 4 ~ 128 and 16 ~ 128 for NMOS and PMOS, respectively. The equivalent model of RF-MOS is shown in Fig. 5-2 and only valid for specific layout and bias conditions at room-temperature 25℃. In these RF-MOS models, customers are advised not to simulate noise figure for frequency > 1GHz since the thermal noise parameter is not verified for this frequency range. Using the NF look-up table in [23] to derive noise figure are suggested, parts of them are adopted in Table 5-1. The RF-MOS model is characterized at the following bias range:

1.8V NMOS: |Vgs|: 0.6 ~ 1.8V, Vbs = 0V

The layout example of the used RF-MOS is shown in Fig. 5-1 [23]. It is a multi-finger type MOS to decrease the noise comes from gate resistor due to performing smaller resistance by parallel many small resistor at the gate. The equivalent circuit model is shown in Fig. 5-2. The following passive elements are added in Fig. 5-2:

(a) Rsb, Rdb and Rb to model the substrate resistance.

(b) Rgate to model the gate resistance.

(c) Drain / Source to bulk junction diodes.

(d) Proximity capacitance and its associated high frequency resistance.

(e) Parasitic resistance connected to the drain / source of the MOS transistors.

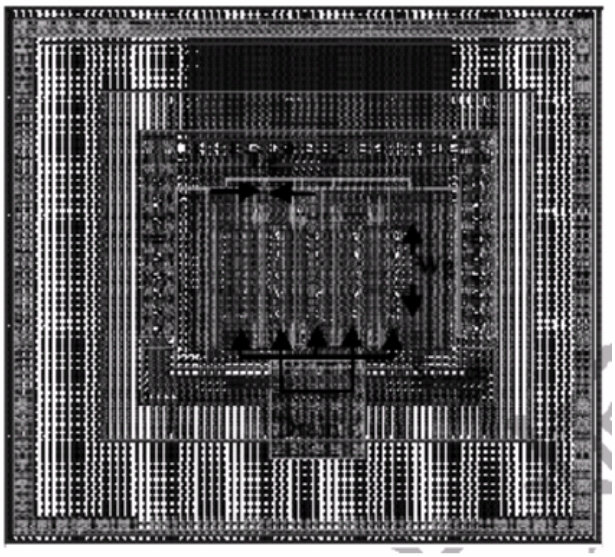

Fig. 5-1 Layout of multi-finger RF device (gate finger = 4).

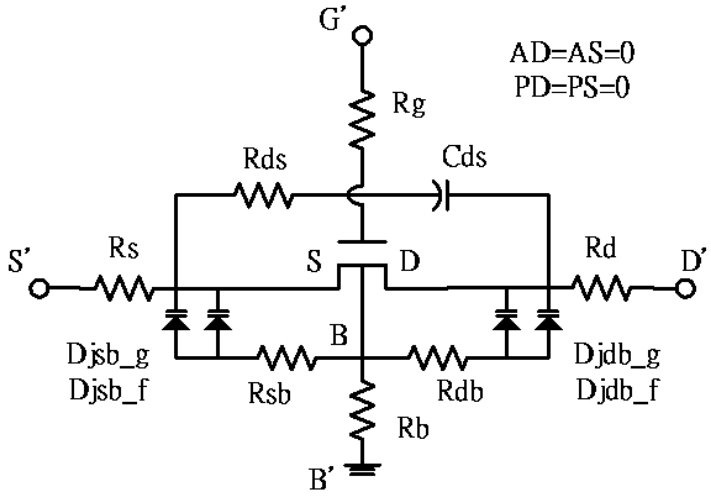

Fig. 5-2 Equivalent circuit model for the RF-MOS transistor.

■ Look-up table of noise figure model

Noise figure models of selected RF-MOS at specified operation conditions are provided in look-up table [23]. We list one of them in Table 5-1 since the used RF-MOS size and operating condition in the stacked LNA-Mixer is closed to that in Table 5-1. It must be highlighted that only devices for 1.8V NMOS with w=2.5um are tabularized. The dependence of noise figure on source admittance, for a linear

two-port device, is described by

$$F = F_{\min} + \frac{R_n}{G_S}\left[\left(G_S - G_0\right)^2 + \left(B_S - B_0\right)^2\right] \quad (5\text{-}1)$$

Where, the source admittance $Y_S = G_S + jB_S$ results in the noise figure F. In the equation, $F_{\min}$ is the minimum noise figure for the device, R_n is the noise resistance (the sensitivity of noise figure to admittance changes), and G_0 and B_0 are the real and imaginary parts for the optimum admittance which yields $F_{\min}$. These four scalar parameters $F_{\min}$, R_n, G_0 and B_0 are referred to as the "Noise parameter".

64*2.5*0.18	Noise parameter condition: (f: frequency in GHz, valid range: 1 – 6 GHz)	@2.4GHz
$V_d = 0.9\ V$	$F_{\min}(dB) = 0.835 \times \exp(-0.025 \times f)$	0.787
$V_g = 0.58\ V$	$Gamma\ Opt(Mag) = 4.02\times10^{-3} \times f^3 - 3.87\times10^{-2} \times f^2 + 1.08\times10^{-1} \times f + 0.74$	0.832
$I_d = 1.92\ mA$	$Gamma\ Opt(Ang) = -9.81\times10^{-2} \times f^3 + 1.05 \times f^2 + 4.23 \times f + 4.173$	19.00
	$R_n(Normalized) = 4.8\times10^{-3} \times f^3 - 4.52\times10^{-2} \times f^2 + 6.23\times10^{-2} \times f + 1.135$	1.091
	$Gain(dB) = -1.48\times10^{-1} \times f^3 + 1.88 \times f^2 - 9.42 \times f + 34.82$	20.97

Table 5-1 An example of look-up table used to determine noise figure.

IF we use 50Ω source termination without input matching, we can get

$$\begin{aligned} F &= F_{\min} + \frac{R_n}{G_S}\left[\left(G_S - G_0\right)^2 + \left(B_S - B_0\right)^2\right] \\ &= 0.787 + 1.091 \times \left[\left(1 - 0.832 \times \cos\left(19^\circ\right)\right)^2 + \left(0 - 0.832 \times \sin\left(19^\circ\right)\right)^2\right] \\ &= 0.917(dB) \end{aligned} \quad (5\text{-}2)$$

Moreover, with perfect input matching, we can get the minimum noise figure

$$F_{\min} = 0.787(dB)$$

■ MIM (Metal-Insulator-Metal) capacitor model

The equivalent circuit for a MIM capacitor is shown in Fig. 5-3. In this circuit, the inter-metal dielectric capacitance C_S is the main element of the capacitor, R_S and L_S are the parasitics existing in the electrodes, C_{OX}, C_{sub1} and R_{sub1} are parasitic that represents capacitance and resistance to ground due to the bottom plate metal.

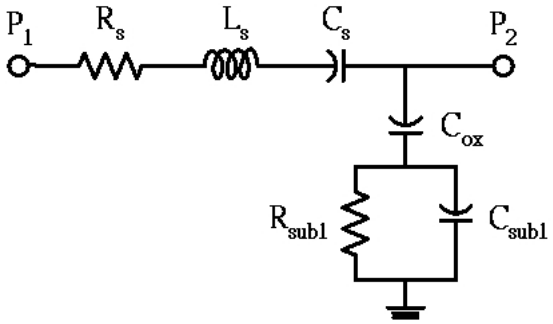

Fig. 5-3 Equivalent circuit of MIM capacitor.

■ Spiral inductor model

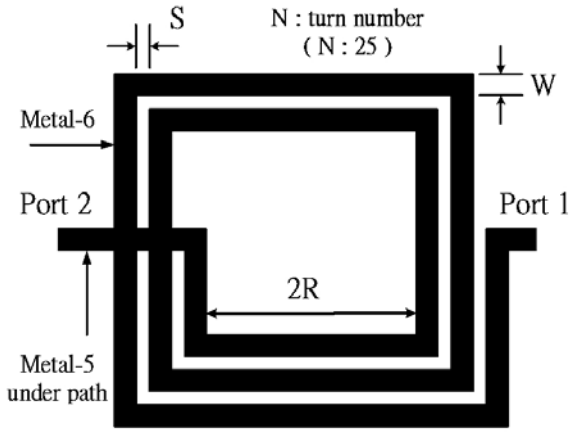

Fig. 5-4 The top view and physical dimension of spiral inductor.

The top view and physical dimension of a spiral inductor are shown in Fig. 5-4. The key parameters of spiral inductor top view are depicted in the following:

N → number of coil turns

W → metal width of top metal

S → metal space of top metal

R → radius inside inner coil

Port 1 → For network analyzer input port

Port 2 → For network analyzer output port

A lumped RLC equivalent circuit is used to model the spiral inductor and is shown in Fig. 5-5. The inductance of this spiral inductor is a function of turns, it can be extrapolated by the following equation:

$$L(nH) = 0.40425N^2 - 0.995N + 2.3295 \quad (5\text{-}3)$$

where L is inductance, and N is number of turns varied from 2.5 to 7.5. The definition of each parameter is listed below:

L_S → inductance

R_S → metal series resistance

C_S → overlap capacitance between the spiral and the center tap underpass

C_{OX} (1 and 2) → oxide capacitance between the spiral and substrate

C_{sub} (1 and 2) → silicon substrate capacitance

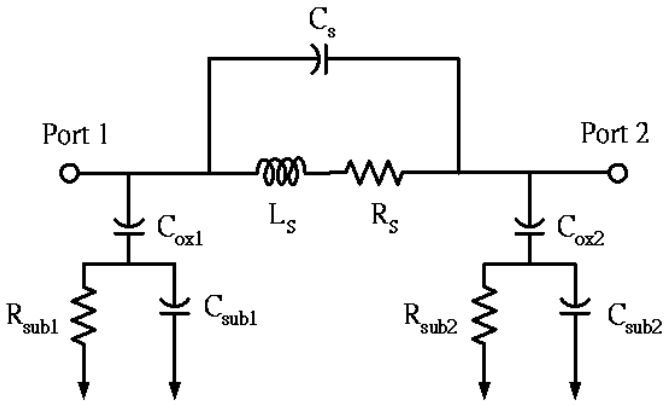

Fig. 5-5 Equivalent circuit of spiral inductor.

5.2 Layout view of stacked LNA-Mixer circuit

The layout of stacked LNA-Mixer has been completed, it occupies a die area about 1.5mm × 1.2mm, is shown in Fig. 5-6. As mentioned before, several multi-finger triple-well NMOS devices, MIM capacitors and six spiral inductors with large sizes are used. To reduce the disturbance from upper sideband signal, we add a capacitor to create a ac ground path, illustrated in chapter 4.3.3.

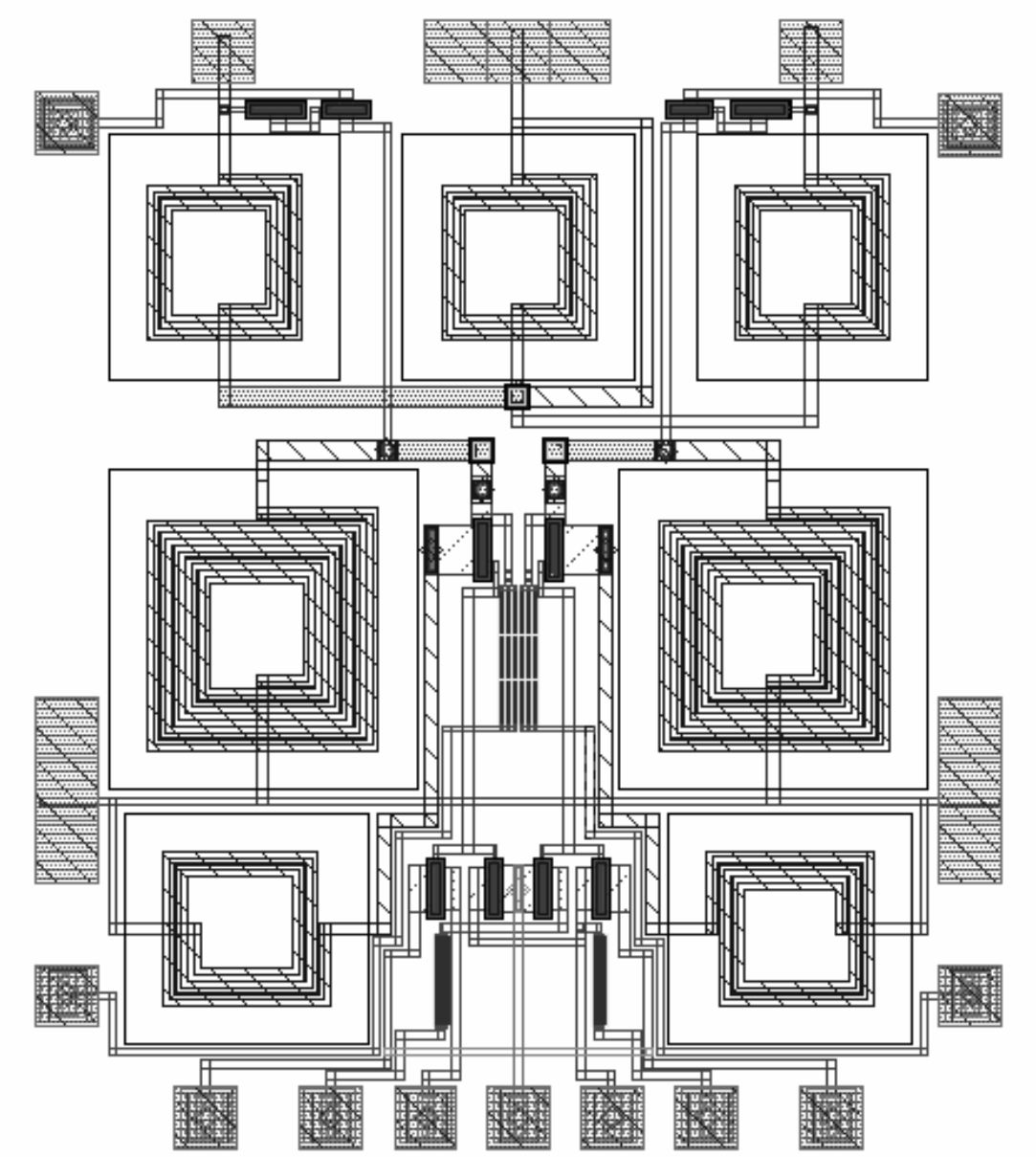

Fig. 5-6 Layout of stacked LNA-Mixer.