Chapter 6 Conclusions and Future Works

6.1 Conclusions

In this thesis, we present a low-power RF receiver front-end with stacked LNA-Mixer using TSMC 0.18μm 1P6M CMOS technology. This stacked LNA-Mixer is designed as the first stage of an integrated low-IF image-reject receiver under development for Bluetooth applications. The frequencies of RF input, local oscillator and intermediate band are at 2.42 GHz, 2.38 GHz and 40 MHz, respectively. Under such a receiver architecture, we can avoid using large inductors and capacitors. Based on simulation results, the stacked LNA-Mixer circuit only consumes 6.3 mW under the 1.8V supply voltage condition. LO available power requirement is -5 dBm at 2.38GHz frequency band. The conversion gain of overall circuit is about 24.4 dB. Noise figure is about 3.8 dB at 40 MHz IF. Input 1-dB gain compression point is -29 dBm while IIP3 point is at -20.5 dBm. The entire stacked LNA-Mixer occupies a die area of 1.5mm × 1.2mm. Although this circuit exhibits poor IIP3, P_{-1dB} and dynamic range due to the transistors are operated at the edge of saturation region and using resistors as the load. In order words, this circuit structure has an inherent shortcoming due to it is operated with tight overdrive of each transistor results poor performance of IIP3 and P_{-1dB}. However, this circuit only consumes 6.3 mW, while without limiting the supply voltage of subsequent stages, is the most charming excellence. Low-power dissipation makes this stacked LNA-Mixer attractive for low-power highly integrated receiver applications.

To implement these circuits, proper layout is needed. Not to reduce performance, we need to concern about many issues such as the mismatch, power line distribution, metal width, signal cross coupling and noise isolation. Moreover, for impedance matching, the circuit leads inductors in design, but inductors are not appropriate to be used in CMOS process because the loss of substrate of CMOS process inherently is considerable and thus quality factor of inductor is low. Recently, many research groups devote to implement inductors with high inductance value and high-Q but occupy small area. Hence, the inductors-research becomes a hot issue in RF design.

CMOS RFICs are widely used in many applications since it possesses the advantage of low-cost and high integration ability. Also, the accurate models of active and passive components at all RF frequency are needed that to make the circuit design more correct and easier.

6.2 Future works

Up to now, the circuit simulation and layout are carried out. It will be taped out and measured in the few days. Moreover, the VCO stage and subsequent stages of proposed receiver also must be simulated, implemented and measured. Another, we must invent more types of inductor, such as multi-layer sandwiched inductor and symmetrically circular inductor, with high inductance value and high-Q but occupy small chip area.