Complementary UWB LNA Design Using Asymmetrical Inductive Source Degeneration

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***Abstract*—This letter proposes a novel LNA design method where the complementary transistor topology is combined with asymmetrical inductive source degeneration to achieve matched input impedance over a wide bandwidth. A 2–10 GHz LNA is designed and fabricated using a commercial 0.18 μm RF-CMOS process to verify the feasibility of our proposed method. In the intended bandwidth, this LNA has matched input impedance, 20 dB power gain, and 2.4–3.4 dB noise figure, with 25.65 mW power consumption.**

***Index Terms*—Complementary, input matching, low noise amplifier (LNA), source degeneration, wideband.**

I. Introduction

THE use of complementary, or known as current re-use, method has been demonstrated in CMOS low noise amplifier (LNA) design to achieve broadband input matching where the equivalent 50 Ω input impedance is made possible by the coupled gate-drain inductors and the loading capacitor [1]. With the external resistive drain bias circuit no more needed in the complementary topology, not just the signal loss can be minimized; noise performance of the amplifier can also be improved. However, since the two coupled inductors are themselves large and lossy, the unavoidable signal attenuation will raise the amplifier's noise figure. In [2], the ultra-wideband LNA mainly utilizes shunt-shunt resistive feedback to achieve input matching; however, the use of the feedback resistor inevitably deteriorates the amplifier's noise. In this letter, we propose a new wideband CMOS LNA design method that is combining the complementary topology with asymmetrical inductive source degeneration. By omitting the use of large inductors and a feedback resistor, superb noise performance can now be expected. As shown in Fig. 1, the complementary transistors have their gate nodes joined together as the input of the amplifier while their common drain is connected to a loading C_d; the two small inductors $L_{s,n}$ and $L_{s,p}$ are used for source degeneration. By properly adjusting the values of these two inductors for a given C_d, low noise figure and wideband input matching can be achieved simultaneously.

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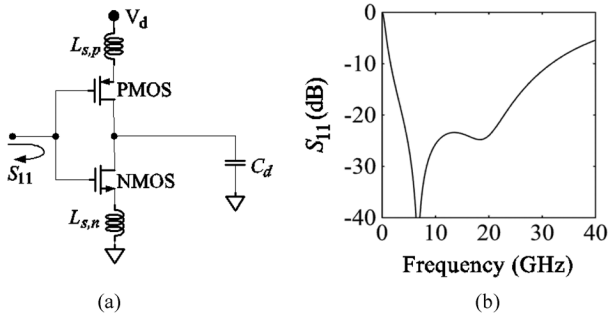

Fig. 1. (a) Proposed method of combining the complementary transistors with asymmetrical source inductors for wideband input matching and low noise figure. The equivalent loading C_d comes from the following stage. (b) The corresponding input reflection coefficient S_{11}.

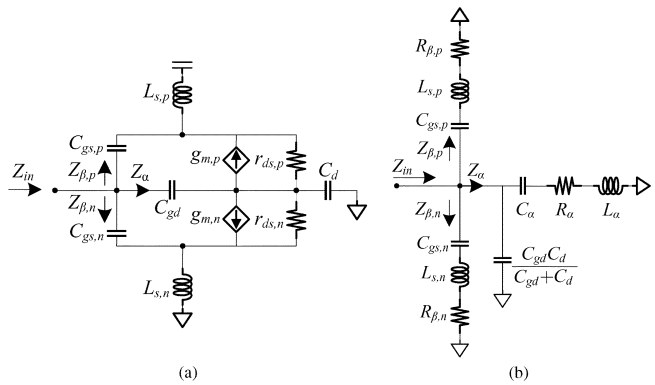

Fig. 2. (a) Small-signal circuit of our complementary transistors with loading capacitor C_d. (b) The rearranged equivalent circuit.

In the following sections, the input matching mechanism will be analyzed first; a 2–10 GHz LNA is then designed and fabricated using commercial 0.18 μm RF-CMOS process. Important parameters such as S-parameters, noise figure, and input-referred third-order intercept point (IIP3) are measured and compared with LNA's designed by other research groups.

II. Input Matching Analysis

To facilitate the analysis of our complementary transistors with inductive source degeneration, the corresponding small signal circuit is presented, as shown in Fig. 2(a), where C_d is the equivalent loading capacitor that comes from the following stage. Two feedback mechanisms can be identified here: one is from the two source inductors, $L_{s,n}$ and $L_{s,p}$, and the other from C_{gd}. Employing the local series-series feedback theory and the local shunt-shunt feedback theory, the two source inductors, $L_{s,n}$ and $L_{s,p}$, and C_{gd} can be absorbed, respectively,

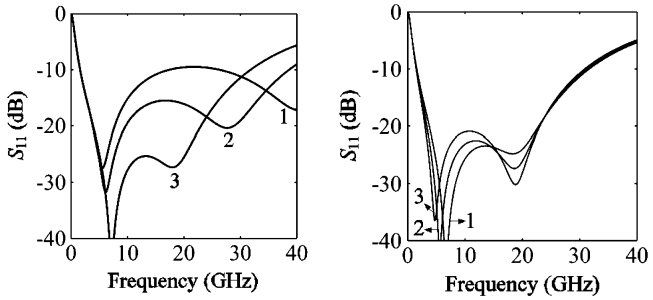

Fig. 3. Simulated input reflection coefficients of our proposed circuit. (a) Curves 1–3 correspond to $L_{s,p} = 0.2$, 0.3, and 0.4 nH, and all have their $C_d = 0.2$ pF and $L_{s,n} = 0.7$ nH. (b) Curves 1–3 correspond to $L_{s,n} = 0.7$, 0.8, and 0.9 nH, and all have their $C_d = 0.2$ pF and $L_{s,p} = 0.4$ nH.

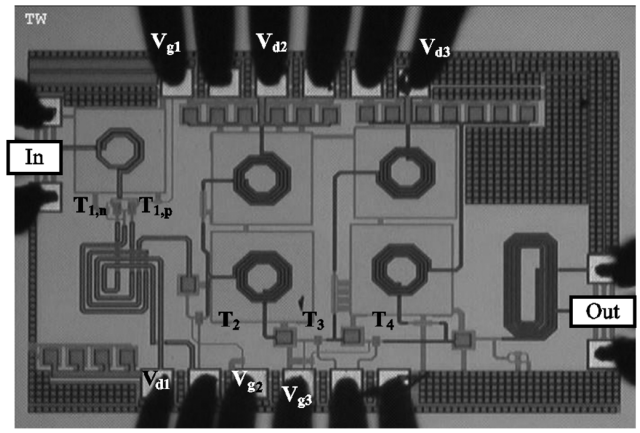

Fig. 4. Photograph of the 2–10 GHz LNA. The chip size is $1250 \times 850\ \mu\mathrm{m}^2$. $\mathrm{T}_{1,\mathrm{n}}$, $\mathrm{T}_{1,\mathrm{p}}$ are the complementary transistors; T_2, T_3, and T_4 are the second-, third-, and forth-stage transistors.

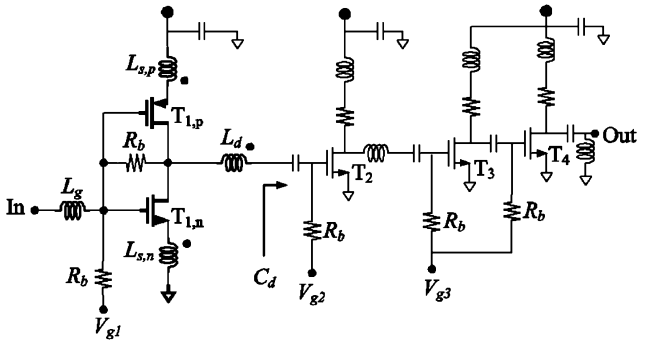

Fig. 5. Schematic of our proposed LNA. The equivalent loading capacitor C_d is 0.3 pF, L_d is 1 nH, $L_{s,n}$ is 0.6 nH, and $L_{s,p}$ is 0.5 nH, L_g is 0.5 nH. The bias resistors R_b are all 5185 Ω.

and the circuit can then be re-arranged as that shown in Fig. 2(b) with

$$R_{\beta,n} = \frac{g_{m,n}L_{s,n}}{C_{gs,n}}; R_{\beta,p} = \frac{g_{m,p}L_{s,p}}{C_{gs,p}}$$
$$C_\alpha \cong (g_{m,n} + g_{m,p})\left[\frac{1}{r_{ds,n}} + \frac{1}{r_{ds,p}}\right]^{-1} C_{gd}$$
$$R = (g_{m,n} + g_{m,p})^{-1}\frac{C_{gd} + C_d}{C_{gd}};$$
$$L_{\alpha,n} = \left(\frac{1}{L_{s,n}} + \frac{1}{L_{s,p}}\right)^{-1}\frac{C_{gd} + C_d}{C_{gd}}. \quad (1)$$

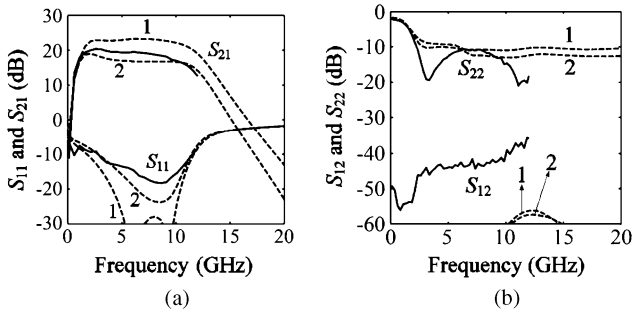

Fig. 6. Measured and simulated S-parameters of the 2–10 GHz wideband LNA. (a) Measured (solid-curve) and simulated (dashed-curve) S_{21} and S_{11}. (b) Measured and simulated S_{12} and S_{22}.

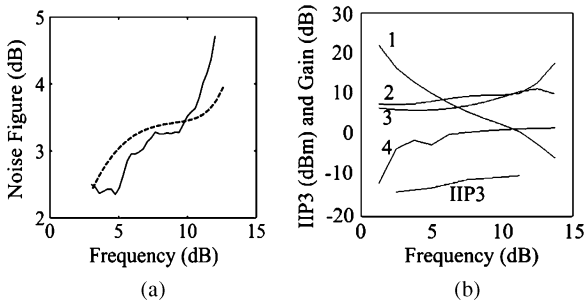

Fig. 7. Noise figure, measured IIP3, and simulated gain of each stage of the 2–10 GHz wideband LNA. (a) Simulated (dashed curve) and the measured (solid curve) noise figure. (b) Measured IIP3, and simulated gain of each stage, where curves 1–4 correspond to the gain of stages 1–4, respectively.

Examining (1) and the equivalent input circuit, we know Z_α accounts for the low frequency response, and $Z_{\beta,n}$ and $Z_{\beta,p}$ play their roles at high frequency. The transistors' sizes are chosen to equate R_α with 50 Ω approximately, thus the real part of Z_{in} can be determined. And, the value of $L_{s,p}$ is chosen to determine the input matching over wide bandwidth, then $L_{s,n}$ can be used to trim the low frequency characteristic. Here, with $g_{m,n} = 43$ mS, $r_{ds,n} = 678\ \Omega$, $C_{gs,n} = 134$ fF, $C_{gd,n} = 55$ fF for the NMOS, and $g_{m,p} = 21.8$ mS, $r_{ds,p} = 1070\ \Omega$, $C_{gs,p} = 156$ fF, $C_{gd,p} = 59$ fF for the PMOS, the simulated input reflection coefficient (S_{11}) is shown in Fig. 3(a) where curves 1–3 correspond to $L_{s,p} = 0.2$, 0.3, 0.4 nH, respectively, and all have $C_d = 0.2$ pF and $L_{s,n} = 0.7$ nH. Fig. 3(b) shows the simulated input reflection coefficient with different $L_{s,n}$ where curves 1–3 have $L_{s,n} = 0.7$, 0.8, 0.9 nH, respectively, and all have $C_d = 0.2$ pF and $L_{s,p} = 0.4$ nH. Obviously, by manipulating the source inductors, we can obtain wideband-matched input impedance. Specifically, with the chosen values of $L_{s,n}$ and $L_{s,p}$, $R_{\beta,n}$ is greater than $R_{\beta,p}$, thus the impedance of the $Z_{\beta,n}$ is greater than that of $Z_{\beta,p}$ and can be omitted. The wideband input matching mechanism can now be comprehended as the composite effects of the two low quality factor resonators which have their impedances Z_α and $Z_{\beta,p}$.

III. LNA Design and Experimental Results

With the matching mechanism explored, a wideband CMOS LNA that covers 2–10 GHz is designed and fabricated using TSMC 0.18-μm RF-CMOS process. Figs. 4 and 5 show the photograph and schematic of the four-stage circuit where the

TABLE I
PERFORMANCE COMPARISON OF LNA CIRCUITS PRESENTED IN PRIOR WORKS AND THE PROPOSED CIRCUIT

	BW (GHz)	S_{21}(dB)	S_{11}(dB)	NF (dB)	P_{diss} (mW)	Topology	Technology	FOM
[1] RFIC 2006	3.1~10.6	10.8~12	<-11.2	4.7~5.6	10.57	Complementary	0.18μm CMOS	1.95
[3] TMTT 2008	DC~13	6	<-12	2.7~5	22	Distributed	0.18μm CMOS	1.24
[4] JSSC 2007	1.2~11.9	6.7~9.7	<-11	4.5~5.1	20	Noise-Canceling	0.18μm CMOS	1.15
[5] MWCL 2007	2.7~9.1	10	<-10	3.8~6.9	7	Distributed	0.18μm CMOS	2.1
[6] MWCL 2010	3.1~10.6	13.2	<-9	4.5~6.2	23	Common Gate	0.18μm CMOS	0.99
[7] MWCL 2009	3~10.35	9.5~12.5	<-8.3	3.3~11.4	7.2	Common Gate	0.13μm CMOS	3.63
[8] MWCL 2008	DC~11.5	12.2~14.2	<-8	5.6	9.1	Complementary	0.13μm CMOS	2.98
[9] MWCL 2007	3.1~10.6	12~13	<-12	3.4~4	12.9	Common source	0.15μm pHEMT	2.69
This work	**2-10**	**17-20**	**<-12**	**2.4~3.4**	**25.65**	**Complementary**	**0.18μm CMOS**	**3.04**

complementary transistor topology is combined with asymmetrical inductive source degeneration, The couplings between $L_{s,n}$, $L_{s,p}$, and L_d (for gain boosting) allow the reduction of chip size. Although the magnetic couplings alter the input match slightly, the inductor values are then adjusted to recenter the matching and resonance characteristics. The small gate inductor L_g is used for S_{11} tweaking. Fig. 6 shows the measured and simulated S-parameters of this LNA where both S_{11} and S_{22} are below -10 dB, S_{21} is around 20 dB, and S_{12} lies below -30 dB. To account for the process variation, two transistor models, both provided by the same foundry, are employed in the simulation. In our measurement, we use $V_{d1} = 1.5$ V and $I_{d1} = 4.2$ mA for the first-stage complementary transistors, $V_{d2} = 1.5$ V and $I_{d2} = 5.8$ mA for the second-stage common-source transistor, $V_{d3} = 1.5$ V and $I_{d3} = 7.1$ mA for the third-stage and last-stage transistors. The total power consumption is 25.65 mW. Although the value of I_{d1} is smaller than that of I_{d2}, the gain first stage is still sufficient to lower the noise contribution from the following stage owing to its current re-use topology. Fig. 7(a) shows the simulated (dashed curve) and the measured (solid curve) noise figure; Fig. 7(b) show the measured input-referred third-order intercepts point (IIP3) and the simulated gain of each stage of the amplifier, where curves 1–4 correspond to the gain of stages 1–4, respectively. Comparison with other LNA's is summarized in Table I, where Figure of Merit (FOM) is defined as

$$FOM = \frac{Gain_{mean}(\text{dB}) \cdot BW(\text{GHz})}{[NF_{mean}(\text{dB}) - 1]\, P_{diss}(\text{mW})}. \tag{2}$$

In terms of gain, input reflection coefficient, and noise figure, our designed wideband amplifier outperforms other LNA's with similar or more advanced CMOS process [1], [3]–[9].

IV. CONCLUSION

In this letter, the complementary topology is combined with asymmetrical inductive source degeneration to achieve broadband input matching while retaining low noise figure. A 2–10 GHz wideband CMOS LNA is then designed and fabricated using commercial RF-CMOS 0.18-μm process. Compared with other CMOS LNA's in similar frequency range, our circuit demonstrates a better performance in gain, input matching, and noise figure.

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