Low-Complexity All-Digital Sample Clock Dither for OFDM Timing Recovery

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***Abstract*—Based on phase adjustment, this work investigates a low-complexity all-digital sample clock dither (ADSCD) to perform coherent sampling for orthogonal frequency-division multiplexing (OFDM) timing recovery. To reduce complexity, only tri-state buffers are acquired to build a multiphase all-digital clock management (ADCM), which can generate more than 32 phases over gigahertz without phase-locked or delay-locked loops. Following divide-and-conquer search and triangulated approximation, the phase adjustment is simple but efficient, such that four preambles are adequate to make analog-to-digital (A/D) sampling coherent. Performance evaluation indicates that the proposed ADSCD can tolerate ± 400-ppm clock offsets with $0.8 \sim 1.3$-dB signal-to-noise ratio (SNR) losses at 8% PER in frequency-selective fading. Hence, this scheme involves a little overhead to ensure fast recovery and wide offset tolerance for OFDM packet transmissions.**

***Index Terms*—Low complexity, multiphase clock, orthogonal frequency-division multiplexing (OFDM), phase adjustment, timing recovery.**

I. Introduction

DIGITAL signal processing (DSP) can enhance wireless access performance, in terms of error probability, data rate, and link reliability. For many wireless applications, powerful standards have been presented to make packet transmissions be more robust and efficient, e.g., multi-band (MB)-orthogonal frequency-division multiplexing (OFDM) UWB, WiFi, WRAN and WiMAX. Timing recovery is one of the most important factors in obtaining a good signal-to-noise ratio (SNR) for wireless OFDM systems. Fixed sampling with an interpolation filter [1]–[4] is a well-developed method in which datums are sampled at Nyquist or higher rate. Interpolation techniques [1]–[4] are usually employed to recover analog-to-digital (A/D) converters samples that the variable fractional-delay (VFD) filters are useful in designs. Then the Farrow structure with VFD filter becomes an efficient method, optimized by exploiting symmetries [5]. The other timing recovery involves adaptive sampling (synchronized sampling) to make A/D coherent. Since lower information loss corresponds to better performance, adaptive sampling (synchronized sampling) outperforms fixed sampling (non-synchronized sampling) [6]–[8]. The key of adaptive sampling is to adjust A/D clock accurately, efficiently and stably. Several mixed-mode schemes [9]–[13] have been developed to control A/D sampling frequency. Instead of analog techniques, an all-digital phase-locked loop (ADPLL) with eight uniform phases [14] has been realized to reduce power dissipation and implementation costs of MB-OFDM UWB systems. Yet, the large number of multiphase of ADPLL is hard to implement over several hundred megahertz. Additionally, pilot-based timing recovery is difficult to use for initial acquisition in WiFi and UWB because OFDM pilots can only be obtained after successful synchronization [8].

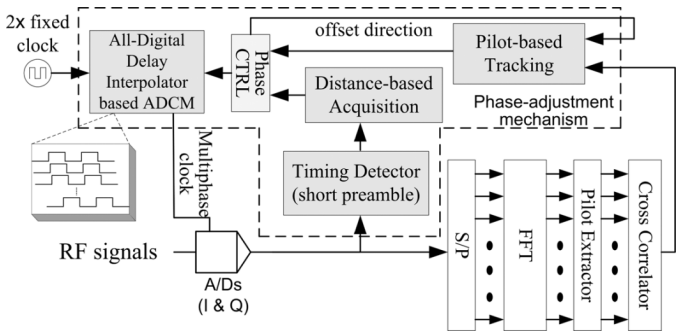

Fig. 1. Block diagram of non-PLL/DLL all-digital sample clock dither for OFDM timing recovery.

This study deals with a low-complexity all-digital sample clock dither (ADSCD) implementation, which allows for fast recovery and provides wide offset tolerance in OFDM packet accesses, as shown in Fig. 1. Unlike other multiphase techniques, e.g., phase-locked loops (PLLs), delay-locked loops (DLLs), and analog circuits, the proposed mechanism is simple yet useful to ensure A/D coherent sampling. This mechanism is also well-suited to new specifications as discussed in IEEE 802.15.3c and IEEE 802.11 very high throughput working group (VHT WG).

The rest of this paper is organized as follows. Section II states the system description and problem statement. Section III describes the low-complexity non-PLL/DLL ADSCD. To verify this work, both MATLAB and software-defined radio (SDR) platforms are built. Section IV shows and discusses the results. Conclusions are finally drawn in Section V.

II. System Assumptions

A. System Descriptions

In most WiFi and UWB systems, each OFDM packet contains several short preambles for pre-fast Fourier transfer (FFT) synchronization and a few long preambles for channel estimation.

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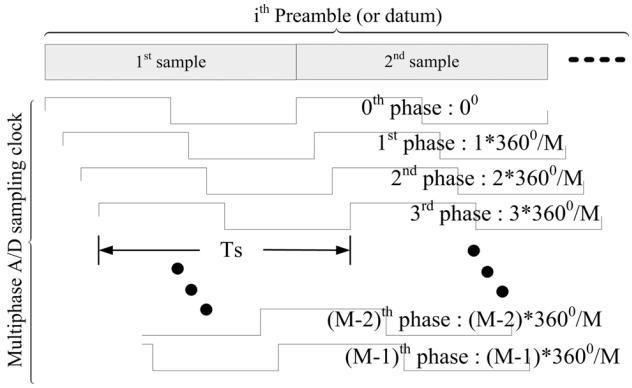

Fig. 2. Phase adjustment-based multiphase A/D sampling: preamble and datum versus clock phases.

Each OFDM (datum) symbol includes several frequency-domain pilots, modulated by QPSK or BPSK, for post-FFT synchronizations [8]. If $c = \{c[0], c[1], ..., c[N-1]\}$ is a short preamble with N samples, the transmitted signal is given by

$$c(t) = \left[\sum_{n=0}^{N-1} c[n] \cdot \Pi(t - nT_s)\right] * f_T(t) \cdot e^{j2\pi f_c t} \quad (1)$$

where $\Pi(t)$ is a function of BPSK modulation and T_s is the symbol period of short preambles. $c(t)$ is filtered by $f_T(t)$ (shaping filter) to be consistent with the spectrum mask, and up-converted to f_c (carrier frequency). After RF down conversion, the received short preamble becomes

$$x_R(t) = \sigma_p(t) \cdot [c(t) * h(t) * f_R(t)] \cdot e^{j2\pi \cdot f_{\mathrm{CFO}} \cdot t} \quad (2)$$

where σ_p is an auto gain controller (AGC) compensated error; f_{CFO} is the carrier frequency offset; $h(t)$ is the frequency-selective fading response, and $f_R(t)$ is the equivalent response of filters in receiver. After RF down conversion, all preambles and datums are sampled using one of clock phases, as shown in Fig. 2. The received short preamble is

$$r(t;\varepsilon) = \sigma_p \sum_{n}^{N-1} [x_R(t) + \mathrm{n}(t)] \cdot \delta[t - (n+\varepsilon)T_s]$$

and

$$\varepsilon \in R, \quad |\varepsilon| \le 0.5 \quad (3)$$

where $\mathrm{n}(t)$ represents additive white Gaussian noise (AWGN), $\delta(t)$ is the delta function, and ε is the sampling error. The cross correlation [6]–[8], [15] can be obtained by

$$\begin{aligned} & R(k;\varepsilon) \\ &= \sum_{n=0}^{N-1} r(nT_s + \varepsilon T_s) \cdot c(nT_s + kT_s) \\ &= \sigma_p^2 \cdot e^{j\theta(\varepsilon)} \cdot \sum_{n=0}^{N-1} c[(n+k)T_s]c[(n+\varepsilon)T_s]g[(k-(n+\varepsilon))T_s] \\ &\cong e^{j\theta(\varepsilon)} \cdot \sum_{n=0}^{N-1} c[(n+k)T_s]c[(n+\varepsilon)T_s]g[(k-(n+\varepsilon))T_s] \end{aligned} \quad (4)$$

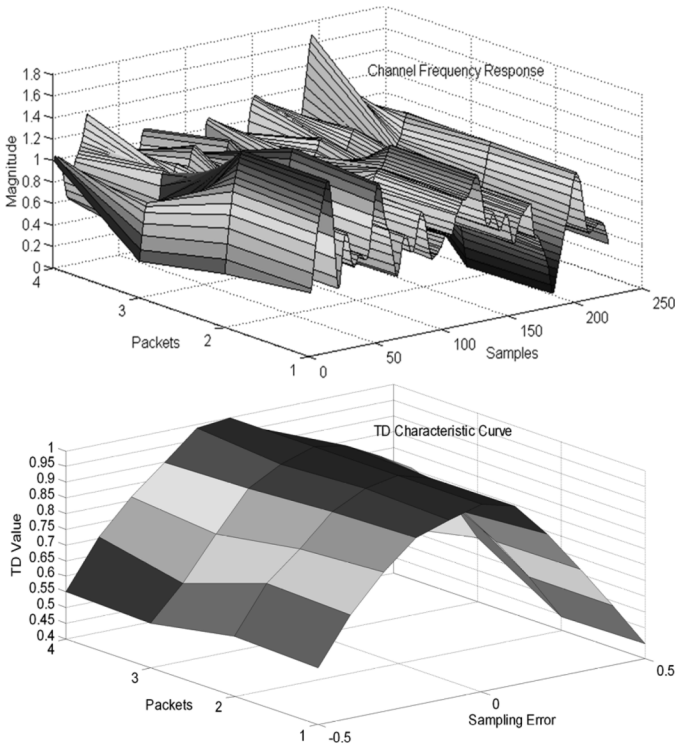

Fig. 3. Proposed timing detection in frequency-selective fading.

where $\sigma_p \approx 1$, $\theta(\varepsilon) = 2\pi f_{CFO} \cdot (n+\varepsilon)T_s$ is a phase offset, and $g = h * f_T * f_R$ is the overall response of fading channel and filters. Because $\sum h^2[kT_s]$ is a constant within each packet in indoor frequency-selective fading (time-invariant or WSSUS [6]–[8]), the window-based timing detection (TD) is proposed by

$$\begin{aligned} & TD(\varepsilon) \\ &= \sum_{k=-N/3}^{4N/3} |R(k;\varepsilon)|^2 \\ &\cong \sum_{k=-N/3}^{4N/3} \left| \sum_{n=0}^{N-1} c[(n+k)T_s]c[(n+\varepsilon)T_s]f[(k-(n+\varepsilon))T_s] \right|^2 \end{aligned} \quad (5)$$

where $f = f_T * f_R$ is the response of filters. Fig. 3 plots the characteristic curve of the proposed TD that a minimal sampling error almost corresponds with a maximum $TD(\varepsilon)$ in frequency-selective fading.

B. Problem Statements

"Multiphase A/D clocking" is one of keys to make phase adjustment as simple as possible. PLLs and DLLs are popular in implementations; however, most of them occasionally exhibit unduly serious phase transients, namely, hang-up phenomenon [16]. It is also difficult for all-digital multiphase PLLs or DLLs to provide a lot of clock phases over gigahertz. Although most high-speed multiphase clocking can be built using analog techniques, the turnaround time is too long. Due to different clock phases causing various timing errors, the coherent clock phase can be found via "step-by-step" scan per preamble

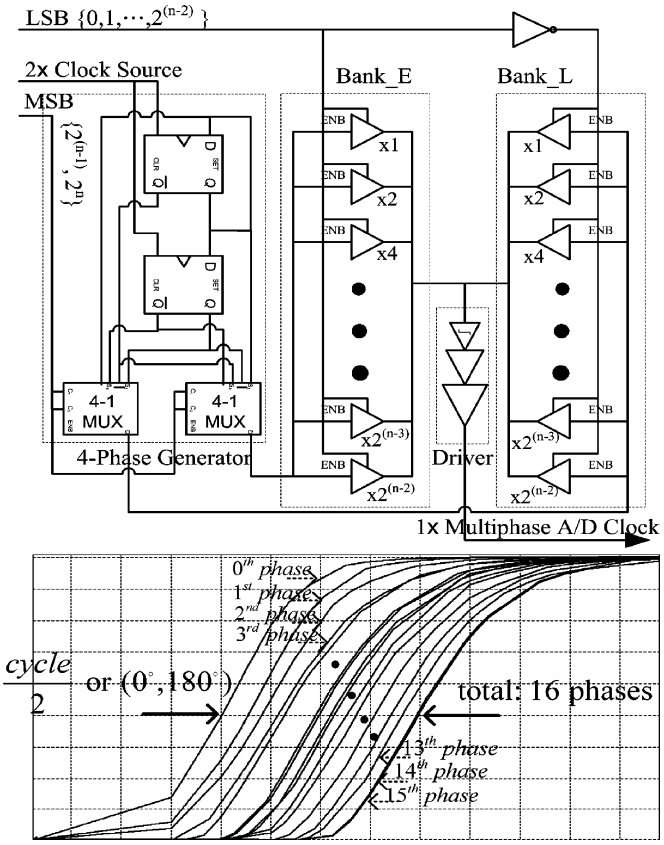

Fig. 4. Structure of the proposed 2^{n}-multiphase ADCM and its Hspice simulation of $0^\circ \sim 180^\circ$ (16 phases), 1 GHz in a 90 nm in-house digital CMOS process.

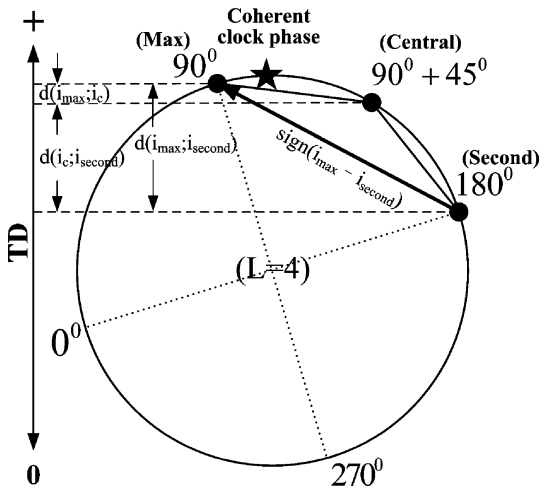

Fig. 5. Phase adjustment-based multiphase A/D sampling—lock phases versus timing detection.

in maximizing $TD(\varepsilon)$. Yet, this process increases cycles. Unfortunately, most wireless systems do not have sufficient preambles. Hence, the objective of this study is to derive a simple and low-complexity multiphase mechanism, assuring fast and robust recovery without PLL, DLL, and analog circuits.

III. Non-PLL/DLL ADSCD

A. Multiphase Clocking

PLL and DLL techniques are not used but delay interpolators [17] with tri-state buffers are built to produce all-digital multiphase clocking with 2^{n} controllability, as plotted in Fig. 4, in which the proposed ADCM is composed of a four-phase generator, two banks of tri-state buffers and a Schmitt trigger-based driver. Two groups of tri-state buffers with $2^{\mathrm{n}-2}$-order control are connected with wire-or logic ($2^{\mathrm{n}-2}$ phases are obtained), namely, Bank_E and Bank_L, where the control words of Bank_E and Bank_L are complementary. Because two groups of tri-state buffers cannot skew more than 1/4 cycle, a $2\times$ system clock is applied to generate four $1\times$ clocks, divided by D-type flip flop, with 0°, 90°, 180°, and 270° skews. As a result, the input of Bank_L is skewed $+90^\circ$ referring to Bank_E, and two 4-to-1 multiplexers are adopted to yield all needed 1/4-cycle combinations of four 0°, 90°, 180°, and 270° skews. For instance, if Bank_E is entirely active (all tri-state buffers of Bank_L are OFF), the input current flows via Bank_E to output (without any skew). On the other hand, the output current is all supported by Bank_L (output with 90° skew), if Bank_E is entirely inactive. Half of the tri-state buffers of Bank_E and Bank_L are enabled, and then the output current is combined by the two banks, being 45° skew. Based on various settings of buffers to change current balance, a phase with $2^{\mathrm{n}-2}$ skews can be performed. The three-stage deriver with $1\times$, $5\times$, and $16\times$ driving capabilities is a key of ADCM because the current summation of two delay banks may create glitches. To eliminate glitches, a Schmitt trigger buffer is applied at the 1st stage to stabilize clock transitions and both second and third stages to enhance the driving capability. Hence, a 2^{n}-multiphase ADCM with full-cycle controllability is realized by cascading the above modules. Although the disadvantage of using such mechanism is a nonuniform skew of clock phases (caused by rise time $\neq$ fall time), it is easy to produce multiphase over gigahertz using an in-house digital cell library. The simulations suggest that 32 nonuniform phases are sufficient in OFDM systems with 64 QAM. Fig. 4 also displays the Hspice simulation of 32-multiphase clocking, up to 1 GHz, in a 90 nm in-house digital CMOS process. The power dissipation is 1.67 μW at 40 MHz and 1.0 V supply voltage. This result is applied to model ADCM in simulations and measurements.

B. Phase Adjustment

Following Tau-Dither tracking loop [15] and divide-and- conquer search [18], each sample of preamble (datum) is divided into L sections and utilize an M-phase clock ($M > L$) to control A/D sampling per symbol, reducing errors via time sharing. The sampling error ε of the kth phase equals

$$\varepsilon = \frac{k}{M} - 0.5. \tag{6}$$

In Fig. 5, the first step is to adjust the A/D sampling clock with M/L-phase changes per preamble. Then there are L short preambles sampled by the $[M/L]^{\mathrm{th}}, [2M/L]^{\mathrm{th}}, \ldots, [(L-1)M/L]^{\mathrm{th}}$ and M^{th} phases, respectively. Both maximum and second of $TD(\varepsilon)$ can be obtained after sorting, namely, coarse search—an addressing region of coherent clock phases with large is found. Substituting (6) into (5), the candidate addresses of coherent

clock phases are ranged by (7a) and (7b), shown at the bottom of the page. The sign of $(i_{\max} - i_{\text{second}})$ specifies the direction of clock offset. Although numerous candidate addresses of coherent clock phases are obtained, it is not accurate enough. The second step uses one additional short preamble, sampled by the clock phase of $i_c = (i_{\max} + i_{\text{second}})/2$, to narrow the search range being a half of L to improve addressing accuracy as a fine search. Using triangulation method, the address of a coherent clock phase, ensuring A/D to sample coherently, can be approximated by (8), shown at the bottom of the page, where $\Delta = M/L$ is the number of clock phases per section, the sign in (8) is determined by the sign of $(i_{\max} - i_{\text{second}})$, and $d(j;i)$ is the distance of timing detection, defined by

$$\begin{aligned} d(j;i) &= TD_{j^{\text{th}}\text{phase}}(\varepsilon) - TD_{i^{\text{th}}\text{phase}}(\varepsilon) \\ &= \sum_{k=0}^{N-1} \left(\left| R\left(k; \frac{j}{M} - 0.5\right) \right|^2 - \left| R(k; \left(\frac{i}{M} - 0.5\right) \right|^2 \right). \end{aligned} \tag{9}$$

This simple method measures only "L + 1" preambles to adjust A/D clock phases coherently. With large L, additional preambles are required; with large M, high quality of A/D coherent sampling is achieved. Thus, L and M must reach a balance between cycle count and quality. For 32 phases ($M = 32$), 120° per section ($L = 3$) is a good choice—then only four preambles are used. During datums, continuous tracking of OFDM pilots will obtain the next coherent clock phase with $TD(\varepsilon)$ maximizing via maximum correlation methods [7].

C. Hardware Architecture

Fig. 1 shows the architectures of the proposed non-PLL/DLL ADSCD, where four functional modules are derived: 1) a distance-based acquisition for searching a good clock phase to make A/D sampling coherent; 2) a pilot-based tracking for measuring the sampling errors of OFDM pilots to retain A/D sampling coherently; 3) a phase CTRL for generating the phase addresses of ADCM; and 4) an ADCM for realizing multiphase clocking within acceptable complexity. In Fig. 6, there are three major blocks of the phase adjustment: 1) four registers to store timing detection; 2) a sorter to search a maximum and a second; 3) an address interpolation with triangulation method to enhance addressing accuracy. Four key components of the phase CTRL are: 1) an address decision to decide phase addressing and to control multiphase clocking; 2) two registers to store the corresponding phase addresses of a maximum and a second; 3) an average to calculate the address of the central phase; and 4) a subtraction with a sign to extract the direction of clock offset. Because both timing detection and addresses of clock phases must be synchronized, two kinds of pointers are adopted to trigger registers: one is generated by the address decision to save four timing detections of 0°, 120°, 240°, and i_c phases, and the other one is generated by the sorter to record the addresses of $i_{\max}$ and i_{second}. The detail operations are explained as follows.

Input signals are initially sampled using one of clock phases. After the packets have been detected, coarse acquisition is used to begin the search procedure where the first preamble is sampled using the first phase; the second preamble is sampled using the $(M/3)$th phase; and the third preamble is sampled using the $(2M/3)$th phase. Their $TD(\varepsilon)$ are measured and stored in registers. A sorter is used to find the "Max" and "Second" $TD(\varepsilon)$ of the first, $(M/3)$th and $(2M/3)$th phases to decide the addressing region of coherent clock phases. Based on $i_{\max}$ and i_{second}, the new phase of $i_c = (i_{\max} + i_{\text{second}})/2$ is decided and the direction of clock offset is obtained. With $i_{\max}$, i_{second} and i_c, a triangulation-based address interpolator is adopted to enhance accuracy. During datums, the correlation-based tracking uses OFDM pilots to keep the A/D sampling coherent. $TD(\varepsilon)$ of the first OFDM pilot is stored as a reference, and $TD(\varepsilon)$ of remainder OFDM pilots is then continuously measured and the reference is subtracted therefrom. The A/D clock phase must be adjusted to retain coherent sampling if the new $TD(\varepsilon)$ is smaller than the reference; the phase addressing of A/D clock does not need to change if the new $TD(\varepsilon)$ exceeds the reference.

D. Implementation and Complexity

Both hardware-description language (HDL) and synthesis tool are sufficient to implement the modules of sorter, address interpolator, phase controller and pilot-based tracking. The critical part is the layout of the proposed 32-phase ADCM whose issues and problems are as follows. 1) The input and output buses of tri-state buffers must be balanced to avoid additional skews. So the metal layer of such buses must be fixed (can not change layers) because the resistances of different VIAs and metals are easy to induce an extra delay in layouts. For

$$i_{\max} = k^{\text{th}}|_{\max\{TD(1/L-0.5), TD(2/L-0.5), \ldots, TD((L-1)/L-0.5), TD(0.5)\}} \tag{7a}$$

$$i_{\text{second}} = k^{\text{th}}|_{\text{second}\{TD(1/L-0.5), TD(2/L-0.5), \ldots, TD((L-1)/L-0.5), TD(0.5)\}} \tag{7b}$$

$$i_{\text{final}} = \begin{cases} i_c, & \text{for } d(i_{\max}; i_c) \cong d(i_c; i_{\text{second}}) \\ i_c \pm \left\lfloor \frac{\Delta}{4} \right\rfloor, & \text{for } d(i_{\max}; i_c) \cong 0 \\ i_c \pm \left\lfloor \frac{\Delta}{4} \left[2 - \frac{d(i_{\max}; i_{\text{second}})}{d(i_c; i_{\text{second}})} \right] \right\rfloor, & \text{for others} \end{cases} \tag{8}$$

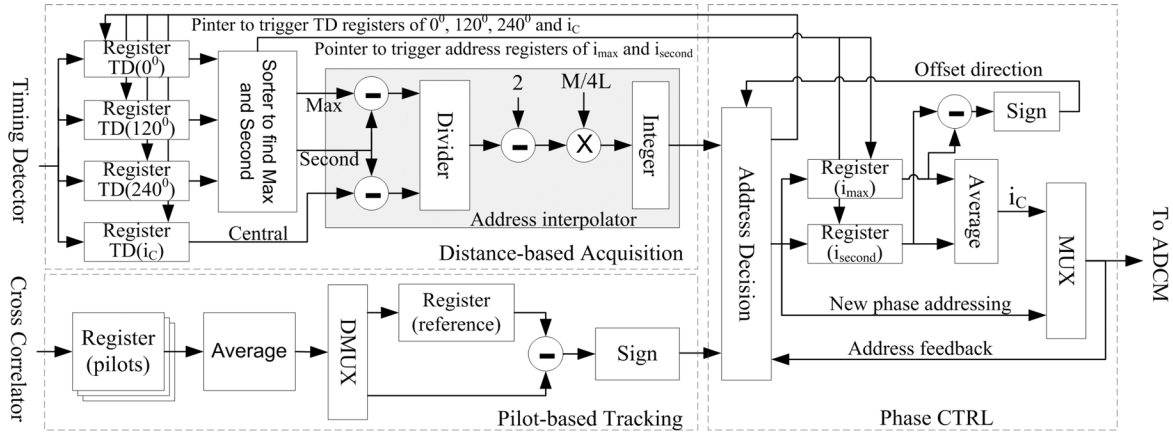

Fig. 6. Architecture ($L = 3$) of phase adjustment in non-PLL/DLL ADSCD for OFDM timing recovery.

an example of an in-house 90-nm 1P9M CMOS technology, VIA_1 is 31.8 Ω and VIA_2 is 28.6 Ω, which produces serious skews at 1.0 V supply voltage. 2) Considering power bounce, it affects the phase jitter of ADCM. In order to stabilize the power bounce, the placement of ADCM layout must be close to the power lines and power PADs to obtain sufficient current in operations.

The hardware complexities of the proposed ADSCD are: the gate count of a sorter is 700; an address interpolator needs about 1250 gates; the timing detector is 780 gates; the phase CTRL requires 900 gates. Because the pilot-based tracking needs only "addition" and "subtraction", the main cost is the register that 420 gates include in implementations (less than 100 bits; using 8-bit A/Ds). For 32-multiphase ADCM, six tri-state buffers (total 80 gates), two D-type flip flops (10 gates per each), two 4-to-1 multiplexes (16 gates per each), two deriving buffers (total 18 gates) and a Schmitt trigger buffer (30 gates) are just used. The total gate count of 32-multiphase ADCM is 180. Because the computation complexities of the pilot-based tracking without multiplication and ADCM without digital control oscillator (DCO), voltage control oscillator (VCO), PLL and DLL are constant; the computation complexity of address interpolator with division and multiplication is $\mathrm{O}(n)$. The overall computation complexity is dominated by divide-and-conquer search, being $\mathrm{O}(n \times \log_2 n)$ [18]. Hence, this multiphase mechanism is less complex than multiphase ADPLL [14] and interpolation filters [19]–[21].

IV. Performance Evaluation

Two platforms are constructed to evaluate this multiphase mechanism; one is MATLAB simulation, and the other one is software-defined radio (SDR) platform. MATLAB simulations include AWGN, frequency-selective (multipath) fading, carrier frequency offset (CFO), clock offset, path loss, and circuit noises. Circuit noises in the proposed clock dither are: 1) A/D random errors and 2) phase jitter of ADCM. Monte Carlo is applied to generate the phase jitter with uniform distribution, ranging $\pm 5\%$ of clock period (A/D sample clock). The nonuniform behavior of the proposed ADCM is built via 128 × over sample. After down sample to 1 ×, the jitter effect of A/D clock is then created using an interpolator. The required packet-error

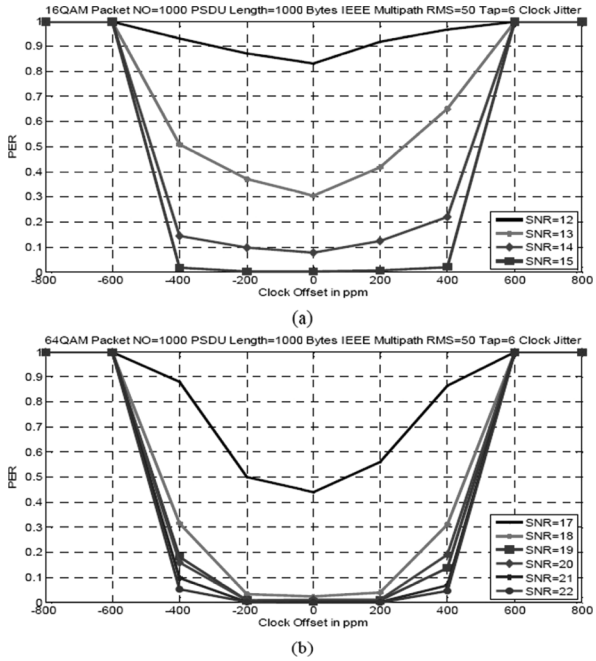

Fig. 7. Offset tolerance with circuit noises, 25-dB path loss, 50-ppm CFO, and 50-ns RMS delay spreading: (a) 16 QAM; (b) 64 QAM.

rate (PER) is 8% under 8-bit A/Ds, 256-step non-ideal AGC with a dynamic range of 70 dB, a packet length of 1024 byte, IEEE frequency-selective fading with an RMS delay spread of 50 ns, a maximum path loss of 65 dB and a CFO of 50 ppm. In Fig. 7(a) and (b), the offset tolerance with various SNR and modulations can be as high as ±400 ppm, much larger than the ±25 ppm in most wireless standards, in that the tracking error of adaptive sampling involves less distortion than the filtering losses associated with interpolation. The SNR losses are about 0.8 dB of 16 QAM and 1.3 dB of 64 QAM compared with perfect synchronization. Table I summarizes the features with related works [9], [10], [14], and [19]–[21].

RF signals are linked with MATLAB and FPGA to verify the proposed multiphase mechanism. Two XilinxDSP Development Kits with on-board 14-bit A/Ds, 14-bit digital-to-analog (D/A) converters and 2-million-gate field programmable gate array (FPGA, Xilinx Virtex-II) are connected with in-house

TABLE I
FEATURES OF THE DIFFERENT TIMING RECOVERY

	[9]	[10]	[14]	[19]	[20]	[21]	THIS WORK
VLSI Type	Mixed-Mode	Mixed-Mode	All-Digital	All-Digital	All-Digital	All-Digital	All-Digital
Architecture	DAC + VCXO	DAC + VCXO	ADPLL (PTCG)	Interpolator	Interpolator	Interpolator	Non-PLL/DLL (ADCM)
Modulation	OFDM + 64 QAM	OFDM + 16 QAM	OFDM + QPSK	OFDM + 64 QAM	16 PSK	OFDM + 16 QAM	OFDM + 64 QAM
Sampling Mode	Synchronous	Synchronous	Synchronous	Asynchronous	Asynchronous	Asynchronous	Synchronous
Control Factor	Frequency	Frequency	8 Phases	Fixed Clock	Fixed Clock	Fixed Clock	32 Phases
Sampling Rate	N/A	4x	1x	4x	2x	4x	1x
Cycle Count	40 symbols	380 symbols	N/A	N/A	32~64 symbols	100 symbols	4 symbols
Tolerant Range	N/A	N/A	N/A	± 200 ppm	N/A	± 100 ppm	± 400 ppm
Complexity	N/A	N/A	$O(a\times n^2)$	$O(n^2)$	$O(n^2\times\log_2 n)$	$O(n^2)$	$O(n\times\log_2 n)$

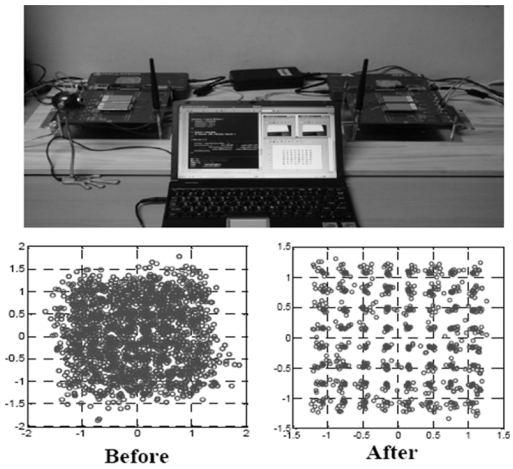

Fig. 8. SDR platform and the measurements of 64-QAM constellations with circuit noises and a clock offset of +400 ppm before and after recovery.

TABLE II
SUMMARY OF THE MEASURED EVM

OFFSET	OFDM + 64 QAM		OFDM + 16 QAM	
	W/O Noises	With Noises	W/O Noises	With Noises
+400 ppm	-23.18 dB	-22.92 dB	-23.03 dB	-22.96 dB
+200 ppm	-23.78 dB	-23.17 dB	-23.71 dB	-23.27 dB
+50 ppm	-24.09 dB	-23.46 dB	-24.07 dB	-23.54 dB
-50 ppm	-24.05 dB	-23.43 dB	-24.08 dB	-23.56 dB
-200 ppm	-23.80 dB	-23.19 dB	-23.69 dB	-23.28 dB
-400 ppm	-23.15 dB	-22.94 dB	-23.10 dB	-22.97 dB

$$EVM = 20\times\log_{10}\sqrt{\frac{\sum_i (Re[r_i(t)-s_i(t)]^2 + Im[r_i(t)-s_i(t)]^2)}{\sum_i (Re[s_i(t)]^2 + Im[s_i(t)]^2)}}$$

2.4-GHz RF modules at 20-MHz bandwidth to transmit and receive real OFDM packets, as displayed in Fig. 8. The proposed method is also mapped onto the FPGA. Yet, the maximal clock rate of on-board 14-bit A/Ds in XilinxDSP Development Kits is 105 MHz – only $\leqq 32\times$ over sample with uniform phases is available, being different to the real. Thus, an interpolator is utilized to simulate additional sample errors of nonuniform sample phase and to model the phase jitter of ADCM. Before measurements, the natural clock offset between TX and RX must be calibrated and precompensated. TX packets with man-made clock offsets are first generated by MATLAB and transferred by 14-bit D/A. The packets are then transmitted using RF module (MATLAB to RF through D/As). After RF down conversion, wireless signals are fed into 14-bit A/Ds and transferred to field-programmable gate array (FPGA) and PC via USB (RF to FPGA and MATLAB through A/Ds), where $32\times$ over sample with such interpolation realizes phase-adjustment behavior in receivers. Fig. 8 also displays 64-QAM constellations before and after recovery. The measured EVM with/without circuit noises are listed in Table II. They demonstrate that the proposed ADSCD functions in certain wireless situations.

V. CONCLUSION

For OFDM timing synchronization, a low-complexity ADSCD is investigated to offer fast recovery and wide tolerance. The proposed multiphase clocking is constructed by tri-state buffers and has low complexity; it can produce more than 32 phases over gigahertz without any multiphase PLL, DLL, or analog circuit. The A/D phase adjustment is simple but efficient to perform coherent sampling within four preambles. At 8% PER and up to $\pm$400-ppm clock offsets, the SNR loss is only $0.8 \sim 1.3$ dB in frequency-selective fading. Hence, this multiphase mechanism produces promising results for WiFi, UWB and new specifications discussed in IEEE 802.15.3c and IEEE 802.11 VHT WG.

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