Chapter 5

Poly-Si TFTs with Elevated Channel and Gate Overlapped Structure by Metal-Induced Lateral Crystallization

MOSFET on SOI wafer with ultrathin channel layers have various advantages. These include high mobility [5.1], kink elimination [5.2], saturation current enhancement [5.3], and steeper subthreshold slope. Recently, Z. Jin et al. proposed a TFT with ultrathin Ni-MILC active layer and obtained electron mobility as high as 110 cm^2/Vs [5.4]; the channel of this TFT is 30 nm and the S/D electrodes are connected to thicker Si pads to reduce the contact resistance. However, since this ultrathin-channel TFT dose not utilize LDD or the other offset structures, kink phenomenon of output drain current can be observed while the hot carrier endurance may be poorer than conventional TFTs.

In the previous chapter, we've proposed a novel ECTFT with gate overlapped structure to improve both the device uniformity and the reliability characteristics. We'll further examine this ECTFT structure with different active layer thickness and doping concentration of LDD region in this chapter. The recrystallization method of a-Si was metal-induced lateral crystallization instead of excimer laser annealing, because ELA would easily evaporate the ultrathin channel region or contribute to large surface roughness when the thickness of a-Si below 100 nm. On the other hand, for the case of solid-phase crystallization, the grain size decreases dramatically as the thickness of poly-Si film decreasing [5.5], since the Si grain would be confined in a limited volume. Comparing to ELA or SPC, the MILC method provides a flat poly-Si surface even with very thin film and is potential for fabricating high performance TFTs in a single poly-Si grain [5.6], [5.7].

5.1 Experimental

5.1.1 Elevated Channel TFTs with Different Thickness of Active Layer

The key processes for fabricating ECTFT with GOLDD structure are illustrated in Fig. 5-1. At first, a 50-nm amorphous silicon layer was deposited on an oxidized silicon substrate by LPCVD at 550°C. Then the thin channel (trench) region was patterned by photo lithography and Si etchant composed of HNO_3, NH_4F and H_2O. Next, without removing photoresist, the samples were soaked into super saturated H_2SiF_6 solution at 23°C; the SLPD-oxide would deposit at the sidewall and the bottom of the trench except the surface of photoresist. Because the wet chemical etching and the deposition of LPD oxide are both isotropic, a planar surface as shown in Fig. 5-1(a) can be established precisely and was checked by surface profiler. After photoresist removal, a phosphorous implantation with a dosage of 1×10^{13} cm^{-2} at 30 keV was performed to generate lightly doped region.

Next, an amorphous-Si layer with different thickness including 15 nm, 30 nm, 50 nm and 100 nm was deposited by LPCVD at 550°C as the active layer. The samples with various thickness of active layer were abbreviated to *ECT15*, *ECT30*, *ECT50*, and *ECT100*, respectively. For comparison, control samples with the active layer thickness from 15 nm to 100 nm were also prepared, and they were abbreviated to *AA15*, *AA30*, *AA50*, and *AA100*, respectively. After the active area was patterned, a 125-nm gate oxide layer by PECVD and 300-nm poly-Si gate electrodes by LPCVD at 620°C were formed. For n-channel transistors, a self-aligned phosphorous implantation with a dosage of 5×10^{15} cm^{-2} at 60 keV was carried out to generate S/D regions, as shown in Fig. 5-1(b). Here, the gate-overlapped length *d* as indicated in the figure ranges from 0 to 3 μm.

After depositing TEOS oxide by PECVD as a passivation layer, the contact holes were etched by buffered oxide etcher (BOE). Without removing photo resists about contact holes, a 5 nm Ni was deposited subsequently by Dual E-Gun evaporation system and the photo resists

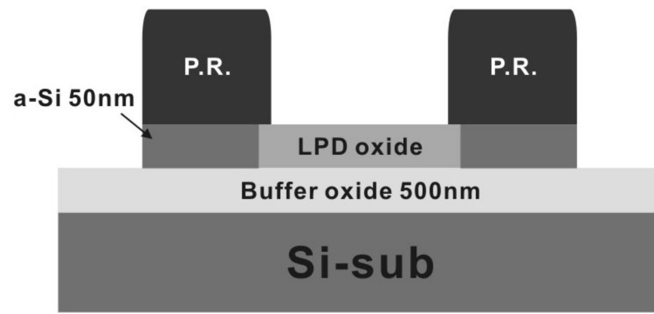
were then lift-off by ACE. Next, the samples underwent a furnace annealing at 550°C in N_2 atmosphere for 48 hr, which not only activated the doped area but also accomplished the Ni-MILC in the channel region, as shown in Fig. 5-1(c). Thereafter, the remaining Ni was removed by hot H_2SO_4 and H_2O_2 mixtures. Then, the samples were dipped in the diluted HF solution to remove the native oxide formed in the previous step. Finally, all samples underwent a standard backend process to form contact pads, as shown in Fig. 5-1(d), while the conventional TFT structure was shown in Fig. 5-2. No further hydrogen passivation process was performed.

The detailed process flow was listed below:

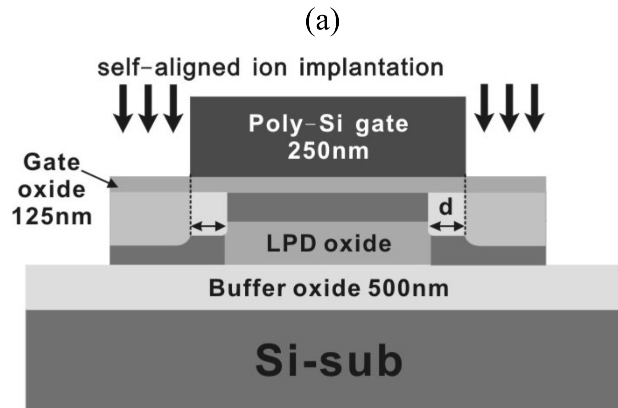
1. Initial RCA cleaning
2. 500 nm SiO_2: thermal wet oxidation at 1050°C
3. 50 nm a-Si: LPCVD, SiH_4 source at 40 sccm, 550°C
4. Mask #1: define the a-Si trench for the thin channel region
5. Wet chemical etching of the a-Si trench: poly etchant (NH_4F, HNO_3 and H_2O mixture) at room temperature
6. 50 nm SiO_2 by S-LPD method: (without removing photoresist) in super-saturated H_2SiF_6, at 23°C for about 2.5 hr
7. P.R. removal
8. Ion implantation for LDD region: P^{31}, 30 keV, 1×10^{13} cm^{-2}
9. RCA cleaning
10. a-Si thin film deposition: LPCVD, SiH_4 source at 40 sccm, 550°C, 100 mtorr
    a. ECTFT: ECT15, ECT30, ECT50, ECT100 (thickness in nm)
    b. conventional TFTs: AA15, AA30, AA50, AA100
11. Mask #2: define the active area
12. Dry etching of the active area: SAMCO® RIE-200L system with SF_6 at 20 Pa
13. RCA cleaning

14. 125 nm gate oxide: PECVD, TEOS and O_2 source, 350°C, 250 W
15. 300 nm poly-Si gate: LPCVD, SiH_4 source at 40 sccm, 620°C, 120 mtorr
16. Mask #3: define gate electrode
17. Dry etching of gate electrode: SAMCO® RIE-200L system with SF_6 at 20 Pa
18. RCA cleaning
19. Ion implantation: P^{31}, 60 keV, 5×10^{15} cm^{-2} for ECTFT series; for AA15, AA30 and AA100 samples, the implantation energy is reduced to 30 – 50 keV
20. RCA cleaning
21. 500 nm passivation layer: PECVD TEOS SiO_2
22. Mask #3: Contact hole definition
23. Wet chemical etching for contact hole formation: buffered oxide etcher (NH_4F : HF = 6 : 1)
24. 5 nm Ni: Duel E-Gun evaporation system, 0.5 Å/sec at room temperature, base pressure below 2×10^{-6} torr

25. P.R. lift-off: ACE with ultra-sonic vibrations
26. Metal-induced lateral crystallization and dopants activation: furnace annealing, 48 hr, 550°C in N_2 atmosphere
27. Residual Ni removal: hot SPM solution at 150°C for 20 min
28. Native oxide removal: diluted HF, 20 sec
29. 500 nm Al: thermal coater, base pressure below 4×10^{-6} torr
30. Mask #4: metallization
31. Wet chemical etching for Al etching: H_3PO_4, HNO_3, CH_3COOH, H_2O mixture
32. Al sintering at 400°C, 30 min in N_2 atmosphere



(a)



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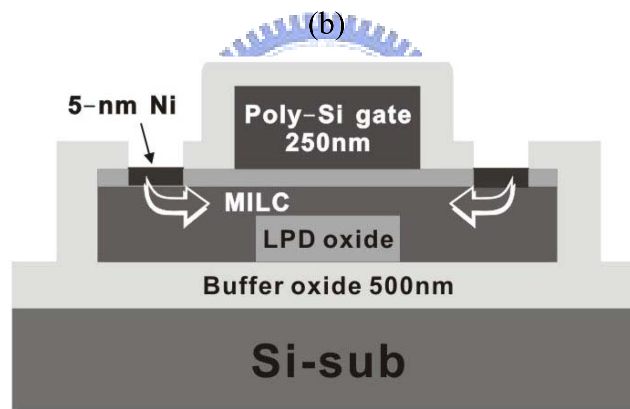

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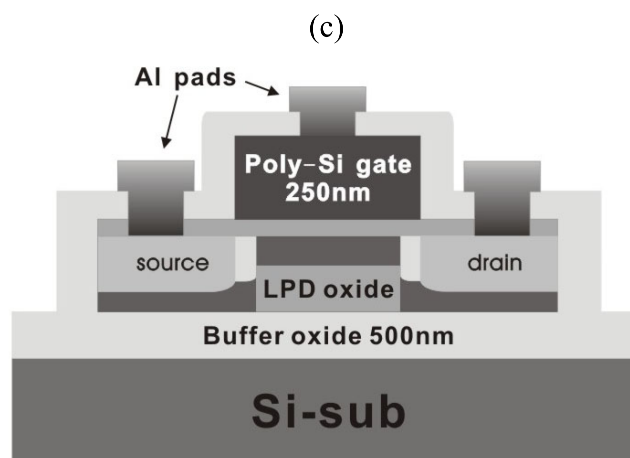


(d)

Figure 5-1 Process flow of ECTFT with GOLDD structure

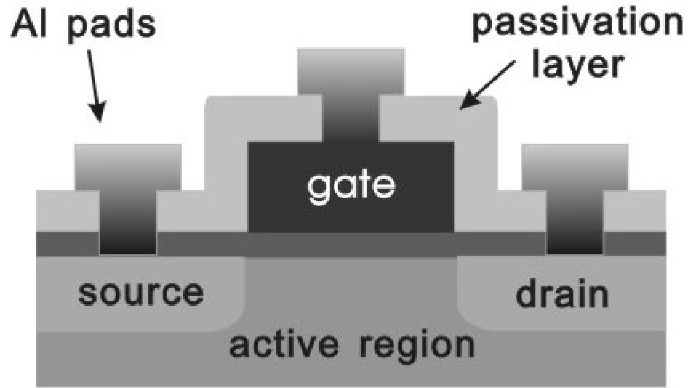


Figure 5-2 Cross-sectional view of a conventional top-gate TFT

5.1.2 Elevated Channel TFTs with Different Doping Concentration of LDD

The impurity concentration of lightly doped drain region would undoubtedly affect the distribution of the electric field near the drain side. In *section 5.1.1*, the LDD concentration was fixed at 1×10^{13} cm^{-2}. Here, four different implantation conditions were applied to the LDD region; they were non-LDD doping, and LDD dosage among 1×10^{13} cm^{-2}, 5×10^{13} cm^{-2} and 1×10^{14} cm^{-2}, but the implantation energy was still kept in 30 keV. Except the LDD concentrations, all of the other process steps were identical with those described in *Section 5.1.1*.

5.2 Results and Discussion

5.2.1 General I-V Characteristics of ECTFT without GOLDD Structure

We'll first discuss about the influence of the channel thickness to the electrical properties of poly-Si TFTs. For ECTFT structure, the overlapped length *d* is kept zero throughout this section.

Figure 5-3 illustrates the transfer curves of conventional TFTs (as shown in Fig. 5-2) with different thickness of active layer ranging from 15 nm to 100 nm. It can be easily observed that the samples of AA100 exhibit the highest ON current and the smallest threshold

voltage, indicating good crystallinity can be achieved because both the I_{ON} and threshold voltage of TFTs depend on the trap-state density in the active layer. However, one can also find a significant OFF-state leakage current which increases with reducing V_{GS} as V_D = 10 V. This leakage current, generally regarded as gate-induced drain leakage (GIDL) current, depends on the trap states density of the active layer and the lateral electric field near the drain side as described in *Section 4.1.1*. On the other hand, the ON current of those TFTs with thinner active layer is notably suppressed, and we believed that the large source/drain series resistance would be the primary reason. Moreover, for sample AA15, the I_{OFF} at V_{GS} = -20 V and V_D = 10 V is as large as sample AA100; this anomalous leakage current may attribute to the process of MILC. Specifically, the deposited Ni layer would first react with a-Si and forms nickel disilicide at the contact area. Since the 5 nm Ni film consumes at least an equal volume of silicon to form $NiSi_2$, the source/drain junction must be very close to the defective silicide layer when the thickness of the active area reduces below 15 nm, resulting in a large leakage current at reverse bias.

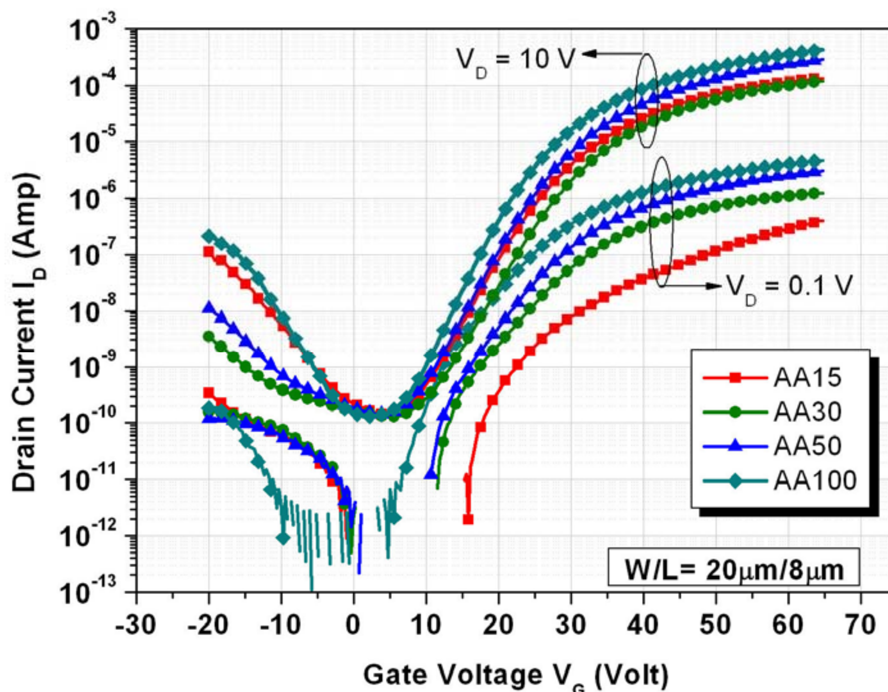


Figure 5-3 I_D - V_{GS} curves of conventional TFTs with different thickness of the active layer

Figure 5-4 compares the I_D - V_{GS} curves of TFTs with elevated channel structure and different channel thickness, while the gate overlapped length is zero (d = 0). In contrast to the case of conventional TFTs, the ECTFT exhibit satisfactory ON current, OFF current, and ON/OFF current ratio exceeding 10^6. With reducing the channel thickness, the amount of the trap states in the active layer is also decreased, so that the Off-state leakage current of sample ECT30 even reaches 10^{-10} A at V_D = 10 V and V_{GS} = 0 V. Besides, since the source/drain regions had been thickened by depositing poly-Si film of 50 nm, the issue of large series resistance originated from the thinner channel was not observed. Nevertheless, the sample ECT15 without GOLDD structure (i.e. S/D = 65 nm, channel thickness = 15 nm and d = 0 μm) was failed in this experiment. A possible reason arose from the misalignment between the top-gate edge and the bottom trench region, and the thin channel region maybe damaged during the definition of gate electrodes by RIE due to over etching, as shown in Fig. 5-5(a). Another possible failure mechanism was the planarization result by S-LPD. As illustrated in Fig. 5-5(b), the planar surface filled by the S-LPD oxide would be slightly etched for approximately 20 ~ 40 Å during the following RCA cleaning process. The trench corner as indicated in the figure would cause problems such as step coverage or result in larger electric field during the operation of TFTs, and a thin active layer was more susceptible to the surface morphology in the trench corner. We cannot conclude which failure mechanism is correct at this stage, maybe both of them, so more investigations such as TEM analysis are required.

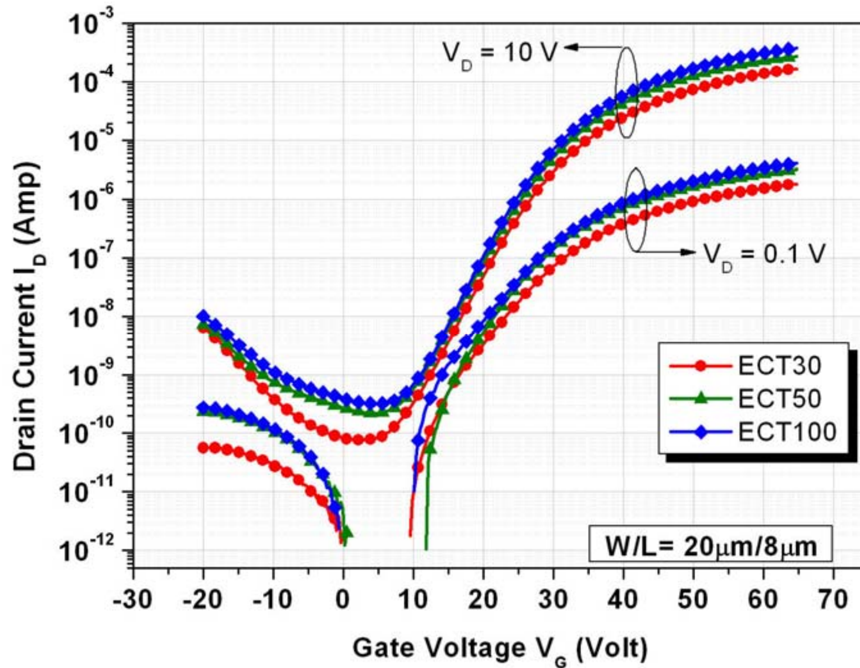
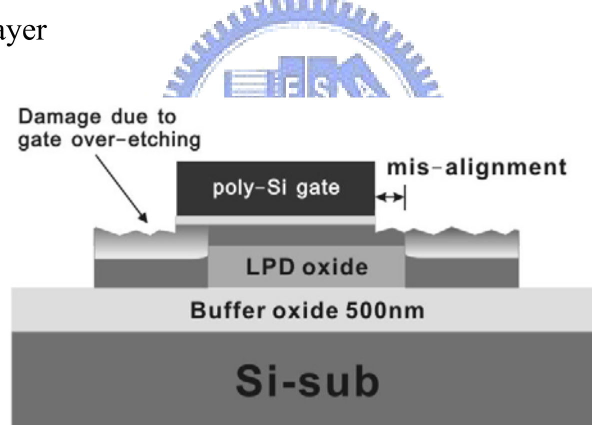
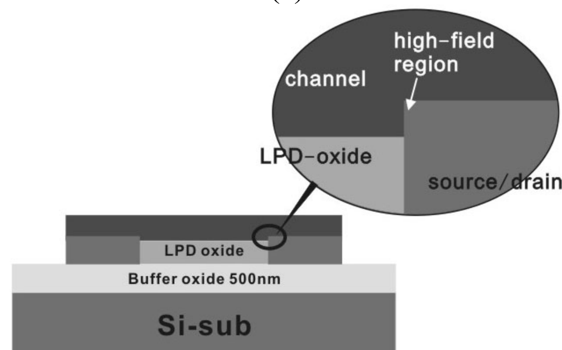


Figure 5-4 Transfer curves of ECTFT structure (d = 0) with different thickness of the active layer



(a)



(b)

Figure 5-5 Analysis of the failure mechanism of sample ECT15: (a) misalignment of top gate electrodes and channel over etching, and (b) planarization of LPD with large electric field at the trench corner

The field-effect mobility versus gate length for TFTs with different channel thickness is compared in Fig. 5-6. The μ_{FE} of sample ECT100 is 25 cm^2/Vs and gradually decreases when increasing the gate length or reducing the channel thickness. The former phenomenon can be explained by the efficiency of MILC process and the number of grain boundaries in the channel region. It had been reported that the efficiency of MILC decreases with increasing the length between the Ni seeding window and the device area, because the MILC depends on the continuous supply of Ni atoms from the seeding window to form the $NiSi_2$ and to induce the rearrangement of a-Si at the crystallization front. Therefore, the rate of MILC becomes slower while the crystallinity is poorer as the crystallization front far from the seeding window of Ni pad. Besides, a larger device, that is, TFTs with long gate length or wide channel width, could occupy more defective grain boundaries in the channel region; these grain boundaries establish potential barriers which impede the transportation of free carriers, contributing to the degradation of the mobility.

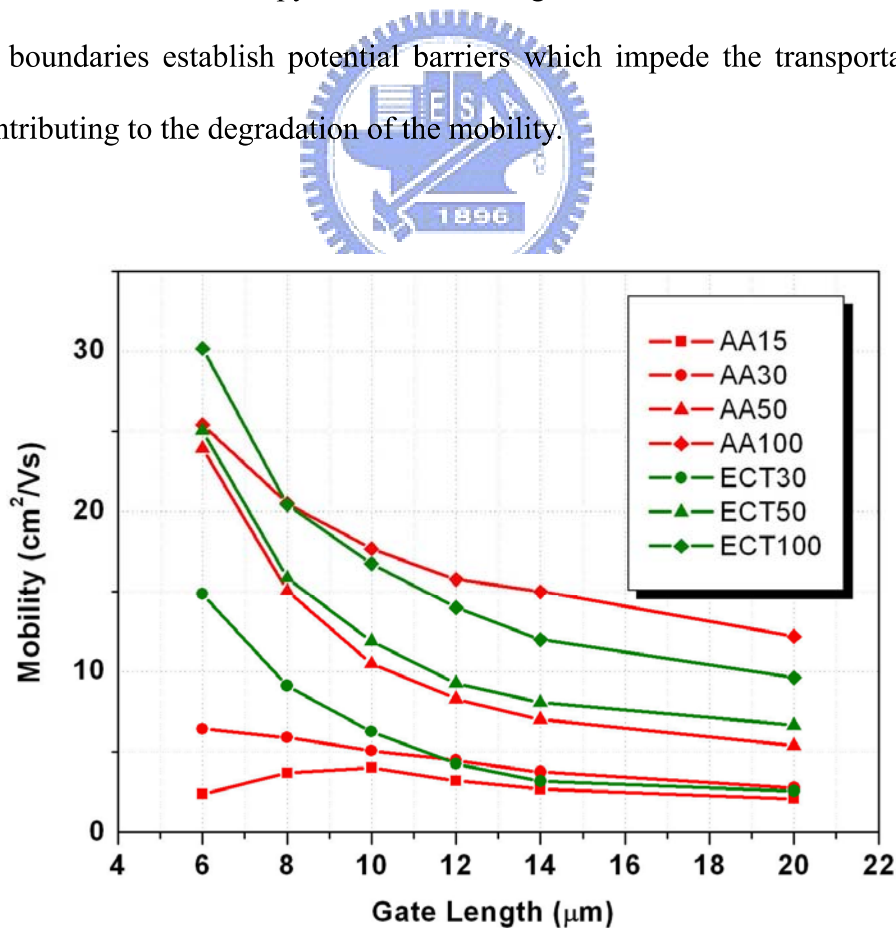


Figure 5-6 The field-effect mobility versus gate length for TFTs with different channel thickness and device structure

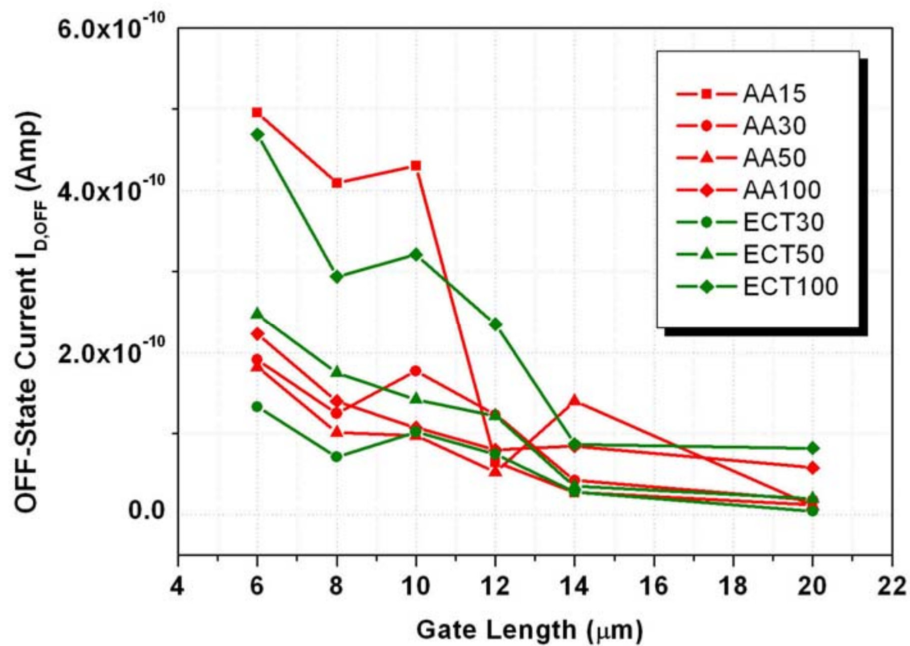
According to the research proposed by T. K. Chang or Z. Jin et al., the field effect mobility would slightly increase as the channel thickness reduces, possibly owing to the ordered crystalline structure confined in a thin channel region [5.8], [5.9]. However, in this work, the carrier mobility decreased with reducing the channel thickness for both conventional and ECTFT structures. This phenomenon is also associated with the characteristics of MILC process. For thick a-Si film, all $NiSi_2$ precipitates can act as nucleation sites and participate in the lateral crystallization process. When the thickness of a-Si film decreases, the migration of $NiSi_2$ precipitates is restricted by the top and bottom surface of the a-Si thin film and thus the recrystallization rate drops significantly for lack of the $NiSi_2$ supply. In addition, the size of $NiSi_2$ precipitate is generally about several tens of nanometers and forms slowly in a thin a-Si film [5.8], [5.10]. For the layout design in this experiment, the distance from the edge of Ni seeding window to the edge of gate electrode is 15 μm, so the channel region should have recrystallized by spontaneous crystallization of a-Si (i.e. SPC) before the growth front of MILC reaches the thinner channel area. This deduction was supported by the fact that the mobility of TFTs recrystallized by conventional SPC is not improved with decreasing the channel thickness [5.5], [5.9]. To make matters worse, through the UV reflectance measurement, it has been reported that the crystalline fraction for MILC decreases obviously as the thickness of a-Si film below 50 nm. The authors speculates that the $NiSi_2$ crystallites required to crystallize a-Si is around 50 nm and a higher annealing temperature of 580°C is required to improve the crystalline fraction for a 20 ~ 40 nm poly-Si layer [5.11].

The trends of μ_{FE} with respect to the gate length as shown in Fig. 5-6 also revealed that the thickened source/drain region was capable for reducing the contact and series resistance. The carrier mobility of sample ECT at almost every gate length is larger than that of the control sample with the same thickness of active layer. Besides, since the contact or S/D series resistance $R_{S/D}$ dominates for a short gate length, the effect of thickened source/drain

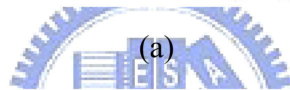
structure becomes more pronounced in this case, such as sample ECT30 versus AA30/AA15 when the gate length *L* smaller than 10 μm. Similar to that of CMOS industry, the geometry of poly-Si TFTs also keeps scaling down to improve the device performance, while an ideal case is to fabricate TFTs in a single grain so that the mobility of TFTs could be as large as that on a single crystal Si. Consequently, the concept for reducing series resistance by ECTFT architecture is crucial to sub-micron thin film devices. On the other hand, channel resistance surpasses the importance of $R_{S/D}$ when the gate length larger than 10 μm or the channel thickness larger than 30 nm. It can be found that the mobility of sample AA100 becomes larger than that of ECT100. The excess trap states introduced between two deposition steps of a-Si (i.e. first for depositing S/D pads and second for forming the active area) were believed to cause the degradation of μ_{FE}.

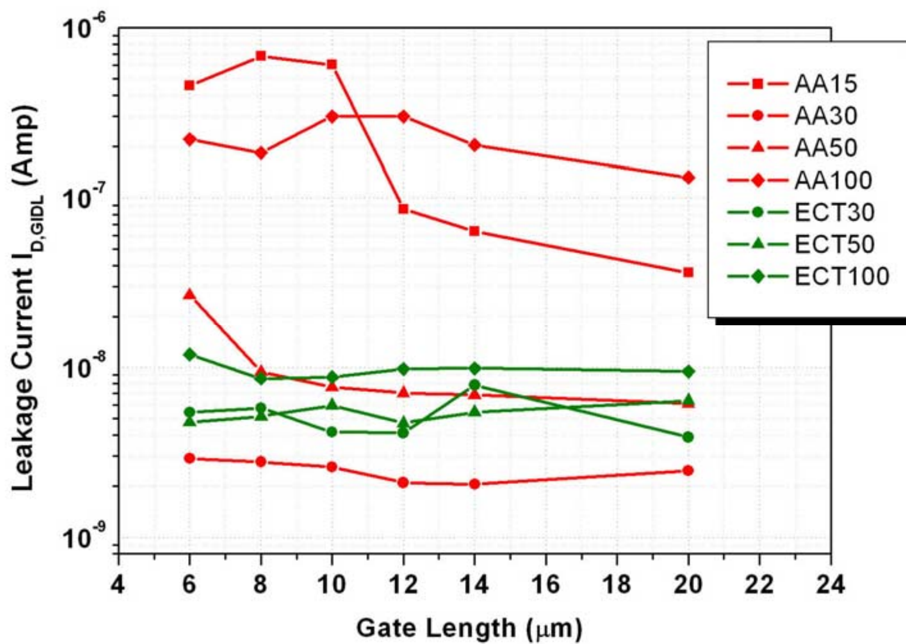
Figure 5-7(a) and 5-7(b) illustrates the off-state leakage current of TFTs at V_{GS} = 0 V and V_{GS} = -20 V, respectively. The sample AA15 notably exhibits large leakage current in both cases possibly due to the incorporation of Ni contaminants as described previously. Comparing to sample AA100, the sample ECT100 also shows larger I_{OFF} because of additional trap states introduced during the fabrication processes of elevated channel structure. For V_{GS} = 0 V or at low electric field regime, the I_{OFF} dominates by the trap-state density in the channel region as well as channel conductance, and therefore the leakage current for the other samples are all around 1×10^{-10} A. However, in Fig. 5-7(b) where the electric field dominates the leakage mechanism, sample AA100 exhibits the $I_{D,\,GIDL}$ an order of magnitude larger than ECT100 does, while the leakage current of AA50 at V_{GS} = -20 V also larger than that of ECT50, implying that the channel electric field has been redistributed and relieved effectively by increasing the junction depth in the S/D region. Nevertheless, if we further reduce the channel thickness as in the case of ECT30 and AA30, the ECTFT structure seems not to alleviate the electric field so noticeably since the thickness of S/D region of ECT30 is only 80 nm. A 2-D simulation for the distribution of the channel electric field in ECTFT

configuration is required to confirm this hypothesis.



(a)





(b)

Figure 5-7 Off-state leakage current of TFTs with different channel thickness and device structure at (a) $V_G = 0$, $V_D = 10$ V, and (b) $V_G = -20$ V, $V_D = 10$ V

5.2.2 General I-V Characteristics of ECTFT with GOLDD

In this section, we're going to discuss about the ECTFT with different doping concentration of LDD and gate-overlapped length. Fig 5-8 compares the transfer curves of ECTFT with various doping concentration of LDD region where the overlapped length d = 0 μm. Although d equals zero ideally, the misalignment between the top gate and the bottom trench region still contributed to a small gate overlapped region about 0.5-μm long, as indicated by an arrow in Fig. 5-9. Moreover, for GOLDD samples, the S/D regions suffered two doping steps from LDD and self-aligned source/drain ion implantation, respectively, so that the S/D resistance became even lower. In contrast, there were no dopants in the misaligned region below the gate electrode for non-LDD device, resulting in slightly lower ON current as shown in Fig. 5-8. In addition to transfer curves, Fig. 5-10(a) compares the mobility versus gate length while Fig. 5-10(b) compares I_{OFF} for ECTFT with different LDD doping concentration; we found no differences among these samples.

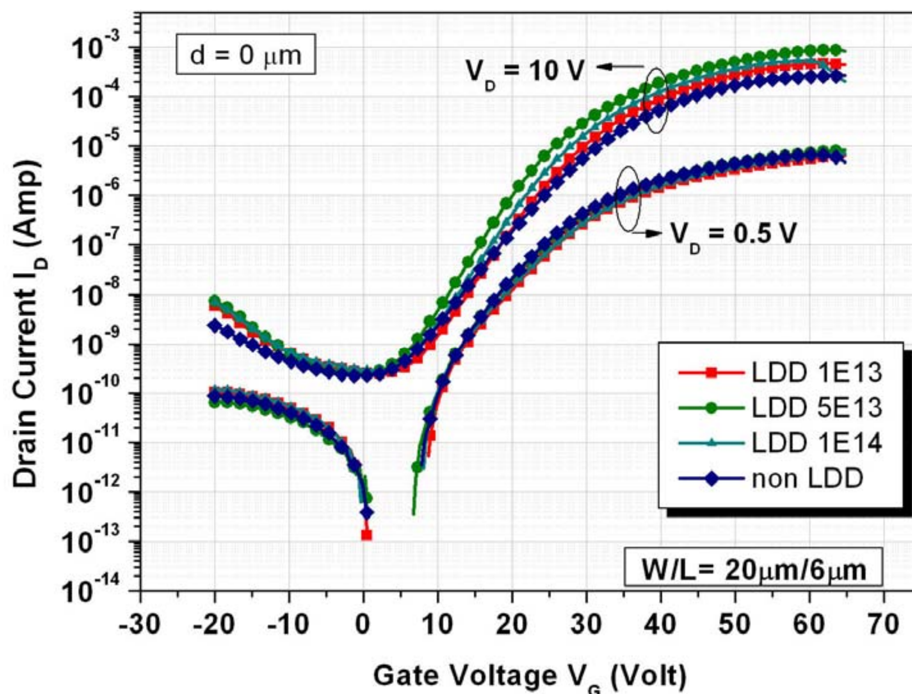


Figure 5-8 I_D - V_{GS} curves of ECTFT with various doping concentration of LDD region; W/L = 20 μm /6 μm and d = 0 μm

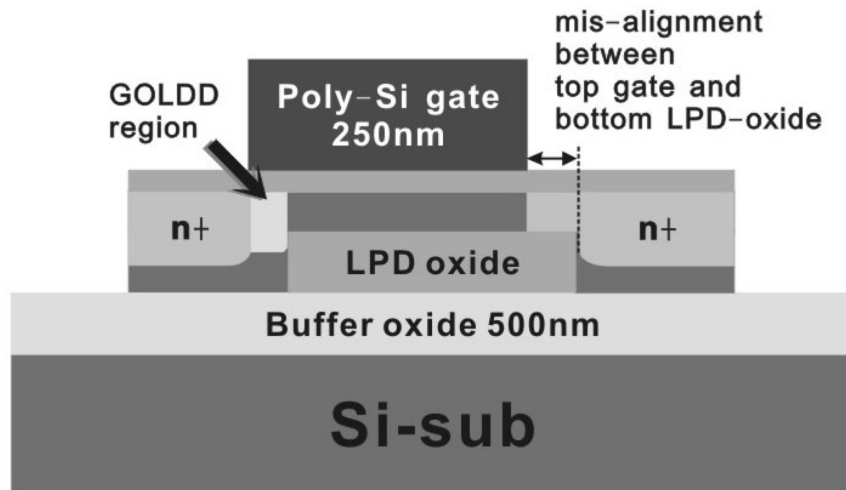
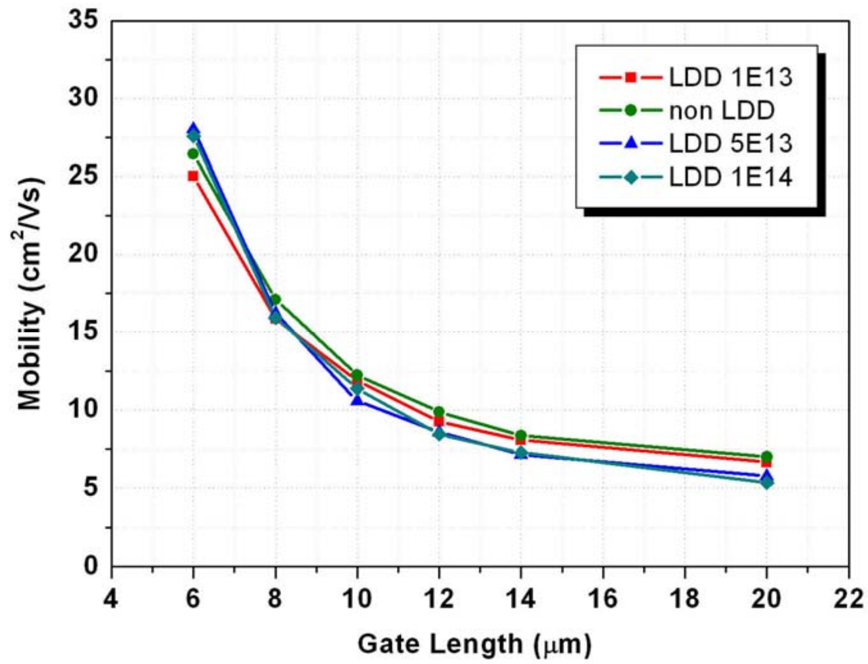
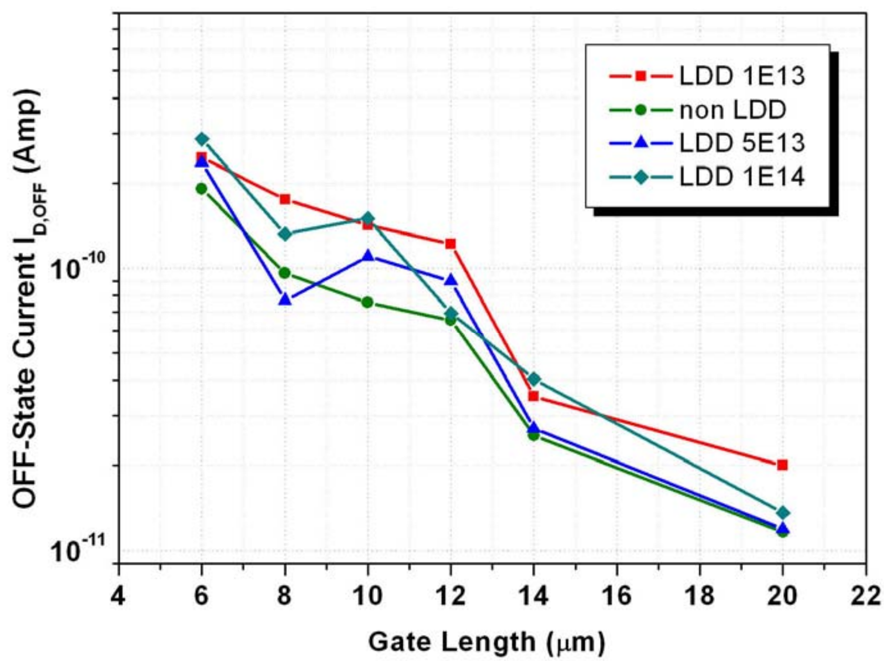


Figure 5-9 The schematic diagram for illustrating a misaligned ECTFT device with overlapped length d = 0 μm



(a)



(b)

Figure 5-10 Comparison of (a) mobility and (b) Off-state leakage current versus gate length for ECTFT with different LDD doping concentration

Figure 5-11 depicts the I_D - V_{GS} curves of ECTFT with various doping concentration of LDD region where d = 2 μm. In this case the overlapped length is large enough to

compensate the error resulted from the misalignment. Since the gate electrode would induce excess carriers in both the thin channel and the thick overlapped region at ON state of TFTs, we did not observe obvious reduction of I_{ON} for the sample without LDD doping. Contrarily, for non-LDD and low LDD dosage (1×10^{13} cm^{-2}) conditions, the overlapped region forms an additional low conductance area and contributes to low leakage current at the OFF state of TFTs. Besides, the threshold voltage decreases with increasing the doping concentration in the overlapped region, which is quite straightforward.

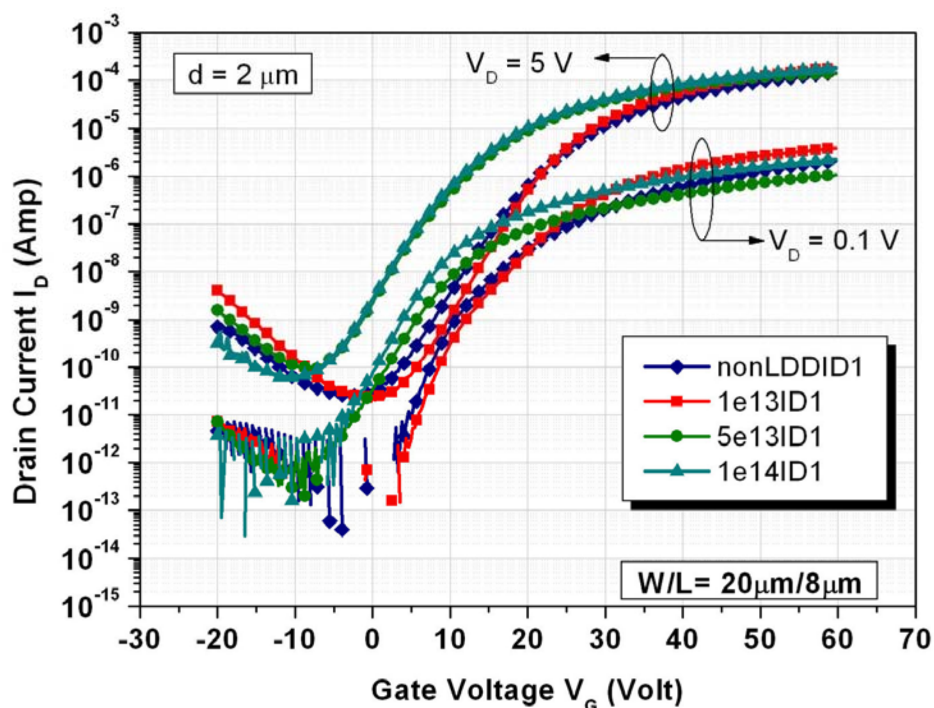


Figure 5-11 I_D - V_{GS} curves of ECTFT with various doping concentration of LDD region; W/L = 20 μm /8 μm and d = 2 μm

Figure 5-12 shows the transfer curves of ECTFT with different gate overlapped length *d*. One can find that the electrical characteristics of ECTFT such as mobility, threshold voltage and ON/OFF ratio, etc. are insensible to the overlapped length. Recalling the situation in Chap. 4 where ECTFT were recrystallized by excimer laser, increasing the gate overlapped length could deteriorate the electrical properties of TFTs owing to the incorporation of

defective thick S/D regions. However, in this chapter, the ECTFT devices were recrystallized by MILC (or partial SPC, especially for the active layer far from the Ni seeding window), and the grain size was uniformly distributed in either the thin channel or the thickened S/D region, so that the I-V characteristics of samples with various length *d* were nearly identical.

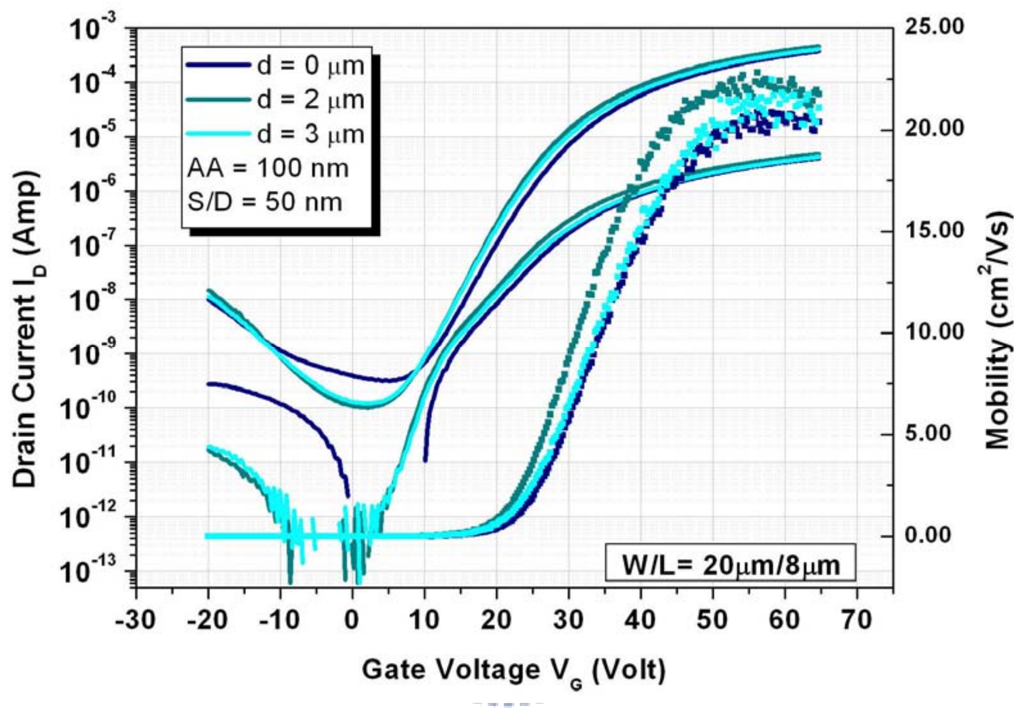


Figure 5-12 Transfer curves of ECTFT with different gate overlapped length *d*

As indicated in Fig. 5-9, there's small asymmetry of the ECTFT structure owing to the misalignment between the top gate electrode and the thin-channel region. However, since the source/drain implantation is still self-aligned and the poly-Si grains exhibit no preference for either thin or thick channel area, the transfer curves of ECTFT are basically independent of the gate overlapped length. Moreover, we made a forward-reverse measurement to the ECTFT devices, that is, the transfer curves of TFTs were measured first as *forward* I-V characteristics and then the source/drain electrodes were interchanged while *reverse* I-V characteristics were obtained. The results are shown in Fig. 5-13, where the solid lines represent a forward measurement and the dash lines represent a reverse measurement.

Although there's small difference in the value of carrier mobility, the other electrical properties such as ON/OFF ratio, threshold voltages and leakage current are nearly identical. In addition, a fully self-aligned ECTFT on glass substrates can be easily manufactured by backside lithography, which utilizes the opaque thick S/D region as the hard mask to define the gate electrode on the front side.

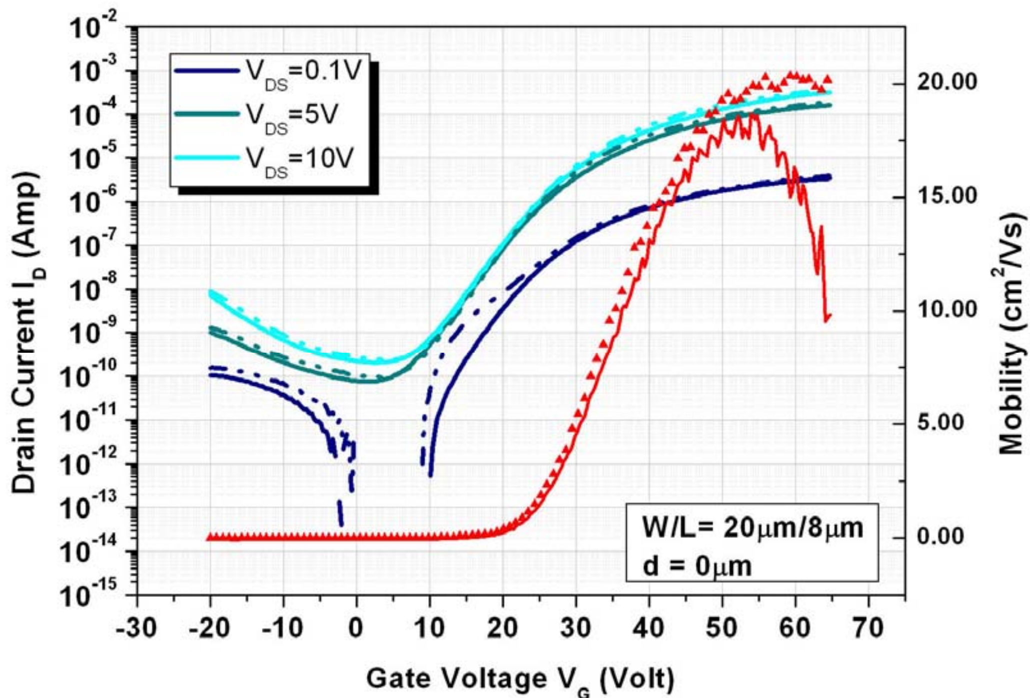


Figure 5-13 Forward (solid line) and reverse (dash line) measurement of the transfer curves of an ECTFT with W/L = 20 μm/8 μm and d = 0

One of the main advantages of the proposed ECTFT devices is that the thickened source/drain region can effectively reduce the series resistance when the channel region becomes thinner. For small drain bias V_D at a high gate drive, it is assumed that the ON resistance R_{ON} of TFTs consists of the channel resistance R_{ch} and the S/D series resistance R_{SD} [5.12], [5.13], that is,

$$I_{DS} = \frac{W}{L}\mu C_i (V_G - V_{th} - \frac{V_D}{2})V_D \qquad \text{as } V_D \ll V_G - V_{th} \qquad (5\text{-}1)$$

$$R_{ON} = \frac{\partial V_D}{\partial I_{DS}}\Big|_{V_D \to 0}^{V_G} = R_{ch} + R_{SD} \qquad (5\text{-}2)$$

and the channel resistance in the linear region is approximately given by

$$R_{ch} = \frac{L}{W\mu C_i (V_G - V_T)} \qquad (5\text{-}3)$$

where L is the channel length, W is the channel width, C_i is the capacitance per unit area of the insulating layer, V_{th} is the threshold voltage, and μ is the field effect mobility. Then the R_{SD} can be extracted by measuring R_{ON} of output characteristics of TFTs in the linear region and by plotting $R_{ON}W$ as a function of L. Hence, the R_{SD} is a set of these straight lines intersecting at a small triangle area. Figure 5-14 shows the value of R_{SD} with respect to different TFT structures, active layer thickness and dopant concentration of LDD. When the channel thickness reduces to 30 nm, the S/D series resistance of conventional TFT architecture cannot be neglected and the large parasitic effects could degrade the performance of TFTs. Contrarily, the thickened source/drain regions of sample ECT30 exhibits a much lowered R_{SD} of 430 kΩ; the sample ECT50 also shows R_{SD} of around 200 kΩ as compared to the sample AA50 with R_{SD} of 250 kΩ. Besides, the LDD doping concentration has no impression upon the S/D series resistance, and when the channel thickness increases to 100 nm, the R_{SD} cannot be further reduced by ECTFT structure.

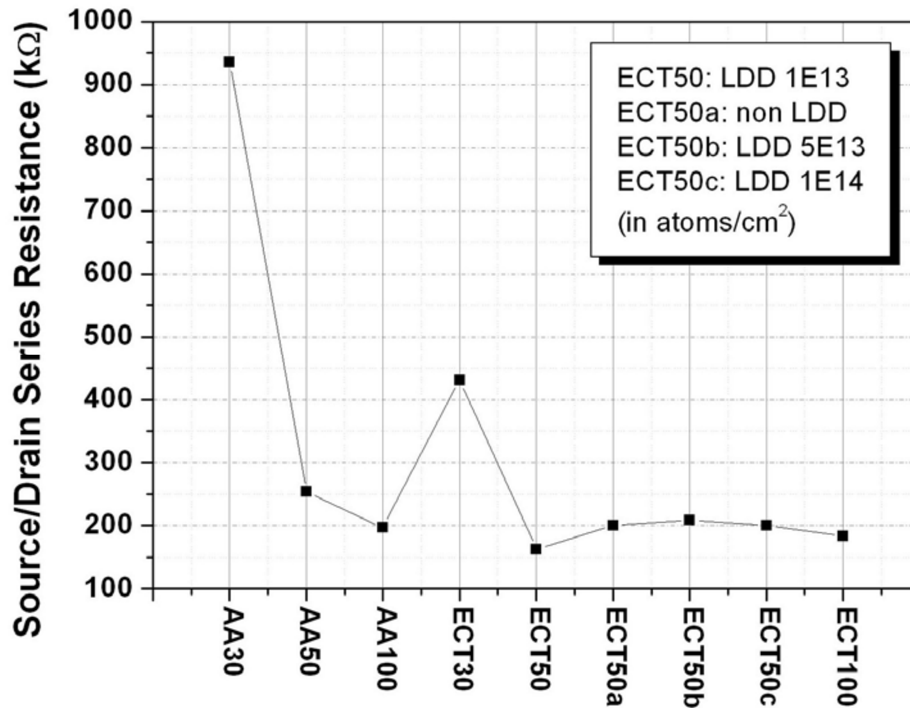
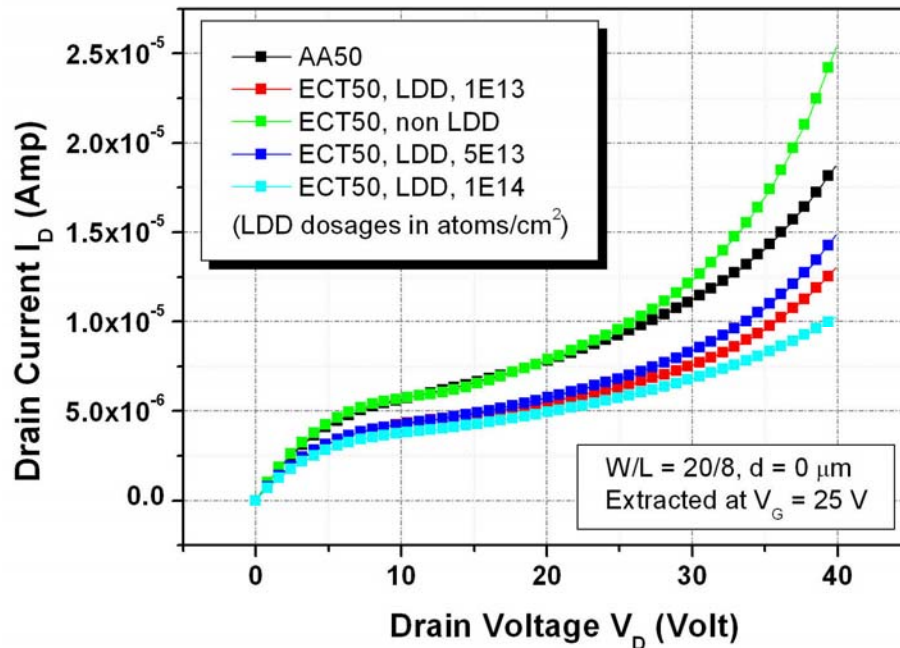


Figure 5-14 The values of the extracted source/drain series resistances for different conventional TFT and ECTFT samples

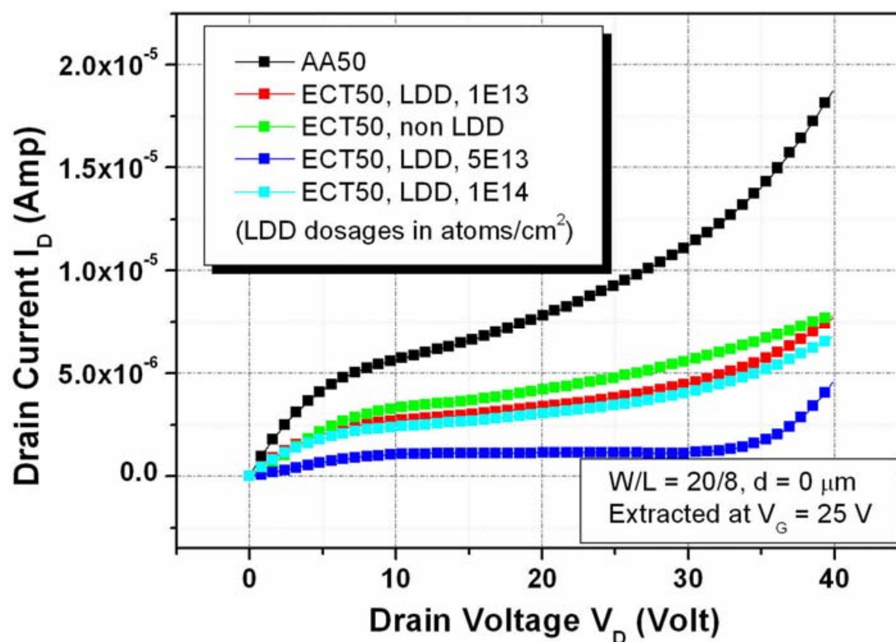
5.2.3 Kink effect and Hot Carrier Endurance

As described in *section 4.4* that the ECTFT architecture would increase the junction depth of the drain side so that the large lateral electric field can be redistributed and relieved. Therefore, the kink phenomenon and the hot carrier endurance of TFTs can be greatly improved by the elevated channel with gate overlapped structure, as can be seen in Fig. 4-9 and Fig. 4-12. Here, we compared the output characteristics of different TFT structures recrystallized by MILC/SPC process. Figure 5-15 illustrates the I_D - V_D curves of TFTs extracted at V_G = 25 V, where the gate-overlapped length *d* is 0 μm in Fig. 5-15(a) and *d* is 2 μm in Fig. 5-15(b). Compared to the sample AA50, the ECT samples with d = 0 exhibit no notable improvement to the kink suppression, while the sample of ECT50 without LDD dopants even shows more severe kink effect than the control sample AA50. On the other hand, the kink phenomenon can be effectively eliminated by increasing the gate overlapped length d to 2 μm. In order to statistically define the kink phenomenon, the kink starting point can be

found by the derivative of drain current, that is, the corresponding drain voltage V_D at which the output conductance dI_{DS}/dV_{DS} curve starts to bend. The averaged kink point from at least three samples for ECTFT with d = 2 μm was depicted in Fig. 5-16.



(a)



(b)

Figure 5-15 I_D - V_D curves extracted at V_G = 25 V for various TFT samples: (a) W/L = 20/8, d = 0 μm, and (b) W/L = 20/8, d = 2 μm

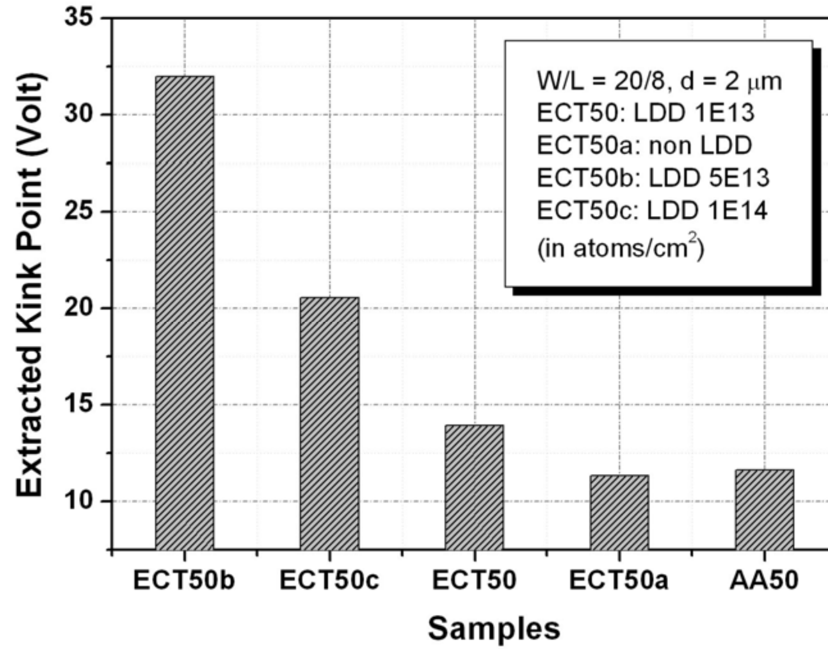


Figure 5-16 Extracted kink point for different TFT samples; W/L = 20/8 and d = 2 μm

From the above figures, we found that the gate electrode must overlap the thick drain junction to acquire the effective improvement for the kink phenomenon, and the GOLDD region was also indispensable to the relief of the large drain electric field. However, compared to the experimental results performed in Chap. 4, the ECTFT recrystallized by excimer laser exhibits less dependence on the overlapped length. Actually, the kink phenomenon of poly-Si TFTs not only depend on the lateral electric field near the drain but also on the drain-induced grain-boundary barrier lowering (DIGBL) [5.14], [5.15] as well as the grain-boundary traps induced avalanche generation effect [4.9]. The DIGBL effect is caused by the drain bias V_{DS} modulating the grain-boundary potential barrier heights in the drain junction to form asymmetric barriers. Extra carriers, which were injected from the lower side of the barriers into the drain junction, would increase the drain current as V_{DS} increases. Besides, the charged states at the grain boundaries of the drain junction also create the high local electric fields. Accordingly, the grain size and the density of the grain boundaries near the drain also affect the kink effect [5.16]. For ELA recrystallized samples, a

lateral growth of poly-Si grain occurred, which started from the thick S/D region (as recrystallization seed) and extended into the thin channel region. Even if the gate electrode did not precisely overlap with the thick drain area, the larger silicon grain in the channel region still provided the resistance to the kink effect and the channel hot electrons.

Figure 5-17 shows the degradation of ON current of TFTs versus stress time. The stress conditions is V_D = 25 V, V_S = 0 V and V_G = 7.5 V. For this situation, the drain bias would result in a large lateral electric field in the drain junction while the channel hot electrons break the weak Si-Si or Si-H bonds, contributing to creation of the interface states and I_{ON} reduction of TFTs. In Fig. 5-17, because the sample ECT50 has enough overlapped length *d* of 2 μm to compensate the alignment error, satisfactory hot carrier endurance was obtained. Moreover, sample ECT50 without LDD doping still possesses good hot carrier reliability, implying that just increasing the drain junction depth is enough to reduce the drain electric field. In contrast, increasing the LDD doping concentration to 1 × 10^{14} cm^{-2} could inversely deteriorate the hot carrier reliability of ECTFT.

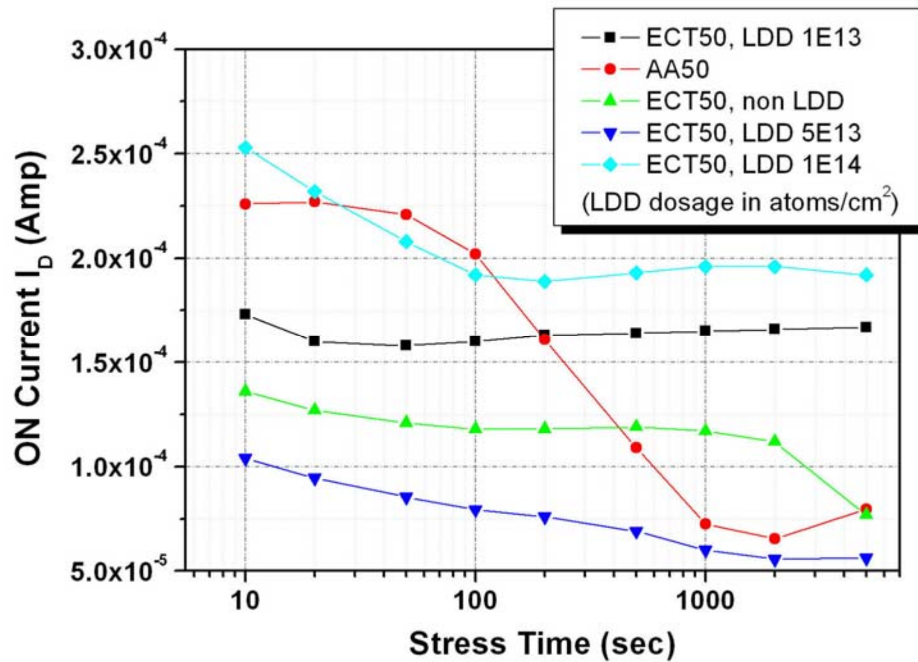


Figure 5-17 Degradation of ON current of TFTs under hot carrier stress; W/L = 20/8, d = 2 μm for ECTFT devices

In addition, Fig. 5-18 shows the variation of threshold voltages with respect to the stress time. It can be found that the V_{th} increased obviously for samples AA50 and ECT50 with high LDD doping concentration. As described in *section 4.1.3*, including charge injection, interface state generation or deep state creation in the grain boundaries all contribute to the change of threshold voltages. Nevertheless, it has been suggested that V_{th} time-dependent degradation under stress can be empirically modeled by a power law of the form [4.16], [5.17], [5.18]:

$$\Delta = C \times t^{n} \tag{5-4}$$

where Δ is $\Delta V_{th} = |V_{th\text{-}initial} - V_{th}|$, C is a pre-factor, t is the stressing time and n is the power-law exponent. The extracted n factor versus different channel thickness or doping concentration is plot in Fig. 5-19. It is generally agreed that for bias-stress induced V_{th} shift in poly-Si TFTs, power-law exponents in the range of 0.1-0.3 are indicative of hot-carrier injection, whereas power-law exponents in the range of 0.4-0.6 are indicative of deep-state generation, presumably at crystal-domain boundaries [4.16], [5.19], [5.20]. Accordingly, the main degradation mechanism of V_{th} shift for all tested samples can be classified as carrier (electron) injection to the gate oxide and thus resulting in a positive V_{th} shift as indicated in Fig. 5-18.

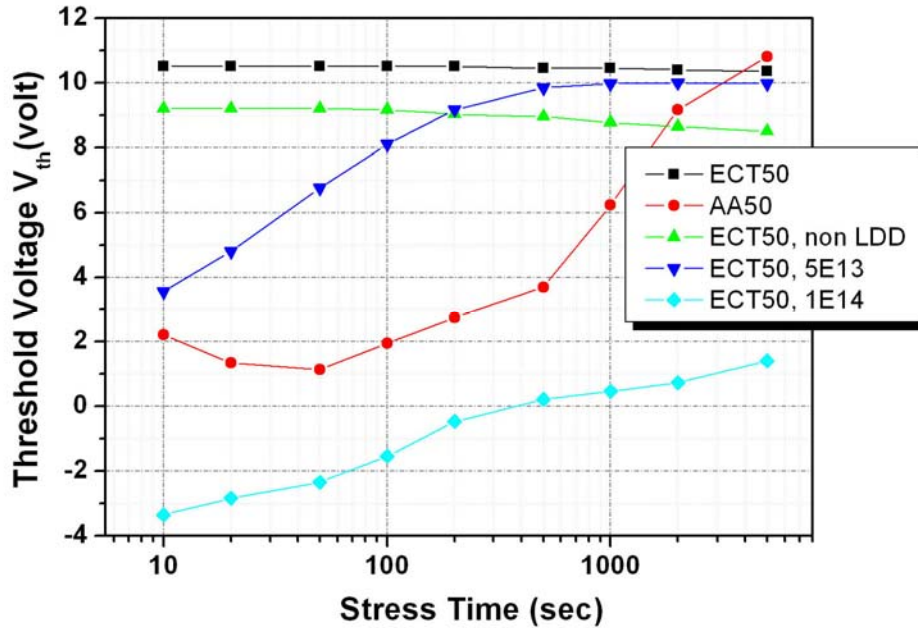


Figure 5-18 Threshold voltage shift of TFTs under hot carrier stress; W/L = 20/8, d = 2 μm for ECTFT devices

Table 5-1 Power-law exponent n of various active layer thickness and LDD doping concentration of TFTs

Samples	ECT30	ECT50	ECT100	AA30	AA50	AA100	ECT50 (non LDD)	ECT50 (5E13)	ECT50 (1E14)
n factor	0.32	0.16	0.15	0.29	0.34	0.09	0.34	0.12	0.35

Finally, we compared the degradation of ON current under forward or reverse stress to examine the symmetry of the reliability characteristics. As shown in Fig. 5-19, the sample ECT50 with d = 2 μm exhibits no dependence on the setting of the source/drain electrode, because the overlapped length is long enough to compensate the alignment error between the top gate and the bottom thin channel region. The electric field can be always redistributed by the LDD region and the thick S/D junction area and therefore the hot carrier reliability is satisfactory for both forward and reverse measurement; in other words, the ECTFT with a suitable gate overlapped length provides good immunity to the alignment error, although the

ECTFT structure itself is not fully self-aligned. On the other hand, the I_{ON} of sample ECT50 degraded seriously, even faster than the control sample AA50, in either forward or reverse measurement. It was speculated that the intense electric field in the thin channel region and the lack of enough LDD region directly cause the fast degradation of ON current. However, the ON current of these samples recovers slowly after being stressed over 100 sec. It may attribute to the weak Si-Si bonds created in the two step deposition process of a-Si would break first by the channel hot electrons and then these trap states were gradually filled in the following stress measurement.

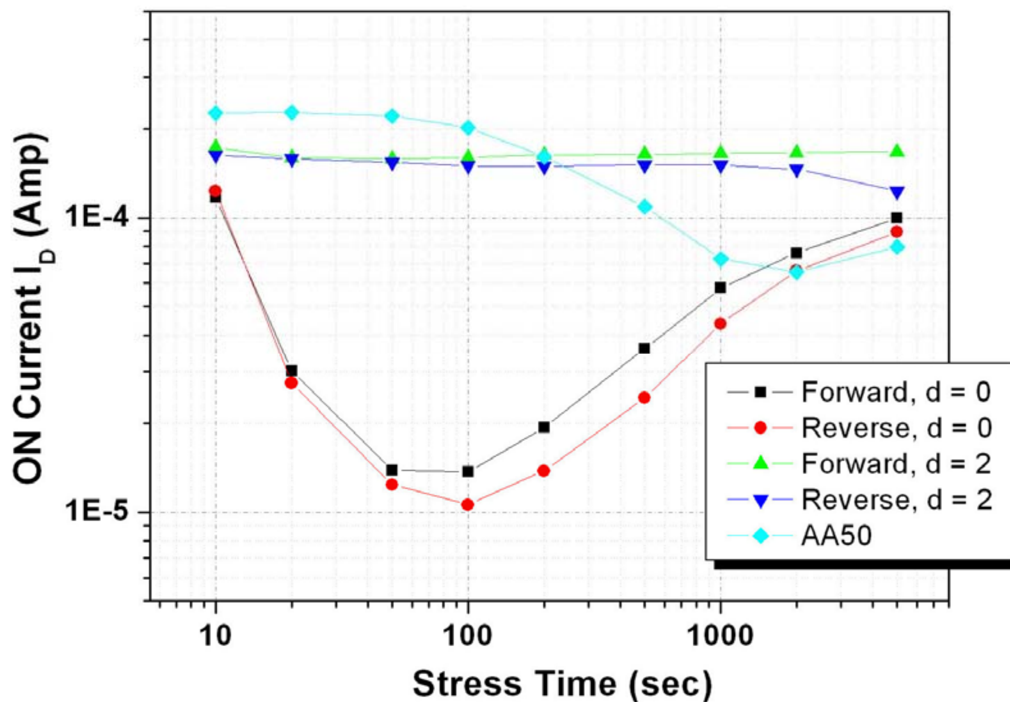


Figure 5-19 Degradation of ON current of TFTs under forward or reverse stress; W/L = 20/8

5.3 Summary

In this chapter, we thoroughly examined the electrical characteristics of the proposed ECTFT architecture. Reducing the channel thickness was beneficial for suppressing the

OFF-state leakage current of TFTs, but the ON current and the mobility did not improved because the poly-Si grains recrystallized by MILC/SPC processes were constrained in a thin channel region. On the other hand, thickened the source/drain region greatly reduced the parasitic R_{SD} of TFTs, especially for those with ultra-thin channel region and short gate length. The anomalous output characteristics and the hot carrier endurance can also be enhanced by connecting the thin channel to the thick source/drain area. A proper gate overlapped length (depending on the precision of photo lithography during TFT fabrication) and LDD doping concentration are required to maintain all of the mentioned benefits of ECTFT structure.

For further optimizing the performance of ECTFT such as μ_{FE}, ON current and ON/OFF ratio, the MILC process should be modified. It was recommended to recrystallize the active area immediately after active layer deposition process and the seeding window should be closer to the channel region to enhance the MILC efficiency. This idea cannot be fulfilled in our lab (nano facility center, NCTU) because the poly-Si layer after MILC contains metal contamination and is prohibited from submitting to the PECVD chamber to deposit gate oxide and gate electrode. Excimer laser annealing is another good candidate for ECTFT architecture because ELA induces super lateral growth of poly-Si grain as described in chapter 4.