Chapter 8

Conclusions and Future Prospects

8.1 Conclusions

Recently, the concept of the so-called “Flexible Electronics” is advocated in semiconductor and flat panel display industry. The applications of flexible electronics include the corporation or product brochure DM, dashboard of cars, PDA, RF ICs, biochemical sensors, electronic papers, e-books, wallpaper-type solar cells, smart cards, clothes, disposable electronics, etc. It is also predicted that the market share of the flexible electronics would reach 58 billion dollars in 2009 and 235 billion dollars in 2012. That’s why we devoted ourselves to the research about fabricating thin film transistors on plastic substrates in this work.

Fabricating thin film devices directly on the plastics suffers many obstacles, most of them arising from the nature of low melting temperature and large thermal expansion coefficient of polymeric backplanes. Therefore, we proposed a device transfer technique (abbreviated to DTBE) to avoid these issues. The thin film devices were first fabricated on a Si wafer and then adhered to the host substrate; the remaining Si was then removed with different methods. In chapter 2, the backside Si was polished by CMP process followed by the wet chemical etching while in chapter 3 the backside Si was etched by spin etching technique. Since the starting material is Si wafer, the DTBE technique is fully compatible for conventional CMOS process and high performance devices with high circuit density can be transferred to virtually any rigid substrate. Additionally, the bending tests were performed to examine the electric characteristics of TFTs after being transferred to a flexible substrate, and no remarkable changes were observed even at a small bending curvature of 2 cm.

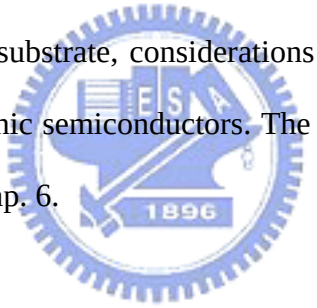
According to the roadmap of LTPS TFTs, the integration of low-end graphic controller

and logic circuits to the glass substrate is one of a future trend to further decrease the production costs and to make a value added flat panel. From this point of view, the device uniformity, electrical performance and long term reliability become very important. In chapter 4 and 5, we proposed a novel elevated-channel TFT architecture (abbreviated to ECTFT) to address the mentioned problems. The ECTFT possesses a thin channel region to reduce the OFF state leakage current; the thin channel region is connected to the thickened source/drain region to reduce the parasitic series resistance. The deeper junction depth formed in the thick S/D region also redistributes the peak electric field near the drain side, so that the kink phenomenon and the hot carrier reliability can be greatly improved. Besides, the a-Si layer with different thickness creates temperature gradients during excimer laser annealing and thus a super lateral growth of poly-Si grains was observed. Through ECTFT structure, the channel of TFTs was located exactly in the large grain region, so that the device performance as well as uniformity was improved. Moreover, we introduced the selective liquid-phase deposition method during the fabrication process of ECTFT. The S-LPD technique is quite applicable for fragile glass substrate because it can deposit SiO_2 at room temperature and also planarize the surface without using CMP or additional photomask.

The development of new materials sometimes gives rise to a revolution in device structures, applications and even human's life. Although conventional poly-Si TFTs can be manufactured on the plastic substrate in virtue of either excimer laser annealing or the proposed DTBE technique, the production costs cannot be drastically reduced and thus the associated applications are probably confined in some niche markets. However, the emergence of polymeric semiconductor devices such as organic TFTs and organic LEDs could have changed the current prospect, because these materials can be easily deposited on the plastic substrate at room temperature with large surface coverage. In chapter 6, we first examined the optimal deposition conditions of spin-on poly-3-hexylthiophene (P3HT) films, and then several kinds of transistor architectures were investigated, including top contact or

bottom contact type OTFTs, and OTFTs with field isolation structure. In order to further reduce the production costs, we found that the source/drain metals can be replaced by Ni/Pt composite layer instead of noble materials such as Pt, Pd or Au, while a satisfactory ohmic contact between P3HT and S/D electrodes is still preserved. In chapter 7, reliability characteristics of P3HT were investigated. Oxygen auto-doping effect seriously deteriorates the electrical properties of OTFTs but can be partially restored by N_2 or vacuum treatment. In addition, several kinds of electrical bias stress on OTFTs were implemented. We did not observe degradation of I-V curves due to hot carriers or self heating effects, but found a significant V_{th} shift with respect to the bias polarity. A polarization model was developed to explain the hysteresis phenomenon of OTFTs.

Finally, we also made some in depth paper reviews about the LTPS technology, specific processes of TFTs on the plastic substrate, considerations of electrical properties of poly-Si TFTs and the background of organic semiconductors. The related discussion can be found in Chap.1, Chap. 2, Chap. 4, and Chap. 6.



8.2 Future Works

8.2.1 High Performance TFTs on Plastic Substrate

In Chap. 2 and Chap. 3, we focused on the device transfer process itself and developed several methods to remove the residual Si of the backside. Nevertheless, we did not fully take the advantage of the DTBE technique, especially the allowed high process temperature of TFTs. There're plenty of ways to improve the performance of TFTs. First, the active layer can be recrystallized by metal-induced lateral crystallization method followed by high temperature annealing with excimer laser or furnace to fix the defects in the grain or grain boundary. Besides, instead of PECVD, the gate insulator can be formed by thermal oxidation with thinner thickness. Actually, the field-effect mobility of a high-temperature processed

poly-Si TFTs crystallized by conventional SPC reaches 100 cm^2/Vs, which is the case of light shutter (on quartz substrate) used in the projectors. Moreover, the silicidation process in the source/drain area is also beneficial for reducing the parasitic resistance.

The transference of single crystal silicon to the plastic/glass substrate had been demonstrated in *section 3.6*. The next step is surely to transfer whole MOS devices from Si wafer to another host substrate. Since the thick film photo resist has high viscosity and low spatial resolution, the frequency of the usage of thick film P.R. should be as low as possible, implying that the mesa type Si-island must be formed at last. At this stage, however, the MOS device cannot suffer from any long term high-temperature process (>600^oC) to prevent dopant redistribution, silicide agglomeration or spiking of the metal interconnection, etc. Therefore, how to fabricate a high quality etching stop layer against backside etching process becomes critical. In addition, there're still some uniformity issues to be addressed about spin etching process as the nozzle cannot spray the etchant evenly to the entire wafer.

Finally, for those devices after being transferred to the flexible substrate, more verification can be made, for example, the bending tests with tensile stress, the electrical or humidity/UV-light stress, and the optical/mechanical characteristics etc.

8.2.2 T-gate Poly-Si TFTs

As described in *section 4.2.2* that the gate-overlapped LDD structure can reduce the lateral electric field without introducing additional parasitic resistance in the lightly doped region. The S-LPD technique was utilized to fabricate this ECTFT with GOLDD structure. Actually, employing the special selective characteristic and planarization ability of LPD oxide, a T-gate structure as shown in Fig. 8-1 can be fabricated with the following procedures. First, the active layer of a-Si and gate insulating layer were deposited and recrystallized on an oxidized Si wafer. The poly-Si gate electrodes (or Ta metal gate) were then deposited and patterned. Without removing the photo resist, the phosphorus ions were implanted as the

LDD region followed by the selective LPD-oxide deposition, as shown in Fig. 8-1(a). Next, the LPD oxide was etched back to a proper thickness and then another poly-Si layer was deposited. After reactive ion etching process, a self-aligned poly-Si spacer can be formed as shown in Fig. 8-1(b). Finally, self-aligned S/D ion implantation was performed to complete the T-gate poly-Si TFT architecture. Since this T-gate structure is quite similar to the conventional GOLDD TFTs, it was believed that the kink phenomenon and hot carrier endurance can also be improved as well.

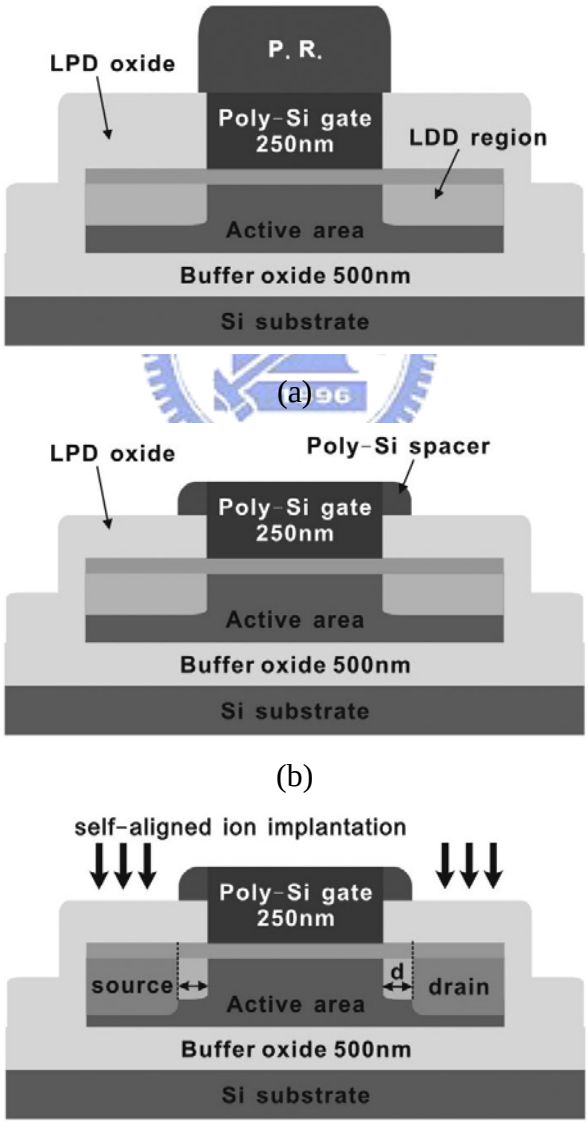


Figure 8-1 Process flow of a T-gate poly-Si TFT

8.2.3 P3HT-based Organic TFTs

The experimental results made in Chap. 6 and Chap. 7 provided very much elemental knowledge about the spin-on deposition, electrical characteristics and reliability issues of P3HT-based OTFTs. Nevertheless, the performance of OTFTs can be further improved in several aspects. First, it has been reported that a plasma treatment such as O_2 or H_2 prior to the organic layer deposition step would reduce the interface states of gate insulator and improve the injection ratio of carriers from the metal surface, so that the field-effect mobility of OTFTs are increased. In a similar concept, we believed that a post treatment directly to the organic active layer with H_2 or NH_3 plasma for a short period can also passivate the trap states in the active area, while the hydrogen radical acting as a reducing agent could restore the electrical properties of P3HT layer doped by oxygen atoms. Moreover, the field-effect mobility of P3HT-based OTFTs can be greatly improved (> 0.15 cm^2/Vs) by mixing single wall carbon nanotubes (SWNTs) as the conducting rods in the P3HT active layer as the soluble semiconducting matrix [8.1], and the P3HT thin film can also be doped by PEDOT or by mixing Au particles in the active layer to reduce the parasitic resistance at the source/drain area. Thus, novel OTFT structures must be developed to apply the mentioned doping process properly.

Second, the operation voltage of P3HT-OTFT is quite large, which is inadequate for the application of portable devices. Reducing the thickness of gate insulating layer and replacing the gate oxide with high-k gate dielectric are both possible approach to reduce the operation voltage. However, higher gate leakage current with reducing the oxide thickness and the interface states at the high-k dielectric/P3hT interface should be addressed carefully.

Third, it had been proved that the oxygen auto-doping effect deteriorated the electrical properties of OTFTs remarkably. Therefore, an oxygen-free deposition environment, possibly in vacuum or with N_2 purge, must be established; the measurement of OTFTs should also be performed in a well-controlled environment to ensure the repeatability and the reliability of

the experimental results from run to run. Besides, a capping layer such as SiO_2, SiN_x or the other spin-on polymeric material (e.g. polyimide) can be applied to the OTFTs to prevent the P3HT layer from exposing continuously to the air.

Finally, since the P3HT film can be easily deposited and cured at relatively low temperature (<150^{o}C), it is straightforward to fabricate P3HT-based OTFTs on the plastic substrates. In doing so, the gate materials such as ITO, Al or Cr can be deposited by E-Gun evaporation system, while the gate insulator was formed at room temperature by liquid-phase deposited oxide or high-k dielectric or their composite structure. Furthermore, integration of OTFTs and OLEDs in the same display panel has become another hot research topic in the near future.