The Research on Novel Device-Transfer Technology and Organic Thin-Film Transistor

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ABSTRACT

In this thesis, we explored several key technologies for fabricating semiconductor devices on the flexible plastic substrates. Since the melting temperature of polymeric substrates is just around 200^{o}C, conventional high-temperature processes of poly-Si thin-film transistors (TFTs) including thin-film deposition, gate oxidation, and recrystallization or activation by furnace, etc. cannot be applied. Compared to glass substrates, the water absorption rate and the thermal expansion coefficient of the plastic substrate are larger, contributing to alignment errors during the lithography process, while the stacking films on the substrate may crack or delaminate due to the inherited thermal stress. Finally, the special physical and chemical properties of a flexible substrate also limit the feasibility of cleaning or wet etching processes and the transport by robots. All of the mentioned obstacles make fabrication TFTs directly on the plastic become even harder.

Therefore, we proposed a concept of device transfer by backside etching (DTBE). The poly-Si TFTs were first fabricated on an oxidized silicon wafer; the carrier mobility was 32.3 cm^2/Vs and ON/OFF ratio was about 4×10^6. On the other hand, the plastic substrate was pre-baked at 150^{o}C to eliminate the size expansion and then treated with ozone water. By utilizing the liquid-phase deposition (LPD) technique, the SiO_2 layer can be deposited at the both side of the substrate at room temperature to serve as the water/gas barrier, contamination

barrier and stress compensation layer. Next, the Si wafer with TFTs on it was adhered to the plastic substrate with proper optical adhesives and then the backside Si was etched by chemical mechanical polishing (CMP) to 20 – 40 μm. Finally, the residual Si was etched by Si etchant (Si/SiO_2 selectivity up to 80) with thermally grown SiO_2 as the etching stop layer. After define the contact windows, the process of transferring thin-film devices to another rigid glass/plastic substrates was completed. The DTBE technique caused neither the change of electrical characteristics nor the yield loss of TFTs; it is also compatible with conventional CMOS process and gets rid of many limitations of polymeric backplanes.

For those flexible or ultra-thin glass substrates, the CMP process may result in the uniformity issues or break the samples, so we adopted the full wet-chemical etching processes to remove the backside silicon. It had been demonstrated that a 4” sized pattern can be transferred successfully to glass by KOH and Si etcher with high selectivity. We also developed the spin-etching technique, proposed a model to explain the correlations among flow rate, spin speed and etching rate, and found an optimal spin-etching condition. The advantages of spin etching include the fast backside etching rate (finished in 3-5 min), low consumption of chemicals, good heat dissipation during etching process and generating no mechanical stress. A pattern with a diameter of 5 cm had been transferred to the surface of a flexible plastic substrate. The mobility of TFTs after DTBE is 43 cm^2/Vs, V_{th} = 10 V and with ON/OFF ratio larger than 10^6. Under a bending test with curvature of 2 cm, the electrical properties of TFTs showed no remarkable change. Moreover, the single crystal silicon had also been transferred successfully by spin etching technique from a normal Si wafer. We’ll examine the electrical properties of MOS transistors after DTBE in the future.

Conventional low-temperature poly-Si (LTPS) TFTs generally suffer from high leakage current, kink phenomenon and hot carrier endurance issues owing to the large lateral electric field near the drain side. Consequently, a novel elevated channel TFT (ECTFT) with gate overlapped LDD (GOLDD) structure was proposed, which includes a 100-nm channel and a

150-nm source/drain region. The planarization between the thin channel and the thick S/D regions was obtained by selective LPD technique, requiring no additional photo mask or CMP step, and fully compatible with the LTPS process on glass/plastic substrates. The excimer laser annealing was performed to recrystallize the a-Si active layer. Since the unmelted Si at the thick S/D region acts as the crystallization seed and also causes the super-lateral growth phenomenon in the channel region, the grain size of poly-Si exceeds 2 μm while the carrier mobility of ECTFT is larger than 150 cm^2/Vs and ON/OFF ratio over 10^7. The process window of laser energy for ECTFT is quite wide, implying a good uniformity of device characteristics. On the contrarily, the carrier mobility decreased to 81 cm^2/Vs if simply increased the active layer thickness to 150 nm. Because the trap state density increased with the channel thickness, the OFF-state leakage current of a conventional TFT structure became large. Notably, the drain electric field can be relieved by the GOLDD and the thick junction depth of drain electrodes, so the kink effect and the hot carrier degradation can be effectively suppressed.

The ECTFT was also fabricated by metal-induced lateral crystallization. When the active layer thickness of a conventional TFT reduced to 50 nm or even 30 nm, the leakage current of TFTs can be suppressed but the mobility also deteriorated due to the large parasitic resistance. In contrast, lower source/drain series resistance was obtained for ECTFT architecture. Besides, we found an optimal doping concentration of 1×10^{13} cm^{-2} at the GOLDD region and a overlapped length of 2 μm, at which the drain electric field can be greatly redistributed. Additionally, the normal I-V characteristics of GOLDD-ECTFT structure were not altered because at ON-state the gate electrode would induce the excess free carriers at the LDD region.

Recently, with the development of organic semiconductor materials, the devices can be fabricated easily on plastic substrates by spin coating process with extremely low production costs. In this work, we chose poly-3-hexylthiophene or P3HT as the active layer of organic

TFTs (OTFTs). At a wt.% of 0.3 in chloroform, the OTFTs possessed the highest ON/OFF ratio and the lowest surface roughness, while the field-effect mobility was up to 2×10^{-3} cm^2/Vs. The primary leakage path of OTFTs lies in the conductive bulk of P3HT, and another one is through the gate insulator. Therefore, the leakage current can be greatly eliminated by growing the field oxide layer at the source/drain junction and adjusting the wt.% of P3HT solution. Besides, the conventional OTFT relies on the noble Pt or Au to form ohmic contacts with P3HT. In this thesis, we found a stacking S/D electrode composed by a thick Ni and a thin Pt layer was capable for forming ohmic contacts with P3HT; no crowding effects were observed while the production costs can be reduced. Furthermore, the contact resistance can also be decreased by reducing the thickness of the adhesion layer Ti.

Organic materials are susceptible to both moisture and oxygen. Exposing OTFTs to an oxygen ambience for 3 hr would increase the threshold voltage significantly because oxygen atoms are effective p-type dopants for P3HT. Further treatment to OTFTs with oxygen degraded the electrical properties. In addition, we found no impacts when immersing the OTFTs in D.I. water for 8 hours, but a longer immersion time could cause OTFTs malfunction because H_2O diffused through the pin holes of the organic layer to the P3HT/SiO_2 interface. For electrical reliability tests, the mobility and leakage current of OTFTs did not change in either gate bias stress or hot carrier/self heating stress for over 10,000 sec. However, a noticeable threshold voltage shift was observed, and the direction of the V_{th} shift depended on the polarity of external bias. A polarization model of P3HT film was proposed to explain the observed phenomenon. This temporary polarization effect can be reversed and would not occur in an ac mode operation.