Chapter 1

Introduction

In 1966, the first polycrystalline silicon thin-film transistors (poly-Si TFTs) were fabricated by C. H. Fa et al. [1.1]. Since then, many investigations have been devoted to the physics, applications, fabrication processes and device structures of TFTs. In 1970s, the conduction mechanism and the electrical properties of polycrystalline silicon film, determined predominately by grain boundaries, were clarified [1.2], [1.3]. Nevertheless, the main motivation that attracts so much attention to the research of TFTs is the emergence of the active matrix liquid-crystal display (AMLCD) industry [1.4]. The concept of an AM drive for use in LCDs goes back to 1971 when Bernard Lechner, Frank Marlowe, and others at RCA laboratories proposed the idea of using an array of TFTs to control cells [1.5]. Thereafter, under a series of funding from the U.S. Air Force and the Office of Naval Research, T. Peter Brody and his colleagues of the Westinghouse Electron Tube Division used cadmium selenide as a semiconductor material for the TFT, and then in 1973, they achieved the first AMLCD panel with 6 inches × 6 inches, 14000 dots [1.6].

At the beginning, CdSe and tellurium (Te) had been used to fabricate TFTs, but these materials are either toxic or leaky at its OFF state. In 1983, by utilizing high-temperature poly-Si processes on quartz, Shinji Morozumi and his colleagues at Seiko Epson succeeded in demonstrating the first full-color display for pocket TVs, a 2.13 inches device with a 240 × 240 resolution, [1.7]. It was not until 1982, W. B. Spear, a researcher at the University of Dundee in Scotland, visited Japan and suggested that with amorphous-Si:H (a-Si:H) he had been able to fabricate an field-effect transistor (FET) [1.4]. This made the liquid-crystal engineers who had been working on tellurium excited and initiated the work on a-Si TFTs. The field was soon crowded with major electronics companies and laboratories such as

Canon, Fujitsu, French Telecommunication Laboratory, French CNET Laboratory, Toshiba, Hitachi and Matsushita. In the following years, based on a-Si technology, all kinds of electronic products equipped with AMLCD panel were commercialized, such as LCD monitor, notebook, PDA, digital camera, cellular phone, mp3 player, and the state of the art: super large sized TFT-LCD TV of 82 inches fabricated by Samsung in 2005 with its 7th-generation production line.

The major advantages of a-Si:H TFTs are low processing temperature compatible with large-area glass substrate and low leakage current due to the high off-state impedance and consequently the a-Si:H TFTs dominate the AMLCD industry for years. However, the low electron mobility (below 1 cm^2/Vs typically) of a-Si limits the application of a-Si TFTs to switching devices. Besides, the hole mobility of p-channel a-Si TFTs are even poorer (10^{-3} – 0.12 cm^2/Vs) because of dispersive nature of hole transport resulted from large density of states in the valence band tail in a-Si:H [1.8]. For these reasons, the implementation of high-performance CMOS circuits on glass substrates by a-Si:H material is retarded seriously.

In this chapter, the reasons of why we need poly-Si thin-film transistor as well as the future trends of poly-Si technology will be clarified. Then the author would like to give a general paper review about the current status of poly-Si TFTs, including the recrystallization technique, gate-insulator deposition, defect passivation and the other low temperature processes. Finally, the motivation of this work and the thesis organization is described.

1.1 Direction of Low-Temperature Poly-Si (LTPS) TFT Technology

Poly-Si TFTs have been expanding in various applications, such as linear image sensors [1.9], thermal printer heads [1.10], photodetector amplifier [1.11], high-density static random access memories (SRAMs) [1.12], [1.13], nonvolatile memories [1.14], [1.15], solar cells

[1.16], three-dimensional CMOS SOI integrated circuit [1.17], and surely AMLCD industry [1.18]-[1.21]. Actually, the main feature of the low-temperature processed poly-Si technology is the ability of circuit integration on glass, which greatly reduces the connection counts between the glass and the driving ICs. Through the integration of peripheral circuits (shift registers, driving IC, etc.), high definition image display (up to 300 pixel per inch, 300 ppi) with mechanical robustness and lower costs can be fabricated. In contrast, the a-Si based panel, which uses tape automatic bonding (TAB) as connections, the image resolution is limited to around 130 ppi [1.22]. If the carrier mobility of poly-Si TFT can boost to 300 cm^2/Vs, even the digital/analog converter (DAC), graphic controller, CPU and memory can be integrated, contributing to the concept of system on panel (SOP) design. Except improving mobility, however, it should be kept in mind that the design rule of poly-Si TFTs would be scaled down simultaneously to implement SOP, but there still exists several critical problems to be solved about fine alignment on glass substrates, such as large coefficient of thermal expansion and poor surface roughness (±10 μm over a distance of 10 cm [1.23]) of glass. Table I summaries the future trends of flat panel display (FPD) with respect to the characteristics of poly-Si thin-film technology [1.22], [1.24], [1.33].

In this table, one can find that the poly-Si TFTs are supposed to combine with the active matrix organic light-emitting display (AMOLED) in the near future. As a self light-emitting device, OLED panel does not require back-light module and thus is lightweight and durable with high brightness, good contrast, wide viewing angle, fast response time, and low power consumption, making it ideal for portable products [1.25], [1.26]. Furthermore, the OLED can produce three fundamental colors (red, green and blue) and can be grown on flexible substrates inexpensively. More details about organic light-emitting materials can be referred to [1.27].

Table 1-1 Technology road map of low-temperature poly-Si

Generation	Existing Technology	2nd Generation (Display Circuit Integ.)	3rd Generation (Hi-value)
Mobility (cm^2/Vs)	100	150-300	300-500
Design Rule (μm)	4	3-1.5	<1
Clock Freq. (Hz)	5M	10M – 40M	100M
Driving Voltage of Panel	12 V	8 V	3 V
Circuit on Glass	Driver, Shift Register	DAC, Graphic I/F, Small Memory, Low Performance CPU	64Mbit Memory, 32bit CPU
System	w/o TAB	XGA, Full Integrated Display	High Image Quality, System Display
Display	LCD	LCD/OLED	2nd Generation OLED
Fabrication Technologies	ELA, MILC	Lateral growth, Continuous Grain (CG) Si, dry process, Cu low-resistivity bus lines	High purity precursor, low-temperature oxidation, new crystallization method

Unlike AMLCD, by far the least demanding in terms of TFT performance, OLED is a current driven device and consequently the 1-TFT pixel structure operating as a switch in LCDs cannot provide the constant current with constant illumination in the OLED pixel. Besides, in order to compensate the variation in the electrical characteristics of TFTs and the threshold voltage shift after a prolonged operation, more than four TFTs were utilized in an OLED pixel [1.28]-[1.30]. To do so, for conventional a-Si:H technology, we have to scale up the W/L ratio of TFT to provide the needed drive current, thus occupying much more pixel area and not applicable to a full-color driver circuit. In general, the aperture ratio (or fill factor, defined as the ratio of active area of light emitting to the total pixel area) of a single-color OLED display is around 45% [1.31]. In this point of view, poly-Si can offer large electron mobility and is advantageous for the design of driving circuits. Figure 1-1 illustrates the OLED pixel structure of bottom emissive and top emissive, respectively. Most matured

OLED processes belong to bottom emissive type, so the fill factor is a critical issue for the panel design. Contrarily, there are roughness and material reliability issues still to be addresses in vertical integration of top-emissive type pixel [1.32].

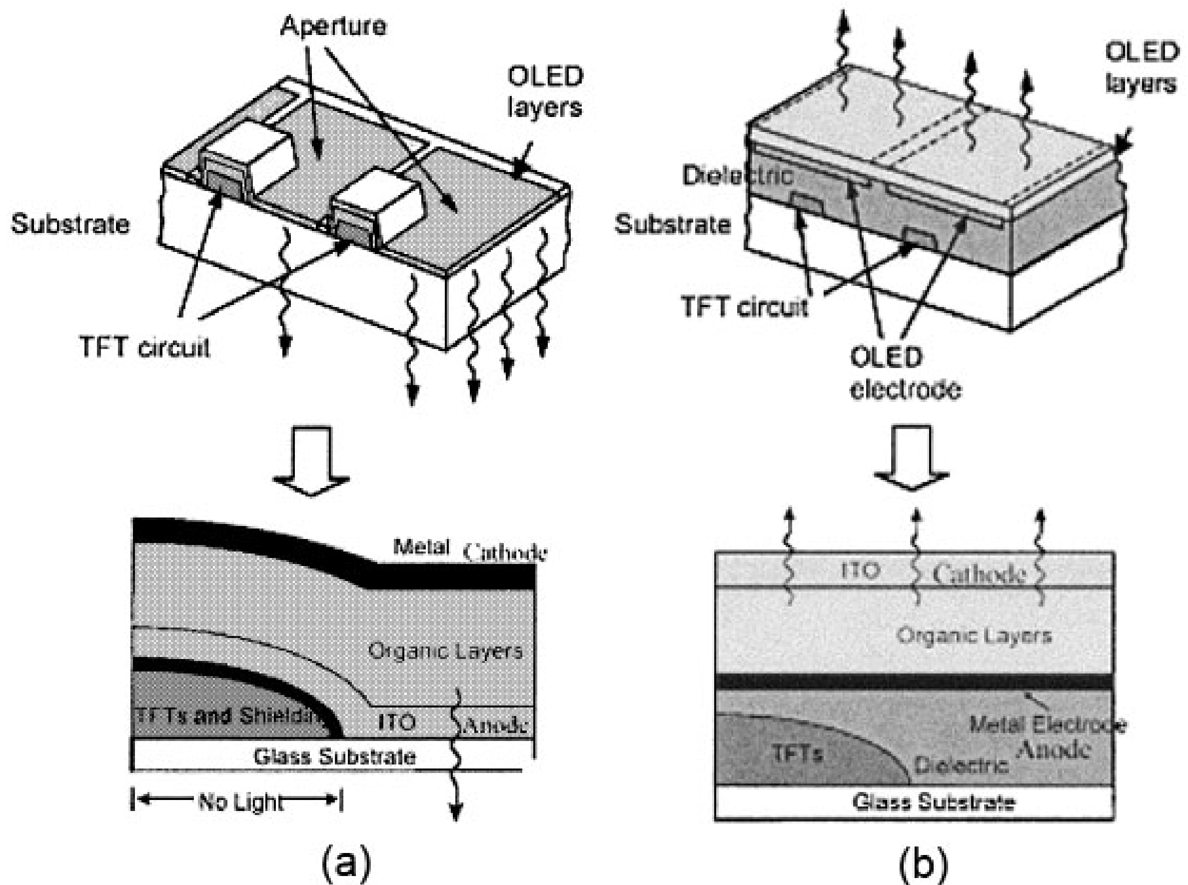


Figure 1-1 (a) Bottom emissive and (b) top emissive OLED pixel structure

For the other applications such as projectors, rear-projection TV or small-sized high resolution displays, poly-Si TFT are more suitable then a-Si:H TFT because the former one provides higher carrier mobility/response time with smaller size of TFT, resulting in a large aspect ratio in every limited pixel area. Additionally, most projective systems utilize high-power lamp placed near the light shutter array, in these cases poly-Si TFTs have better durability against luminance and heat.

1.2 Key Processes in the Fabrication of LTPS TFTs

Compared to the modern CMOS technology on Si substrates, AMLCD/AMOLED industry uses glass as a starting material. Since the glass transition temperature (T_g) is around 640°C for Corning 1733 or 593°C for Corning 7059 [1.34], both of them being specially designed and commonly used in flat panel production, the processing temperature of TFTs must be lower than 600°C. This is not the case for a-Si:H TFT because the steps of thin-film deposition from active layer to gate insulator are performed with PECVD below 350°C while the metallization processes are implemented with sputtering system around room temperature. However, for poly-Si, the recrystallization of amorphous silicon film generally requires quite a high temperature and a long annealing time, so the technique which can form high-quality polycrystalline Si without damaging the glass has become the hottest issue. Moreover, the as-fabricated poly-Si TFT contains lots of defects in the grain boundary or in the interface of poly-Si/gate insulator. Consequently, novel oxidation or passivation methods have been proposed to improve the electrical characteristics of LTPS TFTs. In the following sections, the author will discuss these key fabrication processes of LTPS TFTs.

1.2.1 Solid-Phase Crystallization

A recrystallization method that provides heat to a-Si and causes the grain nucleation and growth in solid phase can be classified into solid-phase crystallization (SPC). Many studies have established that the amorphous phase is an excellent precursor material for forming polycrystalline silicon films. LPCVD a-Si deposited in the temperature range 530-580°C and conventionally furnace annealed in a temperature around 600°C for 20 hours yields crystallized films that are far superior to as-deposited poly-Si [1.35]. Field-effect mobility of poly-Si crystallized by furnace annealing is around 5-30 cm^2/Vs, depending on the dimension of TFTs and the relative number of grain boundaries in the channel region.

In order to reduce the thermal budget and to increase the throughput, several techniques have been proposed, and one of them is rapid thermal annealing (RTA). Since the absorption coefficient of silicon depends on wavelength and its crystallinity, an arc lamp is preferable to irradiate the a-Si; the surface temperature of Si would increase over the strain point of glass (about 700-800°C) in a few seconds while the glass does not absorb the light energy and only be heated by thermal conduction [1.36], [1.37]. Besides, only small portion of substrate is exposed to arc lamp, thus reducing the thermal shock to a minimum. The other composite annealing processes had also been developed such as low-temperature furnace annealing followed by a RTA step for defect reduction [1.38], [1.39].

The reason why conventional SPC requires a long annealing time partly lies in the slow nucleation rate of a-Si. Therefore, foreign atoms including ion-beam/electron-beam [1.40], and oxygen, helium or hydrogen plasma [1.41]-[1.42] were seeded into a-Si before furnace annealing to reduce the nucleation time. Although the mobility of poly-Si TFTs is not significantly improved, the total crystallization time of a-Si reduces by a factor of 5 compared to the untreated film [1.42] while amorphous and polycrystalline Si TFTs can be integrated on one panel by selectively plasma seeding [1.43]. On the other hand, increasing the structural disorder of the precursor, for example, depositing a-Si:H by Si_2H_6 instead of SiH_4, would reduce the nucleation rate and contribute to larger grains. In this manner, it was reported that the minimum nucleation rate is obtained at the substrate temperature of 460°C, and the mobility of TFTs using the recrystallized films reaches 120 cm^2/Vs [1.44]. Finally, Y. W. Choi et al. ever proposed microwave annealing method which can reduce the crystallization time within 2 hours at 550°C. The device parameters of TFTs crystallized by microwave are comparable to those by conventional furnace annealing [1.45].

1.2.2 Metal-Induced Crystallization

It is reported that the crystallization of an a-Si layer occurs at low temperature when the

amorphous film are in contact with one or more of the following metals: Au, Ag, Cu, Al, Zn, Ge, Pd, Ni, Co, etc. [1.46]-[1.55]. According to these reports, a-Si and the metals form a simple eutectic system; the crystallization temperature correlates to the eutectic temperature. Therefore, it is suggested that the melting induced by the lowering of the eutectic temperature occurs at the a-Si/metals interface and followed by the crystallization.

Among these metals, the Ni metal-induced lateral crystallization (Ni-MILC) or so-called silicide-mediated crystallization technology are the most widely studied because Ni-MILC produces large crystalline grains (sometimes over 10 μm) at lower annealing temperature of 450-550°C than conventional SPC and a short annealing time of 5-10 hours depending on the device sizes. The Ni-MILC process is based on the formation of eutectic system of nickel disilicide $NiSi_2$ precipitates and a-Si. The disilicide precipitates are regular octahedra bounded by eight {111} faces, and the lattice mismatch between Si (111) and $NiSi_2$ (111) is only 0.4%, as shown in Fig. 1-2 [1.56].

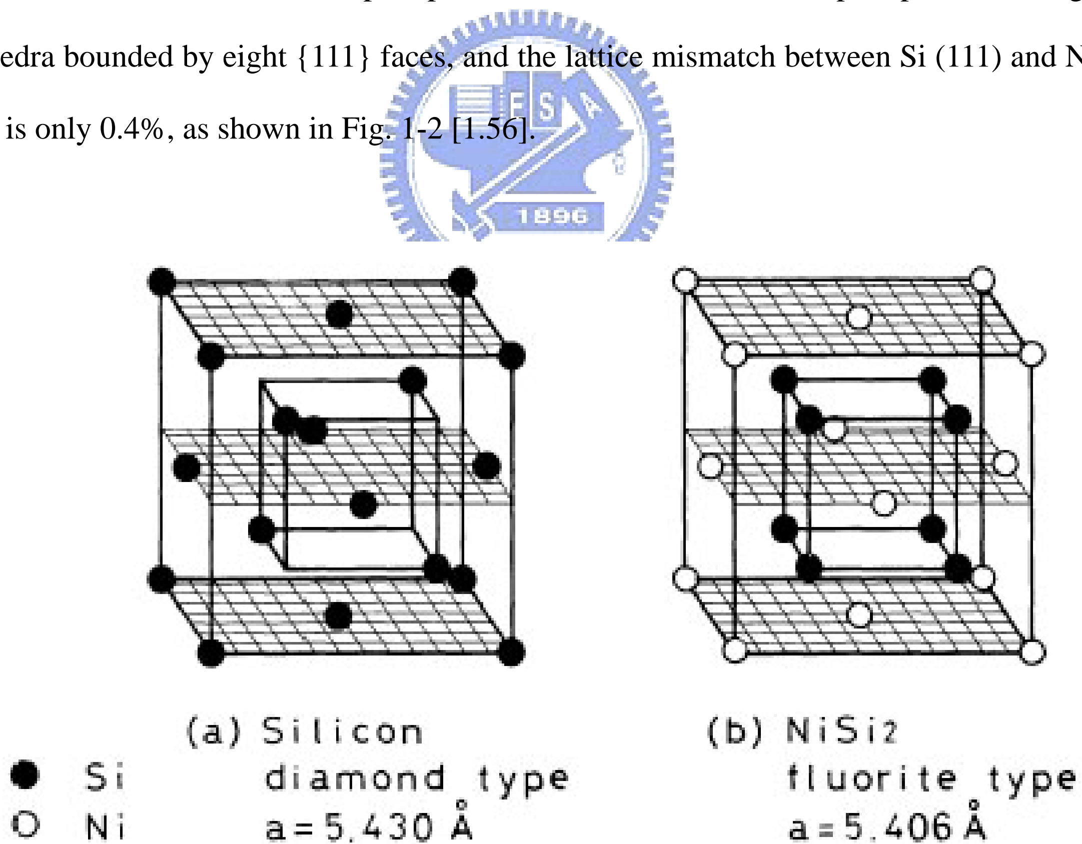


Figure 1-2 The crystalline structure of Si (a) and the $NiSi_2$ phase (b)

Thus it implies that the crystalline-Si (c-Si) induced by the $NiSi_2$ has a high quality. The

driving force for the movement of Ni and Si atoms through $NiSi_2$ precipitates is the free energy difference of them between $NiSi_2$/c-Si and $NiSi_2$/a-Si interfaces. Specifically, the free energy of Si is lower at the $NiSi_2$/c-Si interface and a Ni has lower free energy at the $NiSi_2$/a-Si. Figure 1-3 schematically depicts the mechanism of MILC [1.92]. First, the Ni atoms bond with a-Si atoms to form $NiSi_2$. As the Ni atoms diffuse to the a-Si continuously, Si atoms are dissociated from the rear-edge of growth front and then bond to a more ordered form. Moreover, M. Miyasaka et al. had proposed a delicate experiment of MILC through in-situ TEM observation [1.57]. They found needle-like crystallites scan a large amorphous area, the direction of their growth switching to all possible <111> directions while the crystallites retain the [110] preferred orientation, until the large area is completely crystallized. Besides, only a few $NiSi_2$ precipitates of the exact [110] orientation can contribute to the crystallization of a-Si film. The faster moving rate of growth front of MILC comparing to the spontaneous nucleation rate, together with the small probability of a nickel disilicide precipitate possessing the exact [110] orientation, directly causes the formation of large crystalline grains.

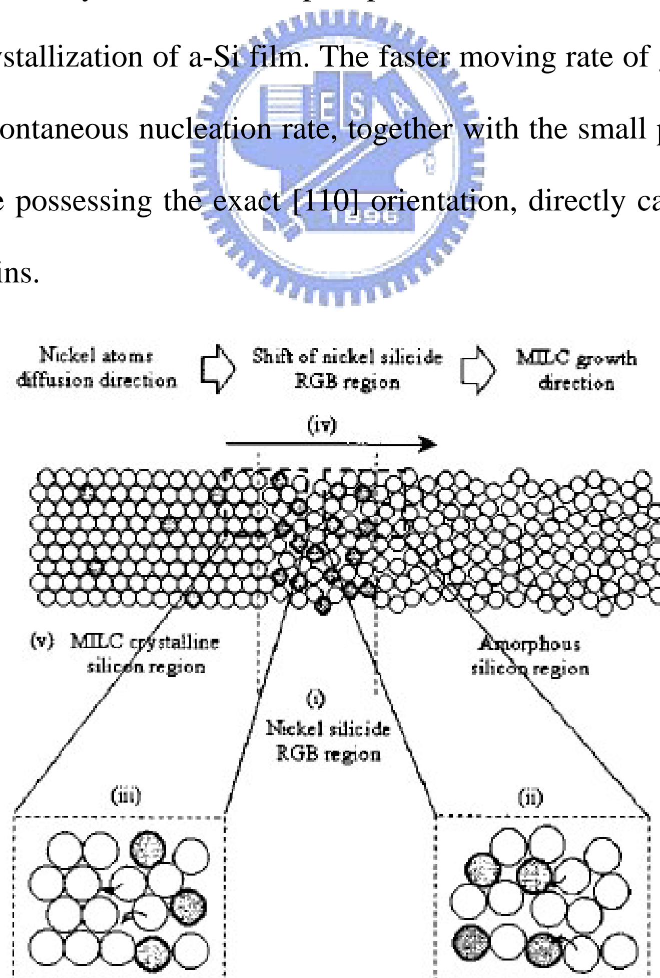


Figure 1-3 MILC mechanism during annealing process

So far, the leakage current in poly-Si TFTs made by MILC are found to be between 4-20 pA/μm at V_{DS} = 5 V and shows a strong V_{DS} dependence. This is too high for display applications, which require a leakage current $I_{leak} < 1$ pA/μm. Generally, it is believed the presence of Ni in the channel region or grain boundaries contribute to the high leakage current, although some researchers supposed that the leakage current originates from the defects of not fully recrystallized a-Si region and is independent on the density of Ni [1.58]-[1.60]. To reduce the anomalous leakage current, a surface treatment by $H_2O/H_2O_2/HF$ mixture was performed after the crystallization [1.61]. Additionally, instead of using sputtering system to deposit Ni film, the other catalysis methods including imprint or electroless plating are proposed to further suppress the Ni incorporation in the active layer [1.62]-[1.64].

Comparing to conventional SPC, Ni-MILC possesses higher crystallization efficiency. However, since thermal diffusion process governs the crystallization velocity, MILC still takes a relatively long time to complete crystallization. In addition, because the rate of crystallization is the same in all directions, defective growth front can end up at the center of the channel region, resulting in the degradation of threshold voltage and sub-threshold swing. Therefore, a technique namely field-enhanced crystallization (FEC) was developed where an electric field is applied to enhance the drift velocity of Ni as well as crystallization velocity [1.65], [1.66]. The crystallization time of a-Si at 500°C decreases form 25 hr to 10 min in the presence of a modest electric field. In general, the electron mobility of poly-Si TFTs fabricated by Ni-MILC/FEC ranges from 50-100 cm^2/Vs.

1.2.3 Excimer Laser Annealing (ELA)

Among all of the current recrystallization methods of a-Si, excimer laser is the most promising solution for future high-performance poly-Si TFTs on glass and thus attracts much attention. Excimer lasers are the most effective and powerful UV light sources available today,

where various gas is filled in a laser resonant chamber and would irradiate strong UV light under a transient high voltage discharge. Depending on the laser gas, different wavelength can be obtained ranging from 157-351 nm, as shown in Table 1-2:

Table 1-2 Different wavelength generated by excimer laser with different gas sources

Laser Gas	XeF	XeCl	KrF	KrCl	ArF	F_2
λ (nm)	351	308	248	222	193	157

Since the a-Si has strong absorption for UV light (absorption coefficient > 10^6 cm^{-1}) [1.37], the energy can be transferred to the Si surface effectively and cause silicon to melt. Nevertheless, the laser pulse duration, typically several tens nanoseconds, is quite short so that the melted Si solidifies in a few hundred nanoseconds, leaving the glass or even plastic substrate undamaged from the heat.

The prime disadvantages of ELA for poly-Si recrystallization lie in the process uniformity and its small process window. Because the beam width of pulsed excimer laser is only a few millimeters or less, a continuous scan with overlapping of laser beam is required to recrystallize a-Si in a large area. Consequently, the accuracy of overlapping and also the deviation of each laser pulse affect the given energy as well as crystalline uniformity after ELA. Moreover, there're three recrystallization mechanisms corresponding to different laser energy: partial melting, complete melting and nearly complete melting (super lateral growth) regimes, as illustrated in Fig. 1-4 [1.67]. Both partial melting and complete melting contribute to small grain size; only a narrow laser energy window can result in nearly complete melting regime where the un-melted islands act as solidification seeds from which a lateral grain growth commences. Besides, laser equipment for mass production is also extremely expensive, since it contains complicate optical system such as lens, mirrors, attenuators and homogenizers, etc.

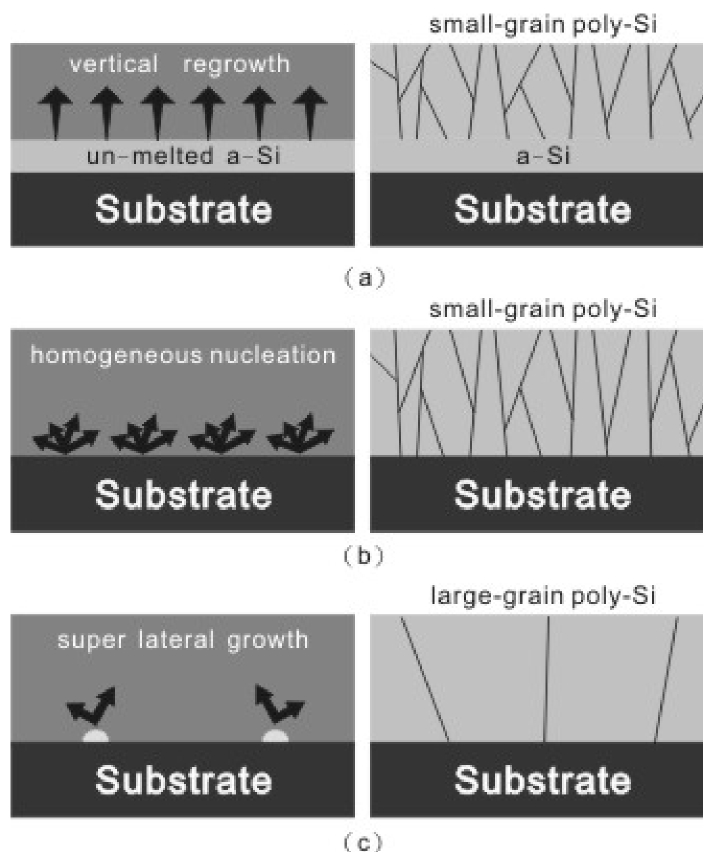


Figure 1-4 Schematic diagrams of recrystallization mechanisms with respect to different energy density of ELA: (a) partial melting, (b) complete melting and (c) nearly complete melting (super lateral growth) regimes

In general, mobility of poly-TFTs fabricated by conventional ELA ranges from 100-300 cm^2/Vs depending on the device size, that is, the number of grain boundaries in the active area. Many researchers have devoted themselves to improve the performance and uniformity of ELA poly-Si TFTs. It is reported that the grain size of poly-Si relates with the heat flow during the solidification process [1.68]. As depicted in Fig. 1-5, if we can create a heat flow parallel to channel, a (super) lateral growth of silicon grain with a size of several micrometers may occur. Based on this concept, versatile techniques have been proposed. For example, one can thicken the source/drain region while keep a thin channel region; the nuclei at the edge of the thicker part (in nearly complete melting regime) grow laterally toward the thinner part, which is still melting [1.68]-[1.70]. A lateral growth can also be obtained by adding a heat reservoir above the channel [1.71], reducing the heat loss in the channel region [1.72], and

modulating the laser energy with light reflector [1.73], phase shift mask [1.74], or multiple laser shots [1.75].

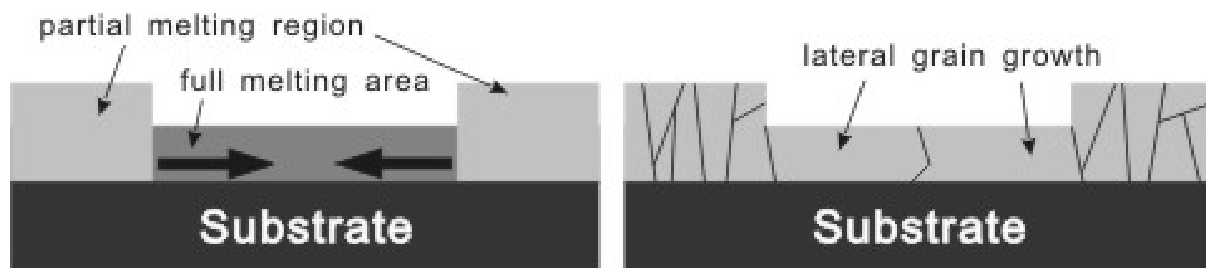


Figure 1-5 Concept of super lateral growth

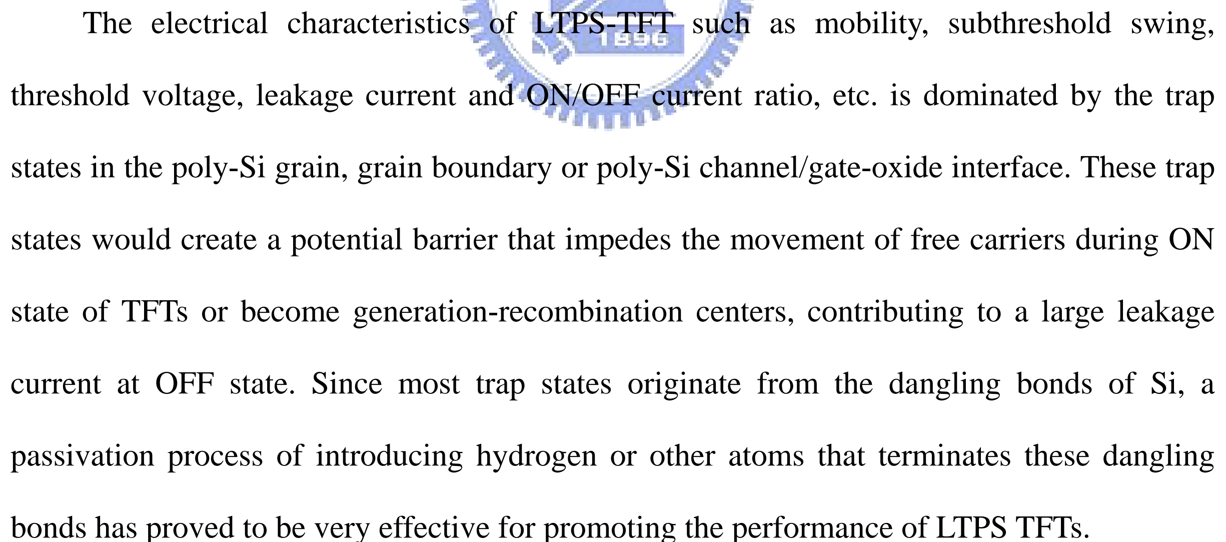
Recently, the mobility enhancement in the LPTS poly-Si TFTs has been established by the continuous-wave (CW) laser lateral crystallization of a-Si film with a stable diode-pumped solid-state laser (DPSS). Field-effect mobilities of 600 cm^2/Vs for n-channel TFTs and 200 cm^2/Vs for p-channel were obtained and the minimum leakage currents per channel width were 3 fA/μm for both n- and p-channel TFTs on 30 cm × 30 cm glass substrates. Moreover, CW-laser crystallization makes it easy to form large grain (~3 × 20 μm^2) with high scan speed (without beam overlapping or multi shots like conventional ELA) and wide energy range; Because of continuous energy supply, directional solidification by laser scanning and slow cooling rate of molten Si can be achieved [1.76], [1.77]. Except CW laser, hybrid crystallization methods have also been developed, such as SPC + ELA or MILC + ELA, etc [1.78]-[1.80]. For these processes, the conventional furnace annealing can produce uniform Si grain followed by ELA to fix the intra-grain defects. Additionally, ELA is widely utilized to activate the dopants for LTPS-TFTs.

1.2.4 Deposition of Gate Dielectric Thin Films

A high-quality gate dielectric film with high breakdown electric field, low leakage, good uniformity, and low interface trap states or fix oxide charge density is inevitable for the

fabrication of LTPS TFTs. Limited by the low T_g of glass substrates, conventional dry oxidation with furnace is not applicable, and thus SiO_2 deposited by PECVD system becomes a good candidate. Among various plasma deposition methods, inductively coupled plasma (ICP) and electron cyclotron resonance (ECR) oxidation are very attractive due to their remote plasma source resulting in smaller plasma damage during oxidation process. ICP/ECR also possesses high radical concentrations (i.e., fast depositing rate), low plasma sheath voltage and the capability of good uniformity over large area [1.81], [1.82]. To further eliminate the interface states, post annealing with H_2O vapor or in N_2 ambient is conducted [1.82]. In addition to plasma enhanced deposition, sputtering technique, especially the one that combines with high-k materials such as Al_2O_3, Ta_2O_5 or HfO_2 etc., is beneficial for the reduction of both process temperature and the circuit operation voltage [1.83].

1.2.5 Defect Passivation



The electrical characteristics of LTPS-TFT such as mobility, subthreshold swing, threshold voltage, leakage current and ON/OFF current ratio, etc. is dominated by the trap states in the poly-Si grain, grain boundary or poly-Si channel/gate-oxide interface. These trap states would create a potential barrier that impedes the movement of free carriers during ON state of TFTs or become generation-recombination centers, contributing to a large leakage current at OFF state. Since most trap states originate from the dangling bonds of Si, a passivation process of introducing hydrogen or other atoms that terminates these dangling bonds has proved to be very effective for promoting the performance of LTPS TFTs.

A variety of methods has been employed to perform this passivation, including the deposition of plasma Si_xN_y:H films [1.84], immersion in hydrogen plasma [1.85], [1.87] and implantation of hydrogen [1.86]. For poly-Si TFTs, the conventional passivation process is usually carried out after all of the high-temperature processes because the weak Si-H bonds are easily broken as temperature exceeding 350^oC. Besides, it is well known that the

hydrogen passivation would cause the instability of electrical properties of TFTs after stress measurements. Other elements instead of hydrogen are hence introduced, such as oxygen, deuterium, ammonia and nitrous oxide (N_2O) [1.88]-[1.90]. For top-gate structure commonly used in LTPS TFTs, ions for passivation should diffuse a long distance through interlayer dielectric and gate oxide to reach the active area beneath the poly-Si gate, requiring a prolonged annealing time over 1 hour and decreasing the throughput. C. H. Kim et al. ever proposed an in-situ fluorine passivation technique which can passivate traps, recrystallize a-Si and activate dopants at the same time by utilizing fluoric SiO_2, PSG as well as excimer laser annealing [1.91].

1.3 Motivation

In contrast to relatively matured CMOS technology, process development of low-temperature poly-Si TFTs just started for the last several decades. Since the usage of glass substrates with limited glass transition temperature, including active layer deposition, gate oxidation, activation and passivation steps are forced to perform in an alternative way with a lower process temperature. The overall performance of poly-Si TFTs is thus inferior to that of MOSFETs on Si wafer. Moreover, there is great interest in the use of plastic substrates for making flat panel displays, light sensors and other electronic products in the near future. Some of the reasons include reduced fragility of the substrate, lighter weight, and greater design freedom by use of non-rectangular and non-planar displays. However, the melting temperature of plastics (~200°C) is even lower than that of glass while the physical and chemical properties of polymeric substrates are also totally different; the LTPS technology as we reviewed in *Section 1.2* may not apply to them thoroughly. To overcome these obstacles, we proposed a device transfer technique that the device was fabricated on silicon wafer first and then adhered to the other substrate, thus getting rid of many constrains from the substrate.

Since the starting material is Si wafer, matured high-temperature CMOS process can be utilized.

As we summarized in Table 1-1 that one of main attractions of LTPS-TFTs is a possibility for integrating peripheral circuits on the same panel. Consequently, the stability of device characteristics after a long-term operation is indispensable for circuit applications. These reliability issues arise from either weak Si-Si/Si-H bonds in the channel region or the hot carriers induced by the intense drain electric field. We demonstrated an elevated channel with gate-overlapped LDD structure to address the reliability problems while gain some other benefits including high mobility, suppressed kink phenomenon, low leakage current and reduced contact resistances through the proposed architecture.

Inorganic semiconductors such as silicon, germanium and gallium arsenide have been used for centuries. However, because the electronic devices based on these materials generally undergo complicate processing steps by expensive production facilities, the cost for fabricating these inorganic semiconductor devices cannot be further decreased. Recently, it was found that many organic polymer or oligomers has similar semiconductive electrical characteristics to their inorganic counterparts, so that these organic materials are emerging as potential competitors to amorphous and polycrystalline Si in the application of large area electronics. Most organic semiconductor materials can be easily deposited by spin coating or by vacuum sputtering system at room temperature with extremely low costs. Such unique processing characteristics suggest that they can be quite suitable for novel thin-film transistor applications or disposable electronics on glass, plastic and even paper substrates requiring large area coverage, structural flexibility and low temperature processing. Integration of organic TFTs with AMOLED is another blue chip that a dream of truly roll-up display (without back-light module) can be finally fulfilled with all-organic materials. To do so, more understanding about the electrical properties and reliability behaviors of organic devices is necessary.

1.4 Thesis Organization

In this thesis, we made efforts toward developing proper processing methods to fabricate thin-film transistor on glass and plastic substrates. In chapter 2, we proposed a novel device transfer technique which could transfer thin-film devices from a Si wafer to glass/polymeric backplanes. We would first review the current status about the issues and how to fabricate TFTs on plastics, which can be classified into direct and indirect (transfer) manners. A device transfer by backside etching (DTBE) technique for manufacturing poly-Si TFTs on *rigid* substrates through chemical-mechanical polishing (CMP) and wet etching were then demonstrated in this chapter.

Next, in chapter 3, all kinds of Si backside etching techniques were investigated including wet chemical etching by KOH, HNO_3/HF, and especially, the spin etching. Instead of using CMP, a modified DTBE with conventional wet etching or spin etching processes were proposed. Then the devices that had been successfully transferred to glass or *flexible* plastic substrates would be measured to study the change of I-V characteristics after transfer or under bending tests.

In chapter 4, we focused on the reliability issues of poly-Si TFTs resulted from the high drain electric field. Benefits and drawbacks of several architectures which could alleviate lateral electric field of drain junctions would be discussed. Thereafter, we developed an elevated channel with gate-overlapped TFT structure, which has a thin channel and a thicken source/drain region. Room-temperature selective liquid-phase deposited (S-LPD) SiO_2 technique was utilized to planarize the trench under the thin channel, while ELA was performed to recrystallize the active area. SEM observations, I-V characteristics and reliability tests were conducted to evaluate the potential advantages of the proposed TFT architecture.

In chapter 5, a similar elevated-channel TFT structure as described in chapter 4 was

fabricated, but the recrystallization method was MILC instead of ELA. Here, we changed the thickness of active area ranging from 15 nm to 100 nm, and also varied the impurity concentration of the lightly-doped regions. Detailed electrical characteristics were examined to figure out the effects of active layer thickness and LDD dosages.

In chapter 6, the attention was diverted from poly-Si materials and focused on organic semiconductors. At the beginning, the author would like to introduce the background information about organic thin-film transistors (OTFTs). Next, we chose one of the most commonly used organic material, i.e. poly-3-hexylthiophene (P3HT), and performed a series experiments to optimize the spin-coating parameters of P3HT. A new configuration of OTFT with field isolation utilizing wet oxidation or S-LPD was then proposed to eliminate the anomalous leakage current through gate oxide and conductive P3HT films. Besides, since the performance of OTFT highly depends on the hole-injection efficiency at the interface between P3HT and S/D electrodes, several S/D metals of different work function were tested.

Finally, in chapter 7, we examined the reliability characteristics of OTFTs under electrical and environmental stress, including hot carrier, constant current (self-heating) stress and the degradation of transfer curves when the OTFTs were exposed to vacuum, N_2, O_2 and humid atmosphere.

In chapter 8, conclusions and recommendation for future works were given.