

Chapter 2

Device Transfer Technology for Fabricating TFTs on the Plastic Substrate

Flat panel displays on flexible substrates are of considerable interest because of several advantages for using plastics or stainless steel instead of glass. Plastic substrates for the cells of LCDs exhibit only 1/6 of the weight of glass substrates. They are virtually unbreakable and their flexibility allows the designer to do elegant styling, to bend it so as to suppress reflections or for placing it on a curved surface. Possible applications of AMLCD on plastics include mobile electronics, “smart” labels on consumer items (radio frequency identification tags), smart cards and disposable sensors. Recently, the blooming researches about organic light emitting diode (OLED) also increases the demand for displays on the thin flexible substrates because the usage of self emitting devices let us abandon thick and heavy back-light module; the OLED panel is thus thinner and consuming less power.

For flexible display using either conventional liquid crystal or novel OLED, an active LTPS TFT array as switching/driving element is inevitable. However, fabricating thin-film device on polymeric substrates would face several critical problems very different from that on glass. In the following sections, we will discuss these issues and the related particular processes.

2.1 Critical Issues for Fabrication TFTs on Plastic Substrates

2.1.1 TFT Process at Extremely Low Temperature < 200°C

Typically, the deposition temperature of CVD films in fabricating TFT array on a glass substrate is 300°C or more. However, T_g of a general plastic substrate is about 100 ~ 200°C.

For conventional PECVD system, if the deposition temperature of a-Si is reduced to this range, the deposition rate would be too low to keep the throughput. Besides, large amount of hydrogen atoms as high as 20 – 30 atomic % (because they cannot diffuse out at lower temperature during a-Si deposition) in the a-Si film could burst out and cause ablation of the active layer during the following ELA process. Moreover, the active layer and gate dielectrics deposited at low temperature contain a lot of trap states or fix oxide charges so that the mobility as well as the other electrical properties could be relatively poor.

2.1.2 Mask Alignment

A conventional plastic substrate has high thermal expansion coefficient about one order of magnitude larger than silicon and glass. This feature makes mask alignment and thin-film patterning very difficult layer by layer during the pre-baking and post baking processes of photo lithography. In addition, the difference between expansion and contraction of the conventional plastic substrate due to water absorption becomes more than 3000 ppm. Figure 2-1 depicts variations of substrate length during the actual TFT process [2.1]. By controlling the temperature and humidity of the TFT process, the maximum allowance of the mask alignment can decrease to 1000 ppm. However, a conventional TFT array structure requires alignment allowance within ± 15 ppm. Thus, mask alignment in each layer is one of the most serious problems to fabricate precise TFT structure on the plastic substrate.

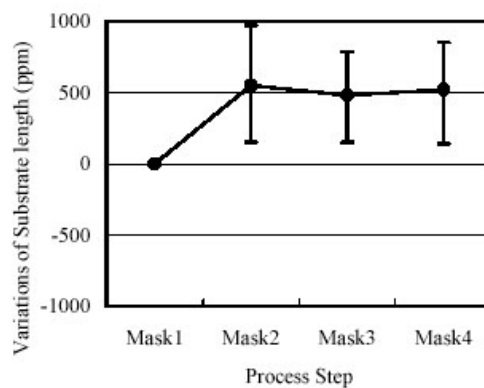


Figure 2-1 Variation of length of a conventional plastic substrate versus process steps

2.1.3 Thermal-Mechanical Problems with Plastics

If the thermal expansion coefficient α_s of a substrate differs from the thermal expansion α_l of a layer on that substrate, then the overall tension σ_{tot} in the layer, including its intrinsic tension σ_i at room temperature T_R , changes for a process temperature T_P to [2.2]:

$$\sigma_{tot} = \sigma_i + (\alpha_l - \alpha_s)(T_P - T_R)E_l/(1 - \nu_l) \quad (2.1)$$

where E_l stands for the modulus of elasticity and ν_l for the Poisson ratio of the layer. As a rule, we have $\alpha_l < \alpha_s$ and $T_R < T_P$, resulting in a decrease in σ_{tot} , indicating an additional compressive stress. This stress may lead to crack or delamination in the layer and also results in a curvature of the substrate with the radius R :

$$R = \frac{E_s d_s^2}{6d_l \sigma_{tot} (1 - \nu_s)} \quad (2.2)$$

valid for $E_s d_s$ much larger than $E_l d_l$.

In Equation (2.2), E_s is the modulus of elasticity, d_s the thickness and ν_s the Poisson ratio of the substrate, d_l the thickness of the layer, and σ_{tot} is taken from Eq. (2.1). For Si wafer, $E_s d_s \gg E_l d_l$, the radius is so large that the substrate remains planar. However, for flexible plastic substrate with thickness of only 100 – 200 μm and with a relatively low Young's modulus, serious bending of the substrate may occur after multiple thin-film deposition such as SiN_x and a-Si:H by PECVD in the process temperature of 200°C. General manufacturing equipments cannot handle the wrapped substrate, much less fabricating the TFT array.

2.2 Direct Approach: Fabricating TFTs on Plastics with Ultra Low-Temperature Process

2.2.1 Plastic Substrates and Their Properties

Direct fabricating TFTs on plastic substrate like the way we familiar with on Si or glass

suffers lots of problems, some of which had been discussed in *Section 2.1*. These problems mostly arise from the unique physical and chemical properties of plastics. Polymeric materials applicable for displays are polycarbonate (PC), polyarylate (PAR), polyimide (PI), polyethyleneterephthalate (PET), polyestersulfone (PES), and polyolefin, etc. Table 2-1 lists general requirements of plastic substrate for LCDs [2.3]:

Table 2-1 General requirements of plastic substrates for LCDs

Temperature stability	As high as possible
Thermal expansion coefficient	≤ 50 ppm/K
Irreversible shrinking	$< 1/20$ of pixel pitch
Surface roughness	≤ 10 nm
Transparency	$\geq 90\%$
Permeation of H ₂ O	< 0.15 g/m ² 24 hr at 40°C and 90% relative humidity
Permeation of O ₂	< 0.1 cm ³ /m ² 24 hr
Chemical resistance	etchants, solvents and other chemicals used in display manufacture

and table 2-2 summaries substrate properties of c-Si, glass, stainless steel, and six organic polymeric backplanes specially synthesized for display fabrication [2.4].

From these tables, one can find that the major differences between plastics and rigid silicon or glass substrates are the Young's modulus, melting/glass-transition temperature, thermal expansion coefficient and thermal conductivity; some plastics even have native color. Since the strain is inversely proportional to the Young's modulus of the substrate, deformation for these flexible plastic materials could be easily observed and requires delicate post treatments.

Table 2-2 Substrate properties of c-Si, glass, stainless steel, and six organic polymeric backplanes

Material () Primary lit. references, see footnotes	Brand or trade name	Density g cm ⁻³	Appearance and range of optical transparency μm	Refr. index n at 0.55 μm	Dielectric constant ε at 0.1-1 MHz	Young modul. Y GPa	T _{mett.} , T _{strain} , or T _{glass} °C	Coeff. thermal exp. α at 20°C 10 ⁻⁶ K ⁻¹	Thermal cond. κ Wm ⁻¹ K ⁻¹
Cryst. Silicon (1,2)		2.33	Opaque	3.4	11.8	190	1415 T _m	2.4	165
Borosilicate glass (3-6)	Corning 7059	2.76	Clear 0.30 ->2.5	1.53	5.9	68	613 T _s	4.7	
	Schott AF 45	2.72	0.25 ->2.5	1.53	6.2	66	662 T _g	4.5	
Stainless steel (7)	AISI 304	7.93	Opaque			190	1400 T _m	18	16
Poly perfluoro-cyclobutane aromatic ether (8)	DowXU-35033.00		Milky white <0.4 ->0.6	1.50	2.45	2.3	400 T _g	90	
Polyimide (7,9,10)	DuPont Kapton E	1.46	Amber		3.4, 50% RH	5.2	≥350 T _g	12 ≤200 °C	.1-.35
Polyether-sulfone (7,11)	Victrex Ultrason	1.37	Slightly yellow	1.65	3.7	2.4	200 T _g	55	.13-.18
Polyarylate (12)	Kaneka F-1100	1.20	Clear	1.60	2.7	≥2 (est.)	215 T _g	51	
Polycarbonate (7,10)	Lexan	1.2	Clear	1.585	2.9	2.3	160 T _g	70	.2
							220 T _m		
Polyethylene terephthalate (7,10)	PET	1.29-1.4	Clear	1.58-1.64	3.0	2 - 4	80 T _g	30 - 65	.14-.4
							267 T _m		

(1) Bell Labs Quick Reference Manual, May 1975. (2) AIP Handbook, McGraw Hill 1972. (3) Corning Product Information PI-0211-87. (4) N.P. Bansal and R.H. Doremus, Handbook of Glass Properties, Academic Press 1986. (5) Schott/DESAG spec sheet on AF 45 and D 263. (6) D.M. Moffatt, Mat. Res. Soc. Symp. Proc. vol 377 (1995) p.871. (7) Goodfellow Catalog 1996/97. (8) D. Perettie, L. Bratton, J. Bremmer, and D. Babb, Liquid Crystal Materials, Devices, and Applications II, SPIE vol.1911 (1993) p.15. (9) J.A. Kreuz, S.N. Milligan, and R.F. Sutton, DuPont Films Technical Paper 3/94, Reorder No. H-54504. (10) W.M. Alvino, Plastics for Electronics, Mc-GrawHill, New York 1995. (11) S.M. Gates, Mat. Res. Symp. Proc. 467 (1997) p.843. (12) Kaneka spec sheet.



2.2.2 Barrier Layers and Thermal Pre-treatment for Plastic Substrates

Most plastic materials are poor barrier for O₂ and H₂O. Typically, plastic materials have a water vapor permeation rate of 0.1 ~ 10 g/m² per day at 25°C. The incorporation of oxygen or water could seriously degrade (oxidize) the cathode/OLED interface and even a whole OLED/LCD pixel region [2.5], while the plastic substrate would expand significantly and cause a misalignment in photo-lithography after it absorb water.

Deposition of thick SiN_x, SiO₂ and Al₂O₃ films by sputtering on plastic substrates have proved to be effective as a water/oxygen barrier [2.1], [2.6], [2.7]. A hybrid substrate that combines ultra-thin glass with polymer coating is also proposed to overcome the fragility of thin glass while maintain several benefits such as low water/oxygen permeation, good thermal stability and flexibility [2.8]. Besides, if barrier layers are deposited at the both side of the plastic substrate with a suitable thickness, it can compensate compressive stresses generated in the multilayer structure during the stack deposition. Nevertheless, pin holes are

commonly observed for $\text{SiO}_2/\text{SiN}_x$ formed by sputtering system, and the deposition of both sides requires double processing time. Accordingly, instead of using sputter, we utilized room-temperature liquid-phase deposition (LPD) technology to form SiO_2 at both sides of plastic backplanes simultaneously. For non-polar plastics, surface oxidizing treatment by UV ozone or ozone water was carried out before primary coating. Although UV ozone treatment may degrade the plastic material seriously, ozone water (@40 ppm, 25°C for 30 min) is quite suitable for surface treatment of plastics. Figure 2-2 depicts the LPD- SiO_2 thickness versus deposition time on Si wafer and the plastic substrate, respectively. The deposition rate on plastics is very uniform and we found no difference with the case on Si substrates. More details about LPD technology will be discussed in *Section 4.3.1*.

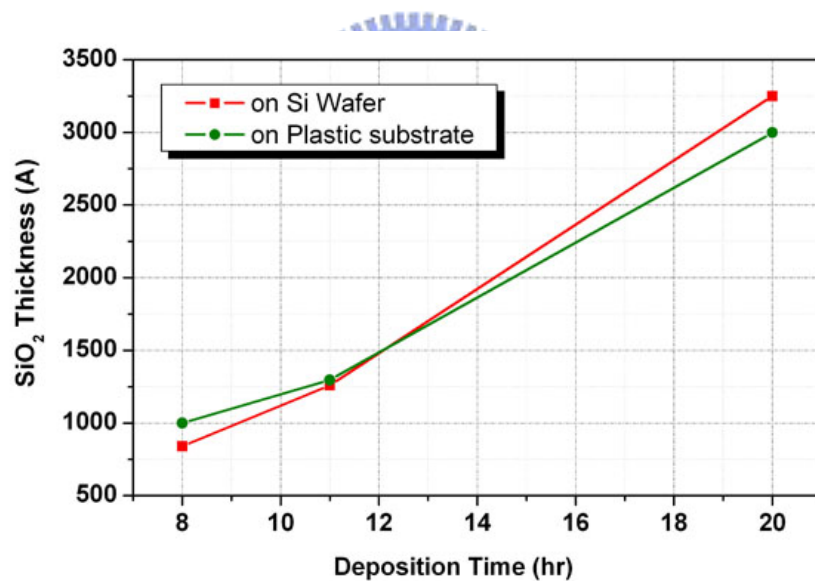


Figure 2-2 LPD- SiO_2 thickness versus deposition time on the Si wafer and the plastic substrate

Except barrier layers, it has been shown that plastic can be stabilized by reducing the heat shrinkage – irreversible dimensional change due to molecular rearrangements and free volume reduction – by an appropriate thermal pre-treatment. When such a pre-treatment is performed, subsequent treatments at lower temperature or for a shorter time cause only small

dimensional changes, ensuring much better accuracy of photomask alignment.

2.2.3 Technology for Thin-Film Deposition, Crystallization and Dopant Activation at Ultra Low Temperature

As described in *Section 2.1.1* that excess hydrogen in the a-Si:H formed at low temperature would effuse out abruptly and damage the film during ELA. Sputtering is a good candidate to replace conventional PECVD to deposit a-Si or SiO₂ [2.9]-[2.11]. Although sputtered a-Si film still contains very low H₂, Ar, or He (<1%) contents, they are easy to effuse out of Si by the leading edge of the laser beam, and thus no further dehydrogenation process is necessary.

On plastic substrates, excimer laser annealing is the only way to recrystallize and activate the dopant atoms. Due to the low thermal conductivity of polymeric material, the poly-Si grains are sometimes larger than those on glass, contributing to carrier mobility of poly-Si TFTs as high as 250 cm²/Vs [2.9], [2.10]. To form source/drain regions, plasma doping or laser doping in an ambience of PH₃ or B₂H₆ is usually utilized [2.12]. Besides, at 285°C or lower, high density plasma such as ECR plasma source can be employed to deposit all of thin film materials needed for the transistor, that is, intrinsic micro-crystalline Si, n-type source/drain and gate dielectric. Field effect mobility of 12 cm²/Vs and ON/OFF ratio of 10⁶ can be achieved [2.13]. On the other hand, fabricating a-Si:H TFT arrays rather than poly-Si TFTs on plastics should be much easier. Optimized thin-film deposition processes by PECVD at 180°C or less have been demonstrated [2.14], [2.15].

2.3 Indirect Approach: Fabricating TFTs on Plastics by Transfer/Substrate Bonding

Since fabricating TFTs in a direct manner is seriously hindered by several unique

physical and chemical properties of plastics, many researchers have manipulated alternative ways that fabricate devices first on a guest substrate and then transfer to the host backplane. These indirect manners can be divided into three types depending on the guest material and the transfer method.

2.3.1 Surface Free Technology by Laser Ablation (SUFTLA)

SUFTLA is so far the most well developed device transfer technique proposed by Seiko Epson Corporation [2.16], [2.17]. The process steps of SUFTLA can refer to Fig. 2-3. First, an a-Si:H film is deposited as the “exfoliation layer” by PECVD on the glass or quartz substrate (guest substrate). After that, a buffer oxide is deposited by ECR-CVD at 100°C. Then the top gate TFT device was prepared on the buffer oxide in a conventional LTPS process (with maximum process temperature < 425°C). In the first transfer process, the original substrate was glued onto a glass substrate (temporal substrate) by using a water-soluble adhesive that stiffened under UV light. An XeCl excimer laser is then used to irradiate the back side of the original substrate, causing the exfoliation layer to melt and release hydrogen. This phenomenon reduces the adhesion between the exfoliation layer and the guest substrate, allowing the TFT arrays to detach. In the second transfer process, the TFT arrays adhered to the temporal substrate was glued onto a PES substrate (host substrate) by using non-water soluble adhesives, and then the temporal substrate was removed to complete the whole SUFTLA process.

SUFTLA technique delicately uses the characteristics of hydrogen-rich a-Si layer that exfoliate under an abrupt annealing process. However, even if it utilizes quartz as a guest substrate, SUFTLA technique still requires low temperature process because a high temperature annealing during array fabrication could anneal out the hydrogen atoms slowly and therefore the exfoliation layer becomes ineffective. The usage of excimer laser also increases the production costs. The carrier mobility of TFTs fabricated by SUFTLA is around

124 cm²/Vs.

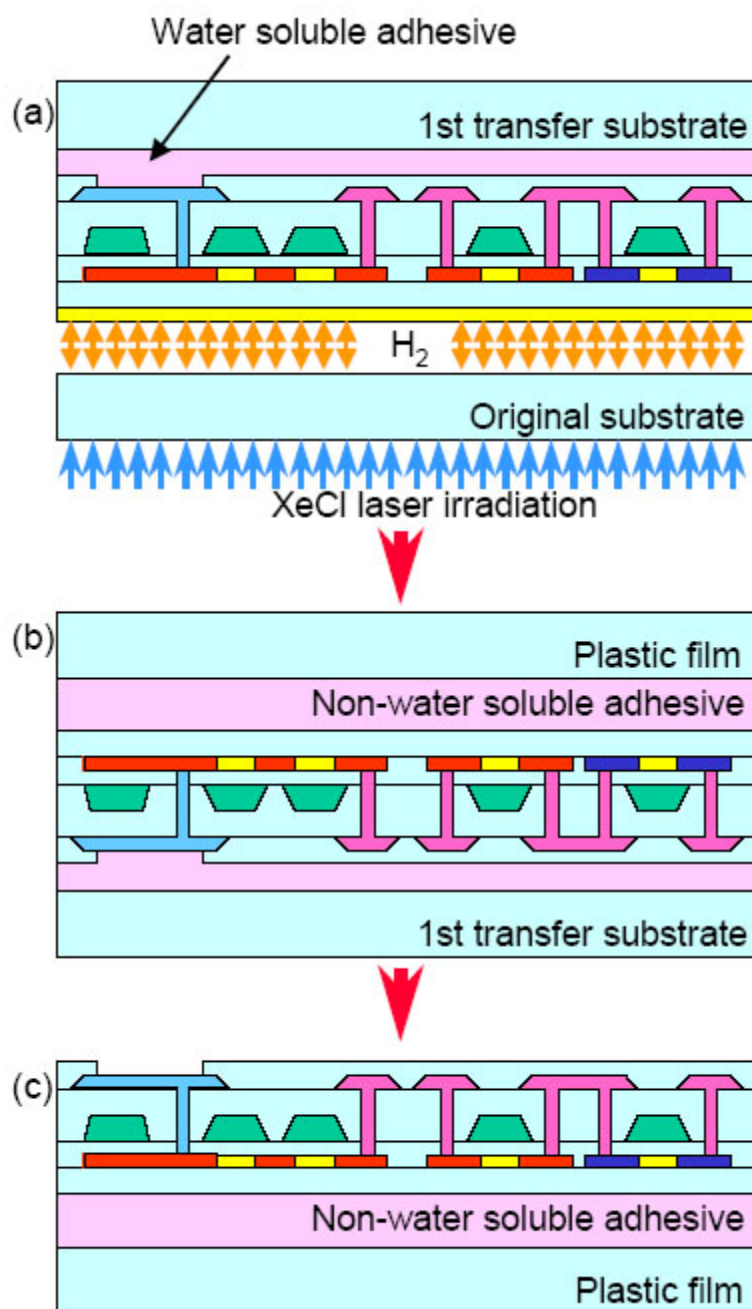


Figure 2-3 Process sequence of SUFTLA: The TFTs and TFT devices are peeled from the original substrate and transferred onto plastic film by XeCl excimer laser irradiation

2.3.2 Device Transfer by Wet Chemical Etching

Instead of using laser ablation, the device can also be transferred through a sacrificial

layer. Figure 2-4 shows a schematic flow of the transfer process proposed by Sony Corporation [2.18]. First, an etching stop layer such as SiN_x was deposited on a glass substrate (guest and sacrificial substrate) by PECVD. TFT arrays were then fabricated on this sacrificial layer with conventional LTPS processes. Next, the TFT arrays were glued to a temporal substrate with a removable, non-water soluble adhesive. The glass substrate was etched away by hydrofluoric acid at room temperature. After sticking a plastic substrate (host substrate) onto the back surface of TFT arrays with a permanent adhesive, the temporal substrate was removed to complete the whole transfer process.

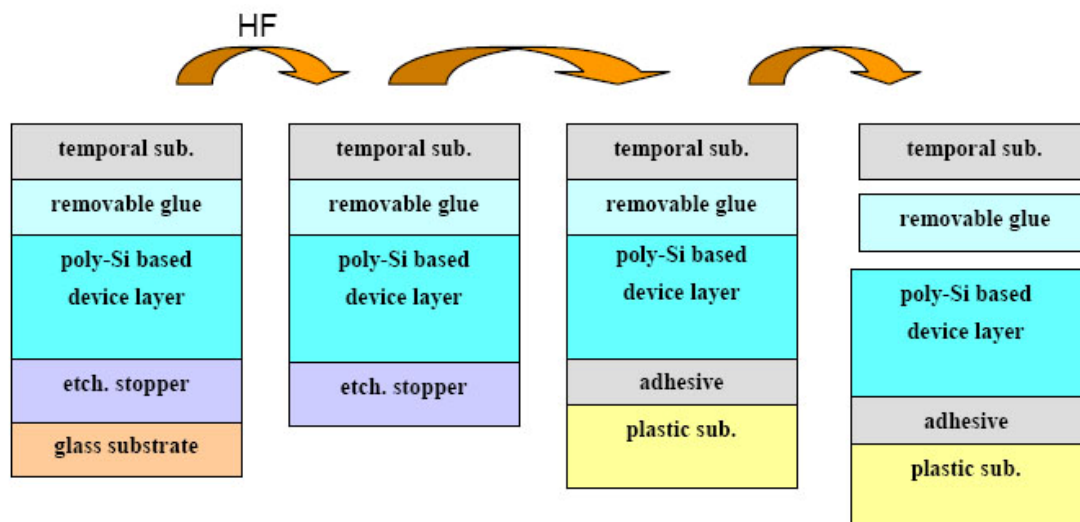


Figure 2-4 A schematic flow of the transfer process to manipulate the thin film device layer from a glass substrate onto a plastic substrate

Again, this process proposed by Sony corp. utilizes glass substrate with LTPS TFT process. Although its process temperature still limited by the T_g of glass, such process is quite compatible with current LTPS production line. The actual transfer size is over 300 mm × 350 mm, the largest panel on plastics ever published. In addition to Sony corp., Y. Lee et al. proposed another device transfer method utilizing Si wafer as a guest substrate [2.19]. The poly-Si TFTs were fabricated on a sacrificial layer of silicon dioxide as shown in Fig. 2-5.

After encapsulating TFTs by benzocyclobutene (BCB), the sacrificial SiO₂ were etched away by KOH solution which reached the bottom of TFTs through pre-patterned via holes. The primary drawback of this technique is the separation time directly proportional to the device size and the density of via holes if the etching rate of KOH unchanged. Under an etching rate of 1 μm/min by KOH at 70°C, separation of a device of 200 μm × 200 μm takes an hour.

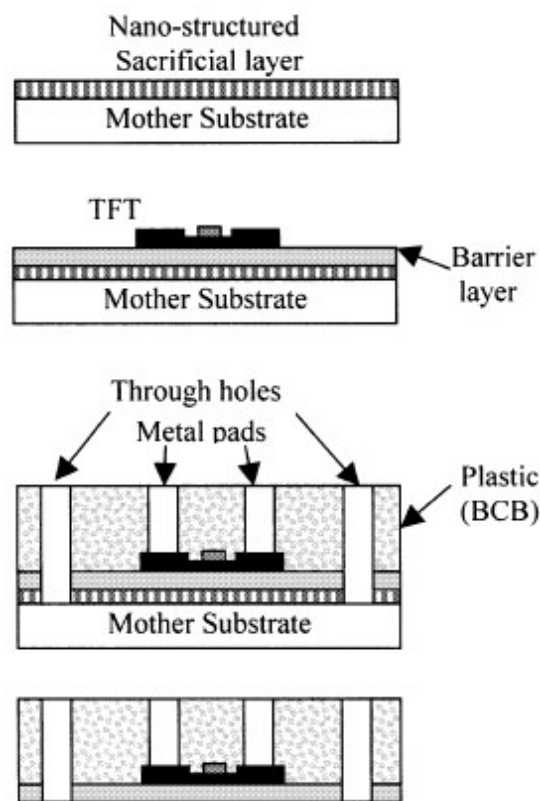


Figure 2-5 Schematic process flow of the separation technique for high performance poly-Si TFTs on plastic

2.3.3 Transfer of Single Crystalline Silicon

It sounds attractive if one can transfer semiconductor devices composed of c-Si. It certainly does because c-Si possesses low defect density and satisfactory carrier mobility. For example, X. Shi et al. had developed an “ion cutting” technique to transfer a layer of single crystal Si to glass [2.20]. Specifically, hydrogen atoms with dosage of $2.5 \times 10^{16} \text{ cm}^{-2}$ at 50 keV were implanted into a (100)-oriented silicon wafer. This wafer was then bonded to

another glass substrate and underwent an annealing process at 450°C for 1 hr in air. The thickness of the transferred film was 450-500 nm with a non-uniformity of 3 nm. Chemical-mechanical polishing (CMP) was used for film thinning and surface polishing. The as-transferred thin films were n-type due to hydrogen-related defects but it can be recovered to p-type conductivity after an extended heat-treatment for 8 hrs in nitrogen at 630°C, close to the highest temperature to which the glass substrates could be exposed. Recently, the strained Si layer was also transferred successfully by the ion cutting method to the glass substrate, contributing to the mobility of n-channel TFTs as high as 820 cm²/Vs [2.35].

Actually, the concept of “ion cutting” is the widely utilized technology that fabricates silicon-on-insulator (SOI) wafers [2.21], [2.22], but in the former example the host wafer was replaced by glass substrate. For ion cutting method, although a high electron field-effect mobility of 427 cm²/Vs can be achieved, the bonding process at moderate temperature and the prolonged annealing process for defect reduction hinder its application to plastic substrates. Additionally, the CMP step for thinning the as-transferred c-Si film is probably not applicable to fragile glass substrates.

Except wafer bonding, the c-Si can also be transferred from an SOI wafer [2.23], [2.24]. However, these methods utilize expensive SOI wafer and the time required for separating the c-Si layer from the SOI wafer still depends on the etching rate of SiO₂ etcher and the device size to be transferred.

In the area of micro-electro-mechanical system (MEMs) and optoelectronics, a technique called fluidic self assembly (FSA) has been studied for years [2.25]-[2.27]. This technique originates from an idea of system integration for transferring optoelectronic devices composed by III-V semiconductors to ICs by modern CMOS process. As can be seen from Fig. 2-6, slurry containing mini components was pumped to a host substrate. The alignment phase is accomplished by hydrodynamic steering using micro-machined tapered sites in a flat substrate, and parts which match those sites. The force driving the assembly is

gravity acting on the density difference between the parts and the fluid. The forces holding the parts in place are Van Der Waals forces and gravity. Finally, the electrical contacts can be made by conventional metallization process after FSA. Although FSA technique is not yet being applied to the fabrication of flat panel display, we speculated that the yield of self assembly could be a major issue for mass production in a large area.

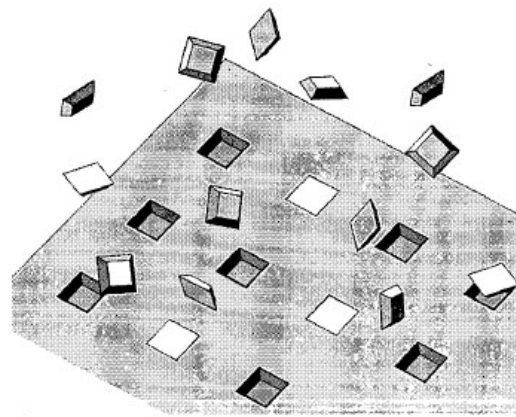


Figure 2-6 Schematic diagram of fluidic self-assembly

2.4 Experimental: Poly-Si TFTs Manufactured on Rigid Substrate Using Device Transfer by Backside Etching Technology

In the following sections, we will propose a novel device transfer by backside etching (DTBE) technique to transfer poly-Si TFTs from Si wafer to a rigid glass/plastic substrate. In *section 2.4* we describe the experimental procedures of DTBE while the results would be summarized in *section 2.5*. Main feature of DTBE is that it utilized Si wafer as a starting material and thus breaks through several native limitations of substrates with low melting temperature. Since the residual Si must be etched by CMP, the host substrate should be a rigid one to sustain the mechanical stress during polishing processes.

2.4.1 Sample Preparation

To accomplish the DTBE process, at the beginning, we manufactured n-channel poly-Si TFTs on Si wafers. Here, we would focus on the transfer process itself so that the efforts for improving performances of TFTs with high temperature processes were discussed elsewhere.

Figure 2-7 schematically depicts the n-channel poly-Si TFT structure. 4-inch silicon wafers of (100) orientation were first washed by standard RCA cleaning process. A 500-nm SiO₂ was thermally grown on the Si substrate to serve as an etching stop layer in the transfer process. An a-Si layer of 100 nm was then deposited with SiH₄ source by LPCVD at 550°C. The gate insulator was formed by liquid-phase deposition method at 25°C. Detailed process of LPD can refer to *Section 4.3.1*. After gate oxide deposition, immediately, a 300 nm thick LPCVD poly-Si film was deposited at 620°C and patterned as gate electrodes. Afterward, a self-aligned phosphorous implantation with dosage of $2 \times 10^{15} \text{ cm}^{-2}$ was performed at 60 keV to form source, drain, and gate electrodes, as shown in Fig. 2-7(a).

After depositing TEOS oxide by PECVD as a passivation layer, the contact holes were etched by buffered oxide etcher (BOE). Without removing photo resists about contact holes, a 5 nm Ni was deposited subsequently by Dual E-Gun evaporation system and the photo resists were then lift-off by ACE. Next, the samples underwent a furnace annealing at 550°C in N₂ atmosphere for 48 hr, which not only activated the doped area but also accomplished the Ni-MILC in the channel region, as shown in Fig. 2-7(b). Thereafter, the remaining Ni was removed by hot H₂SO₄ and H₂O₂ mixtures. Then, the samples were dipped in the diluted HF solution to remove the native oxide formed in the previous step. Finally, all samples underwent a standard backend process to form contact pads. No further hydrogen passivation process was performed. The detailed process flow was listed below:

1. Initial RCA cleaning
2. 500 nm SiO₂: thermal wet oxidation at 1050°C
3. 100 nm a-Si: LPCVD, SiH₄ source at 40 sccm, 550°C

4. Mask #1: Active area definition
5. Dry etching of active area: SAMCO[®] poly-RIE system with SF₆ and O₂ at 20 mtorr
6. RCA cleaning followed by SPM (H₂SO₄ : H₂O₂ = 3:1) at 150°C for 20 min
7. 50 nm gate oxide: LPD-SiO₂ at 23°C with super saturated H₂SiF₆ solution
8. 300 nm poly-Si gate: LPCVD, SiH₄ source at 40 sccm, 620°C
9. Mask #2: Gate electrode definition
10. Dry etching of gate electrode: SAMCO[®] poly-RIE system with SF₆ and O₂ at 20 mtorr
11. RCA cleaning
12. Ion implantation: P³¹, 60 keV, $2 \times 10^{15} \text{ cm}^{-2}$
13. RCA cleaning
14. 500 nm passivation layer: PECVD TEOS SiO₂
15. Mask #3: Contact hole definition
16. Wet chemical etching for contact hole formation: buffered oxide etcher (NH₄F : HF = 6 : 1)
17. 5 nm Ni: Duel E-Gun evaporation system, 0.5 Å/sec at room temperature, base pressure below 2×10^{-6} torr
18. P.R. lift-off: ACE with ultra-sonic vibrations
19. Metal-induced lateral crystallization and dopants activation: furnace annealing, 48 hr, 550°C in N₂ atmosphere
20. Residual Ni removal: hot SPM solution at 150°C for 20 min
21. Native oxide removal: diluted HF, 20 sec
22. 500 nm Al: thermal coater, base pressure below 4×10^{-6} torr
23. Mask #4: metallization
24. Wet chemical etching for Al etching: H₃PO₄, HNO₃, CH₃COOH, H₂O mixture
25. Al sintering at 400°C, 30 min in N₂ atmosphere

At this stage, the MILC poly-Si TFTs had been well prepared for the following bonding and device transfer process. Before the next step, electrical characteristics of TFTs such as $I_{DS} - V_{GS}$ curves and transconductance were measured. Moreover, the samples with thick Al strips on an oxidized Si wafer were also prepared for the observation of scanning electron microscope (SEM).

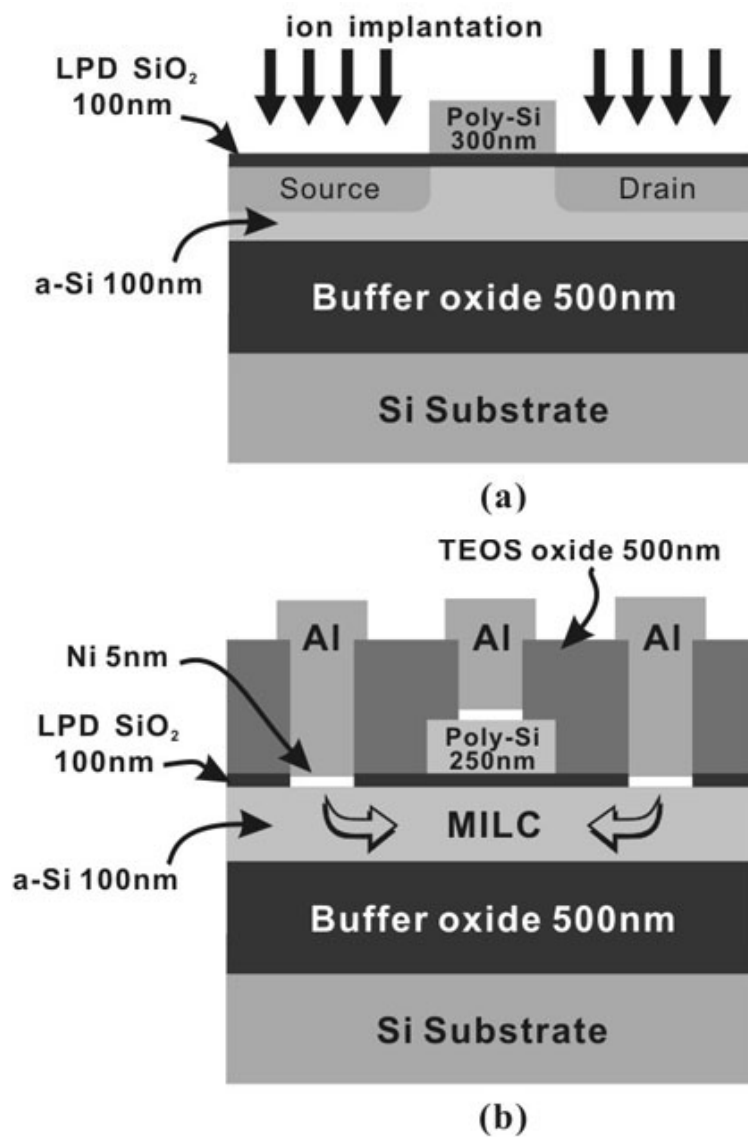


Figure 2-7 Process flow of poly-Si TFTs before DTBE: (a) self-align ion implantation, and (b) recrystallization process by MILC and metallization

2.4.2 Bonding Process

After measurement of TFTs, a layer of PECVD TEOS oxide of 500 nm was deposited on the wafer surface to protect it from being damaged by organic contamination of optical adhesives. As a test sample, and also to overcome the restriction of our CMP facility, the wafers were then cut into small pieces of 4 cm × 2 cm. Thereafter, as shown in Fig. 2-8, the sample was glued with front-side down to the glass/plastic substrate using high transparency optical adhesive. The adhesive was a two component epoxy that can be cured with or without heat. Due to extremely large viscosity of the adhesive at the room temperature, several methods had been tried to solve this problem including pre-backing the adhesive, Si wafer or rigid substrate. Here, the thickness of glass substrate is 1 mm while the thickness of plastic substrate, metallocene cyclic olefin copolymers (mCOC), is 700 μm.

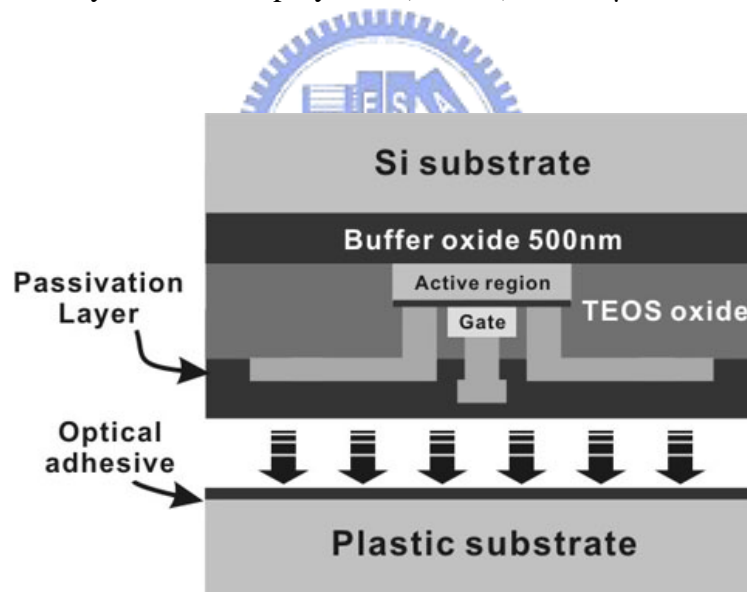


Figure 2-8 Schematic diagram of the wafer bonding process

2.4.3 First Step Thinning Process by CMP

In modern CMOS technology, the chemical-mechanical polishing (CMP) has widely utilized at the backend processes to provide a global planarization for either inter-metal dielectric or Cu damascene structure [2.28], [2.29]. Actually, ICs have to be polished to a thickness of 400 – 500 μm for standard ball grid array (BGA) package and even thinner for

smart card application [2.30], [2.31]. So matured process technology, good uniformity of film thickness, high removal rate and good selectivity are all reasons that we chose CMP as the first thinning process. We utilized CMP to polish the wafer backside to a thickness of 20-40 μm .

2.4.4 Second Step Thinning Process by Wet Chemical Etching

After the CMP thinning process, the residual backside silicon was less than 40 μm . If CMP was used for the entire backside wafer etching process, the extrinsic stress would grow larger as wafer becomes thinner. Finally the wafer or the substrate may break and cause an irreversible damage to the devices being transferred. In contrast, wet chemical etching provides less mechanical stress with relatively high Si/SiO₂ selectivity, proving a better second step thinning process than CMP.

The chemicals used in the second step thinning process were purchased from MERCK[®] Corp. [2.33], composed by HF and HNO₃. We immersed the samples into the chemical etcher until the devices can be observed clearly. The 500 nm thermal oxide layer here became the etching stop layer during second step thinning process.

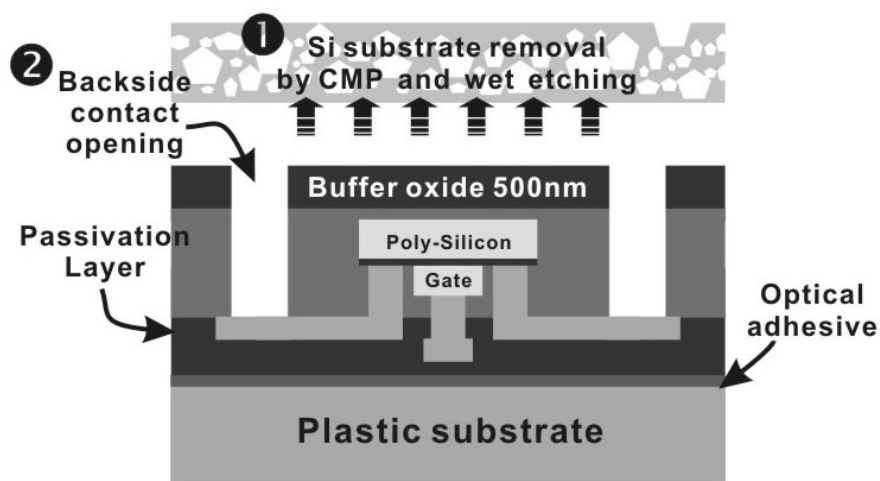


Figure 2-9 Cross-sectional view of poly-Si TFTs after DTBE

2.4.5 Via Hole Opening After DTBE

At this time, the devices on glass/plastic substrates can be clearly observed. In order to measure the electrical characteristics of TFTs after DTBE, we use Mask #4 (for Al metallization mask) with negative photo resist and BOE ($\text{NH}_4\text{F}:\text{HF} = 10:1$) for exposing the contact pads. The cross-sectional view of samples after DTBE was shown in Fig. 2-9.

2.5 Results and Discussion: TFT Manufactured on Rigid Substrate by DTBE

2.5.1 Sample Preparation, Bonding, Etching and Related Issues

Epoxies usually utilized in the bonding process of multiple optical glass lens offer high working temperature, good chemical resistance, good barrier properties (second to only fluoropolymers), and high transparency. Thus they are the most suitable adhesive that meets our demand. In this work, the epoxy used for adhering the silicon wafer to the glass/plastic substrates was EPO-TEK 301-2, manufactured by Epoxy Technology, Billerica, MA. It is a special optical adhesive with light transmission of 98% ~ 99%, glass transition temperature $T_g > 65^\circ\text{C}$ and low water absorption rate of 0.01% (at room temperature, 94%R.H., 30 days) [2.33]. The linear thermal expansion coefficient of EPO-TEK 301-2 is $62 \times 10^{-6} / ^\circ\text{C}$, while the other typical properties of this epoxy were listed in Table 2-3.

There are two solidification methods of the optical adhesive. The retailer provided a curing schedule of 1.5 hr at 80°C or 2 days at room temperature. However, we recommended a better curing schedule of 3 hr at 90°C (thermal solidification) or 3 days at room temperature (natural solidification). Figure 2-10 shows samples bonded on glass substrate by optical adhesive with the thermal solidification or natural solidification method, respectively. One can easily find that many little bubbles located around the devices, as shown in Fig. 2-10(a). These bubbles were generated during the baking process, since the gas resolved in the

adhesive diffused out at an elevated temperature. On the other hand, large bubbles can be observed in Fig. 2-10(b) in a case of natural solidification. These bubbles originated from the manual bonding process and are hardly avoided. We believed that the problem of bubbles can be resolved by bonding samples in vacuum. In our experiments the thermal solidification method was utilized because it is faster and provides better bonding strength.

Table 2-3 Optical, physical, and electrical properties of epoxy EPO-TEK 301-2

Optical Properties	Refraction Index	1.564
	Transmission Rate	90% @ 3000 Å 98% ~ 99% @ 3100 Å ~ 2.5 μm
Physical properties	Color	Clear
	Specific Gravity	0.95
	Viscosity	300 ~ 600 cPs @ 100 rpm/23°C
	Glass Transition Temperature (T _g)	> 65°C
	Water Absorption Rate (30 days, 94% R.H. at room temperature)	0.01 %
	Weight Loss (200°C, 300 hrs)	0.07 %
	Coefficient of Linear Thermal Expansion (30°C ~ 90°C)	62 × 10 ⁻⁶ /°C
	Operating Temperature Range	-45°C ~ 200°C
Electrical Properties	Dielectric Constant	3.1 @ 25°C, 100 KC 3.67 @ 115°C, 100 KC
	Volume Resistivity (ohm-cm)	> 3.5 × 10 ¹⁴

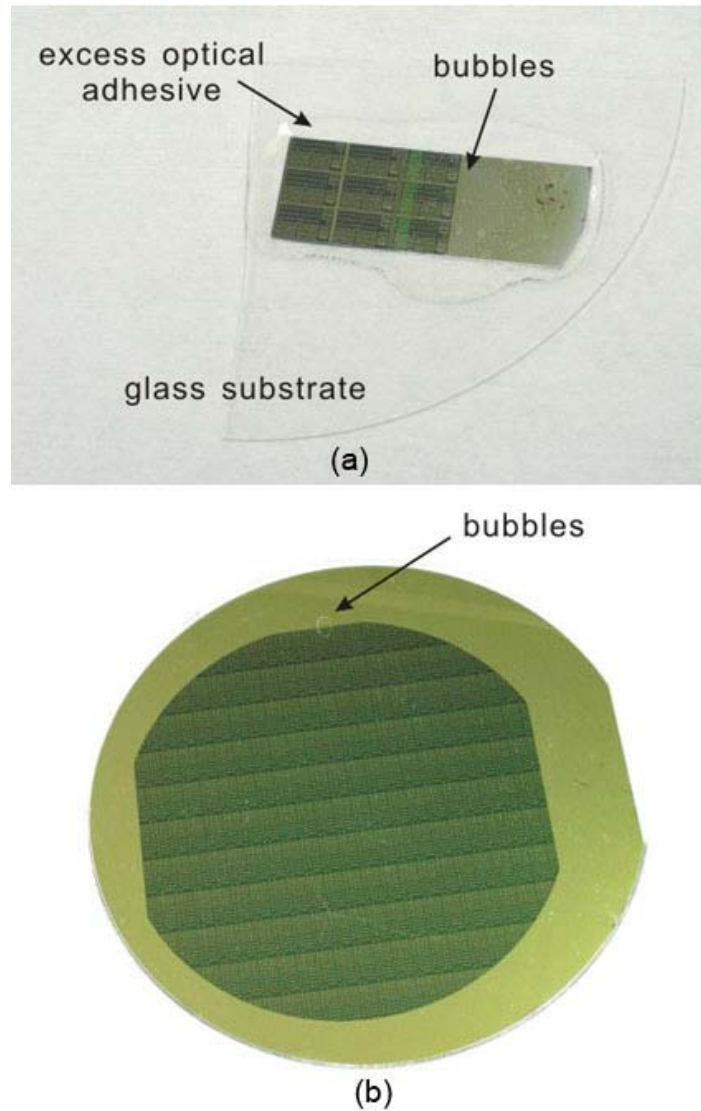


Figure 2-10 Samples bonded on glass substrate by optical adhesive with the (a) thermal solidification method of 90°C, 3 hr or (b) natural solidification method at room temperature

2.5.2 The Observations after DTBE

Figure 2-11 shows photographs at different stages of DTBE technology. In Fig. 2-11(a), excess adhesive solidified around the Si wafer with thickness of 0.5 ~ 1 mm can be observed. After CMP process, as shown in Fig. 2-11(b), the CMP step not only polished the Si wafer from the backside, but also thinned those excess adhesives around the samples, which is advantageous for the following wet chemical etching step. The reason is that the silicon etcher contains nitric acid, which attacks the optical adhesive slowly; finally the damaged

adhesives may twist or curled up, causing the entire patterns being transferred peeling. To prevent this thing from happening, the contours of the sample were protected by wax after the CMP step, alleviating the attack from the chemical etcher. Finally, the sample after wet chemical etching process is illustrated in Fig. 2-11(c), where the diameter of the MCOC substrate is around 2.5 inches.

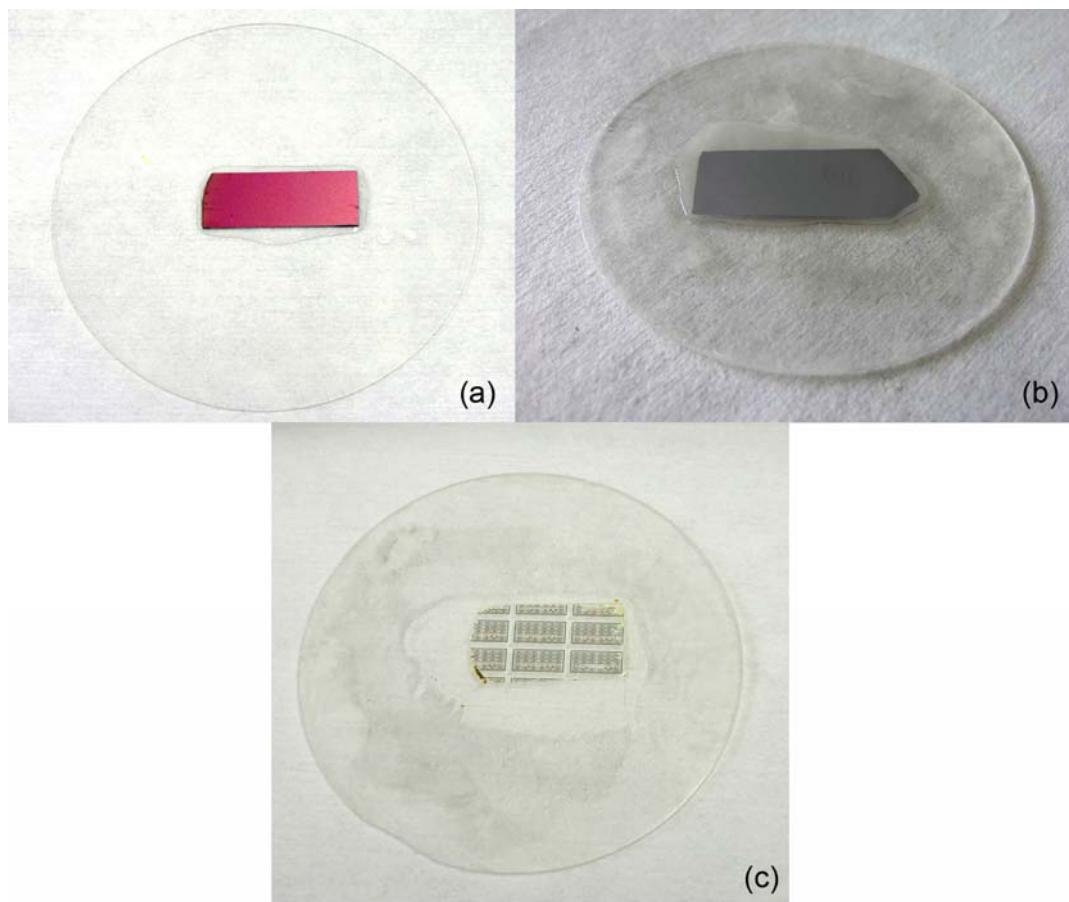


Figure 2-11 Photographs of different stages of DTBE process: (a) as-bonded, (b) after CMP, and (c) after wet chemical etching

Figure 2-12 shows the optical microscope (OM) pictures of devices after DTBE process on the transparent substrate, where the light source of OM in Fig. 2-12(a) came from the top side and the light source of Fig. 2-12(b) came from the back side. Different layers including poly-Si and metallization can be observed clearly. In Fig. 2-12(b), the dark areas are Al pads, source/drain and gate electrodes which are opaque to light while the white area is the

transparent substrate. These photographs reveal that the remaining Si was completely removed; no physical damage was observed. For comparison, figure 2-13 shows the OM photographs of the DTBE process nearly completed. Under a top light source, we can find that some silicon islands still remained on the Al electrode, implying the surface roughness resulted from the second step wet etching is significant. Now that the over etching step is required, the selectivity of Si etcher to barrier layer (etching stop layer) becomes critical.

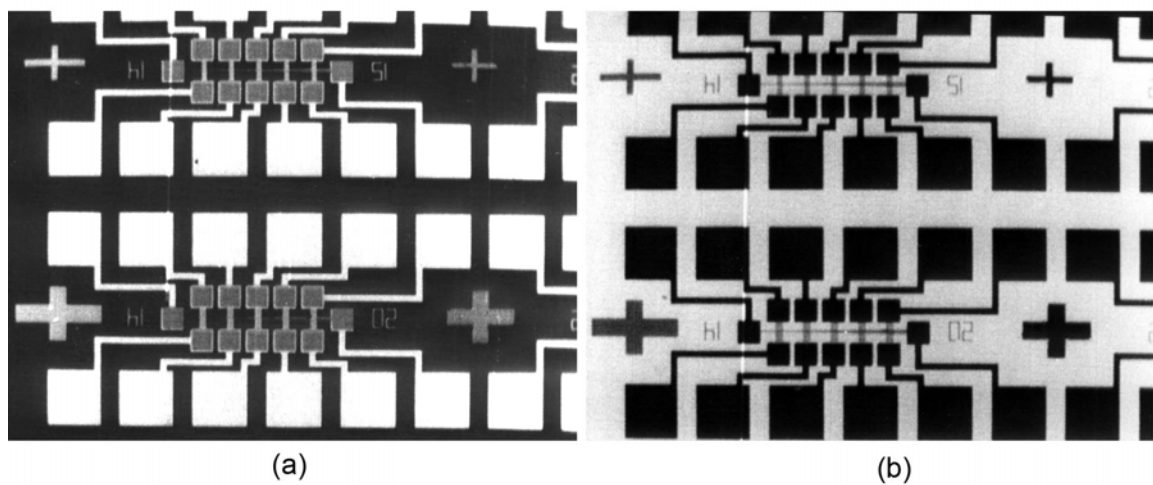


Figure 2-12 The optical microscope pictures of TFTs on a rigid plastic substrate with (a) top light source, and (b) back light source

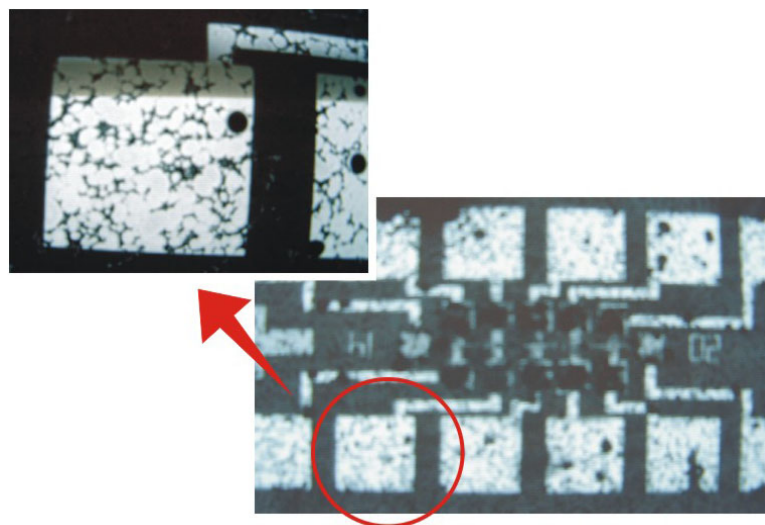


Figure 2-13 OM images of the DTBE process nearly completed

To further observe the back etching process closely, we prepared a test structure with thick Al strips deposited on an oxidized silicon wafer and the patterns were then transferred to another plastic substrate by DTBE method. In order to clearly observe the surface geometry after DTBE, some backside Si was deliberately kept at the second chemical etching step. The cross-sectional view acquired by scanning electron microscope (SEM) was shown in Fig. 2-14; each material indicated in the picture had been confirmed by energy-dispersive spectrometer (EDS). It can be found that the residual Si substrate, polished by CMP and wet-chemical etching, exhibits low surface roughness and uniform thickness; the Al strip is well protected by thick thermal oxide layer.

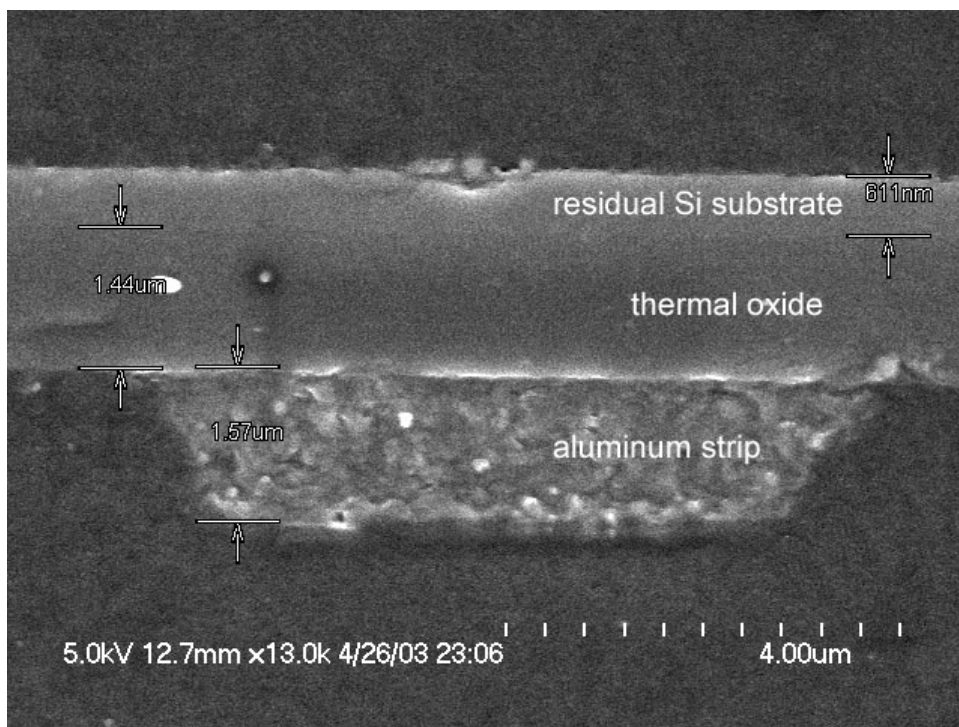


Figure 2-14 The SEM cross-sectional view of an aluminum strip after DTBE process

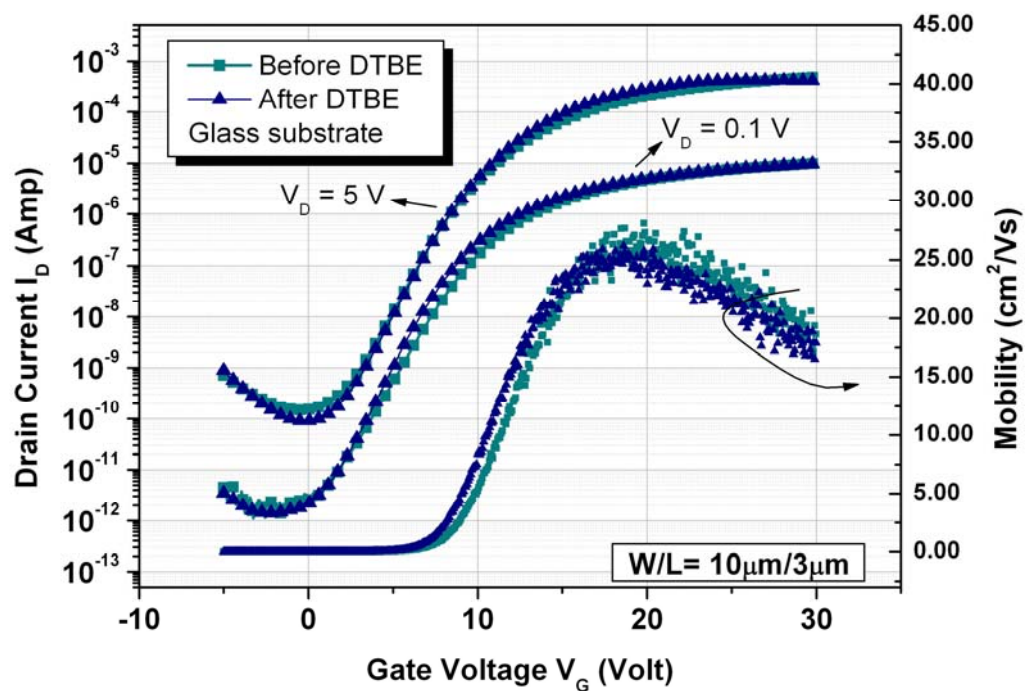
In the fabrication process of TFTs, the total thickness variation of a Si wafer was 25 μm (from the specification provided by the retailer of wafers), and the thickness of the SiO_2 etching layer was 500 nm. Both CMP and backside chemical etching affect the uniformity of thinning process. However, typical CMP equipment provided quite high planarity because no

difficulties concerning dishing, erosion, or pattern dependence. Since the rate of wet chemical etching of Si is 80 times faster than that of SiO₂, the maximum tolerable thickness variance was 40 μm (i.e. 80 × 500 nm), much larger than that attributed to the thickness variation of substrate itself and the subsequent removal processes of backside Si. The satisfactory consequences of DTBE in Fig. 2-12 and Fig. 2-14 imply that the practical etching result is very consistent with the above estimation. Therefore, combining CMP/wet-etching processes of modern CMOS technology, DTBE shows a great promise of transferring devices to a substrate as large as 12 inch.

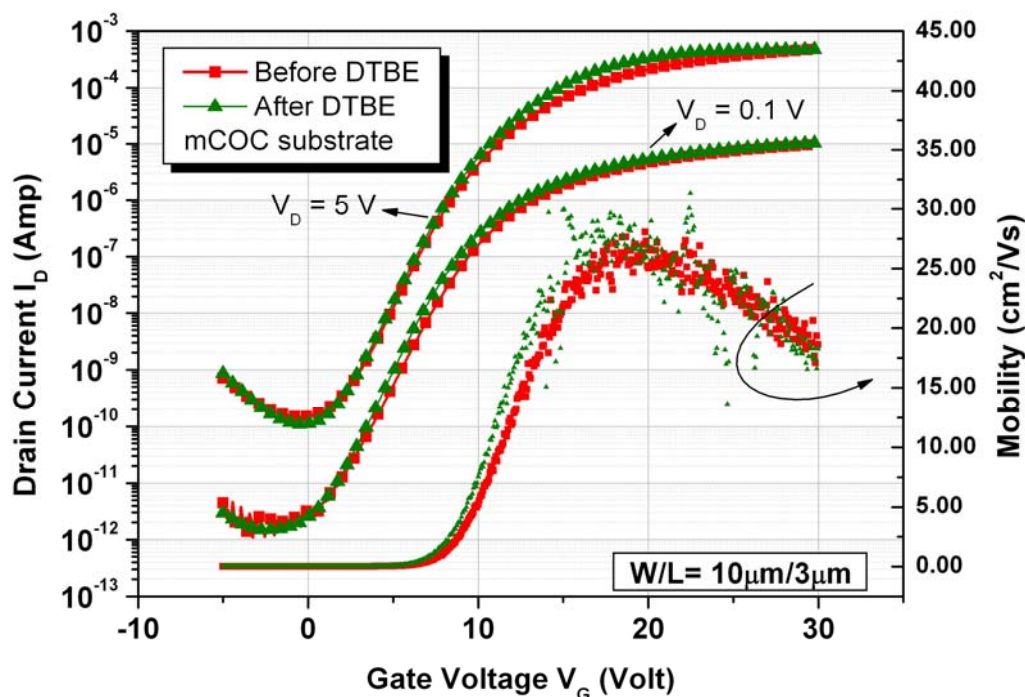
2.5.3 Electrical Characteristics of poly-Si TFTs Before and After DTBE

Figure 2-15 depicts the I_{DS} - V_{GS} and transconductance curves before and after DTBE with different host substrate. Notably, on either glass or mCOC backplane, no device degradation was observed after adhesion, CMP and wet etching processes. On the contrary, the device characteristics, such as ON/OFF current ratio, swing, threshold voltage and mobility were a little bit better than those before DTBE. For these devices, conventional hydrogen passivation process was never performed but a final TEOS SiO₂ layer was capped above the Al interconnections when finishing electrical measurements before transferring. This oxide layer was deposited in a 13.56 MHz parallel plate reactor at 300°C in a 300 mtorr gas mixture of 7 sccm TEOS and 450 sccm O₂. The plasma power was 250 W and the processing time was about 5 min. Because metal-induced crystallization process contributes to large amount of intra-granular defects and defective crystallization front, the O₂ radicals in the plasma could partially passivate the trap states in the channel region of poly-Si TFTs, resulting in the fluctuation of device characteristics after DTBE [2.34]. Additionally, we found few differences between electrical properties of poly-Si TFTs on either glass or mCOC substrates, indicating that the type of the substrate does not affect (or not significantly) the performance of TFTs after DTBE. Detailed electrical parameters of poly-Si TFTs

manufactured on rigid glass or plastic substrates were listed in Table 2-4.



(a)



(b)

Figure 2-15 $I_{DS} - V_{GS}$ and field-effect mobility curves before and after DTBE with different host substrate: (a) glass and (b) MCOC

Table 2-4 Comparison of device characteristics among as-fabricated poly-Si TFTs and those being transferred to rigid glass or mCOC substrates by DTBE technique

W/L = 10 μm/3 μm					
Device	I _{ON} (10 ⁻⁴ A)	I _{OFF} (10 ⁻¹¹ A)	I _{ON} /I _{OFF} (10 ⁶)	μ _{FE} (cm ² /Vs)	V _{th} (volt)
As-fabricated	4.85	14.8	3.27	28.9	4.17
On glass	4.25	9	4.72	26.9	4.23
On mCOC	4.75	11.1	4.27	32.3	4.3
W/L = 10 μm/5 μm					
Device	I _{ON} (10 ⁻⁴ A)	I _{OFF} (10 ⁻¹¹ A)	I _{ON} /I _{OFF} (10 ⁶)	μ _{FE} (cm ² /Vs)	V _{th} (volt)
As-fabricated	1.80	3.67	4.90	18.38	4.5
On glass	1.49	3.38	4.40	20.59	4.51
On mCOC	3.37	4.30	7.83	29.93	4.38

The difference of ON current between device transferring steps has been statistically evaluated by the following equation:

$$Difference(\%) = \frac{I_{ON-after} - I_{ON-before}}{I_{ON-before}} \times 100\% \quad (2.3)$$

Both the mobility and OFF-state leakage current have been treated in the same manner. Figure 2-16 summarizes the results for devices with various channel length/width. It is found that both mobility and ON current after DTBE increased while the OFF-state leakage current decreased. Notably, however, for large devices (W/L = 20 μm/9 μm), not only the OFF current but also the transconductance apparently degrades after DTBE. It can be attributed to the stress induced damage because the thermal expansion coefficient of optical adhesive is $6.2 \times 10^{-5} / ^\circ\text{C}$, which is 25 times larger than that of Si ($2.4 \times 10^{-6} / ^\circ\text{C}$). When suffering from annealing or cooling steps during bonding and photo-resist backing, larger devices tends to generate more micro-defects than the smaller ones, resulting in noticeable degradation of electrical properties. To suppress the induced extrinsic stress, a thick oxide or nitride layer

could be deposited on the wafer surface before bonding, and the curing temperature of optical adhesive would be modified. Details about the relationship between the extrinsic stress and device performance will be discussed in *Section 3.5.4*.

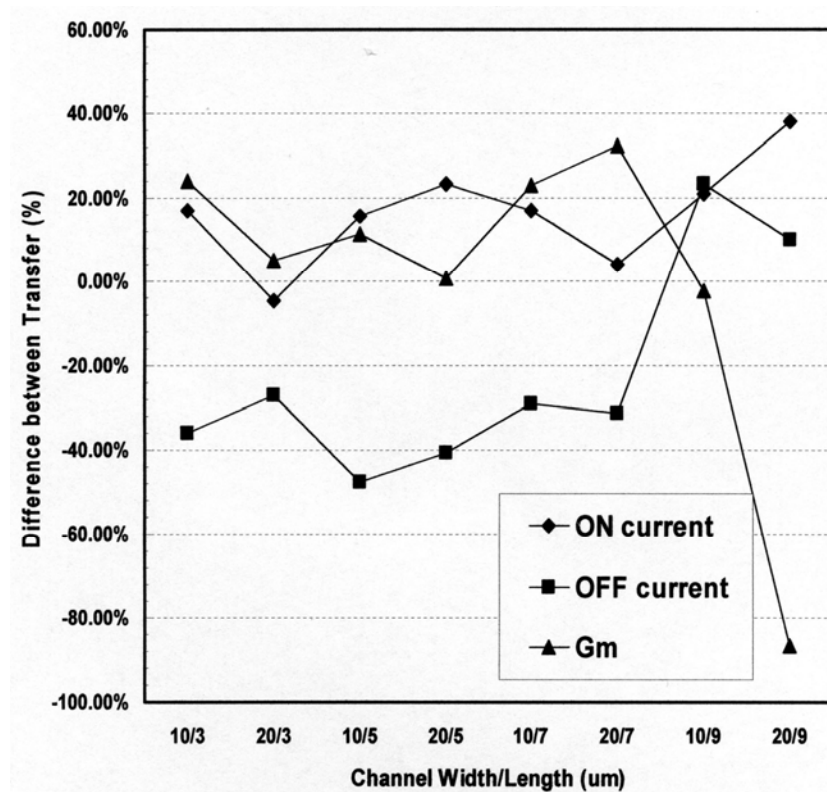


Figure 2-16 Statistical differences in properties of devices due to DTBE process

In this research, the process temperature of poly-Si TFTs did not exceed 620°C so that the average field-effect mobility (μ_{FE}) was only 20 ~ 30 cm²/Vs. Nevertheless, several high temperature processes, including high-quality gate oxidation and MILC with 950°C post annealing, can be introduced to optimize the device performance because the starting material is Si wafer rather than glass/plastic substrates. Moreover, thanks to the lithographic technique of CMOS process, not only active matrix devices but also high-density peripheral circuits can be integrated with low costs and low-melting temperature materials, contributing to wide applications in multi-functional portable displays, LCD projector or rear-projection TVs. Compared with a reflective-type liquid-crystal on Si (LCOS) module, a transmissive panel

with similar resolution and higher light efficiency can be fulfilled by DTBE. Undoubtedly, DTBE technology potentially provides the feasibility of high temperature processes and great compatibility as well as production yield to integrate devices on glass/plastic substrates.

2.6 Summary

In this chapter, we discussed the critical issues about fabricating poly-Si TFTs on plastic substrates, including the limitation of low T_g , precision mask alignment, and the unique physical/chemical properties of polymeric substrates. Next, we reviewed several specified technique for fabricating TFTs *directly* on plastics, such as a proper selection of the backplane, barrier layer deposition, thermal pre-treatment, and thin-film deposition, etc.

The obstacles from the plastic substrates can be greatly overcome by device transfer technique. Here we reviewed several transfer methods including laser ablation, sacrificial layer etching, and even the transfer of crystalline silicon. However, these *indirect* methods introduced the other drawbacks to be addressed. That's way we proposed the device transfer by backside etching (DTBE) technique.

In the wafer bonding process, we tried two different methods to solidify the optical adhesive. The samples with thermal solidification method can sustain larger thermal stress than natural solidification. But the little bubbles generated during the curing step of adhesive should be resolved.

The samples underwent a two-step thinning process by CMP and wet etching. The devices were successfully transferred to rigid glass and mCOC plastic substrate. Through OM and SEM observation, we found no physical damage during DTBE and a superior planarization ability of CMP.

For the case of the electrical measurements after DTBE, the electrical characteristics of poly-Si TFTs such as ON/OFF current ratio, swing and mobility seem to be a little better than

those before DTBE. The TEOS-SiO₂ capping process by PECVD prior to wafer bonding was believed to introduce O₂ radicals to the active layer and the poly-Si/gate oxide interface, resulting in the variation of TFTs properties. Statistical data exhibit that the demonstrated DTBE technique is advisable for manufacturing poly-Si TFTs on those substrates with low melting temperature.

